UNIT - 1

Introduction & Basic Electrical properties of MOS ckts:-

VLSI - very large Scale integration

Definition of Ic:-

Ic is an electronic for integrated circuit and may be given as combination of active of passive. elements that are integrated on signle silicon chip.

As there are several advantages of using Silicon which includes, if acts as good insulating material, oxiding material.

Most of the Ic's avaliable in the market are made using silicon only [i.e., 90 %]

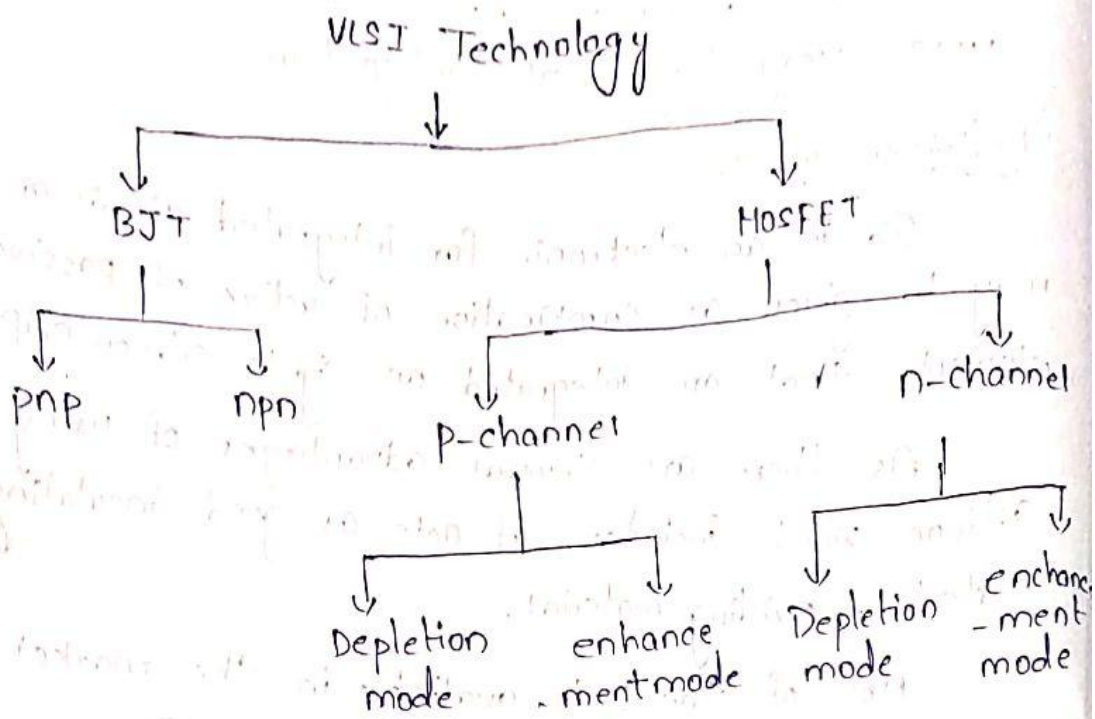
Trends in micro electronics:-

The electronics now a days available in the market are categorized by reliability, size, weight, volume, cost.

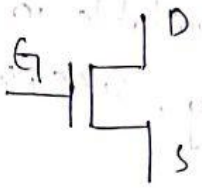
In addition these the VLSI technology made an aduantage to have a more powerful & flexible processor for availing a good source.

* The BJT was first invented by william shockley & John barden in 1947 at bell laboratories..
* up to 1950's the BJT technology was dominated by vaccum tubes.
* The 1st Ic technology was deveioped in 1960's and there by a revolutionary come into the electronics industries.

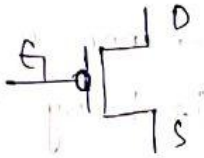
Symbols of MOSFET:-



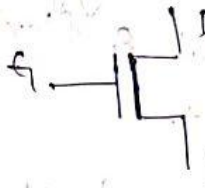
N-MOS

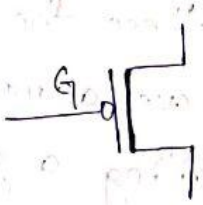


P MOS

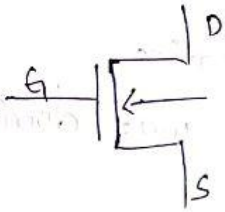


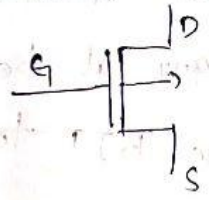
enhancement mode





Depletion mode





current Supply

BJT is a Current Controlled device where as MOSFET is a Voltage Controlled device.

Levels of integration:-

Depending upon the complexity of integrated ckt the classification can be given as

SSI (small scale integration) - 10 to 100

MSI (Medium scale integration) - 100 to 1000

LSI (large scale integration) - 1000 to 10^5

VLSI (very large scale integration) - 10^5 to 10^6

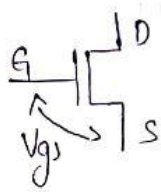
the upcoming technology i.e.,

ULSI (ultra large scale integration) - 10 to 100 million

Difference Between BJT and MOSFET

BJT	MOSFET
1. It is current control device.	1. It is voltage control device.
2. Collector and emitter terminal's are not inter change.	2. Drain and Source terminals are interchange.
3. Impedance is low.	3. Impedance is high.
4. Ip Impedance is low	4. Ip Impedance is high
5. Trans conductance is high.	5. Transconductance is low

* Why it is called FET?

A) 

Vgs = Voltage blw gate and source terminals.

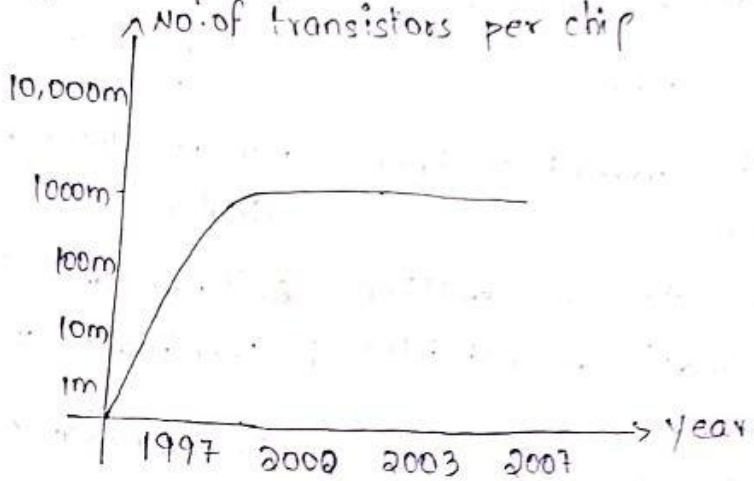
By the external application of vgs they is an electric field development blw gate and source

V1

and hence it will get effected in corresponds with V_{GS}. Hence it is called field effect Transistor (FET).

The IC Era:-

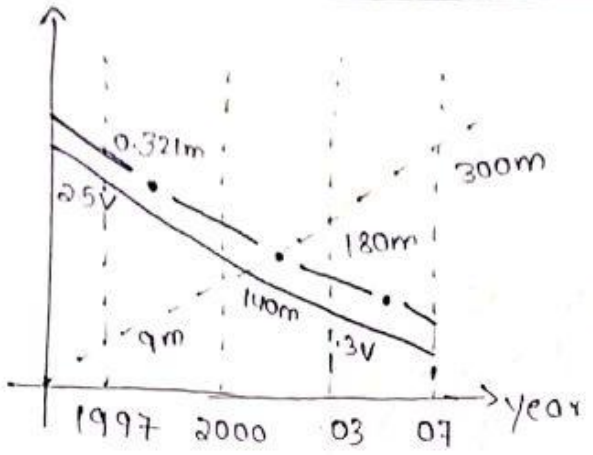
* The first IC emerged in the early 1960's.
* Depending upon the potential of that IC, we can find no. of transistors that are being integrated in the single silicon chip.
* In less than 3 decades the no of transistors count has rasin form 100 to 1000 millions of transistors per chip.



Moore's law:-

The graphical representation that gives the relation-ship b/w the year. V/s no. of transistor per chip is called moora's law.

No of transistors per chip	supply voltage	channel length (um)
10000m	3v	0.3
1000m	2.5v	0.25
100m	2v	0.2
10m	1.5v	0.15
1m	1V	1



Channel length (μm) — • — • — • —

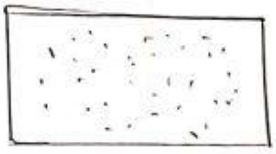
Supply voltage ————————————

No. of transistors per chip - - - - - - - - - - - - - -

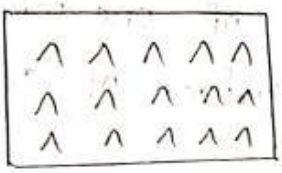
To have powerful and flexible processors, some more modifications are made to moore's law which includes reducing supply voltage and channel length.

Symbol's for Ic fabrication process:-

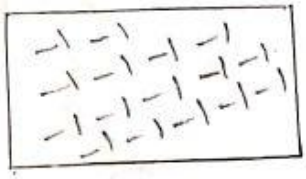
oxide layer →



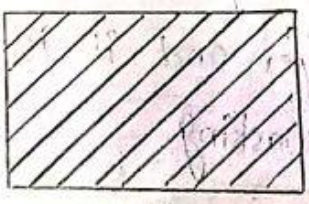
P-Subtrate →



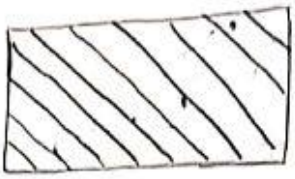
N-Subtrate →

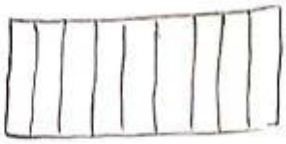


P- diffusions →



n-diffusions 

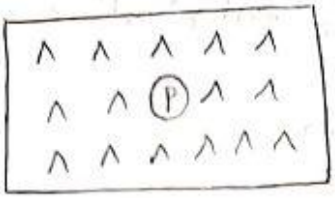
polysilicon 

metal 

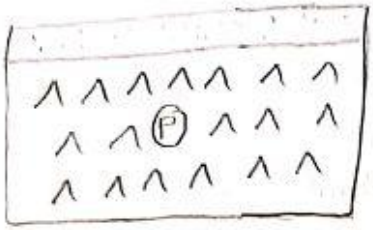
depletion 

N-MOS fabrication process:-

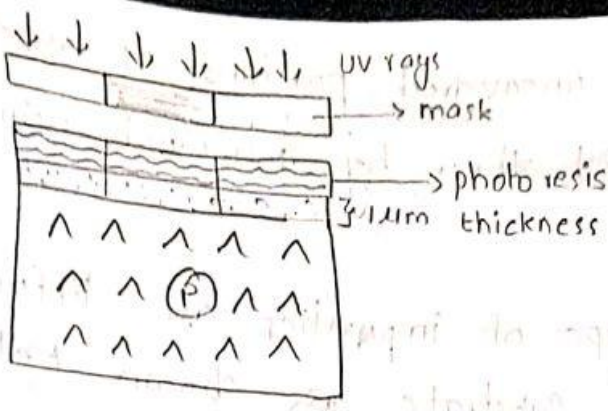
Step 1:- for the desiging of n-mos transistor we have to Consider P type of substrate material.



Step 2:- To improve the quality and protection an oxide layer of one micrometer thickness is grown over all surface of p-substrate.

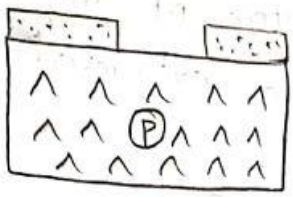


Step 3: A photo resistive layer is grown at the top of oxide layer and it is exposed to uv light through suitable masking.

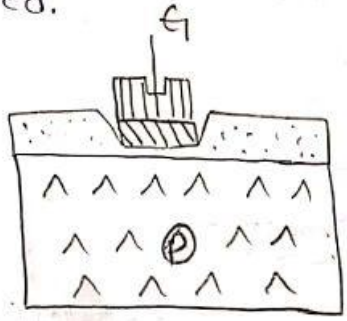


Step 4:- The uncovered portion of mask allows UV light to flow through it, the oxide layer will be get softened and remain covered position will be remain harden.

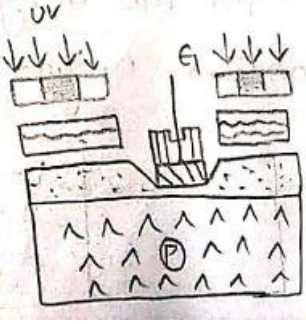
The portion which is softned will be remove and the process is called "Etching".



Step 5:- An oxide layer of 0.1μm thickness is grown and using polysilicon and metal gate terminal can be extracted.

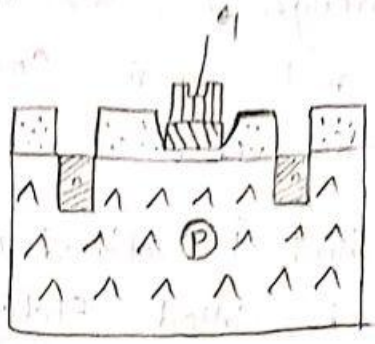


Step 6:- To diffuse n-type of impurities into p-type of substrate the masking and Etching processes are again carried out

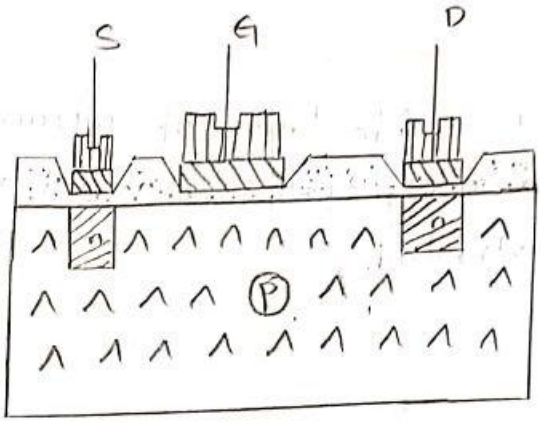


Step 7:- The uncovered portions of mask will be get softend and their by removed using Etching process.

The n-type of impurities are diffused into the P-type of substrate as shown below.



Step 8:- From the n-type of impurities drain and Source terminals can be extracted using polysilicon and metals.

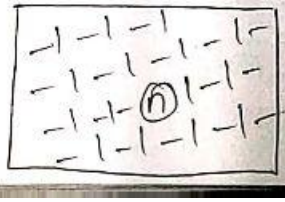


9) P-MOS fabrication Process:-

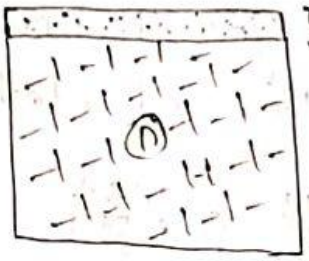
P-(N)-P P-diffusion

Substrate

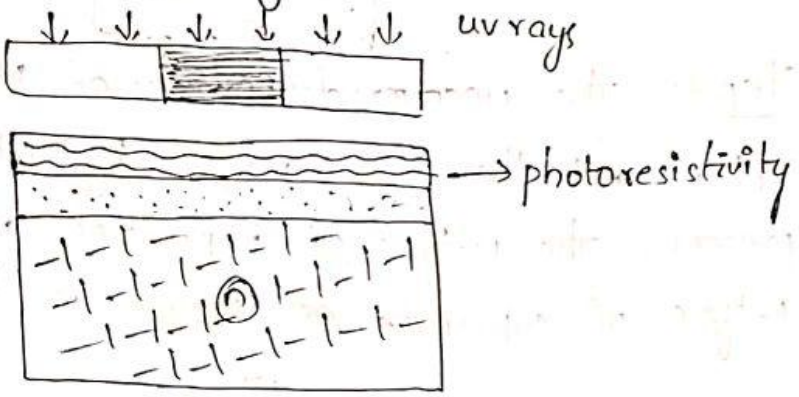
Step 1:- for the designing of P-MOS transistor we have to consider n-type of substrate material.



step 2:- To improve the quality and protection on oxide layer of 1um thickness is grown overall surface of n- substrate.

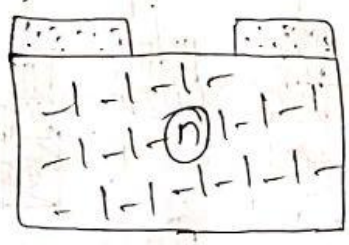


step 3:- A photoresistive layer is grown at the top of oxide layer and it is exposed to uv light through suitable Masking.

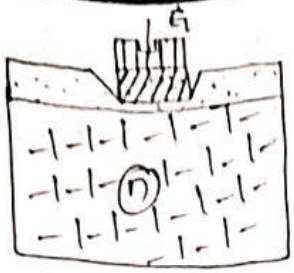


step 4:- The uncovered position of mask allows uv light to flow through it. the oxide layer will get soften and remain covered portion will remain harden.

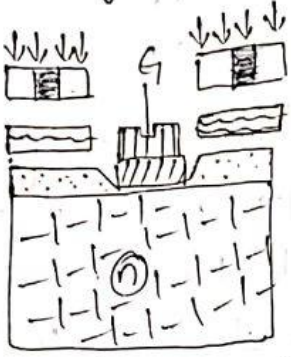
the portion which is soften will be removed and this process is called Etching.



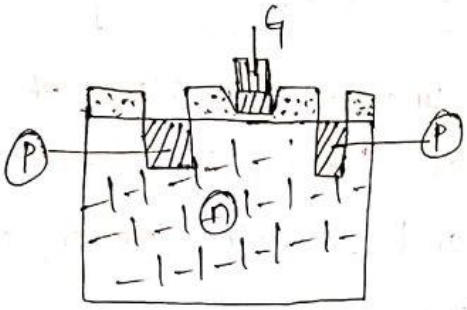
step 5:- An oxide layer of 0.1um thickness is grown and using polysilicon and metal gate terminal can be exerted.



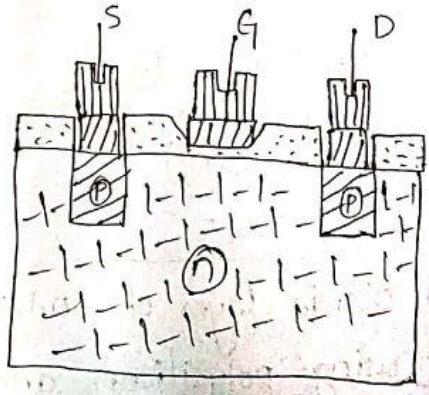
Step 6:- To diffuse p-type of impurities into n-type of substrate the Masking and etching process are again carried out.



Step 7:- The uncovered portion of Mask will be get soften and there by removed by using "Etching" process. the n-type of impurities are diffused into P-type of substrate as shown in below.



Step 8:- from the p-type of impurities drain and source terminals can be extracted by using polysilicon and metals.



CMOS Inverter:-

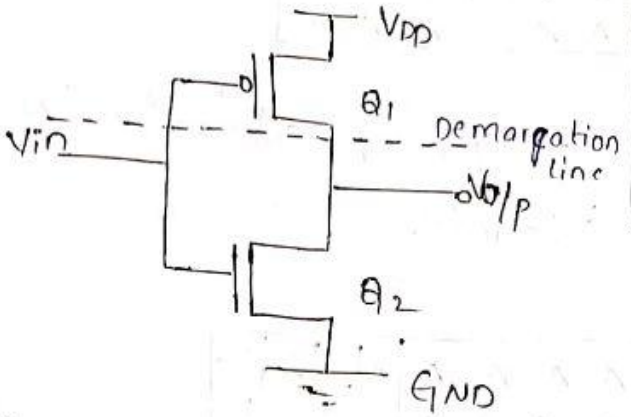
* CMOS is known as complementary metaloxide semi-conductor and it will produce output has complemen-tation of input.

* the CMOS can be designed with the help of PMOS and NMOS.

* NMOS transistors are faster than pmos devices because the Mobility of electrons are greater compare to Mobility of holes.

i.e., $\mu_n = 2.5\mu_p$

CMOS Inverter circuit:-



Vin	Q1	Q2	Vo/p
0	ON	OFF	1
1	OFF	ON	0

Operation:-

Case(1):- when Vin is zero

when the input is logic 0 then the transistor Q_1 will get ON, Q_2 will get off there by producing Vo as logic '1'.

Case(2):- when Vin is logic '1'.

when the Input is logic 1 then Q_1 will get turn off, Q_2 will get turn on, hence the Vo as logic '0'.

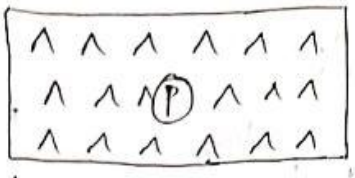
Fabrication of CMOS:-

For the fabrication of CMOS we have different types

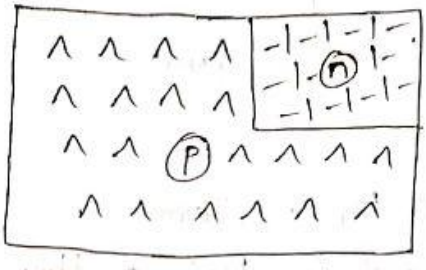
1. CMOS using p-well process
2. CMOS using n-well process
3. Twin-Tub process

CMOS fabrication using n-well process:-

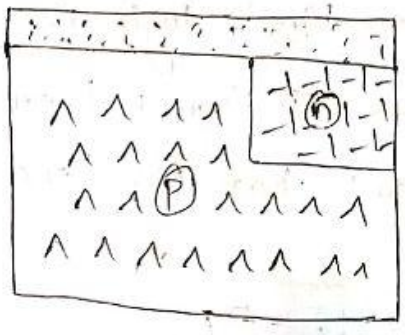
Step 1:- for the designing of CMOS using n-well process we have to consider a p-type of substrate.



Step 2:- Diffuse n-type of substrate (n-well) into p-type of substrate.

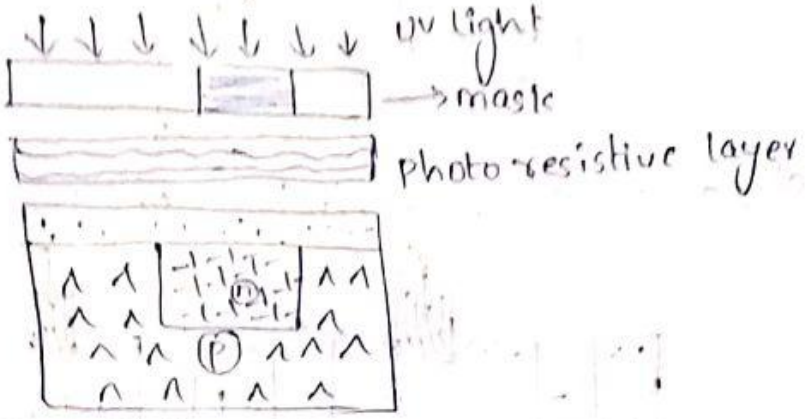


Step 3:- grow oxide layer on the surface of p-type substrate of 1um thickness

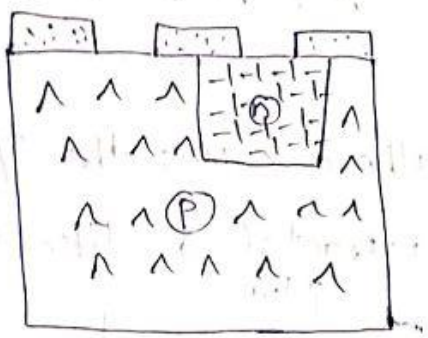


} 1um thiox

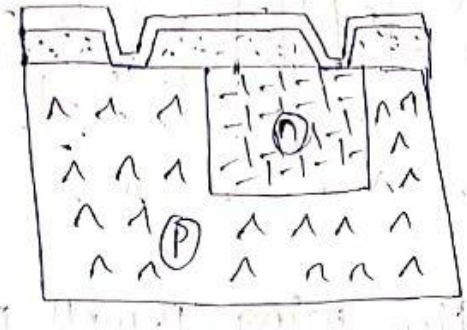
Step 4:- To improve photoelectiveness, a photoresistive layer is grown and it is exposed to uv light through suitable Masking.



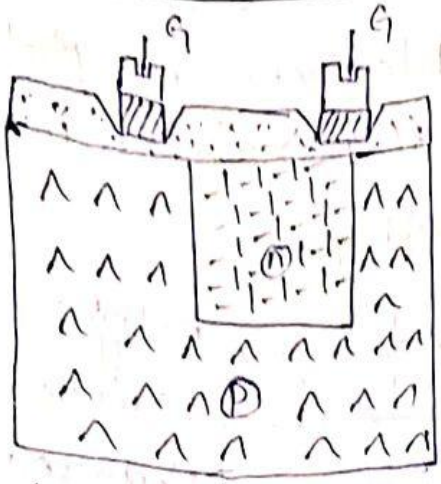
Step 5:- The uncovered portions of mass will get soften and removed by etching process.



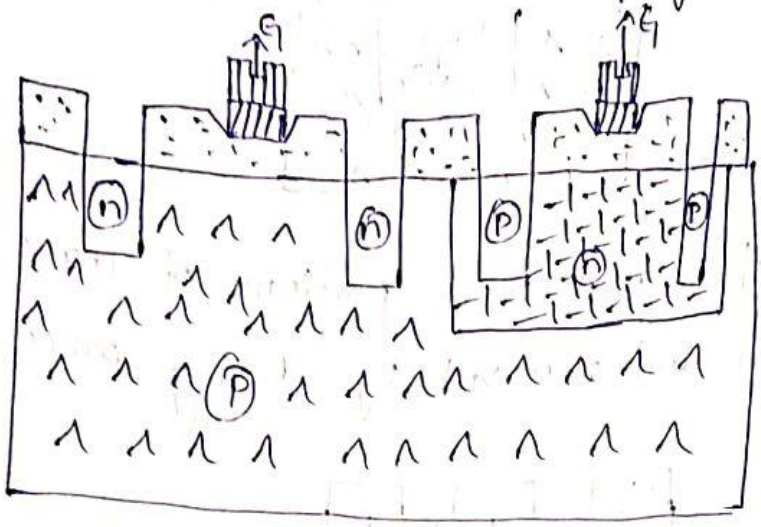
Step 6:- An oxide of 0.1 layer is grown on the top of p-type of substrate.



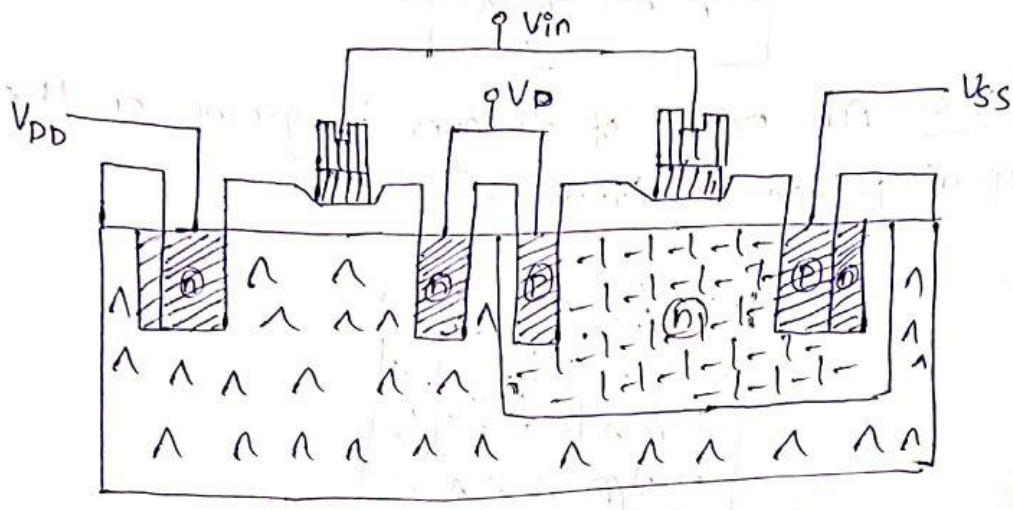
Step 7:- The gate terminals can be extracted from p and n type of substrates using polysilicon and metal.



Steps:- To have diffusions of n-type and p-ty

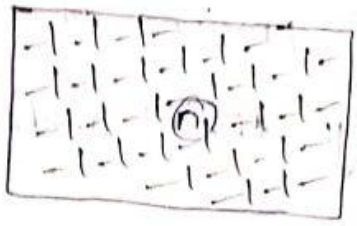


Step9: finally Furthere C-MOS the i/p and o/p terminals can be extracted as like shown below.

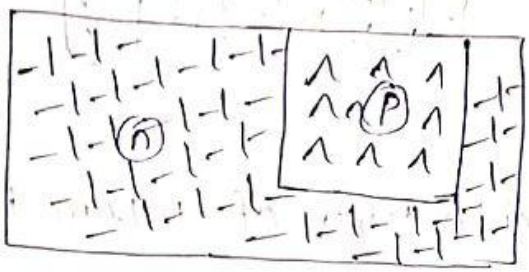


2) C-MOS fabrication using P-well process:-

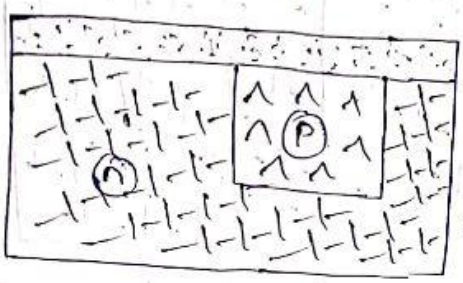
Step 1: For the designing of C-MOS using P-well process we have to Consider a n-type substrate.



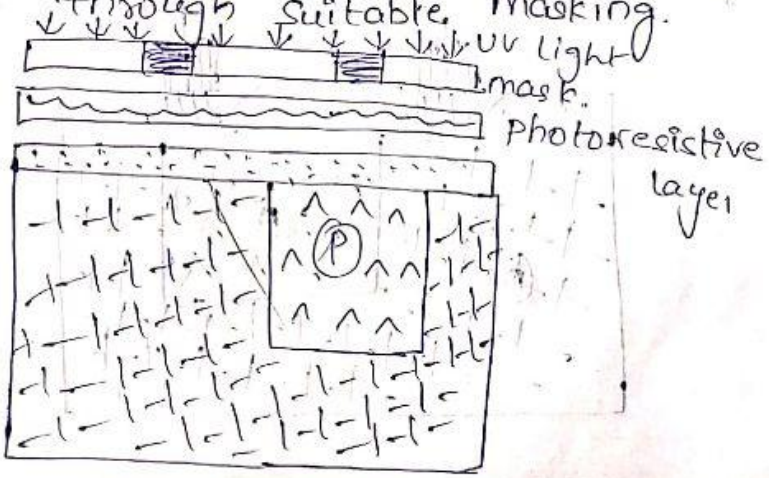
Step2:- diffuse p-type substrate (p-well) into n-type of substrate.



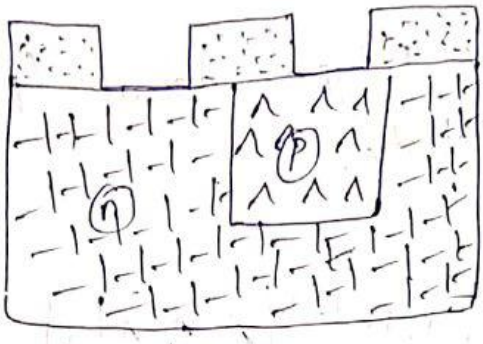
Step 3:- grow oxide layer on the surface of P-type of substrate of 1um thickness.



Step4:- To improve the protectiveness a photo resistive layer is grown and it is exposed to uvlight through suitable masking.

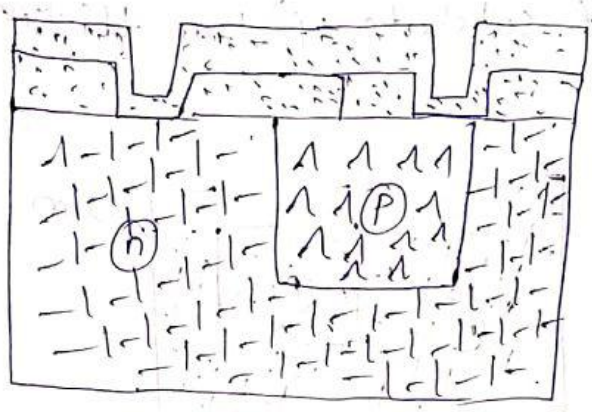


Step 5: The uncovered portions of mask will get soften and removing the "etching" process.

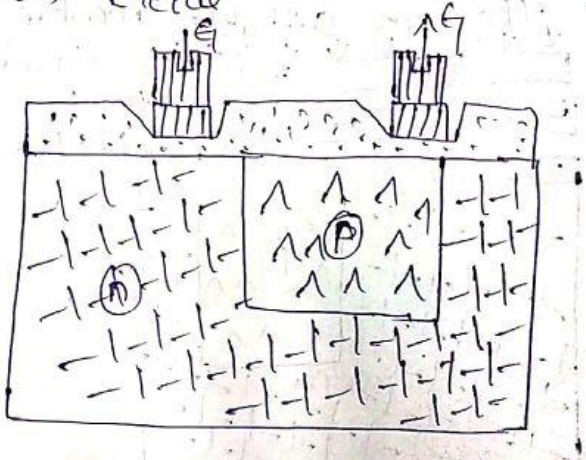


Step 6:-

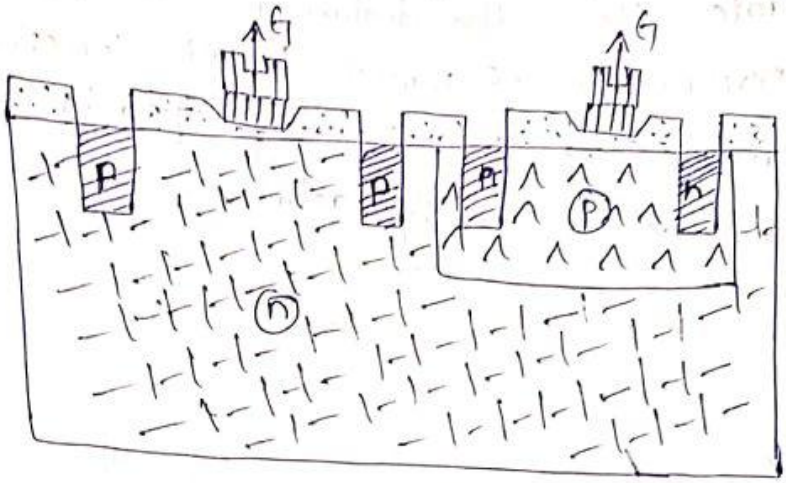
An oxide layer of 0.1um is grown on the top of P-type substrate.



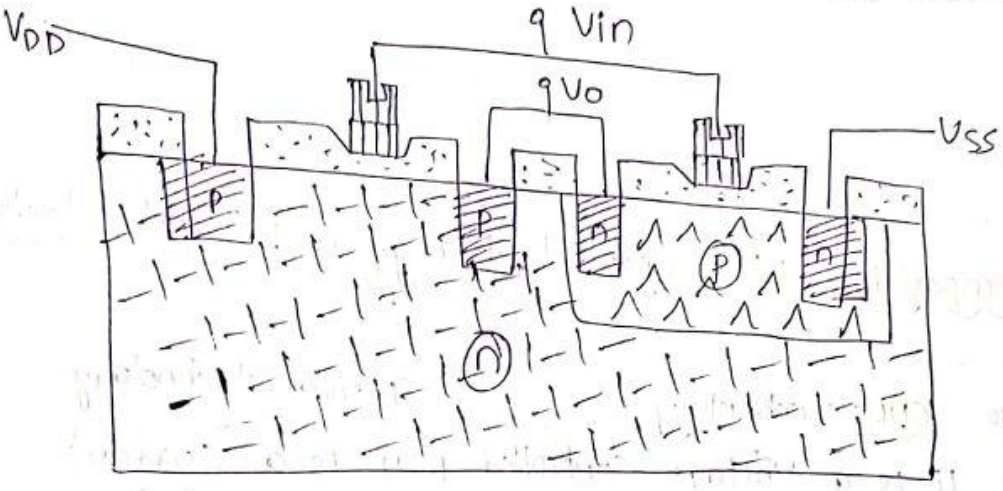
Step 7:- The gate terminal can be extracted from P and n-type of the substrate using polysilicon metal



Step8:- To have diffusion p-type and n-type into corresponding n & p type of substrates Repeat the steps from (4) to (6).

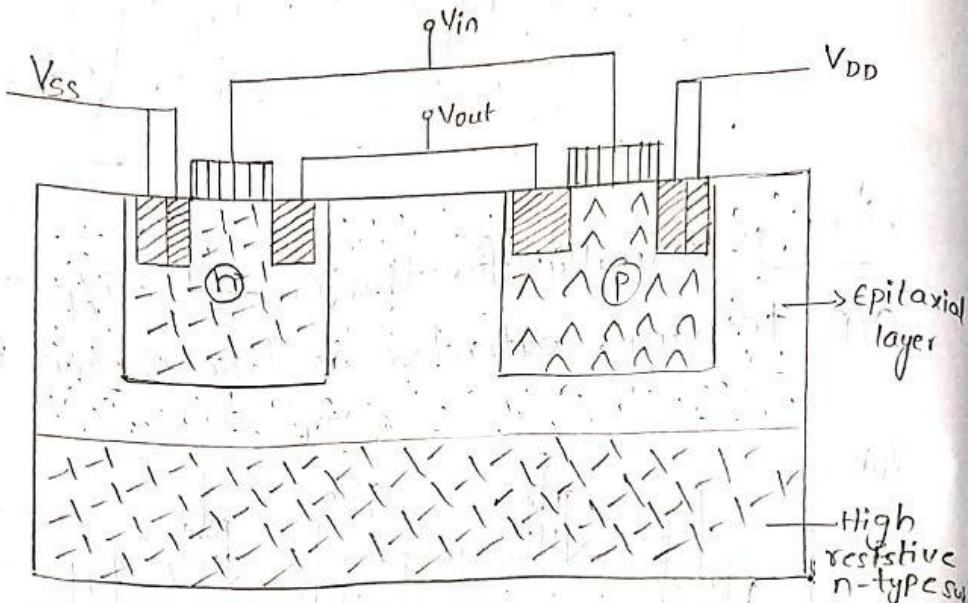


Step 9: finally for the cmos the i/p and o/p terminals extracted as like shown below.



CMOS fabrication using Twin-Tub process:-

CMOS using twin-tub process is the logical extension of P-well and N-well process. The desiging can be carrier out by taking a high resistitive n-type of Substrate. Here the design is consider such that the performance of P-well do not comprise the Performance of N-well using Epitaxial layer. Hence doping level is readily acheieve.



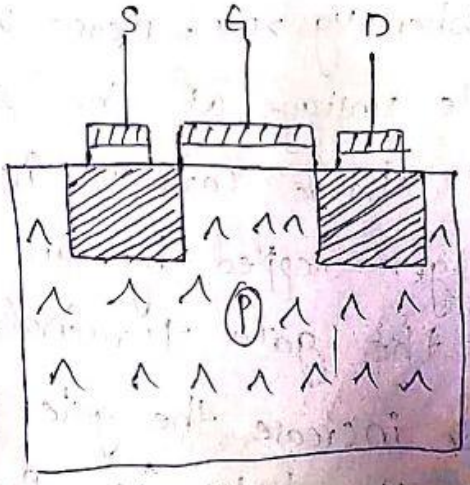
Comparision blw CMOS technology and Bipolar technology

S.No	CMOS technology	Bipolar technology
1.	It is a Voltage controlled device.	1. It is a current controlled device.
2.	High input impedance and low output drain current	Low input impedance and high output drain current.
3.	Low static power dissipation	High static power dissipation
4.	Scable threshold voltage	threshold voltage may depend on type of Semiconducting material & on device parameters.

5.	Bidirectional Capability that is drain and source terminals can be inter change.	These are essentially uni -directional,
6.	low transconductance. i.e., g_m is directly proportional to 1/impedance $g_m \propto \frac{1}{\text{Impedance}}$.	High transconductance that is $g_m \propto eV_{in}$
7.	High package density	low package density.
8.	High noise margin	low voltage swing levels

Enhancement mode MOSFET:- [nmos]

While desinging N-MOS we have to take p-type of substrate and it has two n-type of diffusions to form drain and source terminals for extracting gate, drain and Source terminals polysillicon and metal contacts are use for necessary leads. Here we have to apply a suitable positive voltage at the gate terminal to create channel blw drain and Source



Operation of NMOS:-

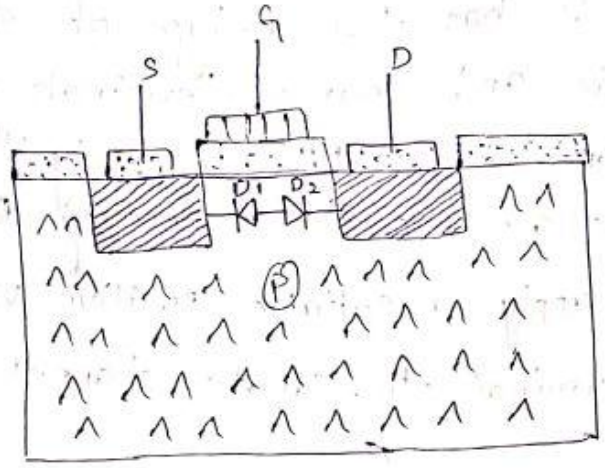
The designing of N-mos includes Considering a P-type of substrate and to heavily doped n+ impurities are diffuse into p-type of substrate to get drain and Source terminals.

Case (1):-

When $V_{gs}=0V$

When $V_{gs}=0V$ no channel will be form and no current condition takes place.

* Here when $V_{gs}=0$ we can find two junction diodes that are connected in series back to back manner in b/w drain and source and these two diodes are in reverse bias condition.



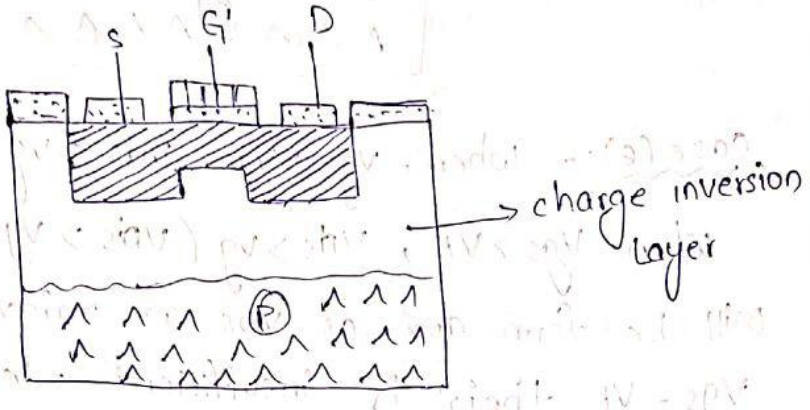
Case (2):- when $V_{gs}>0V$, means we are applying Some possible voltage at the gate terminal then the majority charge carriers in N-mos that is holes will get repelled by an amount of voltage applied at the gate terminal.

* If We increase the gate potential step by step then the holes in the substrate will get

rippled and pushed down leaves a depletion region b/w drain and source. Hence it is called charge inversion layer.

* After having a charge inversion layer the holes in the gate terminal will get attracted to n+ diffusions present in drain and source terminals, thereby forming N-channel b/w drain and source.

** Note:- The voltage at which charge inversion layer forms and the gate terminal can be inverted is called threshold voltage of mos device.



Case(3):- when $V_{gs} < V_t$, $V_{DS} = 0$

No channel will be form and hence no current conduction takes place i.e., $I_{DS} = 0$

Case (4):- $V_{gs} > V_t$, $V_{DS} = 0$

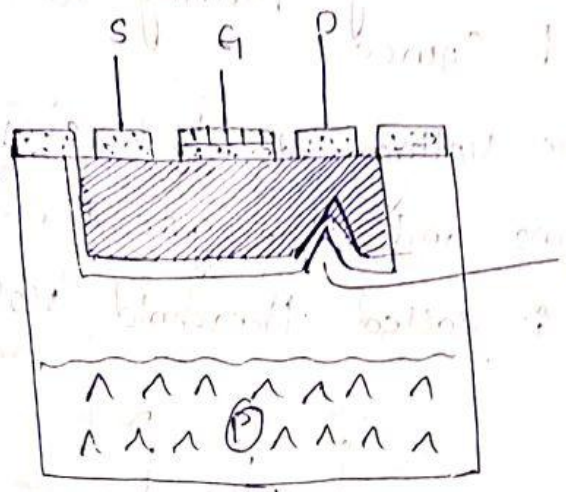
when $V_{gs} > V_t$ then channel will be form but no current conduction takes place i.e., cutoff region.

Active region → current conduction takes place

Saturation region → Acts as constant current source

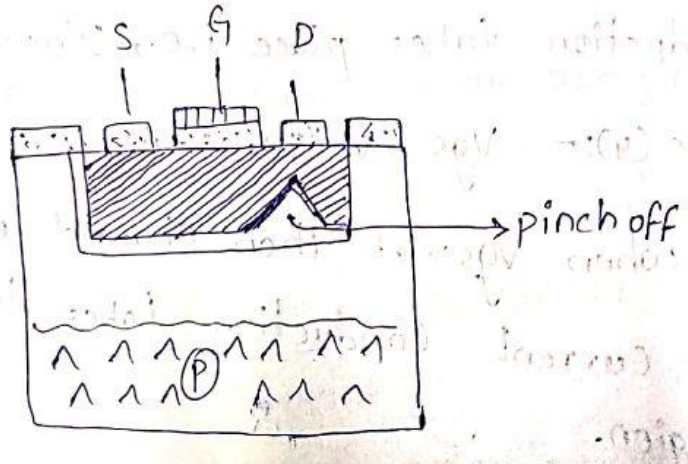
Case(5):- when $V_{gs} > V_t$, $V_{ds} \leq V_g$

When $V_{gs} > V_t$ channel will be form, when $V_{DS} = V_g$ ($V_{DS} = V_{gs} - V_t$) then near drain terminal their is an insufficient electric field and it is in non-saturation condition.



Case(6):- when $V_{gs} > V_t$, $V_{ds} \geq V_g$

When $V_{gs} > V_t$, $V_{DS} > V_g$ ($V_{ds} > V_{gs} - V_t$) then channel will be form and as V_{DS} as raised greater than $V_{gs} - V_t$ their is insufficient electric field near the drain terminal which causes the channel pinch off



Here when $V_{gs} > V_t$, $V_{ds} > V_{gs} - V_t$ it is in saturation mode and hence acts as constant current source.

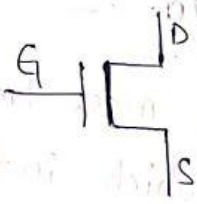
Note:- for an enhancement mode n-mos the channel will be created by applying a suitable positive voltage at the gate terminal.

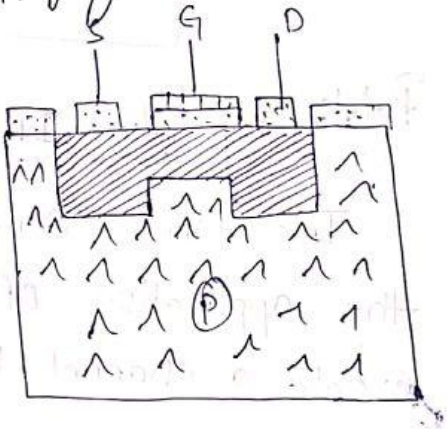
* If it is p-MOS, to create channel we need to apply negative voltage at the gate terminal.

Depletion Mode N-MOS:-

In Depletion mode MOSFET it is having an inbuilt channel that is no need to apply external voltage.

In this depletion mode n-mos the channel will be created blw drain and source prior to Manufactoring stage before applying insulating and metals.



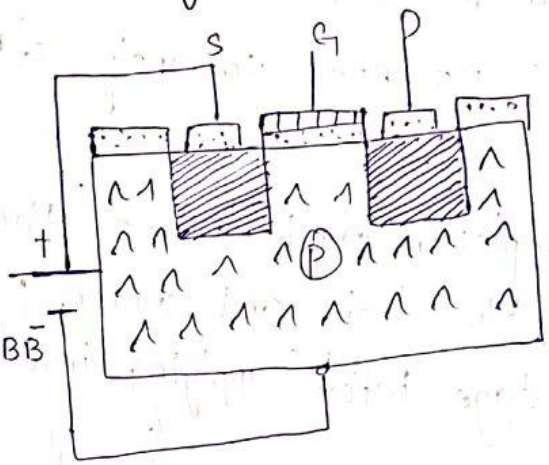


Body Mass effect:-

Note:- Depletion mode N-mos is always ON. If you want to remove channel, we need to apply the Negative voltage at the gate terminal.

Body Mass Effect:-

-for N-mos, basically the source voltage and Body potential should be equal that is $V_S = V_B = 0$. If $V_B \neq 0$ i.e., it is having some inbuilt possible potential than it causes an effect on threshold voltage. hence threshold voltage level is increased. to avoid this the body is connected to suitable negative voltage w.r.to source hence this effect is called Body Mass effect.



Relationship b/w I_{ds} Vs V_{ds} :-

The whole concept of mass transistor revolves the application of V_{gs} which in turn causes to create a channel b/w drain and source.

∴ The current I_{ds} is a dependent on both V_{gs} and V_{ds}.

The current I_{ds} can be given by

$$I_{ds} = -I_{sd}$$

$$\therefore I_{ds} = \frac{Q_c}{\tilde{\tau}_{ds}} \longrightarrow (1)$$

where Q_c is charge and

$\tilde{\tau}_{ds}$ is electron transit time

we know that $\tilde{\tau}_{ds} = \frac{L}{v} \longrightarrow (2)$

where L = length of the channel and

v = velocity

The velocity 'v' can be given as

$$v = \mu E_{ds} \longrightarrow (3)$$

where μ is called mobility constant

E_{ds} = Effective electric field b/w drain and source.

$$E_{ds} = \frac{V_{ds}}{L} \longrightarrow (4)$$

Sub (4) in (3)

$$v = \mu E_{ds}$$

$$V = \mu \frac{V_{ds}}{L} \longrightarrow (5)$$

Sub (5) in (2)

$$\tilde{\tau}_{ds} = \frac{L}{v}$$

$$\tilde{\tau}_{ds} = \frac{L}{\frac{\mu V_{ds}}{L}}$$

$$\tilde{\tau}_{ds} = L^2/\mu V_{ds} \longrightarrow (6)$$

Sub (6) in (1)

$$I_{ds} = \frac{Q_c}{\tau_{ds}}$$

$$I_{ds} = \frac{Q_c}{\frac{L^2}{\mu V_{ds}}}$$

$$\boxed{I_{ds} = \frac{Q_c \mu V_{ds}}{L^2}}$$

* μ_n - 650 $cm^2/vsec$
μ_p - 240 $cm^2/vsec$ at room temperature

Case (1):- Non-saturation

when it is in non-saturation then the effective voltage is $\frac{V_{ds}}{2}$.

The charge 'Q_c' can be given as

$$Q_c = E_g \varepsilon_0 \varepsilon_{ins} \omega L \longrightarrow (1)$$

where E_g is effective gate voltage

ε_0 is permittivity of free space

$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

ε_{ins} = Relative Permittivity

$\varepsilon_{ins} = 4$ (for silicon)

ω = width

L = length

we know that $E_g = \frac{\left[V_g - \frac{V_{ds}}{2}\right]}{D}$

where D = oxide thickness,

wkt $V_g = V_{gs} - V_t$

$$E_g = \frac{\left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right]}{D} \longrightarrow (2)$$

$$Q_c = \frac{\left[(V_{gs}-V_t)-\frac{V_{ds}}{2}\right]}{D} \varepsilon_0 \varepsilon_{ins} \omega L$$

$$Q_c = \left[(V_{gs}-V_t)-\frac{V_{ds}}{2}\right] \frac{\varepsilon_0 \varepsilon_{ins} \omega L}{D} \longrightarrow (3)$$

ωKT

$$I_{ds} = \frac{Q_c \mu V_{ds}}{L^2}$$

Sub eqn (3) in I_{ds}, we get

$$I_{ds} = \left[(V_{gs}-V_t)-\frac{V_{ds}}{2}\right] \frac{\varepsilon_0 \varepsilon_{ins} \omega}{D} \frac{\mu V_{ds}}{L}$$

$$I_{ds} = \left[(V_{gs}-V_t)-\frac{V_{ds}}{2}\right] \frac{\varepsilon_0 \varepsilon_{ins} \mu \omega V_{ds}}{DL}$$

$$I_{ds} = \left[(V_{gs}-V_t)V_{ds}-\frac{V_{ds}^2}{2}\right] \frac{\varepsilon_0 \varepsilon_{ins} \mu}{D} \frac{\omega}{L}$$

Let $k = \frac{\varepsilon_0 \varepsilon_{ins} \mu}{D}$

$$\boxed{I_{ds} = \frac{k\omega}{L}\left[(V_{gs}-V_t)V_{ds}-\frac{V_{ds}^2}{2}\right]}$$

Let $\frac{k\omega}{L} = \beta$

$$\boxed{I_{ds} = \beta\left[(V_{gs}-V_t)V_{ds}-\frac{V_{ds}^2}{2}\right]}$$

$$C_g = \frac{k\omega L}{\mu} \Rightarrow k = \frac{C_g \cdot \mu}{\omega L}$$

C_g = gate to channel capacitance

$$I_{ds} = \frac{C_g \mu}{\not{W} L} \cdot \frac{\not{W}}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

$$\boxed{I_{ds} = \frac{C_g \mu}{L^2}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]}$$

WKT $C_g = C_o W L$

$$\boxed{I_{ds} = \frac{C_o W \mu}{L^2}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]}$$

Case(2):- Saturation $[V_{ds} = V_{gs} - V_t]$

$$I_{ds} = \frac{kw}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \longrightarrow (1)$$

→ Saturation starts at $V_{ds} = V_{gs} - V_t$

→ $$I_{ds} = \frac{kw}{L}\left[V_{ds}^2 - \frac{V_{ds}^2}{2}\right]$$

$$I_{ds} = \frac{kw}{L}\left[\frac{V_{ds}^2}{2}\right]$$

$$\boxed{I_{ds} = \frac{kw}{L}\left[\frac{(V_{gs} - V_t)^2}{2}\right]}$$

let $\frac{kw}{L} = \beta$

$$\boxed{I_{ds} = \beta\left[\frac{V_{gs} - V_t}{2}\right]^2}$$

$$I_{ds} = \frac{kw}{L}\left[\frac{(V_{gs} - V_t)^2}{2}\right]$$

WKT $C_g = \frac{K W L}{\mu} \Rightarrow K = \frac{C_g \cdot \mu}{WL}$

$\Rightarrow I_{ds} = \frac{C_g \mu}{WL} \frac{W}{L} \cdot \left[\frac{(V_{gs}-V_t)^2}{2}\right]$

$$\boxed{I_{ds} = \frac{C_g \mu}{L^2}\left[\frac{(V_{gs}-V_t)^2}{2}\right]}$$

WKT $C_g = C_o W L$

$I_{ds} = \frac{C_o W L \mu}{L^2} \left[\frac{(V_{gs}-V_t)^2}{2}\right]$

$$\boxed{I_{ds} = \frac{C_o W \mu}{L}\left[\frac{(V_{gs}-V_t)^2}{2}\right]}$$

Trans Conductance (g_m)

Trans conductance is defined as the relationship between output current 'I_{ds}' and input voltage 'V_{gs}'.

$\because g_m = \left.\frac{\delta I_{ds}}{\delta V_{gs}}\right|_{V_{ds} = \text{constant}}$

WKT $I_{ds} = \frac{Q_c}{\tilde{T}_{ds}}$

$\tilde{T}_{ds} = \frac{L^2}{\mu V_{ds}}$

$$\boxed{I_{ds} = \frac{Q_c \mu V_{ds}}{L^2}}$$

$$\boxed{\delta I_{ds} = \frac{\delta Q_c \mu V_{ds}}{L^2}}$$

WKT $C_g = \frac{K W L}{\mu} \Rightarrow K = \frac{C_g \cdot \mu}{WL}$

$\Rightarrow I_{ds} = \frac{C_g \mu}{WL} \frac{W}{L} \cdot \left[\frac{(V_{gs} - V_t)^2}{2}\right]$

$$\boxed{I_{ds} = \frac{C_g \mu}{L^2} \left[\frac{(V_{gs} - V_t)^2}{2}\right]}$$

WKT $C_g = C_o W L$

$I_{ds} = \frac{C_o W L \mu}{L^2} \left[\frac{(V_{gs} - V_t)^2}{2}\right]$

$$\boxed{I_{ds} = \frac{C_o W \mu}{L} \left[\frac{(V_{gs} - V_t)^2}{2}\right]}$$

Trans Conductance (g_m)

Trans conductance is defined as the relationship between output current 'I_{ds}' and input voltage 'V_{gs}'.

$\because g_m = \left.\frac{\delta I_{ds}}{\delta V_{gs}}\right|_{V_{ds} = \text{constant}}$

WKT $I_{ds} = \frac{Q_c}{\tau_{ds}}$

$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$

$$\boxed{I_{ds} = \frac{Q_c \mu V_{ds}}{L^2}}$$

$$\boxed{\delta I_{ds} = \frac{\delta Q_c \mu V_{ds}}{L^2}}$$

WKT

$$C_g = \frac{Q_c}{V_{gs}}$$

$$V_{gs} = \frac{Q_c}{C_g}$$

$$\boxed{\delta V_{gs} = \frac{\delta Q_c}{C_g}}$$

$$\therefore g_m = \frac{\delta I_{ds}}{\delta V_{gs}}$$

$$= \frac{\frac{\delta Q_c \mu V_{ds}}{L^2}}{\frac{\delta Q_c}{C_g}}$$

$$\boxed{g_m = \frac{C_g \mu V_{ds}}{L^2}}$$

WKT $C_g = C_o \omega L$

$$\therefore g_m = \frac{C_o \omega L \mu V_{ds}}{L^2}$$

$$\boxed{g_m = \frac{C_o \omega \mu V_{ds}}{L}}$$

Output Conductance [g_{ds}]:-

The output conductance g_{ds} is defined as the relationship between output current I_{ds} and input voltage V_{gs}.

$$g_{ds} = \left.\frac{I_{ds}}{V_{gs}}\right|_{V_{ds}=\text{constant}}$$

WKT $I_{dc} = \frac{Q_c \mu V_{ds}}{L^2}$ and $V_{gs} = \frac{Q_c}{C_g}$

$\therefore$ $g_{ds} = \frac{\frac{Q_c \mu V_{ds}}{L^2}}{\frac{Q_c}{C_g}}$

$$\boxed{g_{ds} = C_g \frac{\mu V_{ds}}{L^2}}$$

$\therefore$ $\boxed{g_{ds} \propto \frac{1}{L^2}}$

An increase in the channel length of a device may cause reduce output conductance g_{ds}.

Figure of Merit (ω_0):-

The figure of merit ω_0 is defined as the ratio of transconductance to the gate to channel capacitance (C_g).

$\therefore$ $\boxed{\omega_0 = \frac{g_m}{C_g}}$

WKT $g_m = \frac{C_g \mu V_{ds}}{L^2}$

$\omega_0 = \frac{\frac{C_g \mu V_{ds}}{L^2}}{C_g}$

$$\therefore W_D = \frac{\mu V_{ds}}{L^2}$$

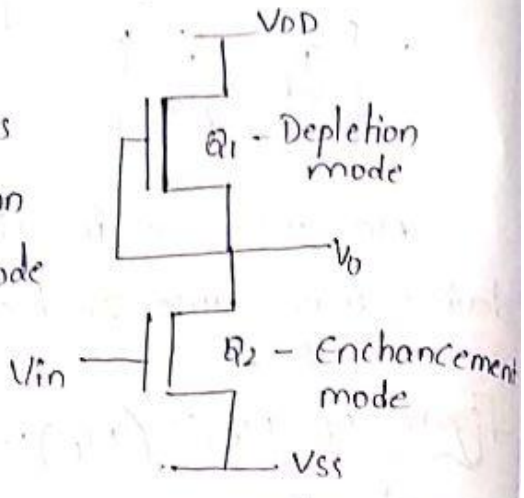
Since $V_{ds} = V_{gs} - V_t$

$$\boxed{W_D = \frac{\mu (V_{gs} - V_t)}{L^2}}$$

N-MOS Inverter:-

The N-mos inverter is more oftenly use and it can produce full amount of logic levels.

Description:-



* The arrangement of nmos inverter consists of depletion mode and enchancement mode transistors.
* Here the gate terminal of depletion mode nmos is connected to the drain terminal of enchancement mode nmos.
* The depletion mode transistor is always on because of the inbuilt channel.

Operation:-

Case(1):-

When Vin is logic '1'

When Input is logic 1 the transistor Q_2 turns ON and transistor Q_1 is always turns ON because it is depletion mode

Truth Table:-

V_{in}	Q_1	Q_2	V_o
0	ON	OFF	1
1	ON	ON	0

then Vout is logic 0.

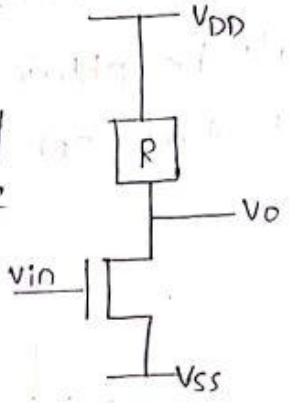
Case(2):-

When V_1 is logic '0'

When input is logic '0' then the transistor Q2 remains OFF and Q1 is ON hence the o/p voltage is logic '1'.

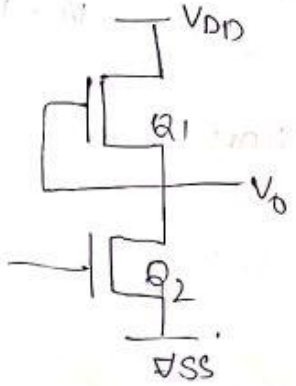
Alternative Forms of pull-up:-

1. Resistive pull-up:- the Resistive pull-up configuration is not oftenly used while designing silicon substrate because high Resistive values are not incooperated in that silicon substrate.



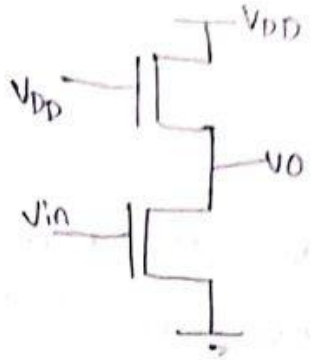
2. Depletion mode pull-up:-

It can produce High power disspitation and there may be a current flow in blw supply rails when vin is logic '1'.



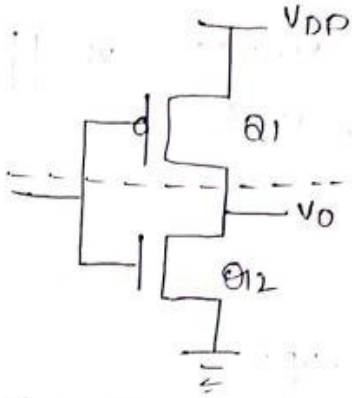
3. Enchancement mode pull-up:-

It produces high power disspiation blw supply rails and conduction starts when $V_{DD} = V_{gg}$



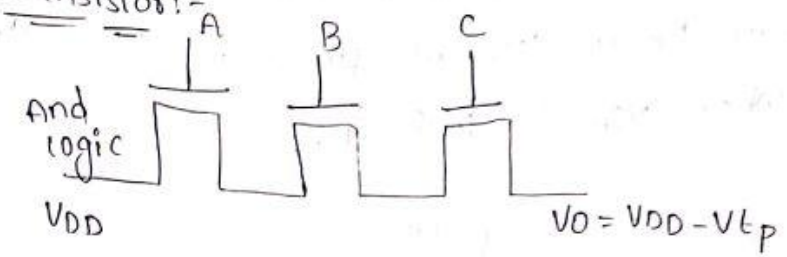
4. Complementary mass pull-up:-

In this configuration full-amount of logic level can't be obtained and only one transistor will get turn ON either for logic '0' or (1).



Pass transistor:-

Eg:-



* unlike Bipolar transistors

pullup to pulldown ratio of nmos-inverter driven by another nmos inverter :-

The arrangement of pullup to pulldown ratio for one nmos inverter driven by another nmos is shown as below.

WKT

I_{ds} for saturation mode

$$I_{ds} = \frac{k w}{L}\left[\frac{(V_{gs}-V_t)}{2}\right]^2$$

for depletion mode $V_{gs}=0$

$$I_{ds} = k\frac{w_{pu}}{L_{pu}}\left[\frac{(-V_{td})}{2}\right]^2 \longrightarrow (1)$$

I_{ds} for enchancement mode, $V_{gs} = V_{inv}$

$$I_{ds} = \frac{k w_{pd}}{L_{pd}}\left[\frac{(V_{inv}-V_t)^2}{2}\right] \longrightarrow (2)$$

equating ① and ②, ① = ② we get

$$\frac{k w_{pu}}{L_{pu}}\frac{(-V_{td})^2}{2} = \frac{k w_{pd}}{L_{pd}}\frac{(V_{inv}-V_t)^2}{2}$$

$$\frac{1}{Z_{pu}}(-V_{td})^2 = \frac{1}{Z_{pd}}(V_{inv}-V_t)^2$$

$$(-V_{td})^2 = \frac{Z_{pu}}{Z_{pd}}(V_{inv}-V_t)^2$$

$$\frac{Z_{pu}}{Z_{pd}} = \frac{(-V_{td})^2}{(V_{inv}-V_t)^2}$$

$$\frac{Z_{pu}}{Z_{pd}} = \frac{(0.6V_{DD})^2}{(0.5V_{DD} - 0.2V_{DD})^2}$$

$V_{td} = 0.6V_{DD}$

$V_t = 0.2V_{DD}$

$V_{inv} = 0.5V_{DD}$

$$= \left(\frac{0.6V_{DD}}{0.3V_{DD}}\right)^2$$

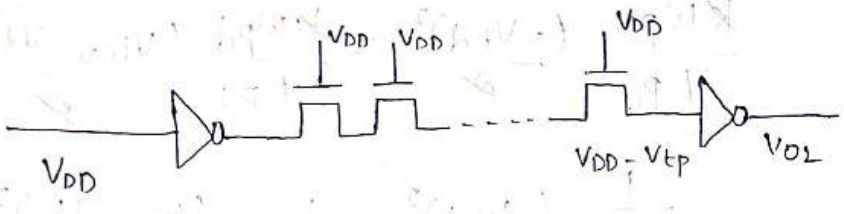
$$\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$$

$$\boxed{\frac{Z_{pu}}{Z_{pd}} = 4:1}$$

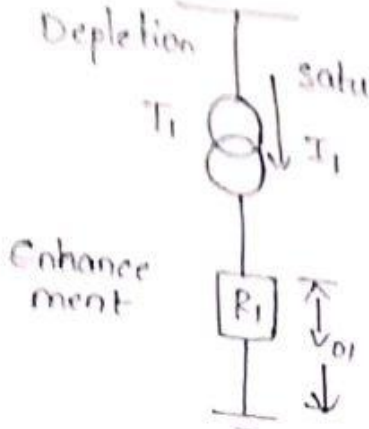
∴ The pullup to pulldown ratio of nmos inverter driven by another nmos is 4:1

Pullup to pulldown ratio of nmos driven by another nmos with one or more pass transistors:-

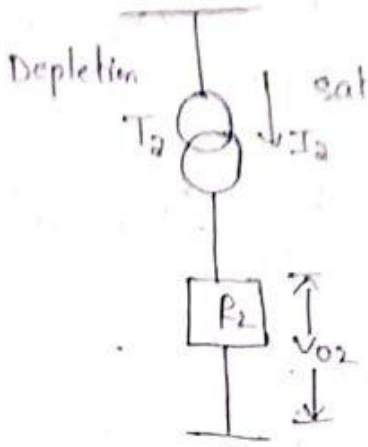
The arrangement of pullup to pulldown ratio for nmos driven by another nmos with one or more pass transistors is depicted as below.



* when the output of inverter 1 is passed through series of pass transistors then full logic levels are not obtain due to threshold voltage of pass transistors. ie., $V_{inv2} = V_{DD} - V_{tp}$.



(a) inv_1 with i/p as V_{DD}



(b) inv_2 with i/p as $V_{DD}-V_{tp}$

for inverter 1

I_{ds} for saturation mode

$$I_{ds} = \frac{kw}{L}\frac{(V_{gs}-V_t)^2}{2}$$

for depletion mode, $V_{gs}=0$

$$I_{ds1} = \frac{k w_{pu1}}{L_{pu1}}\frac{(-V_{td})^2}{2}$$

$$\boxed{I_1 = \frac{K}{Z_{pu1}}\frac{(-V_{td})^2}{2}}$$

for non-saturation, I_{ds} can be similar

$$I_{ds} = \frac{kw}{L}\left[(V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

for enhancement mode, $V_{gs}=V_{DD}$

$$I_{ds1} = \frac{kw_{pd1}}{L_{pd1}}\left[(V_{DD}-V_t)V_{ds1} - \frac{V_{ds1}^2}{2}\right]$$

$$\frac{I_{ds1}}{V_{ds1}} = \frac{kw_{pd1}}{L_{pd1}}\left[(V_{DD}-V_t) - \underbrace{\frac{V_{ds1}}{2}}_{\text{neglecting}}\right]$$

$$\frac{I_{ds1}}{V_{ds1}} = \frac{k}{Z_{pd1}} (V_{DD} - V_t)$$

$$\frac{1}{R_1} = \frac{k}{Z_{pd1}} (V_{DD} - V_t)$$

$$\boxed{R_1 = \frac{Z_{pd1}}{K(V_{DD} - V_t)}}$$

$$V_{O1} = I_1 R_1$$

$$V_{O1} = \frac{K}{Z_{pu1}} \frac{(-V_{td})^2}{2} \times \frac{Z_{pd1}}{K(V_{DD} - V_t)}$$

$$\boxed{V_{O1} = \frac{Z_{pd1}}{Z_{pu1}} \frac{(-V_{td})^2}{2(V_{DD} - V_t)}}$$

For inverter 2

For saturation mode, I_{ds} can be seen by

$$I_{ds} = \frac{k\omega}{L} \frac{(V_{gs} - V_t)^2}{2}$$

For depletion mode, $V_{gs} = 0$

$$I_{ds2} = \frac{k\omega_{pu2}}{L_{pu2}} \frac{(-V_{td})^2}{2}$$

$$\boxed{I_2 = \frac{K}{Z_{pu2}} \frac{(-V_{td})^2}{2}}$$

I_{ds} in non-saturation can be given by

$$I_{ds} = \frac{k\omega}{L} \left[[V_{gs} - V_t] V_{ds} - \frac{V_{ds}^2}{2} \right]$$

For enhancement mode, $V_{gs} = V_{DD} - V_{tp}$

$$I_{ds2} = \frac{k' W_{pd2}}{L_{pd2}} \left[(V_{gs} - V_t) V_{ds2} - \frac{V_{ds2}^2}{2} \right]$$

$$\frac{I_{ds2}}{V_{ds2}} = \frac{k'}{Z_{pd2}} \left[(V_{gs} - V_t) - \underbrace{\frac{V_{ds}}{2}}_{\text{neglecting}} \right]$$

$$\frac{1}{R_2} = \frac{k'}{Z_{pd2}} \left[V_{gs} - V_t \right]$$

$$\therefore \boxed{V_{gs} = V_{DD} - V_{tp}}$$

$$\frac{1}{R_2} = \frac{k'}{Z_{pd2}} (V_{DD} - V_{tp} - V_t)$$

$$\boxed{R_2 = \frac{Z_{pd2}}{k' (V_{DD} - V_{tp} - V_t)}}$$

$$V_{O2} = I_2 R_2$$

$$= \frac{k'}{Z_{pu2}} \frac{(-V_{td})^2}{2} \times \frac{Z_{pd2}}{k' (V_{DD} - V_{tp} - V_t)}$$

$$\boxed{V_{O2} = \frac{Z_{pd2}}{Z_{pu2}} \frac{(-V_{td})^2}{2 (V_{DD} - V_{tp} - V_t)}}$$

$$V_{O1} = \frac{Z_{pd1}}{Z_{pu1}} \frac{(-V_{td})^2}{2 (V_{DD} - V_t)}$$

$$\boxed{V_{O1} = V_{O2}}$$

$$\frac{Z_{pd1}}{Z_{pu1}} \frac{(-V_{td})^2}{2 (V_{DD} - V_t)} = \frac{Z_{pd2}}{Z_{pu2}} \frac{(-V_{td})^2}{2 (V_{DD} - V_{tp} - V_t)}$$

$$\frac{Z_{pd1}}{Z_{pu1}(V_{DD}-V_t)} = \frac{Z_{pd2}}{Z_{pu2}(V_{DD}-V_{tp}-V_t)}$$

$$\frac{Z_{pd2}}{Z_{pu2}} = \frac{Z_{pd1}(V_{DD}-V_{tp}-V_t)}{Z_{pu1}(V_{DD}-V_t)}$$

$$\frac{Z_{pu2}}{Z_{pd2}} = \frac{Z_{pu1}(V_{DD}-V_t)}{Z_{pd1}(V_{DD}-V_{tp}-V_t)}$$

$$\frac{Z_{pu2}}{Z_{pd2}} = \frac{4}{1} \times \frac{V_{DD}-0.2V_{DD}}{(V_{DD}-0.3V_{DD}-0.2V_{DD})}$$

$V_t = 0.2V_{DD}$

$V_{tp} \simeq 0.3V_{DD}$

$$= \frac{4}{1} \times \frac{0.8\,V_{DD}}{0.5\,V_{DD}}$$

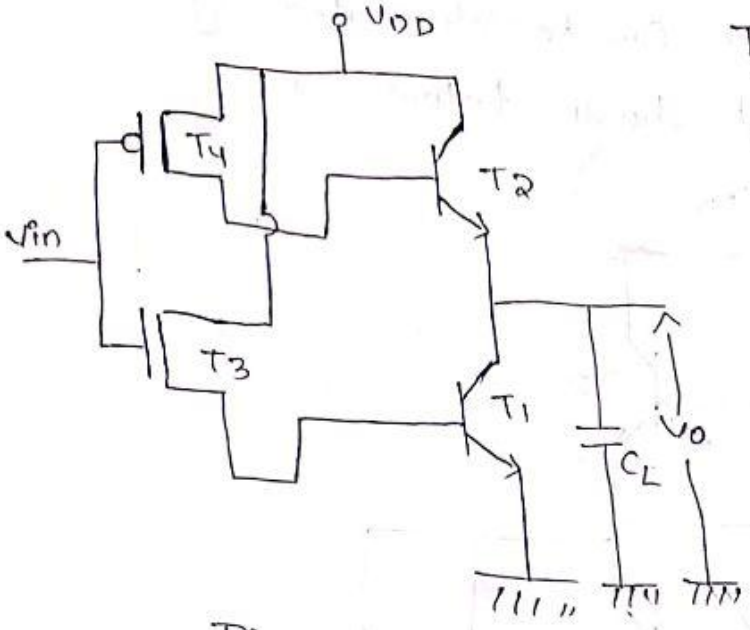
$$\simeq \frac{4}{1} \times \frac{8}{5}$$

$$\boxed{\frac{Z_{pu2}}{Z_{pd2}} \simeq \frac{8}{1}}$$

∴ The pullup to pulldown ratio of nmos driven by another nmos with one or more pass transistors is 8:1

BiCMOS Inverter:-

To get logical switching of mos transistor, bipolar transistors are attach at their ends.



Truth Table

Vin	T_1	T_2	T_3	T_4	V_o
0	OFF	ON	OFF	ON	1
1	ON	OFF	ON	OFF	0

BiCMOS Inverter

operation:-

Case(1):- when Vin = logic '0'.

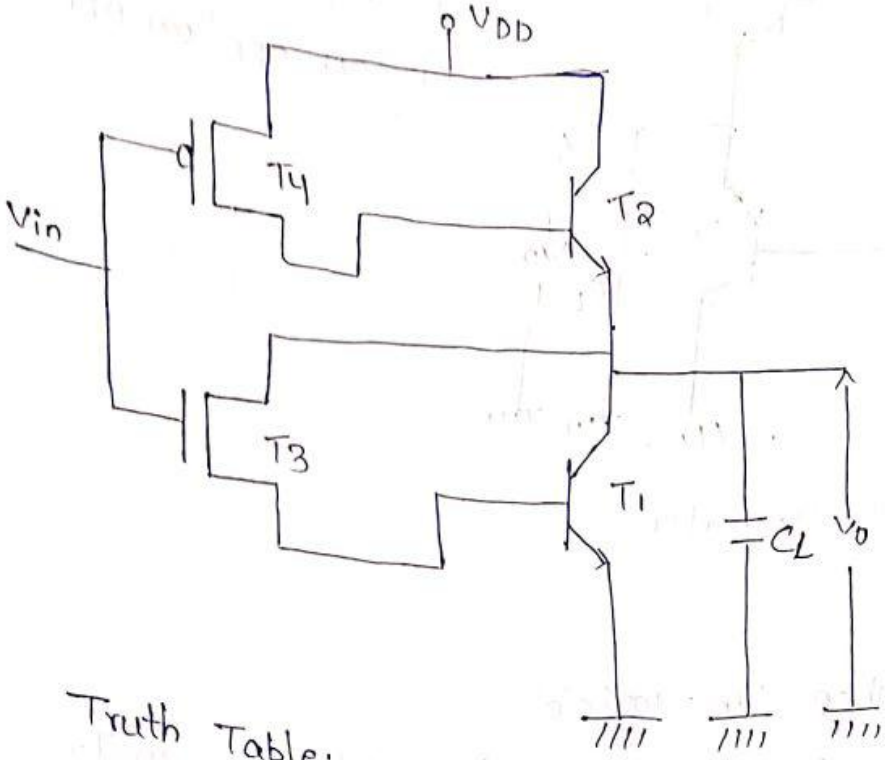
when Vin is logic '0' but transistor T_4 on T_2 will get turn ON and transistor T_3 and T_1 will get turn OFF. then the capacitor C_L gets change hence output is logic 1.

Case(2):- when Vin is logic '1'.

when Vin is logic '1' then t_3 and t_1 will get ON and t_2 and t_4 will get OFF. Here that capacitor C_L gets discharge hence output is logic '0'.

* for logic '1' t_1 and t_3 will get ON and their by it forms a short circuit path between V_{DD} and V_{SS} which inturn cause static power disspiation and this will slowdown transistor action.

* The above drawback can be eliminated by the modified arrangement shown below.



Truth Table:-

Vin	T1	T2	T3	T4	Vo
0	OFF	ON	OFF	ON	1
1	ON	OFF	ON	OFF	0

Alternative BiCMOS with no static power dissipation

* In this circuit for logic '1' their is no short ckt path between V_{DD} and V_{SS}, means their is no static power dissipation.

* Hence output swing is reduce.

Since output voltage can't fall below the base emitter of T_2 that is V_{BE} of T_2 and this can be overcome by another improved circuit shown below.

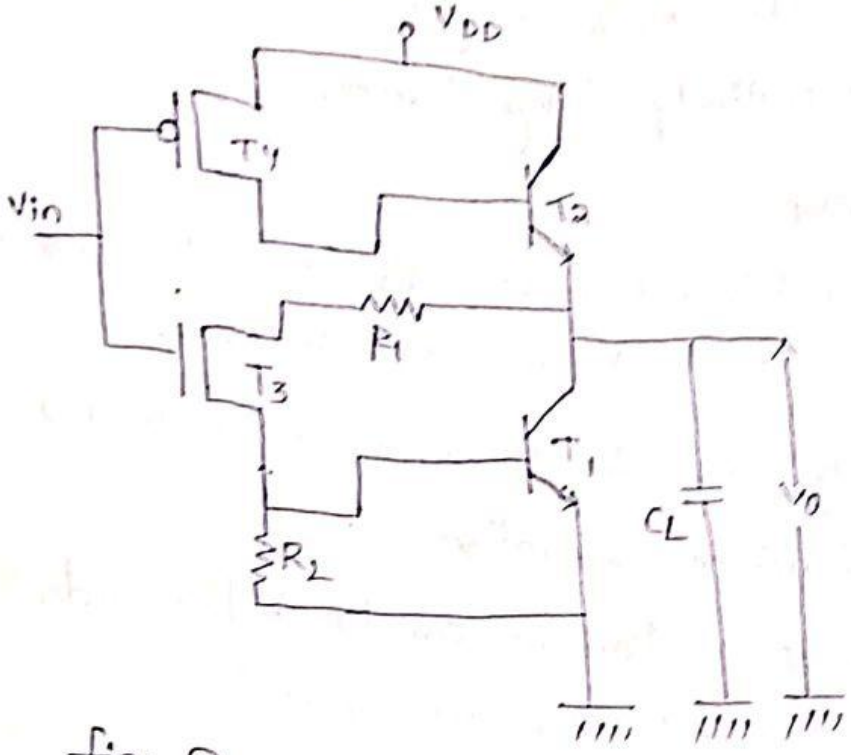


fig: Improved Bicmos with Better logic levels

* In this arrogement the resistors provide the improved swing of output voltages when BJT's are off and also provide discharge path for Base Currents during turn off.

* However the profision of onchip Resistors of Suitable value is not always convient and maybe Space consuming so the above circuit may be further modified as shown below.

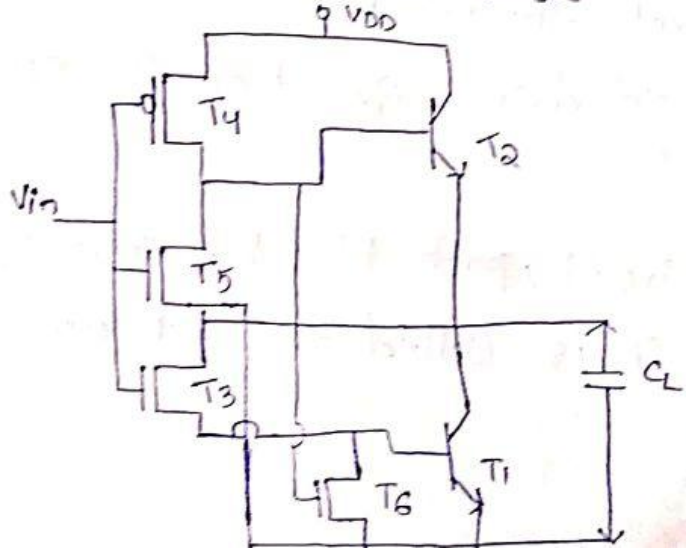
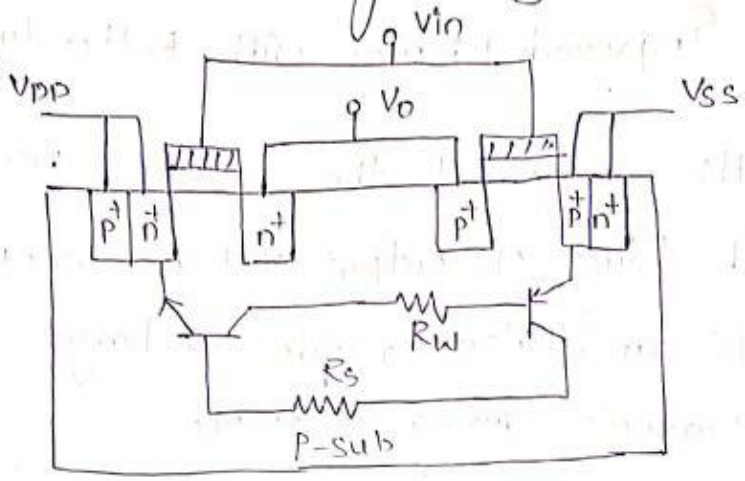


fig: Improve bicmos Inverter using mos transistors for base current drive

The Transistors T_5, T_6 will get turn ON when T_1 and T_2 respectively being turn off.

Latch up in CMOS:-

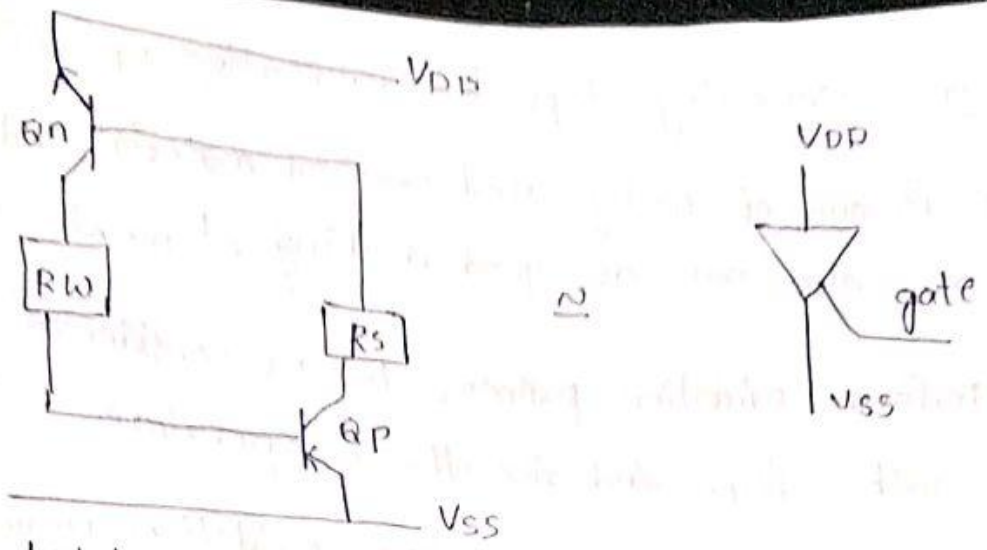
* Latch of is a inherent problem in CMOS, that provide a low impedance path between V_{DD} and V_{SS}.
* latch up may arise due to noise, switch ON and OFF or by Incident radiation.
* The latch up mechanism can be better understood with the following arrangement



Latch up effecting n-well substrate

* In the above figure, if Sufficient substrate current flows for Q_P, then Q_P will turn ON & it draws some current through R_S.
* If it is enough to drive Q_n then it will also turn ON.

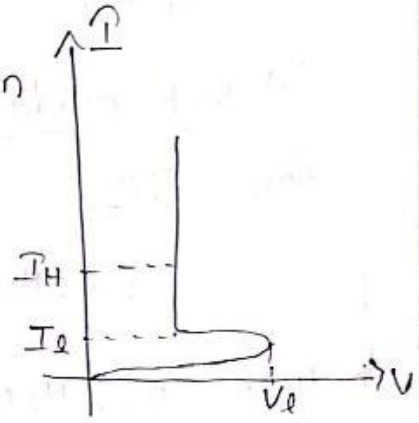
Hence a short circuit path blw V_{DD} and V_{SS} is obtained and it is called as latch up problem.



Latch up circuit model

* The swinging characteristics of the arrangement are shown as below.

* once it is latch, this condition will be maintain untill latch up Current drops below I_L



latch up V I Characteristics of SCR.

Remidies for latch up:-

* Introduction of gard rings Can eliminate latch up problem.

* Increase in the substrate dopping levels, with a constitute drop in the value of Rs.

* Reduce Rw by control of fabrication parameters and by ensuring low contact resistance to Vss.

* **Oxidation:-** Processing steps for fabrication of ICs:

Silicon is one of mostly used oxidised material and which may also acts as good masking element.

* To perform oxidation process let us consider a furnace with silicon and rise the temperature.

* Oxidation is two types 1) Dray oxidation: Here the silicon is reacting with O_2 to form SiO_2.

$$Si + O_2 \longrightarrow SiO_2$$

2) Wet oxidation: Silicon reacts with H_2O to form SiO_2.

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

* Here O_2, H_2O are called oxidants that are use to oxidise silicon.

* **Ion implantation:-**

ion implantation process is use to diffuse the dopands into a specified material (or) Substrate.

* Here the dopand is to be diffuse into a substrate material with a sufficient energy.

* By the strength of the dopand it penterates through the substrate and may cause some effect on lattice atom.

Nuclear stoping:- when the dopand is injected into the Substrate, depending upon the strength the dopand

may change the position of lattice atom and may damage the lattice atom. If the strength is further more increase. Hence it is called Nuclear stoping.

electronic
* During ion implantation process, if the dopands change the position of the lattice atom and it is shows no damage of lattice atom. Hence it is called electronic stoping.

* photolithography (or) Lithography :-
(light → photo, stone → litho)

photolithography is a process that is used to diffuse dopands into substrate in a selected position through masking element.

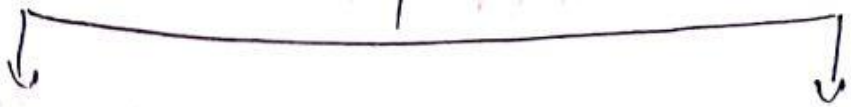
i.e; Lithography (or) photolithography is the process of transfering geometrical patterns from masking element to silicon.

* In olden days, we don't have photolithography technology then a mask of suitable pattern is transfer into silicon using a litho (stone).

* Metalization :-

Metalization is the process that is use to extact terminals from the device. these terminals are used to have contact to the outside world that is means to measure output (throughput).

Metalization



ohmic contacts (Al)

Normal silicides (poly + silicon)

* Encapsulation:-

Encapsulation is the process that is use after manufacturing of the device.

Encapsulation provides protection to the whole body (or) package.

Unit-2

Basic Circuit Concepts

Sheet Resistance :-

The sheet resistance is a measure of resistance of thin films that have a uniform thickness

* It is used to characterize materials by semiconductor doping, metal deposition, resistive paste printing and glass coating.
* Example of these processes are : doped semiconductor regions (eg : silicon or polysilicon) and resistors
* Sheet resistance is applicable to 2-dimensional systems where thin film is considered to be a 2-dimensional entity.
* It is same to resistivity as used in 3-dimensional systems
* when the sheet resistance is used, the current must be flowing along the plane of the sheet, not perpendicular to it
* Consider a uniform slab of conducting material of resistivity ρ, of width w, thickness t, and length between faces L. The arrangement is shown in fig

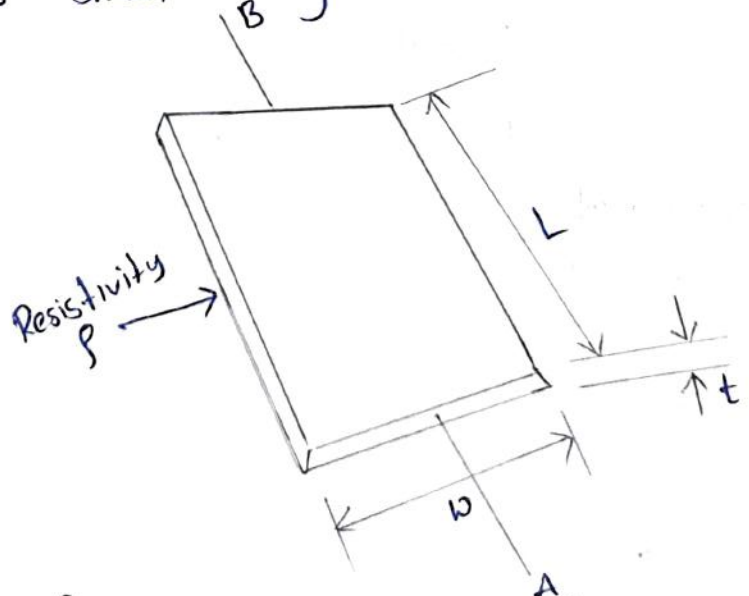


fig: Sheet resistance model

* Consider the resistance R_{AB} between two opposite face

$$R_{AB} = \frac{\rho l}{A} \text{ ohm}$$

A = cross-section area = tw

Thus $$R_{AB} = \frac{\rho l}{tw} \text{ ohm}$$

* consider the case in which $l = w$, that is, a square of resistive material then

$$R_{AB} = \frac{\rho}{t} = R_S$$

R_S = ohm per square or sheet resistance

$$R_S = \frac{\rho}{t} \text{ ohm per square}$$

* Typical sheet resistances of R_S of MOS Layers for 5μm, & orbit 2 μm, & 1.2μm technologies

	R_S ohm per square		
	5μm	2μm	orbit 1.2μm
metal	0.03	0.04	0.04
Diffusion	10 → 50	20 → 45	20 → 45
Silicide	2 → 4	—	—
polysilicon	15 → 100	15 → 30	15 → 30
n-transistor channel			
p-transistor channel			

Sheet Resistance Concept Applied to MOS Transistors and Inverters

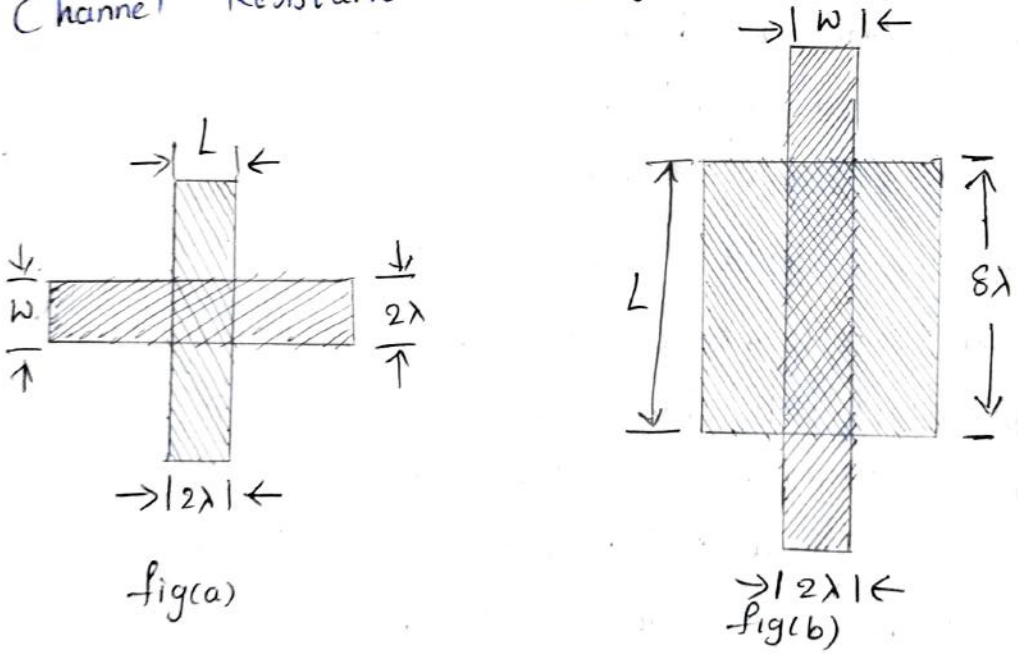
* consider the transistor structures of fig1. the simple n-type pass transistor length $L = 2\lambda$ and a channel width $W = 2\lambda$. The channel is square & channel resistance with or without implant is

$$R = 1 \text{ square} \times R_s \frac{\text{ohm}}{\text{square}} = R_s = 10^4 \Omega$$

* The length to width ratio, denoted by Z, is 1:1, in this case. The transistor structure of fig(b) has a channel length $L = 8\lambda$ and width $W = 2\lambda$

$$Z = \frac{L}{W} = 4$$

Channel Resistance $R = Z R_s = 4 \times 10^4$ ohm



fig(a) fig(b)

fig : Resistance calculation for transistor channel

* the channel is taken as $2\lambda \times 2\lambda$ squares in series

Calculation of ON Resistance of a Simple Inverter :-

* consider the simple nMOS inverter in fig

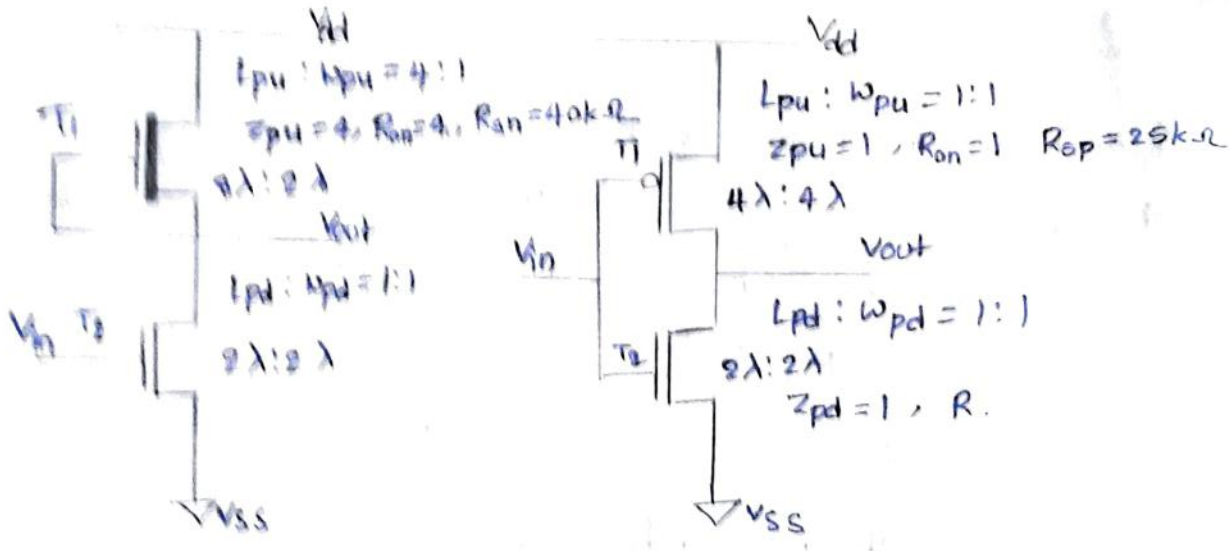


fig : (a) NMOS inverter (b) CMOS Inverter resistance calculation

* From fig(a)
* For the pull-up transistor (depletion mode MOSFET) the L:W value is 4:1, hence the value of Z is 4, $R_{on} = 4$ and value of on resistance is $4R_s$ i.e $4 \times 10^4 = 40k\Omega$
* Similarly for pull down transistor (enhancement mode MOSFET) the L:W value is 1:1 hence the value of Z is 1 $R_{on} = 1$ and value of resistance is $1R_s$ i.e $1 \times 10^4 = 10k\Omega$
* Consider the simple CMOS inverter in fig(b)
* For pull-up transistor (p-enhancement mode MOSFET) the L:W value is 1:1, hence the value of Z is 4 $R_{on} = 4$ value of resistance is $4R_s$ i.e $1 \times 25 \times 10^4 = 25k\Omega$
* Similarly, for the pull down transistor (n-enhancement mode MOSFET) the L:W value is 1:1 hence Z is 1, $R_{on} = 1$ & value of resistance is $1R_s$ i.e $1 \times 10^4 = 10k\Omega$.
* In this case there is no static resistance b/w V_{DD} and V_{SS} Since at any point of time only one transistor is ON, but not both
* when $V_{in} = 1$ the ON Resistance is $10k\Omega$, when $V_{in} = 0$ the ON Resistance is $25k\Omega$

Area capacitance of Layers :-

from the concept of the transistors, it is apparent that as gate is separated from the channel by gate oxide an insulating Layer, it has capacitance. similarly, different Interconnects run on the chip and each layer is separated by Silicon dioxide

Area capacitance can be calculated as $C = \frac{\varepsilon_0 \varepsilon_{ins} A}{D}$ farads

D = thickness of silicon dioxide

A = Area of plates

ε_{ins} = Relative permittivity of SiO_2

$\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm (permittivity of free space)

* The layer area capacitance are given below

Capacitance	value in pF $\times 10^{-4}/\mu m^2$ (Relative values in brackets)		
	5 μm	2 μm	1.2 μm
Gate to channel	4 (1.0)	8 (1.0)	16 (1.0)
Diffusion	1 (0.25)	1.75 (0.22)	3.75 (0.23)
polysilicon to substrate	0.4 (0.1)	0.6 (0.075)	0.6 (0.088)
Metal 1 to Substrate	0.3 (0.075)	0.33 (0.04)	0.33 (0.02)
Metal 2 to Substrate	0.2 (0.05)	0.17 (0.02)	0.17 (0.01)
Metal 2 to metal 1	0.4 (0.1)	0.5 (0.06)	0.5 (0.03)
metal 2 to polysilicon	0.3 (0.075)	0.3 (0.038)	0.3 (0.018)

Table : Typical Area capacitance value for Nos Circuits

Standard unit of capacitance :-

A standard unit is employed that can be used in calculations. The unit is denoted as C_g and is defined as the gate to channel capacitance of a MOS transistor having W = L = feature size that is a 'standard' or 'feature size' square

* C_g may be evaluated for any MOS process
* For example, for 5μm MOS circuits

Area / standard square = $5\mu m \times 5\mu m = 25\mu m^2$

Capacitance value = 4×10^{-4} pF/μm²

Standard value $C_g = 25\mu m^2 \times 4 \times 10^{-4}$ pF/μm² = 0.01pF

* For 2μm MOS circuits

Area/standard square = $2\mu m \times 2\mu m = 4\mu m^2$

Gate capacitance value = 8×10^{-4} pF/μm²

Standard value $C_g = 4\mu m^2 \times 8 \times 10^{-4}$ pF/μm² = 0.0032pF

* For 1.2μm MOS circuits

Area/standard square = $1.2\mu m \times 1.2\mu m = 1.44\mu m^2$

Gate capacitance value = 16×10^{-4} pF/μm²

Standard value $C_g = 1.44\mu m^2 \times 16 \times 10^{-4}$ pF/μm²

= 0.0023pF

Some Area capacitance calculations :-

* The approach will be demonstrated using λ-based geometry
* The capacitance values obtained by establishing the ratio between the area of interest and the area of standard gate ($2\lambda \times 2\lambda$ for λ-based rules) and multiplying this ratio by the appropriate 'C' value. The product will give C_g

*Consider the area defined in fig, the Relative area to that of Standard gate is

$$\text{Relative area} = \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda} = 15$$

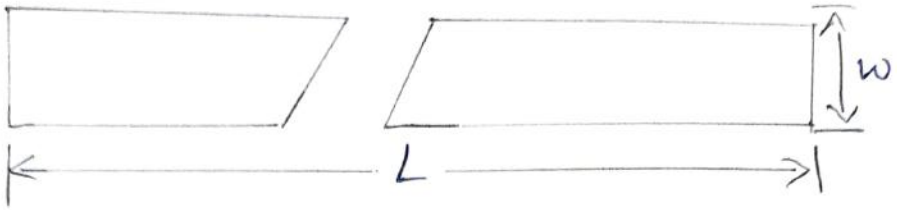


fig: Simple area for Capacitance calculations

Now,

1. Consider the area in metal

Capacitance to substrate = Relative area × Relative C value

$= 15 \times 0.0750\ C_g$

$= 1.125\ C_g$

2. consider the same area in polysilicon

Capacitance to substrate $= 15 \times 0.1\ C_g$

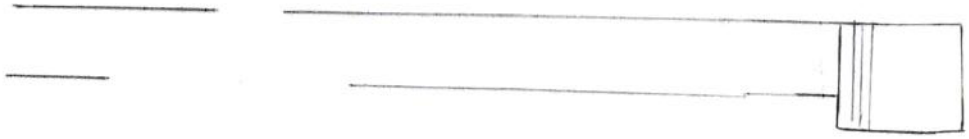
$= 1.5\ C_g$

3. Consider the same area in n-type diffusion

Capacitance to substrate $= 15 \times 0.25\ C_g$

$= 3.75\ C_g$

* calculations of area capacitance values with structures occupying more than one layer as shown below figure are equally straight-forward.

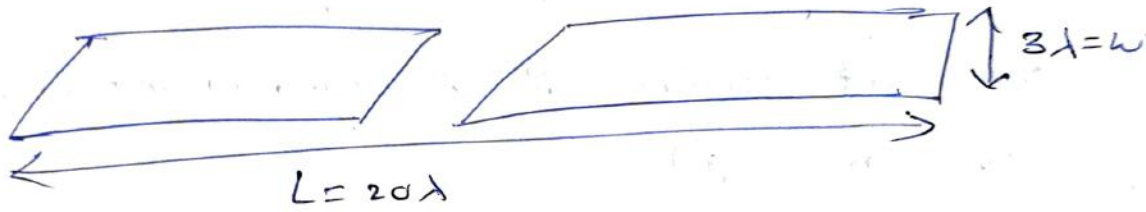


Area capacitance Calculations

→ In this the relative values of capacitance can be used for the representation of capacitance and all values carried out in 'λ' based rules

→ 'Relative area' can be represented as the ratio of 'Area of interest' to the standard area

$$\text{Relative area} = \frac{\text{Area of interest}}{\text{standard area}}$$



$$\text{Relative area} = \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda}$$

$$= \frac{60\lambda^2}{4\lambda^2}$$

$$= 15$$

for 5μm technology

(i) The capacitance to substrate is can be given as

* Relative area × Capacitance

$= 15 \times 0.0750 C_g = 1.1250 C_g$

∴ The capacitance to substrate is 1.125 C_g times of square C_g ($\square C_g$)

(2) The diffusion capacitance can be calculated as

= Relative area × Capacitance

$= 15 \times 0.25 \square C_g = 3.75 \square C_g$

∴ The diffusion capacitance is 3.75 times of $\square C_g$

For polysilicon

The capacitance for polysilicon can be calculated

CP = Relative area × capacitance

= 15 × 0.1 □Cg

= 1.5 □Cg

the polysilicon capacitance is 1.5 times of □Cg

Delay unit :- (τ)

The delay unit (τ) can be given as the product of Sheet resistance (R_s) & standard unit of gate capacitance (C_g)

$$\tau = R_s \square C_g$$

For 5μm technology :-

$R_s = 1 \times 10^4\ \Omega$

$C_g = 0.01\ PF$

Wk T $\tau = R_s \square C_g$

$= 10^4 \times 0.01\ PF$

$= 100 \times 10^{-12}$

$= 1 \times 10^{-10} = 0.1 \times 10^{-9} = 0.1 nsec$

For 2μm technology

Wk T, $R_s = 2 \times 10^4$, $C_g = 32 \times 10^{-4} PF$

$\tau = 2 \times 10^4 \times 32 \times 10^{-4} PF = 64 PF$

$= 0.064 nsec$

For 1.2μm technology :-

$\tau = R_s \square C_g$

$= 2 \times 10^4 \times 23.04 \times 10^{-4} PF$

$= 46.08 \times 10^{-12}$

$\tau = 0.046 nsec$

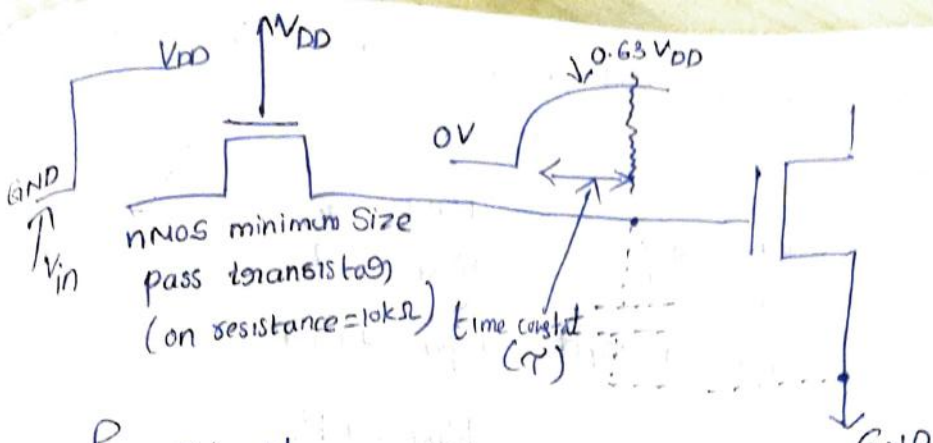


Fig: Simple model to calculate delay time

→ We know that the electron transit time τ_{ds} as

$$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$$

* When i/p signal is transmitted through the pass transistor the o/p voltage will get reduce for 63% of V_{DD} that is $0.63 \times V_{DD}$

$$= 0.63 \times 5 \cong 3V$$

For 5μm technology

$$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$$

$$= \frac{5\mu m \times 5\mu m}{600\ cm^2/Vsec \times 3V} = \frac{25 \times (10^{-6})^2\ m^2}{650\ (0.01)\ m^2/Vsec \times 3V}$$

$$= \frac{25 \times 10^{-12}}{650 \times 0.01 \times 3}\ sec = \frac{25 \times 10^{-12}}{19.5}$$

$$= 0.128 \times 10^{-9}$$

$$= 0.13\ nsec$$

Note: The delay time T is approx equal to electron transit time τ_{ds}

Inverter Delay :-

nMOS inverter Delay

Here let us consider an nMOS inverter with ratio of 4:1

→ The pull up to pull down ratio of nMos driven by another nMos is 4:1

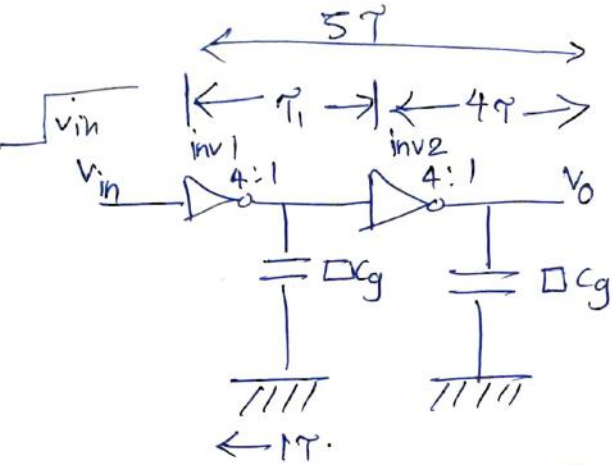
$$\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1} \qquad \frac{R_{pu}}{R_{pd}} = \frac{4}{1}$$

$$Z_{pu} = 4 Z_{pd} \qquad R_{pu} = 4 R_{pd}$$

$$R_{pu} = 4 R_S$$

$$R_{pu} = 4 \times 10^4$$

$$R_{pu} = 40 k\Omega$$



* the delay is not effected by the cascade connecting of inverters but it is due to the turning on/off action of inverters

* the total delay 'τ_d' is the combination of both inverters

i.e $\tau_d = 1\tau + 4\tau = \tau(1+4) = 5\tau$

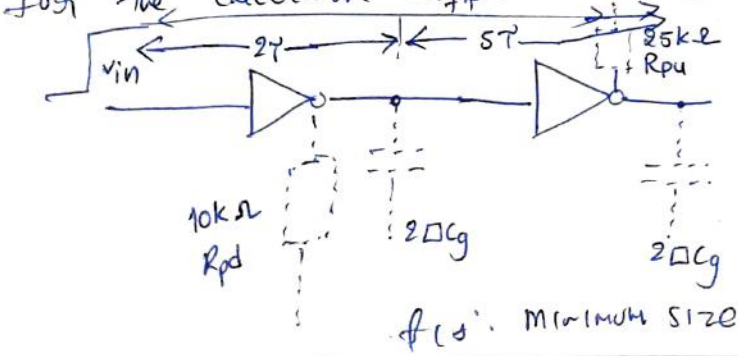
$$\tau_d = \tau\left(1 + \frac{4}{1}\right)$$

$$= \tau\left(1 + \frac{Z_{pu}}{Z_{pd}}\right)$$

The total delay is combination of nMos inverters $\tau_d = 5\tau$

CMOS inverter delay

Here let us consider an arrangement shown below for the calculation of τ_p CMOS inverter delay



τ_d: Minimum size CMOS inverter delay

UNIT - II

Mos and Bicmos circuit designing processes

Introduction:-

To design any circuit first of all we need to take the design considerations that is the specifications of the component of the system.

All those individual components are to be interconnected and metalizations are used to have a package circuit.

Mos layers:-

The basic mos layers that are used to design a circuit includes n^+ diffusions, p^+ diffusions, poly-silicon and etc..

Stick diagrams:-

Stick diagroms are outlined representations of layouts.

The stick diagrams convey the designing of the circuit through colour codes.

* For the designing of stick diagroms and layouts the Mos layers using colour codes are drawn as below.

For Nmos

S.No	layer	color	stick diagram representation	layout representation
1.	n+ diffusion	Green		
2.	p+ diffusion	yellow		
3.	Polysilicon	Red		
4.	Metal	Blue		
5.	Ion implantation	yellow		
6.	Burried contact	Brown	•	
7.	Contact cut	Black	•	
8.	Supply lines	Black	X	
9.	Demarkation line	Brown	-----	

For PMOS:-

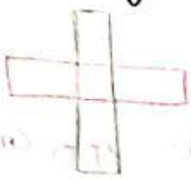
for pmos designing the only charge is ion implantation.

S.No.	layer	color	stick diagram representation	layout representation
1.	Ion Implant -ation	green		

Mos transistor representations:-

NMOS Enhancement

stick diagram



layout

PMOS Enhancement

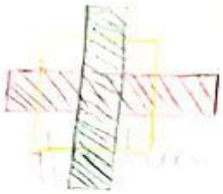
stick diagram

layout

NMOS depletion mode

stick diagram

layout

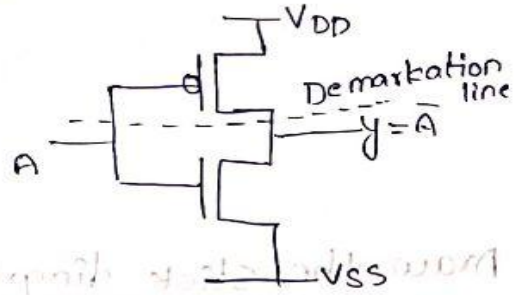


PMOS depletion mode

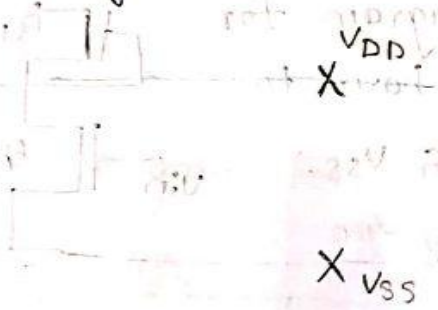
stick diagram

layout

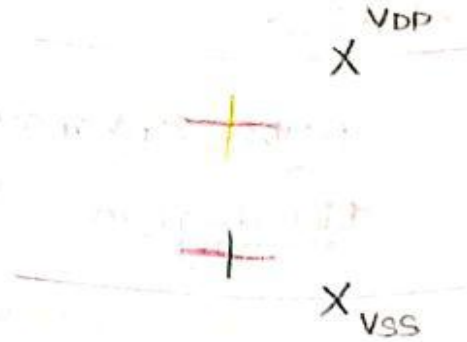
1. Design a stick diagram for Cmos inverter:-



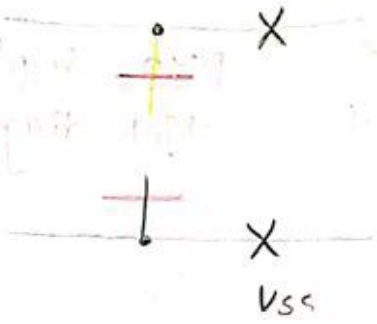
Step 1:- To design a cmos inverter, first we have to draw the supply lines V_{DD} and V_{SS}



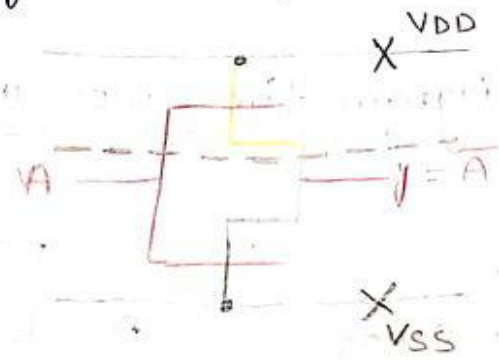
Step 2:- After V_{DD} and V_{SS} place the required transistors at a given place.



Step 3:- extend the transistors towards V_{DD} and V_{SS} and make contact cuts

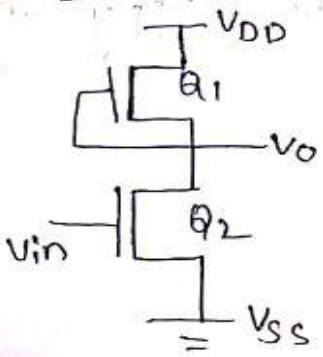


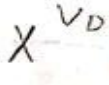
Step 4:- finally take i/p and o/p terminals

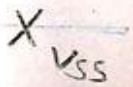


Q. Draw the stick diagram for nmos inverter:-

Step 1: To draw stick diagram for nmos inverter first we have to draw supply lines V_{DD} & V_{SS}.

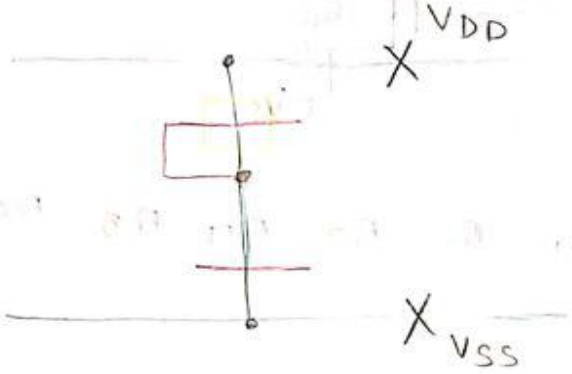




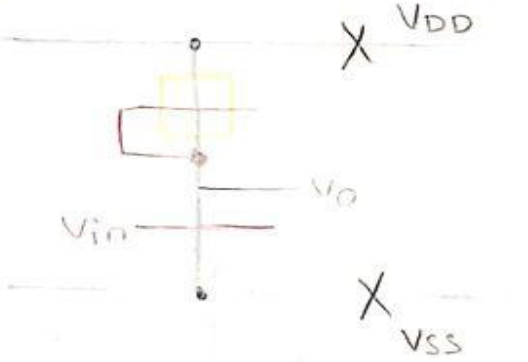


Step2:- After drawing supply lines place the required transistors.

Step3:- extend the transistor lines toward VDD and Vss and place contacts and Burried Contact



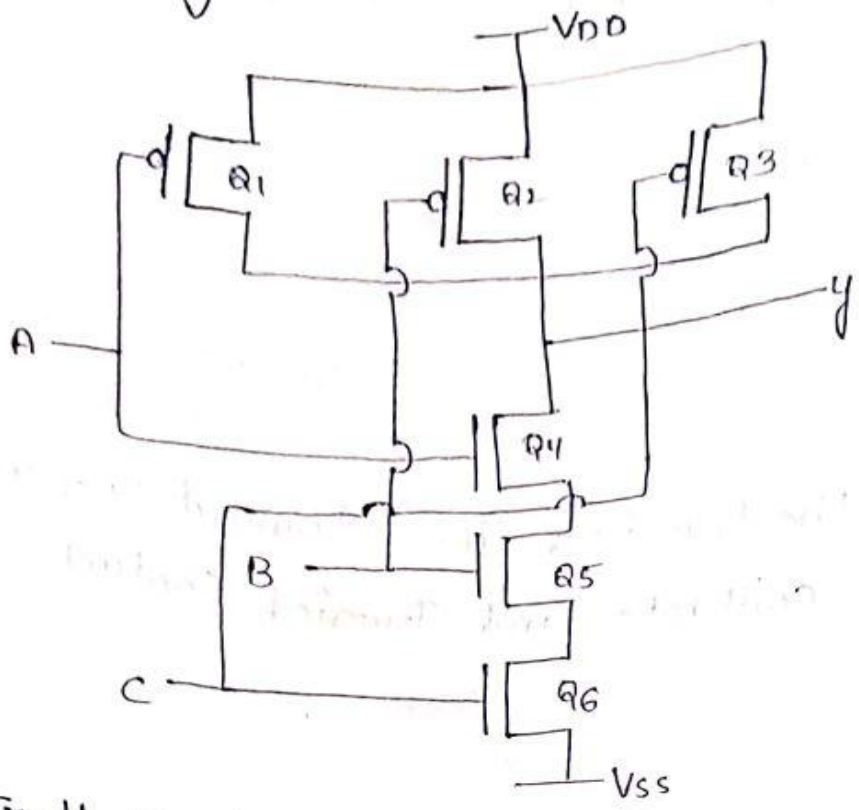
Step4:- finally take i/p and o/p's terminals.



3. Draw stick diagram for three input NAND gate using cmos technology.

	Nmos	pmos
NAND	series	parallel
NOR	parallel	series

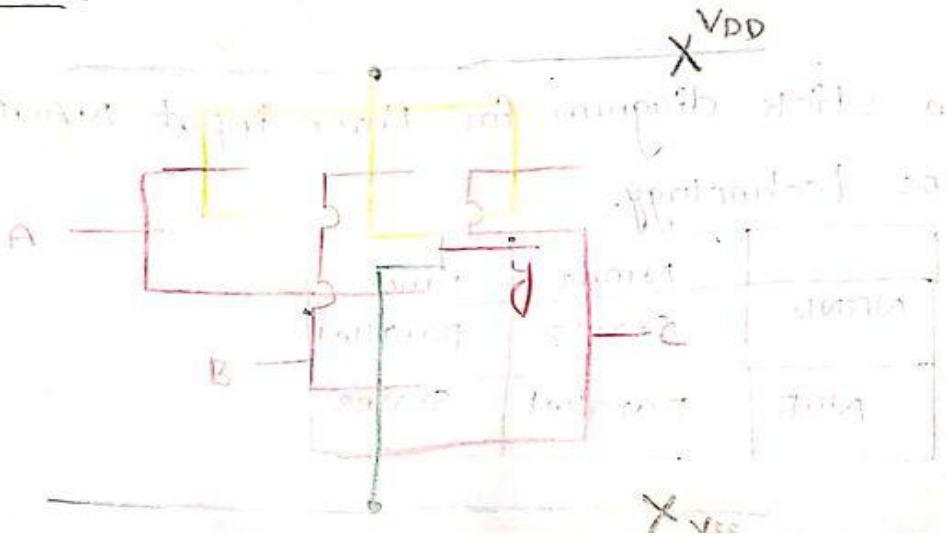
Circuit diagram



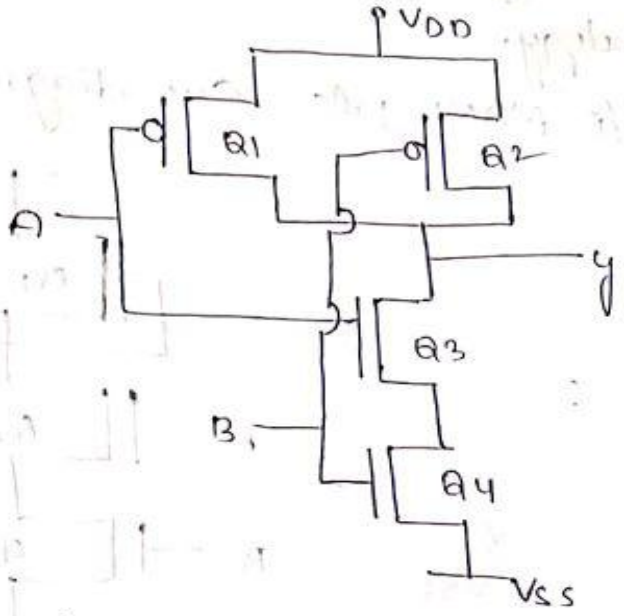
Truth Table

A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	y
0	0	0							
0	0	1							
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

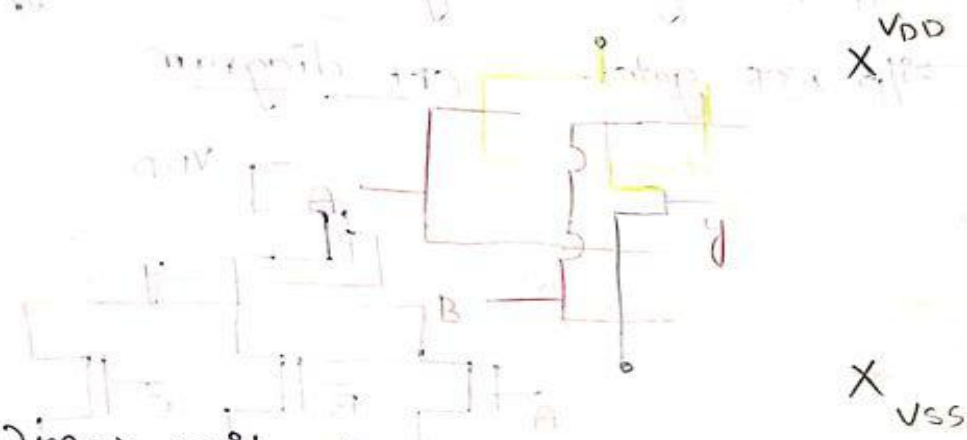
Stick diagram:-



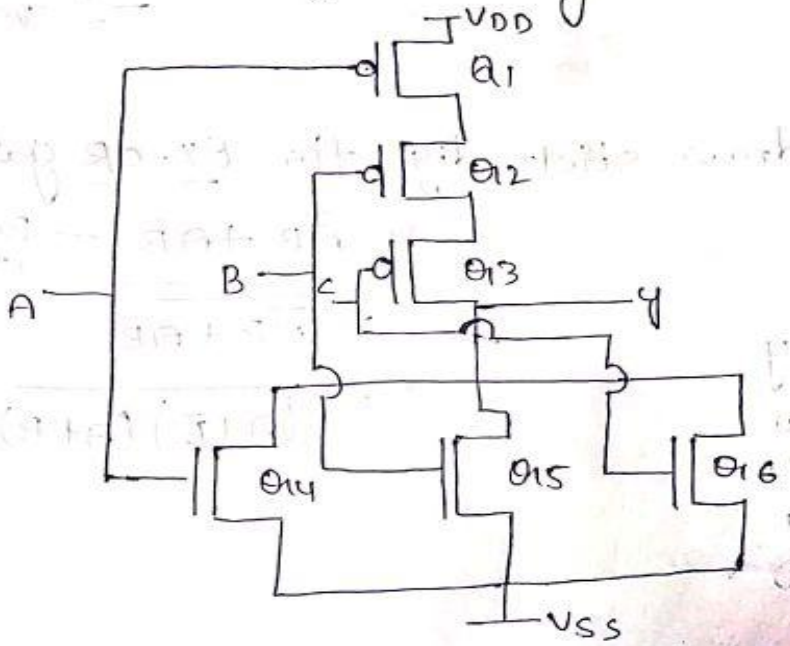
4. Draw the 2i/p NAND gate using cmos technology



stick diagram:-

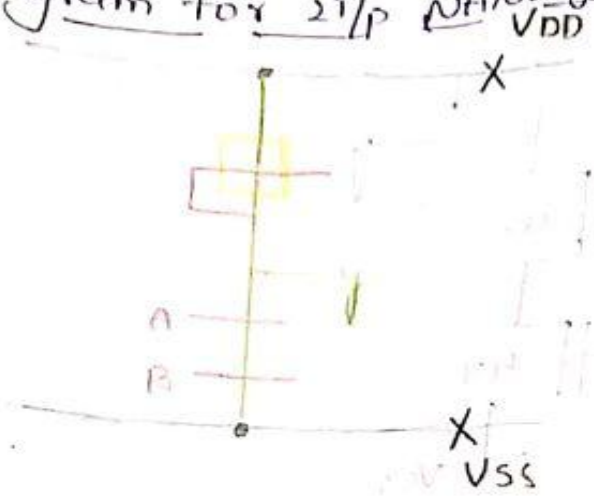


5) Draw 3 i/p NOR gate using cmos technology

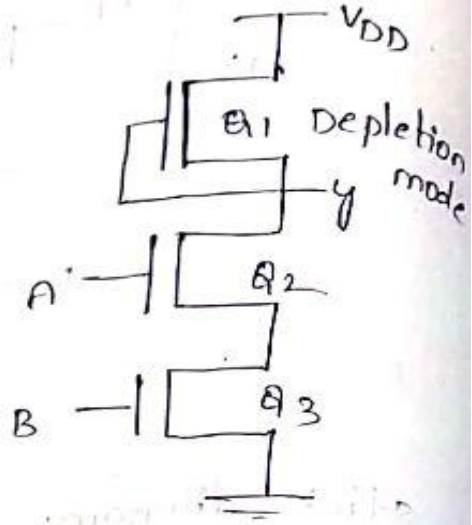


6) Draw the stick diagram for 2 i/p NAND gate using Nmos technology.

Stick diagram for 2i/p NAND gate

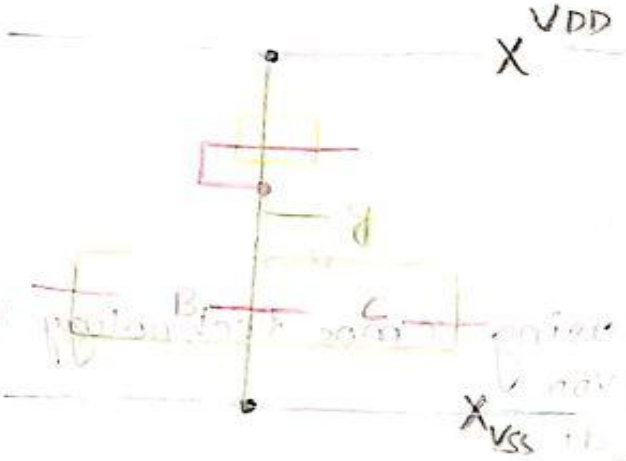


Ckt diagram

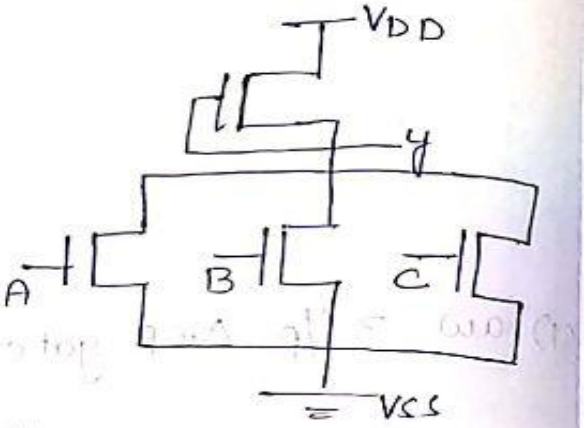


7) Draw the 3i/p NOR gate using Nmos technology

Stick dig for 3i/p NOR gate:-



Ckt diagram



8) Desig and draw stick dig for EX-OR gate

Truth Table

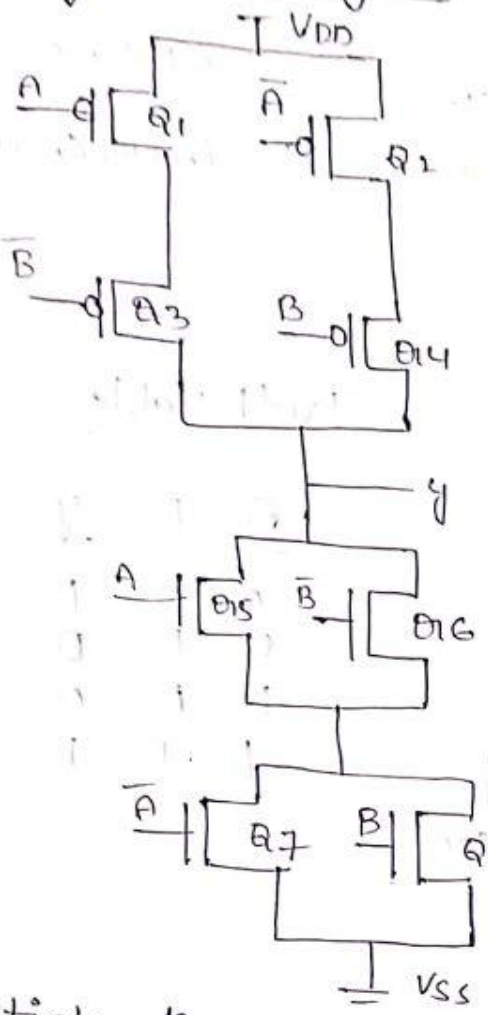
A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

$y = \bar{A}B + A\bar{B}$ — Boolean expression

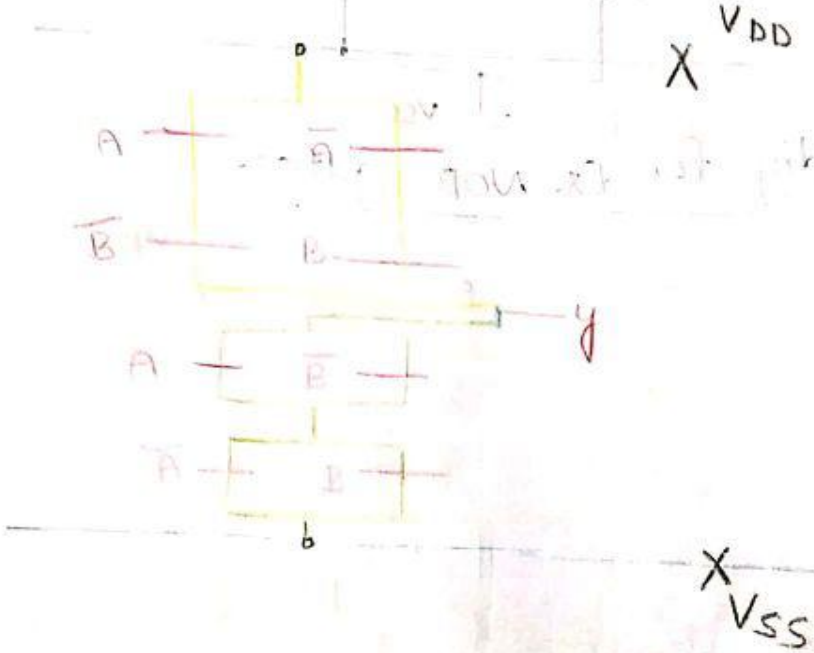
$= \overline{\bar{A}B + A\bar{B}}$

$= \overline{(A+\bar{B})(\bar{A}+B)}$

CKt dig for Ex-OR gate:-



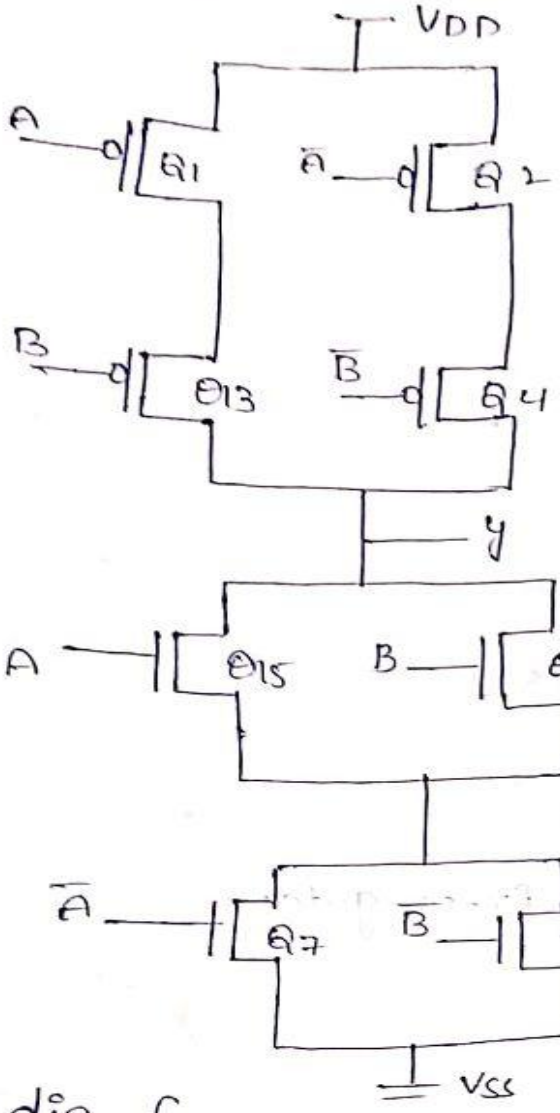
Stick diagram for Ex-or gate:-



9) Design ckt for Ex-NOR gate

$$y = \bar{A}B + A\bar{B}$$
$$= \overline{\bar{A}B + A\bar{B}}$$
$$= \overline{(A+B)(\bar{A}+\bar{B})}$$

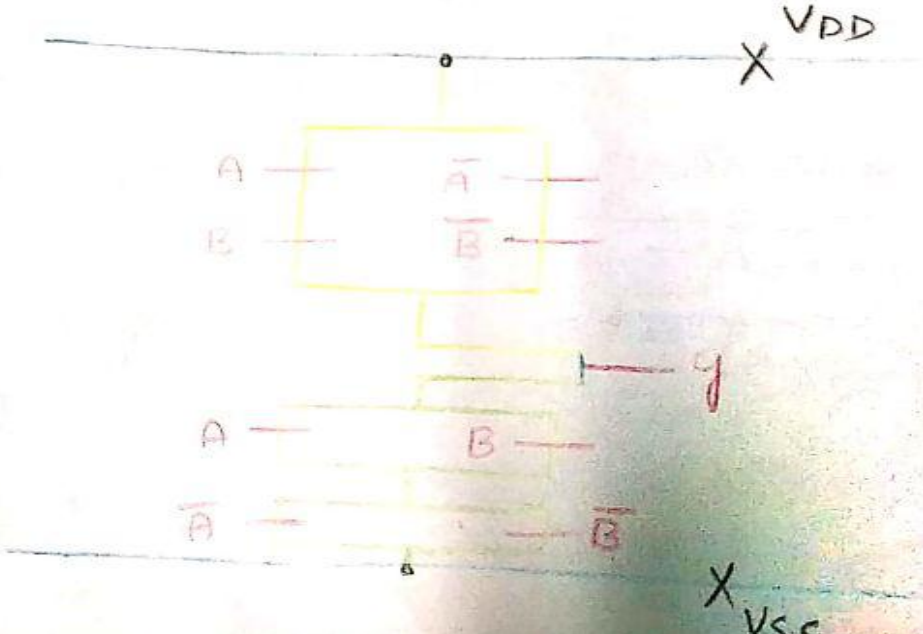
Ckt dig for Ex-NOR gate:-



Truth table

A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

Stick dig for Ex-NOR gate:-



Design rules and layouts:-

* As the complexity of VLSI technology is more and more to have better understanding we are using a set of rules called Design rules.
* The design rules are the effective interface b/w Design Engineering and fabrication Engineering.
* ckt designers in general want tighter, smaller layouts for improved performance and reduced silicon area.
* The process Engineer want's Design rules that result's in a controlable and reproduces process.
* So, we need to have compromise b/w ckt design-er and process engineer requirments.
* Basically we are having two types of design rules
  1. Scalable Design rules ('λ' base)
  2. Absolute Design rules (micron base)

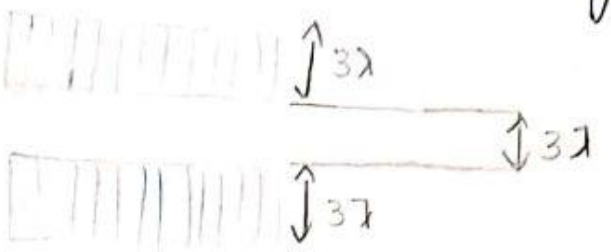
Scalable Design rules:-

1. The minwidth of metal 1 is 3λ and spacing b/w metal 1 and metal 1 is 3λ.
2. The minwidth of metal 2 is 4λ and spacing b/w metal 2 & metal 2 is 4λ.
3. The minwidth of n^+ diffusion (or) p^+ diffusion is 2λ and spacing b/w n^+ diffusion to n^+ diff & p^+ diffusion to p^+ diffusion is 3λ.

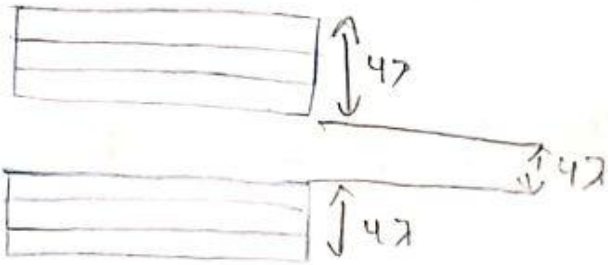
4. The minwidth of polysilicon is 2λ and spacing b/w polysilicon to polysilicon is 1λ.

Minwidth Min spacing

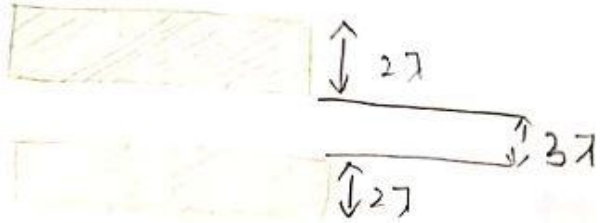
Metal 1:



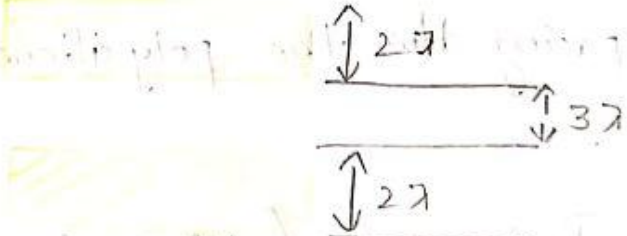
metal 2:-



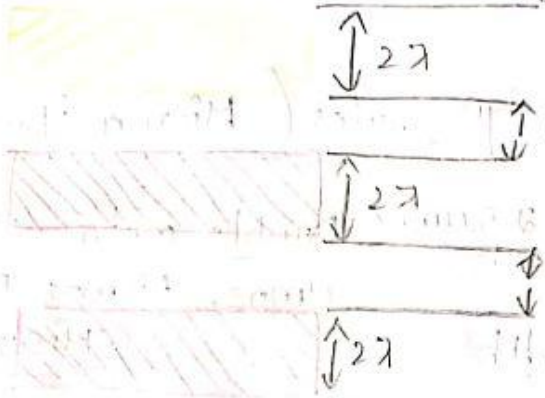
n^+ diffusion:



p^+ diffusion:

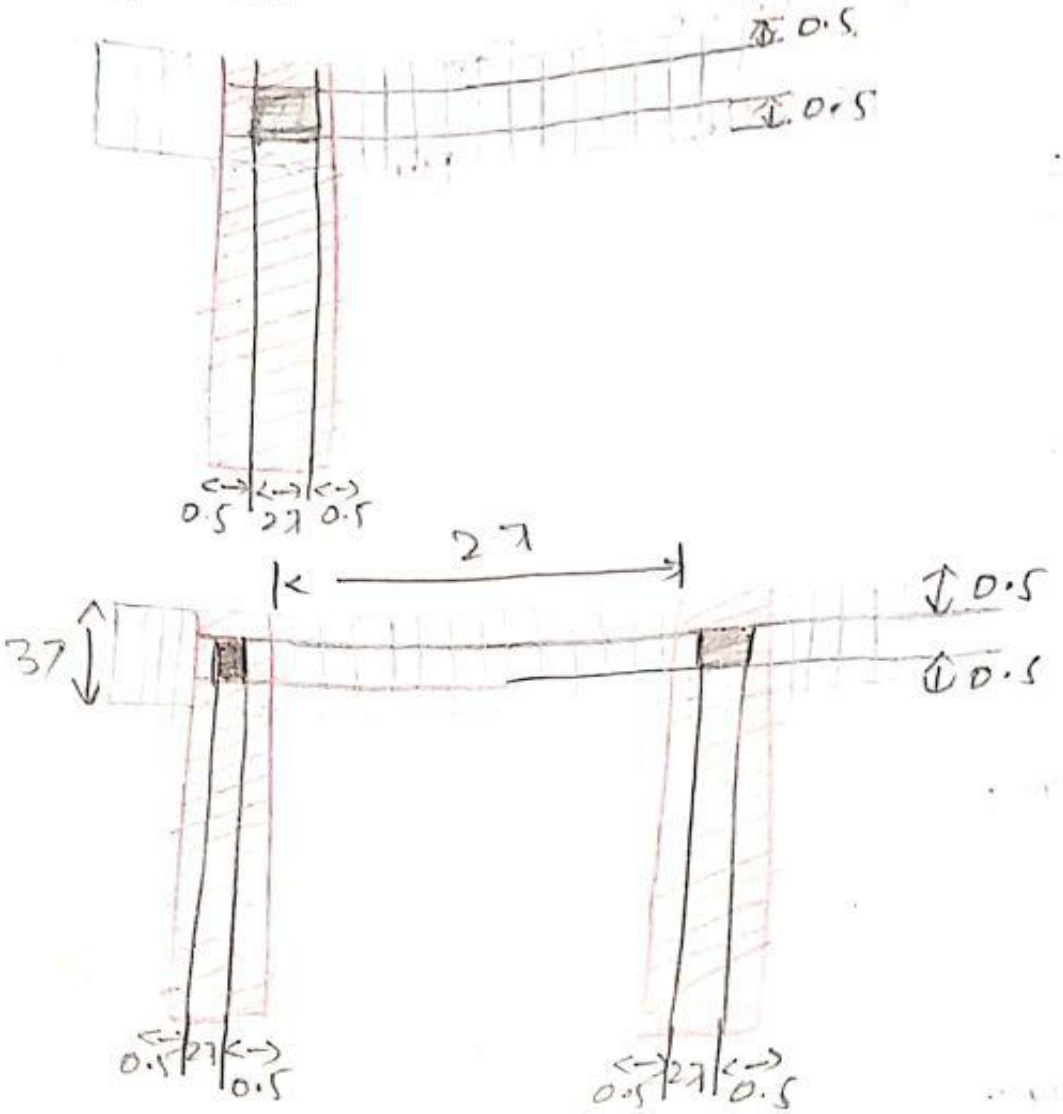


poly silicon:



n^+ diffusion:

Contact cut :-



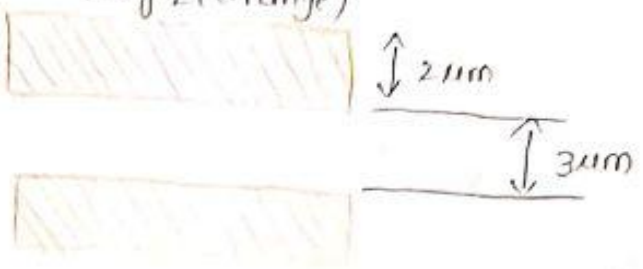
The spacing blw the polysilicon 1 & polysilicon 2 is 2λ.

Absolute Design Rules (Micron Base) :-

1. 2μm and 2.5μm (Double metal ; Double poly) :-
cmos, bicmos processes

Minwidth	Minspacing

Poly 2 (orange)

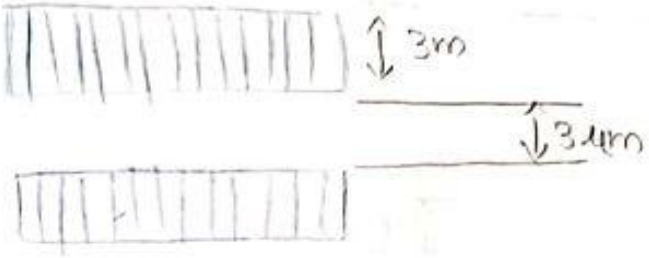


$P^+/n^+ \rightarrow P_1 \rightarrow 1\mu m$

$P^+/n^+ \rightarrow P_2 \rightarrow 1.5\mu m$

$P_1 \rightarrow P_2 \rightarrow 2\mu m$

Metal 2



$P_1 m_1$

$P_1 \rightarrow 2\mu m$ & $2.5\mu m$

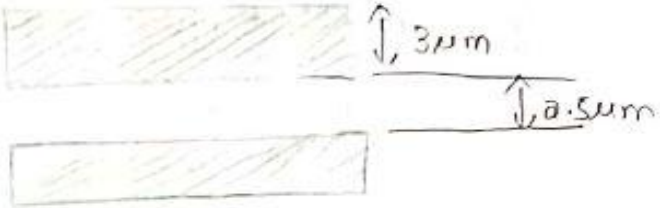
$m_1 \rightarrow 2\mu m$ & $2.5\mu m$

$P_2 \rightarrow 2\mu m$ & $3\mu m$

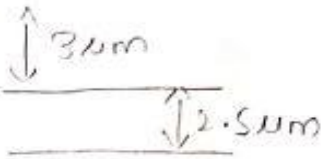
$m_2 \rightarrow 3\mu m, 3\mu m$

$P^+/n^+ \rightarrow 3\mu m$ & $2.5\mu m$

n^+ Diff



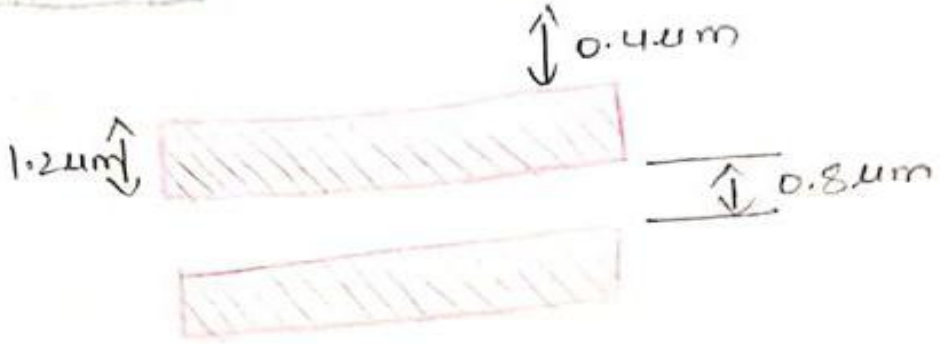
P^+ Diffusion

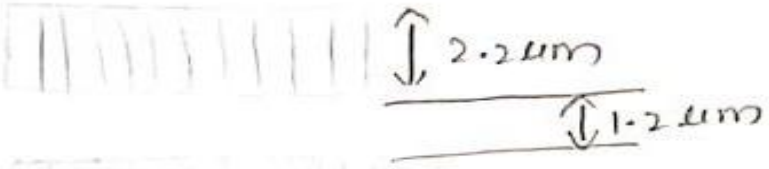


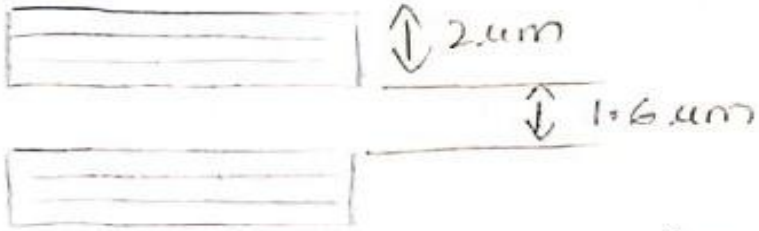
1.2um (Double metal and single poly):-

Minwidth

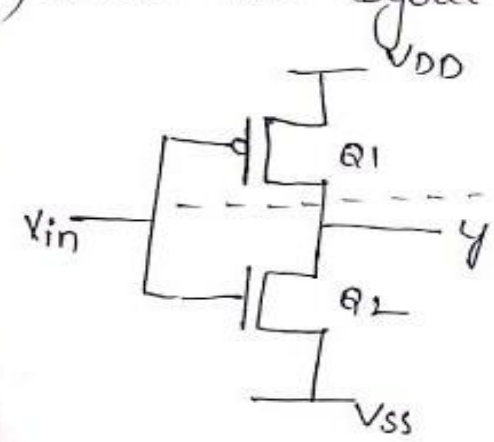
Minspacing

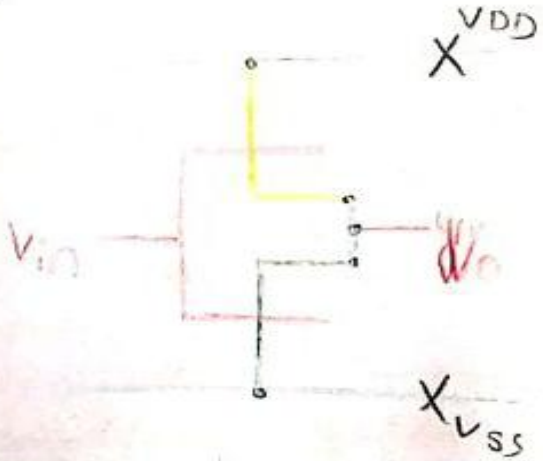






1) Draw the layout for Cmos inverter.

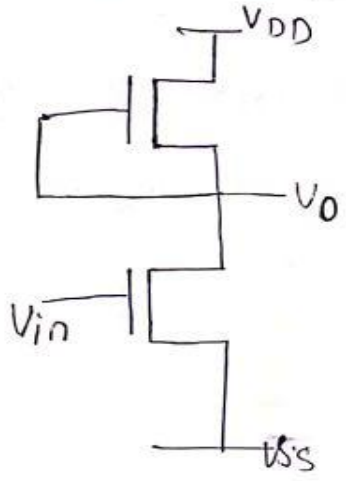


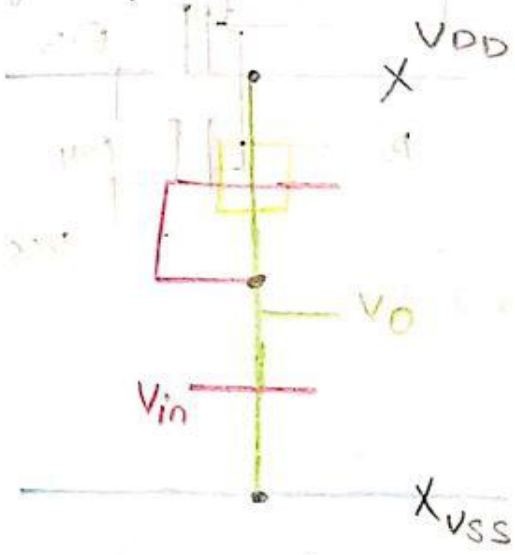


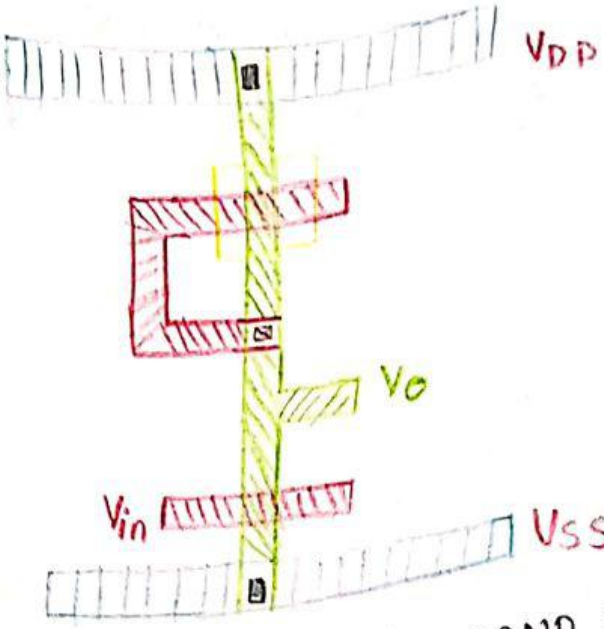
CMOS inverter ckt

2) Draw the layout for nmos inverter.

Nmos inveiter ckt

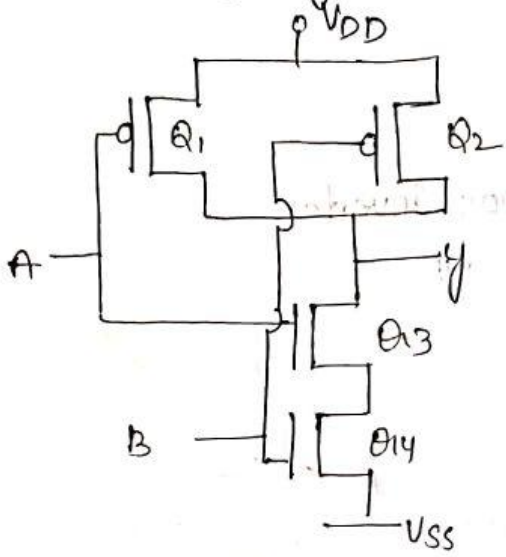




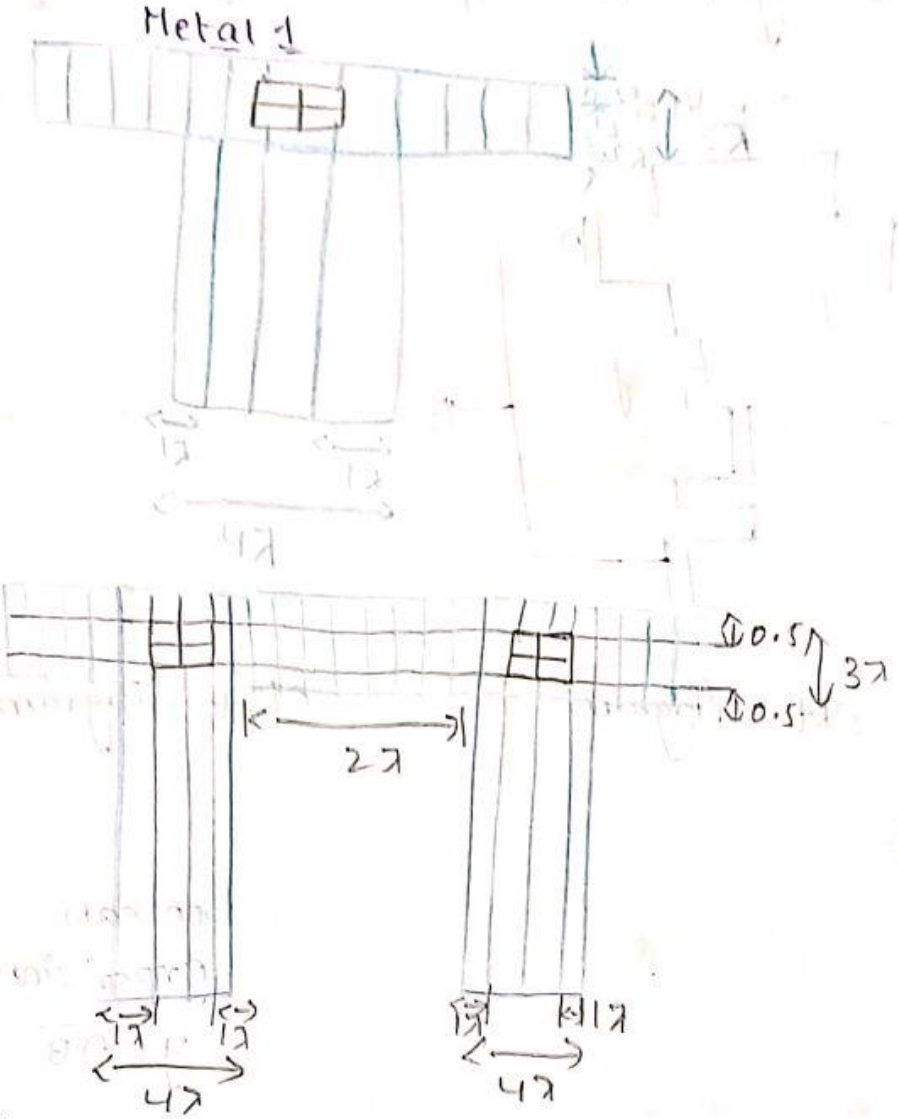


* Draw the layout for 2 i/p NAND gate using Cmos logic.

A. Circuit Diagram



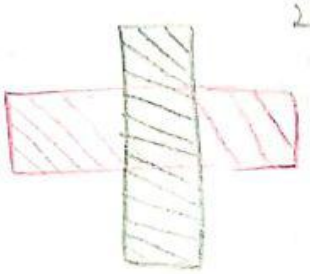
Via



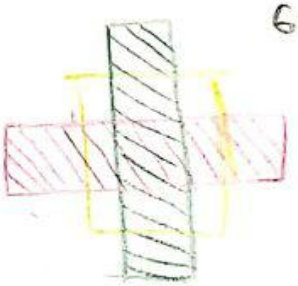
The spacing b/w via 1 & via 2 length is 2λ

Transistor representation:-

nmos enhancement

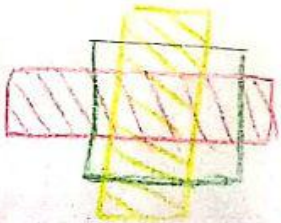


nmos Depletion

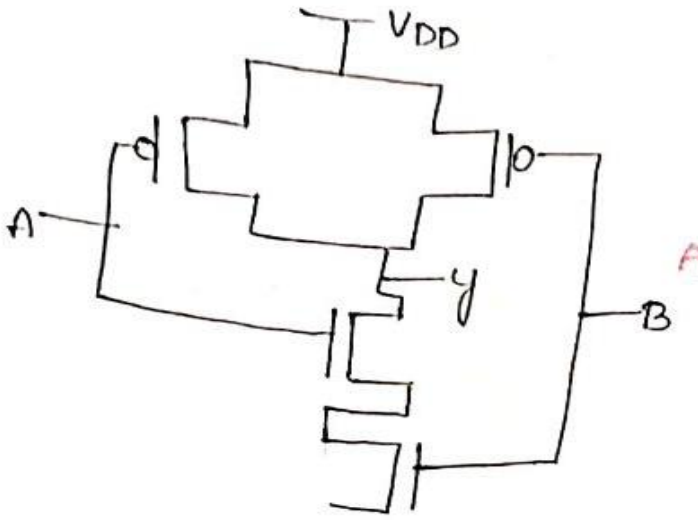


pmos enhancement

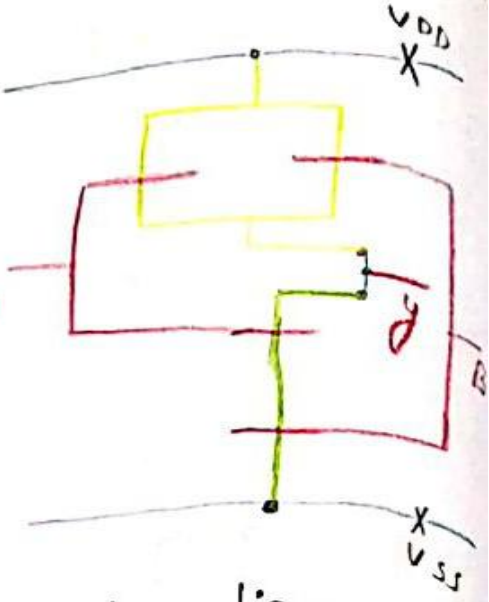
pmos depletion



* Draw the layout for 2 i/p NAND gate using cmos logic.

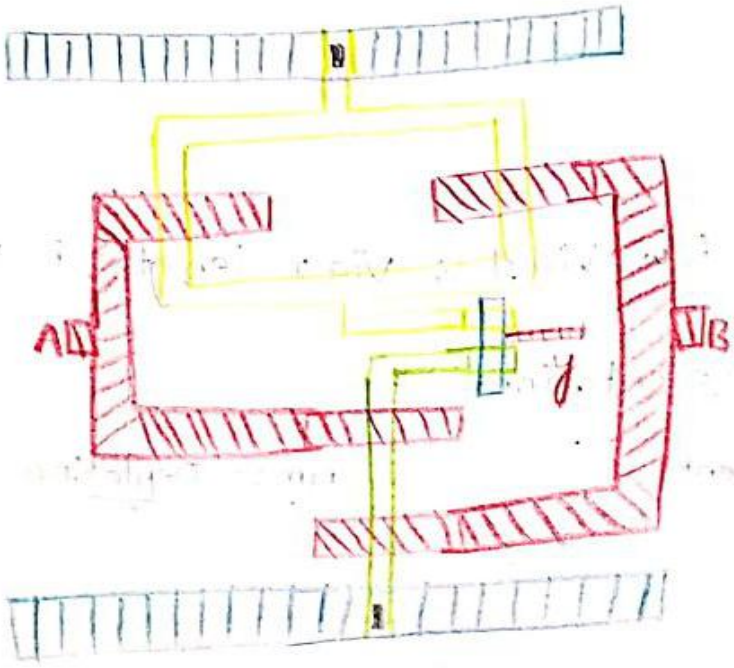


ckt diagram



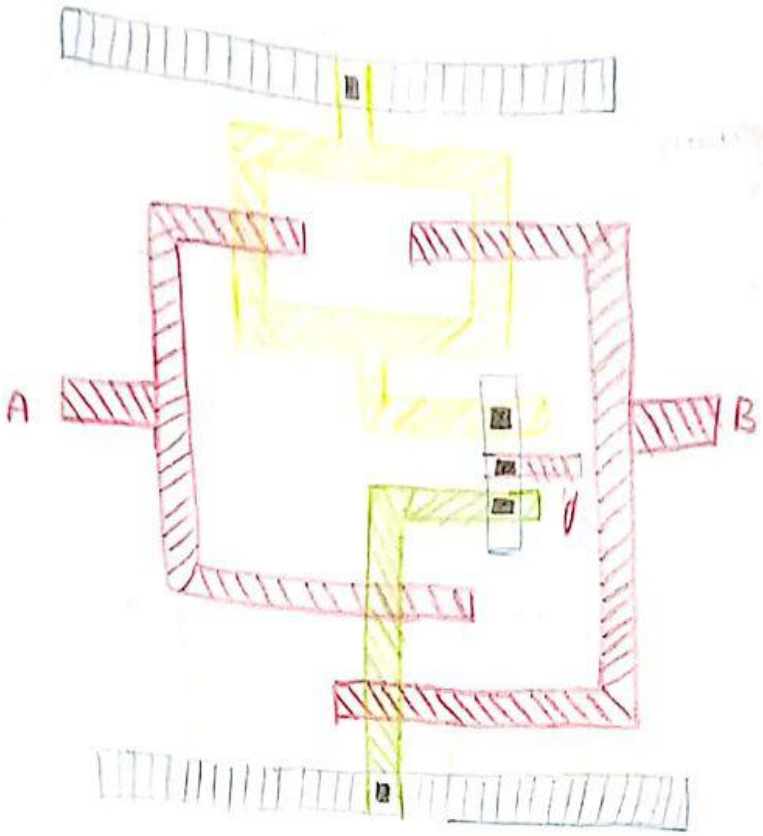
Stick diagram

layout



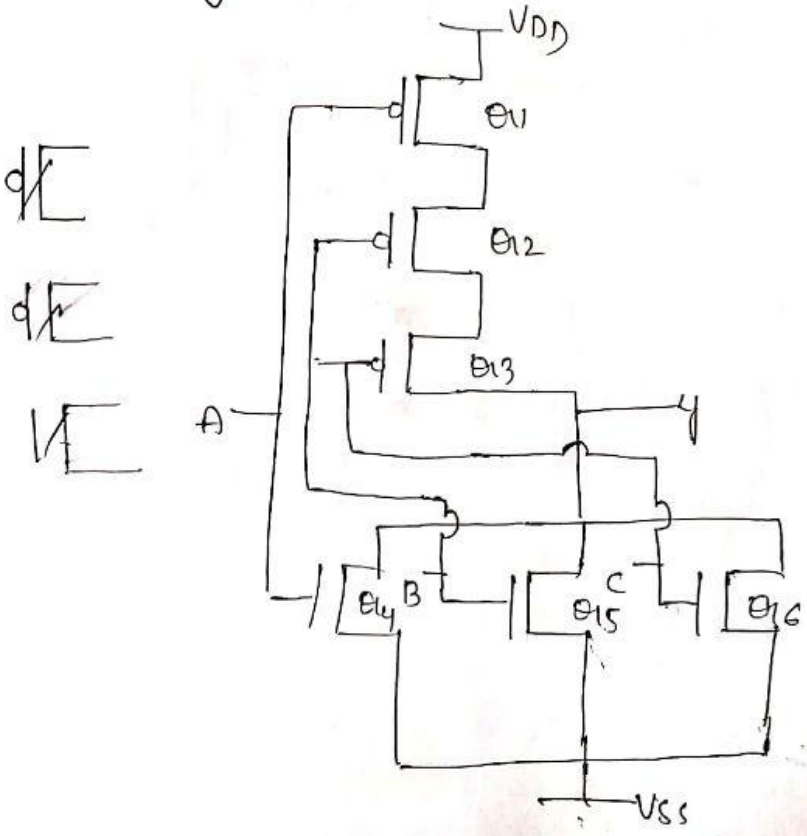
boolean expression

$y = \overline{AB}$



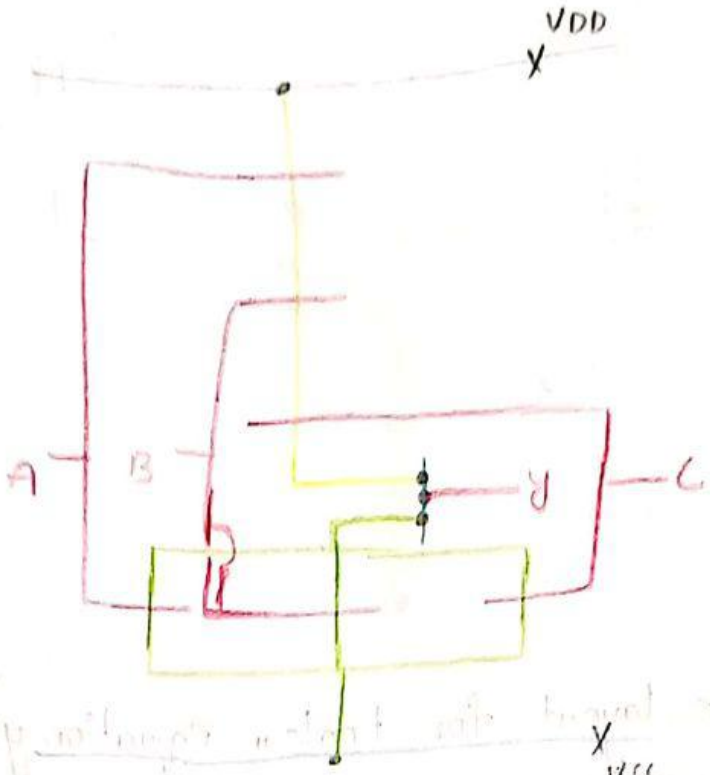
*Draw the layout for boolean equation $y=\overline{(A+B+C)}$ using cmos logic.

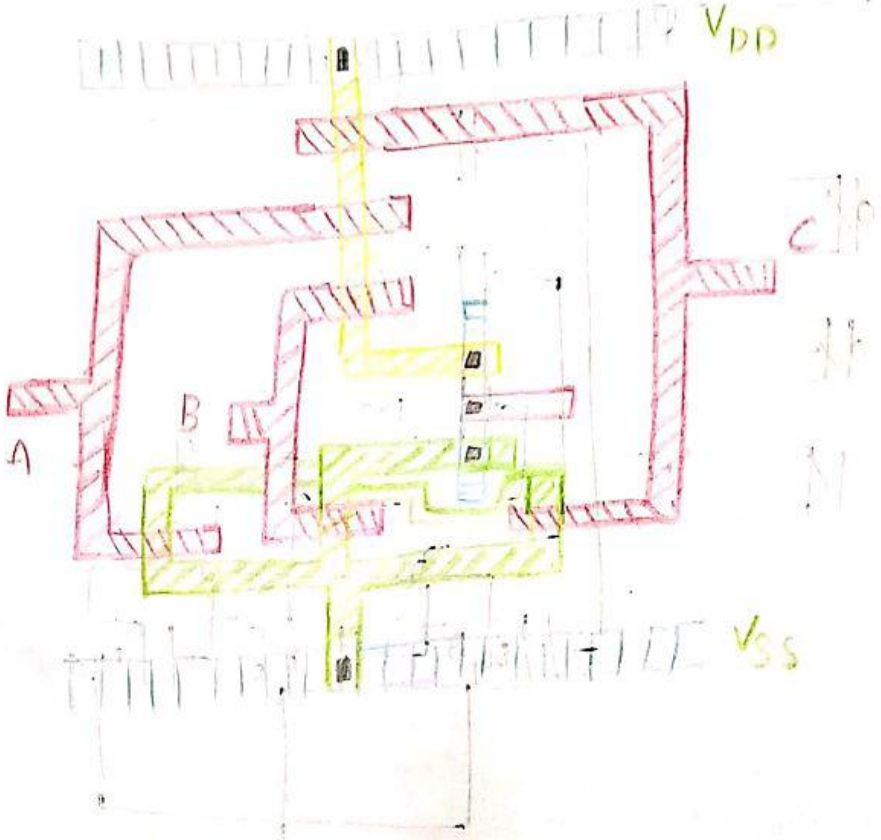
A. Circuit Diagram



General

Stick diagram

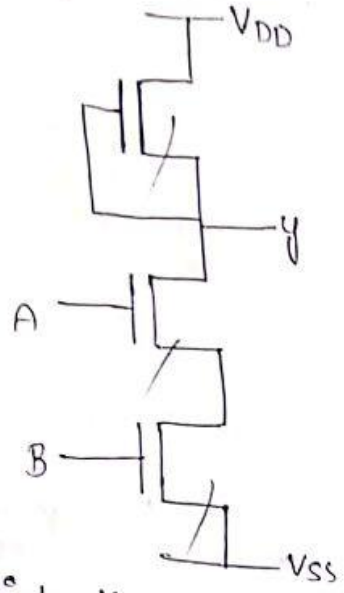


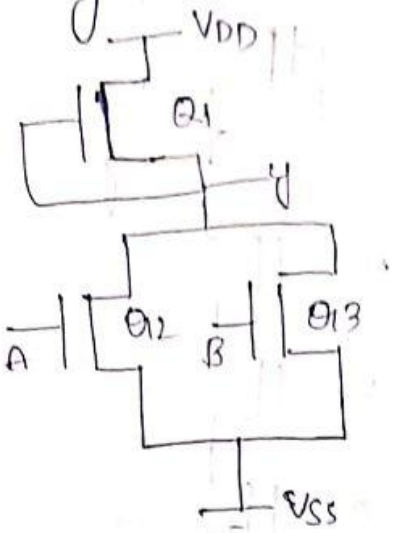


→ 2 i/p NOR gate using nmos logic → $y = \overline{(A+B)}$

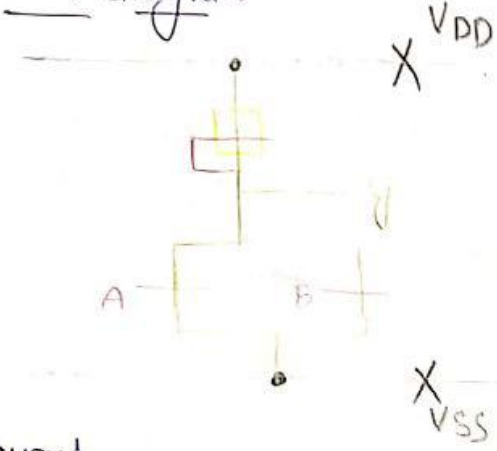
→ 3 i/p NAND gate using nmos logic → $y = \overline{ABC}$

1. 2 i/p NOR gate using nmos logic.

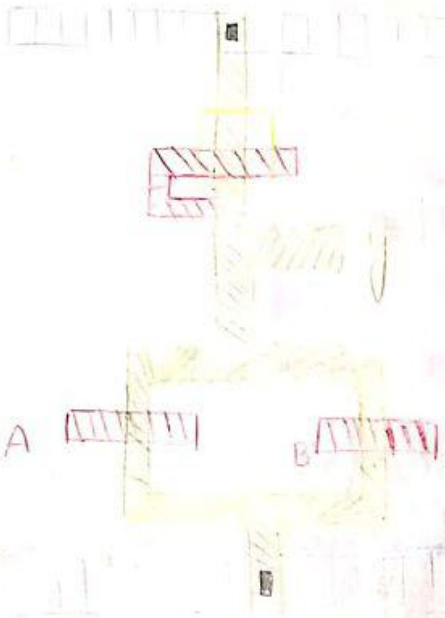




Stick diagram

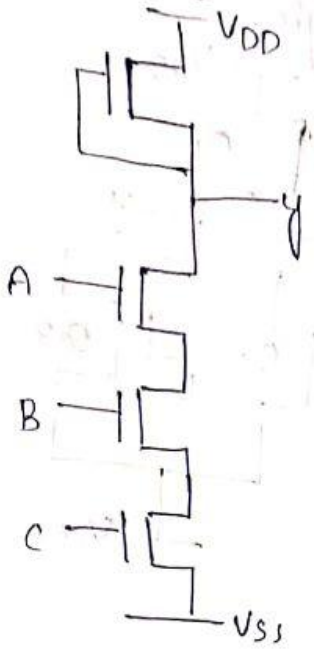


Layout

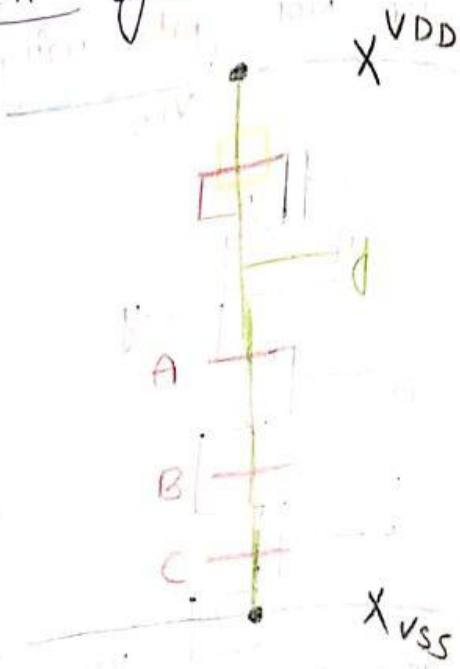


* 3 i/p NAND gate using nmos logic. $y = \overline{ABC}$

Circuit diagram



Stick diagram



Layout

General observations for design rules:-

A VLSI designer is dealing with silicon circuits whose dimensions and features are extreamly microscopic in nature.

* If the line widths are to small, the lines so define may tend to be discontinuous case places (or) may accordingly merge at places.

* The main purpose of design rules are

1. provides Communication links between circuit designer and process Engineer responsible for fabrication.
2. The goal of any set of design rules should be optimise yield while keeping the geometry as small as possible without Compromising the realibity of the finished circuit.
3. Try to exculed poly from the areas of p+mask/ n^+ mask that may Effect the resistance of poly at certain paths.
4. Metal is depoisted at the top of all oxide layers, Since it is light reflective, these factors combine poor edge defination.
5. Metal 2 is having even more unevent terriains on which to be depoisled and patterend. Hence metal 2 is wided than metal 1.
6. metal to metal seperation is also large and is brought above mainly by difficulties indefining metal edges.

In fitting step, a fitter maps the synthesized components onto available device resources.

Place & route process lays components and finds ways to connect them. The designer can usually specify additional constraints at this stage, like placement of modules within a chip or the pin assignments of external I/p & O/p pins.

The final step is post-fitting timing verification of the fitted circuit. At this stage actual ckt delays due to wire lengths, electrical loading and other factors can be calculated.

MOS LAYERS

MOS circuits are formed on 4 basic layers:

(i) n-diffusion
(ii) p-diffusion
(iii) Poly Si
(iv) Metal.

→ The thinox mask region includes n-diff, p-diff & transit channels.

→ Poly Si & thinox regions interact so that a transistor is formed where they cross one another.

→ Contacts formed by joining layers.

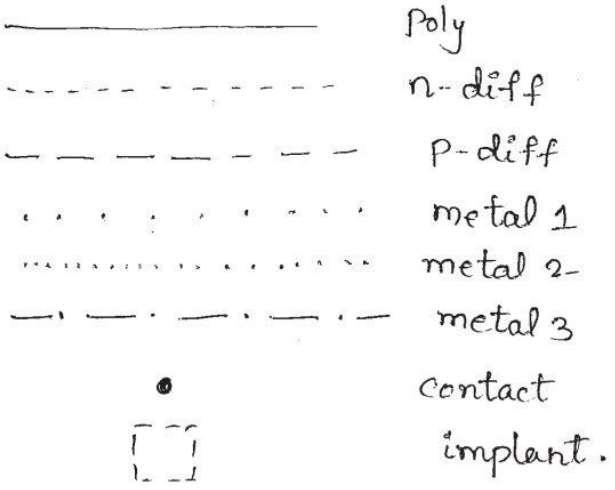
→ Some processes includes 2nd metal layer, also 2nd polysi layer.

→ Bipolar transistors can be included in design by addition of extra layers to CMOS process.

STICK DIAGRAMS :

A stick diagram is a cartoon of a chip layout. It represents rectangles with lines which represent wires and component symbols.

Representation



Colors :-

(nMOS design style).

Red : Poly
Green : n-diff
Blue : Metal
Black : Contact
Yellow : implant

(CMOS design style)

Red : Poly
Green : n-diff
Yellow : P-diff
Blue : Metal
Black : Contact

→ A Tr is formed wherever poly crosses diffusion.

→ Area and aspect ratio are difficult to estimate from stick diagrams.

→ Faster to design.

→ Important tool for layouts built from large cells & testing connections b/w cells.

→ A stick diagram is interface b/w symbolic ckt & the actual layout.

→ Often used to solve routing problems.

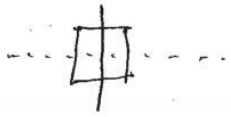
→ Rules:- (1) When two or more sticks of same type cross or touch each other represent electrical contact.

(2) When two or more sticks of different type cross or touch each other there is no electrical contact.

(3) When poly crosses diff^n, it represents MOSFET.


nMOS


pMOS


depletion nMOS.

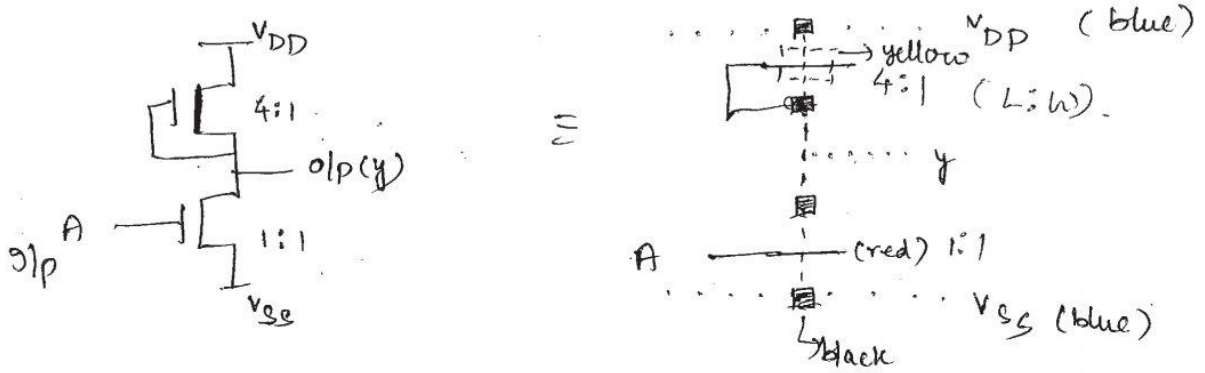
nMOS Design style :-

A transistor is formed wherever poly crosses n-diff (red over green) and all diffusion wires (interconnections) are n-type (green).

Draw V_{DD} & gnd rails in parallel using metal (blue) allowing enough space b/w them for other circuit elems.

ex: ① nMOS inverter

$y = \bar{A}$



implant in yellow.

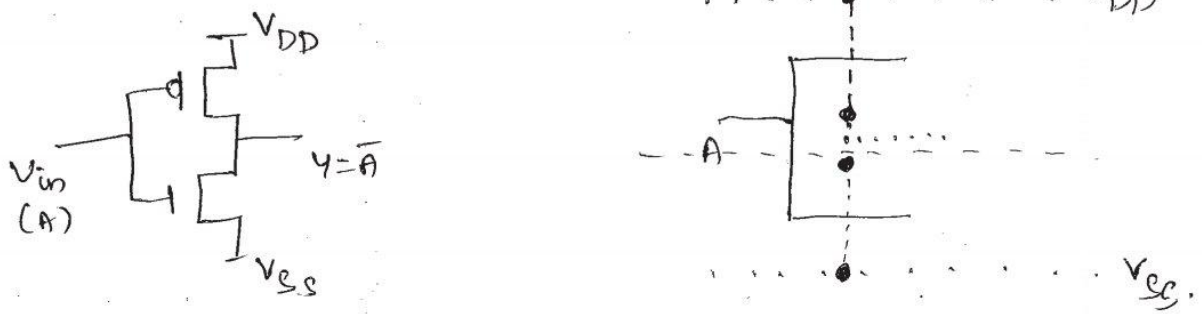
CMOS Design Style :-

→ Logical extension of nMOS approach.

→ The two types of trs used 'n' & 'p' are separated in the stick layout by the demarcation line above which all p-type devices are placed. The n-devices (green) are placed below the demarcation line. and are thus located in the p-well.

Diffusion paths must not cross the demarcation line and n-diff & p-diff wires must not join. The 'n' & 'p' features are normally joined by metal where a connection is required.

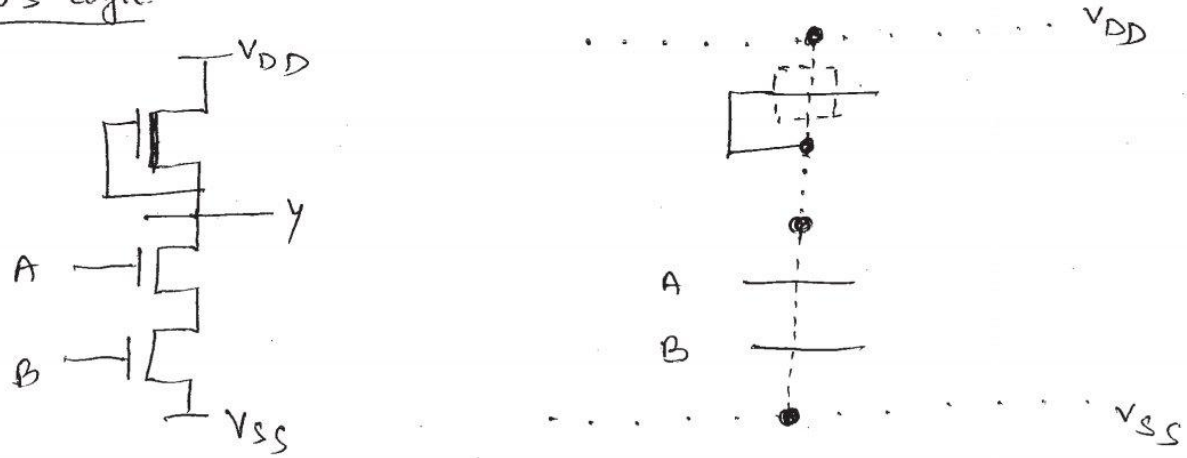
ex:- PMOS inverter.



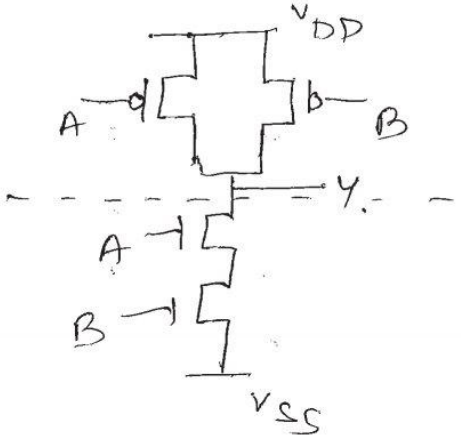
More Examples

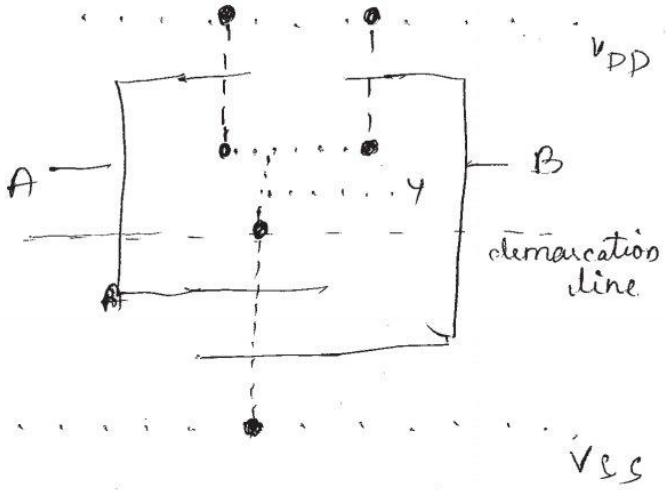
1) $Y = \overline{A.B}$ (Nand Gate)

nMOS Logic



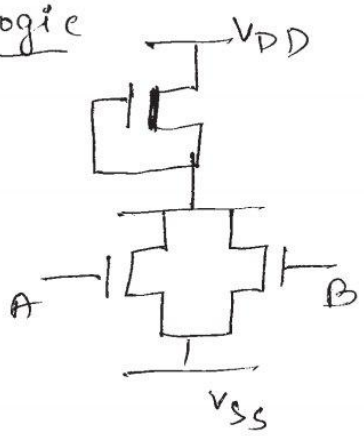
CMOS logic

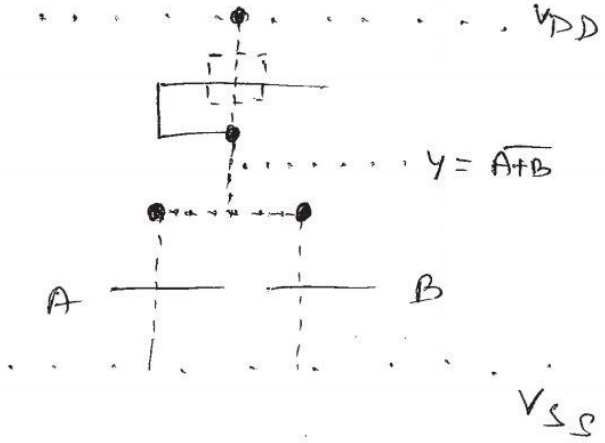




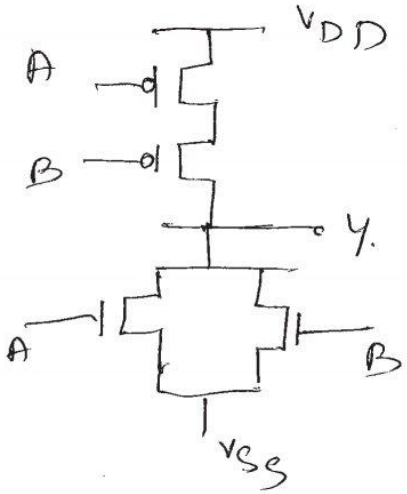
2) $Y = \overline{A+B}$ (NOR).

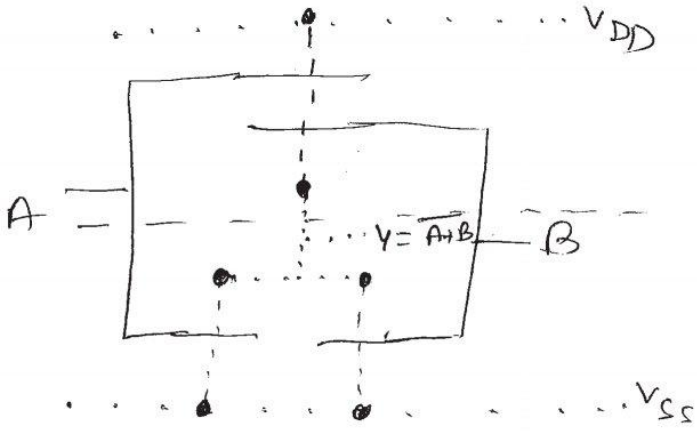
nMOS logic





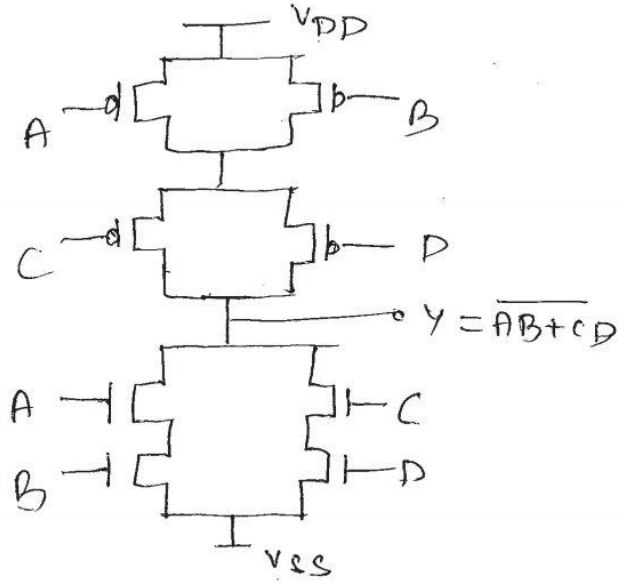
3) CMOS logic

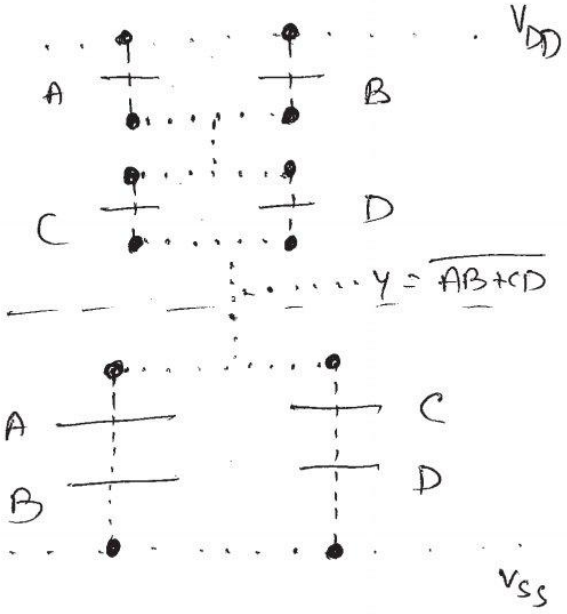




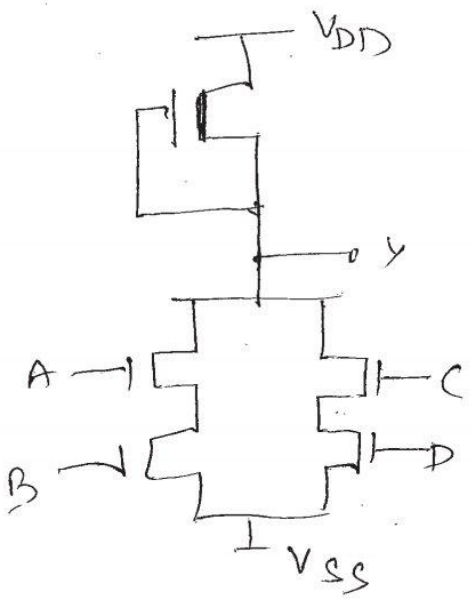
3) $Y = AB + CD$

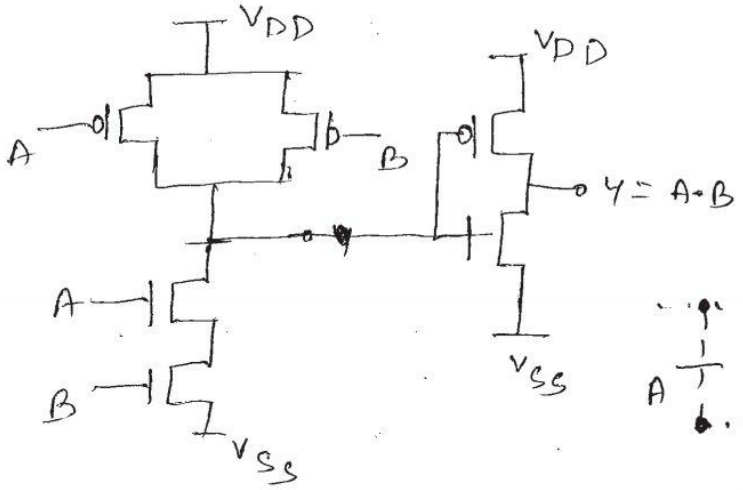
CMOS logic

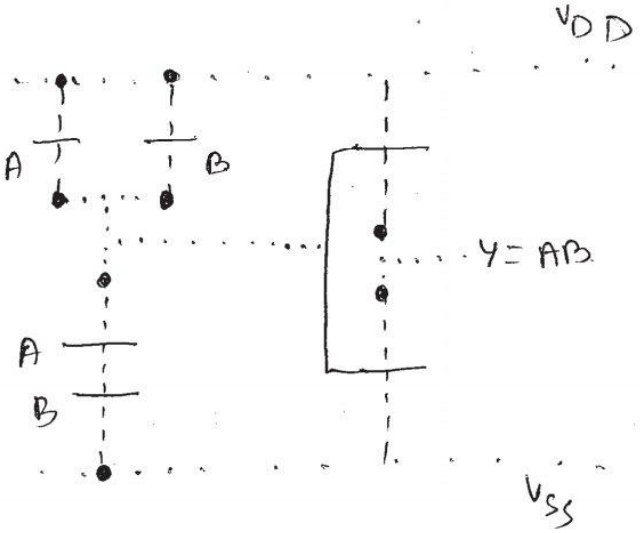




similarly nMOS logic.

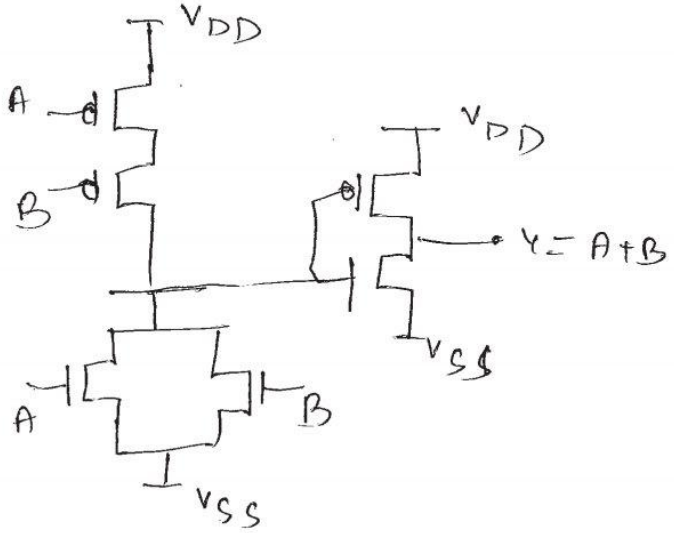


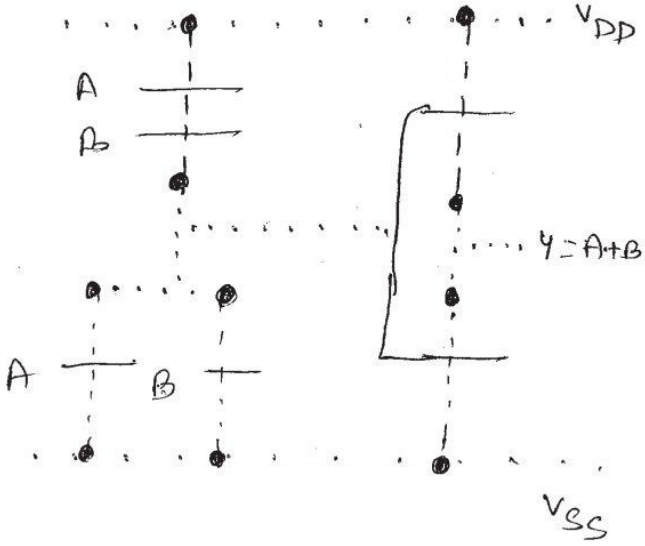




* similarly nMos. logic

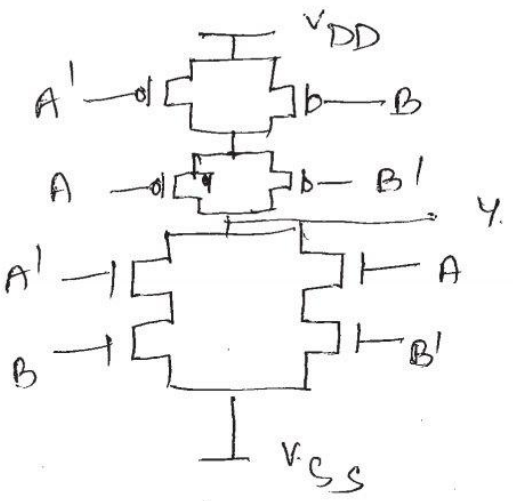
5) $Y = A + B = \overline{\overline{A+B}}$

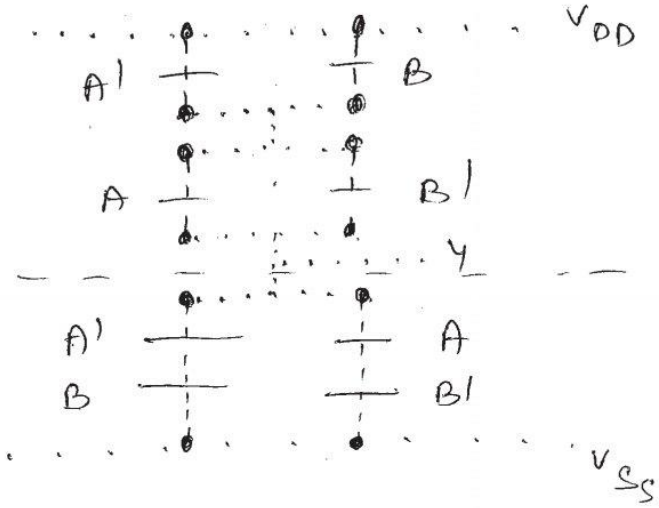




* Do nMos logic.

6) $Y = A'B + AB'$ (xnor)





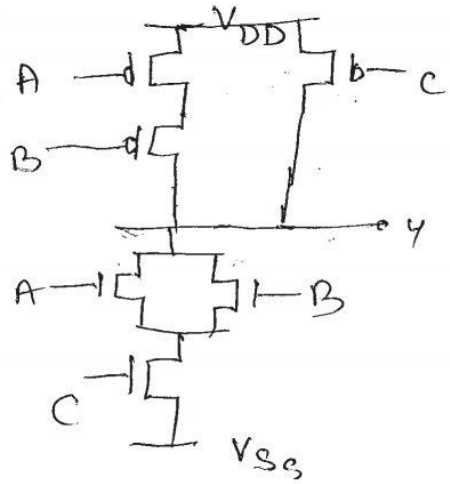
* for nMOS logic: Replace Pull up with nMOS depletion mode transistor with gate connected to source.

7) Similarly $Y = \overline{A'B + AB'}$ (xor gate).

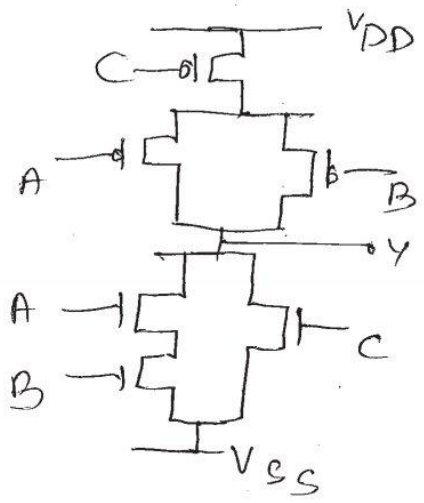
$Y = \overline{A'B + AB'}$

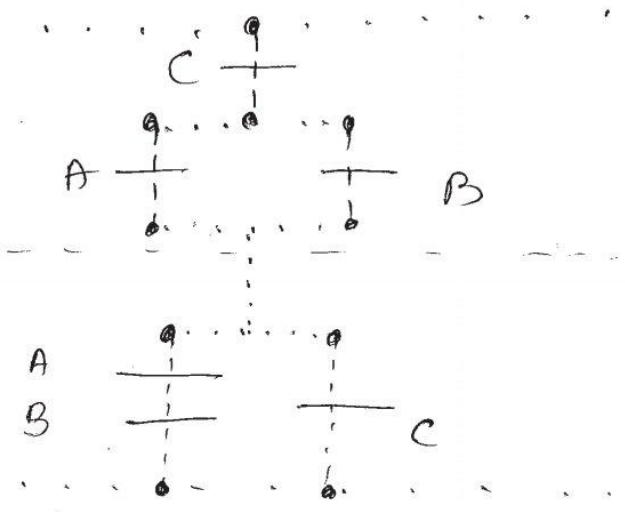
Connect inverter to o/p of xnor gate

8) $Y = \overline{(A+B)C}$



9) $Y = AB + C$





DESIGN RULES AND LAYOUTS

→ Design rules allow the translation of circuit design concepts, usually in stick diagrams or symbolic form into actual geometry in silicon.

→ Design rules govern the layout of individual components and interactions - spacings & electrical connections b/w the components.

→ Design rules are specific to a particular semiconductor manufacturing process. It determines low-level props of chip designs (how small individual logic gates are made, how small can the wires be).

→ As small a component size as possible is desired to increase the no. of functions in the chip. But fabrication error arise such as shorting together of wires, or absence of connection b/w wires, faulty transistors etc.

Design rules are used to minimize the occurrence of common fabrication problems and to bring yield of correct chips to acceptable level.

One of fabrication problem is that a wire or any feature being made too wide or too narrow. A too narrow wire may never conduct or may burn off when conducting. A wide wire may short itself with other wires. If poly crosses or cuts diffusion, then it is formation of a new element.

Remedy

1) Introduction of spacing rules
2) Introduction of min - width rules.

Min width rule:

Gives min size for layout element. It also ensures that even with minutest variations, the elem will be of acceptable size.

Spacing rule:-

Gives min distance b/w the edges of layout elems, so that even with minor variations it will not cause the element to overlap nearby layout elems.

Composition rules:-

Ensures that components are well- formed.

Construction rules (vias)

→ Material on both layers to be connected must extend beyond SiO_2 cut and cut must be [illegible]

Scalable Design Rules

→ Design rules can be scaled in terms of 'λ', which is the size of the smallest elem in the layout.

→ When devices shrink, layouts need not be completely redesigned. All features can be measured in integral multiples of 'λ'.

→ By choosing a value for λ, all dimensions set at a scalable layout.

→ Scalable layouts are advantageous as chips become faster as size shrinks.

→ Digital ckt designs scale, b'coz the cap loads that must be driven by logic gates shrink faster than the currents supplied by the Trs.

→ Assuming that the basic physical paramtrs of chip are shrunk by a factor of $1/x$.

Length = $L \rightarrow L/x$; Width = $W \rightarrow W/x$.

Thickness = $D \rightarrow D/x$

Supply $V_t = V_{DD} - V_{SS} \rightarrow (V_{DD} - V_{SS})/x$

Doping $\rightarrow N_d \rightarrow N_d/x$

Tr transconductance:

$$\hat{g_m} = x \cdot g_m$$

Threshold vtg:

$$\boxed{\hat{V_t} = \frac{V_t}{x}}$$

Sat^n Drain Current:

$$I_{ds} = K \frac{W}{L} [(V_{gs} - V_t)^2] .$$

$$K = \frac{\mu \epsilon_0 \epsilon_{ins}}{D}$$

$$\boxed{\hat{K} = K \cdot x}$$

$$\Rightarrow \boxed{\frac{\hat{I_{ds}}}{I_{ds}} = \frac{1}{x}}$$

&

$$\boxed{\frac{\hat{C_g}}{C_g} = \frac{1}{x}}$$

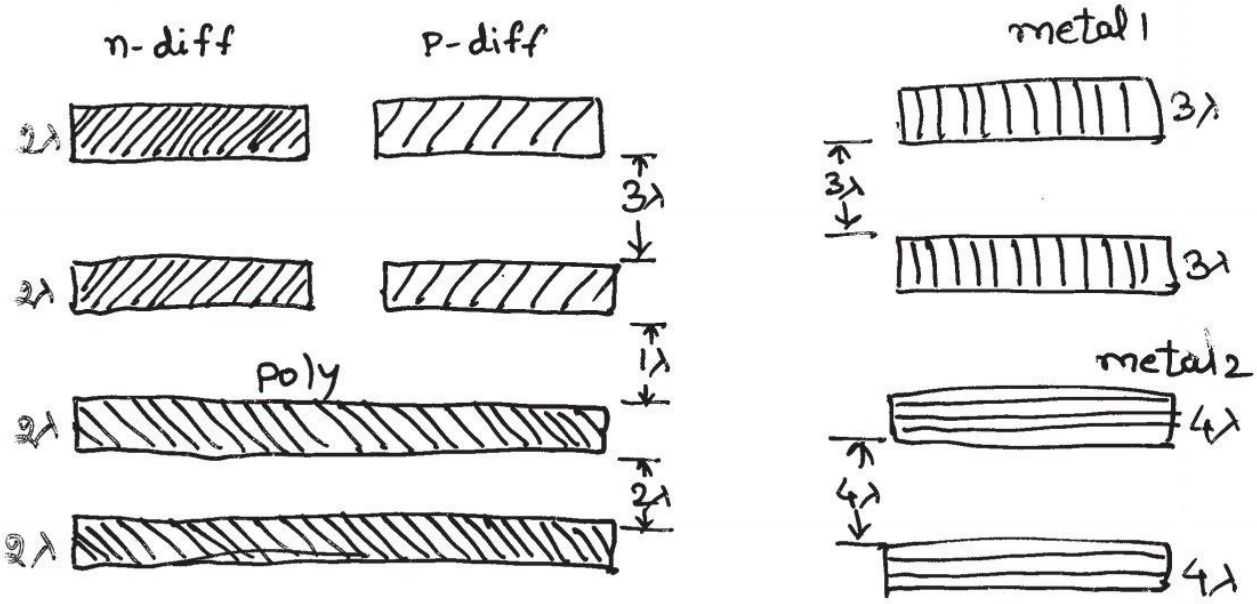
$\rightarrow$ $\frac{CV}{I}$ is measure of speed of ckt over scaling.

$$\therefore \frac{\hat{C}\hat{V}/\hat{I}}{CV/I} = \frac{1}{x}$$

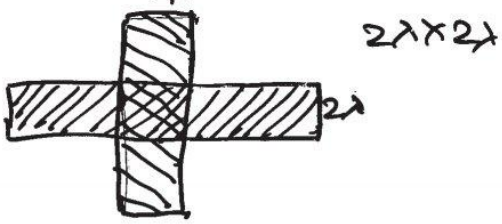
$\Rightarrow$ Scaling is done on λ, thus $\frac{\hat{\lambda}}{\lambda} = \frac{1}{x}$.

(thus speed up by factor x)

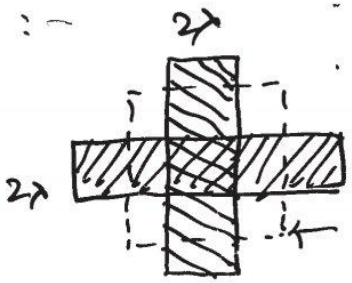
Design rules for wires (nMOS & CMOS)



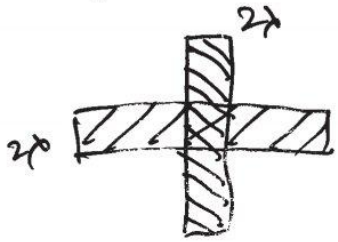
nMOS (enhancement) :-



nCMOS (Depletion) :-



pMOS (Enhancement)



Summary:

1) Metal 1 : min-width = 3λ
min-sep^n = 3λ

2) Metal 2 : min-width = 4λ
min-sep^n = 4λ

3) Poly : min-width = 2λ
min poly-poly sep^n = 2λ

4) P & n diffusion: min width = 2λ
min sep^n b/w same diff = 2λ.

5) Tubs: 10λ wide.

Min Separation b/w tub & src/drain = 5λ.

Tub Tie: P-tub tie : 2λ × 2λ cut, 4λ × 4λ metal, 4λ × 4λ p$^+$ diff
Ily n-tub tie.

Construction rules:-

1) Transistors : width = 2λ
Length = 2λ

2) Poly extends 2λ beyond active region.

3) Diffusion extends 2λ.

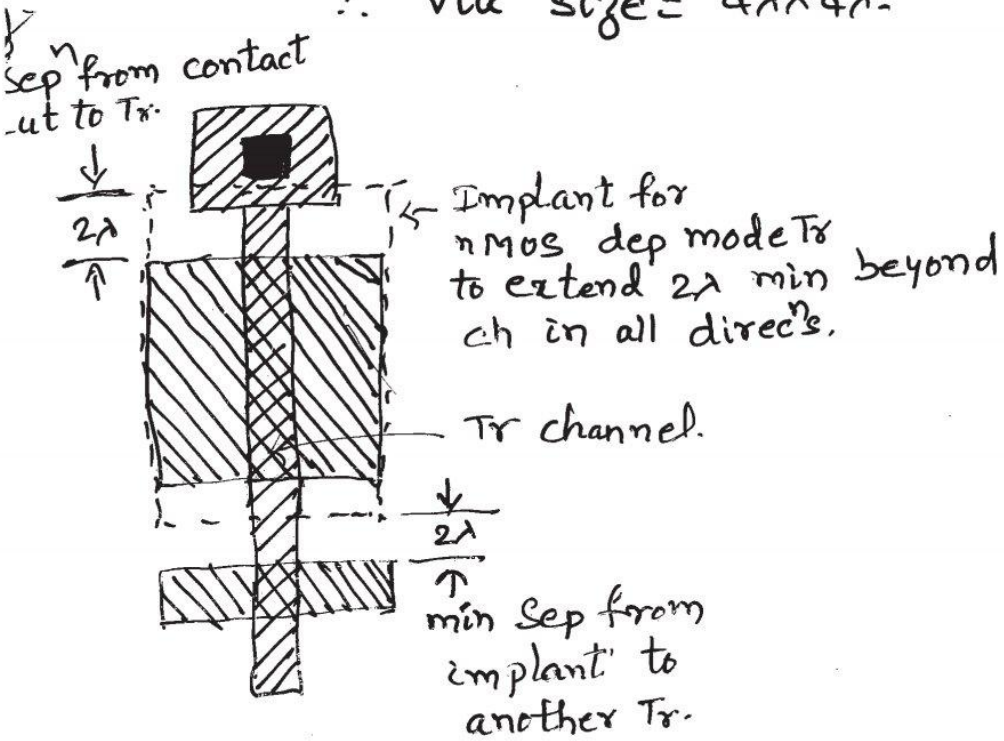
4) Active region must be atleast 1λ from poly-metal via, 2λ from another Tr,

Vias :

→ cuts : $2\lambda \times 2\lambda$

→ Material on both layers extend 1λ in all dirⁿ from cut.

∴ via size = $4\lambda \times 4\lambda$.



Extentions & Separations (Trs.)

Contact Cuts :

3 ways to make contacts b/w poly & diffusion in nMOS ckts :

(i) poly to metal then metal to diffusion
(ii) buried contact (poly to diff).
(iii) butting contact (poly to diff using metal).

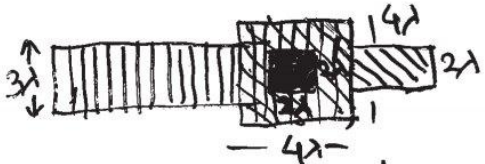
The $2\lambda \times 2\lambda$ contact cut indicates an area in which the oxide is to be removed down to the underlying polysi or diff surface

When deposition of metal layer takes place the metal is deposited thru contact cut areas onto underlying area so that contact is made b/w the layers.

ex:-

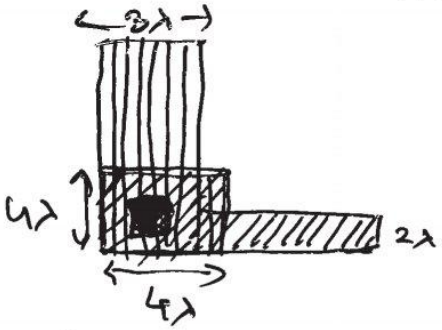
1) Metal1 to polysi or to diffusion.

Metal1 to poly.

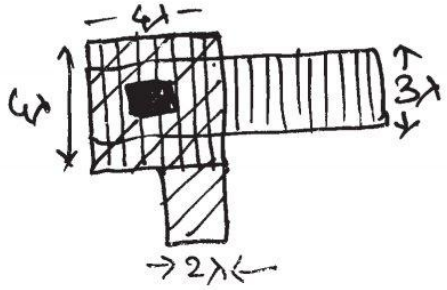


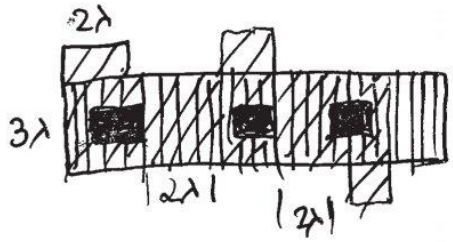
$2\lambda \times 2\lambda$: cut centered on $4\lambda \times 4\lambda$ superimposed areas of layers to be joined in all cases.

Metal1 to n-diff



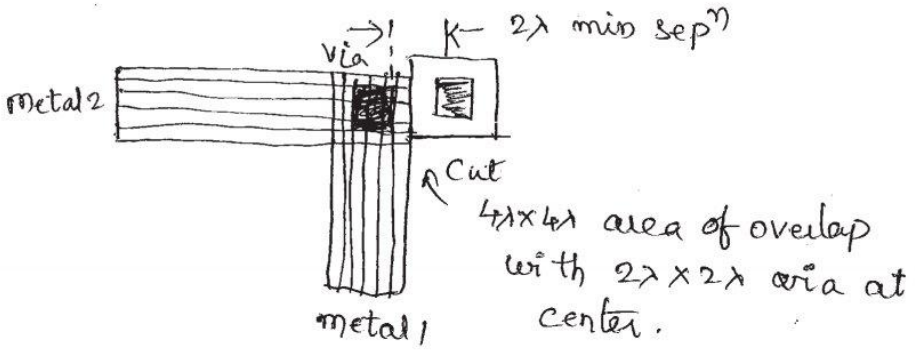
Metal1 to P-diff





Min Sep, Multiple cut

2) Via (Contact from metal2 to metal1)



NOTE: min sepⁿ b/w ~~me~~diffⁿ wire and poly wire = 1λ.

→ Contact cuts are also known as via cuts.

→ 4λ×4λ size.

→ Contact cut types:

(i) n/p diffⁿ to polysi
(ii) poly to metal1
(iii) n/p diffⁿ to metal1
(iv) metal1 to metal2.

Contact b/w polysi and diffusion wires can be done in 3 ways:-

(a) Polysi to the metal and then metal to polysi.

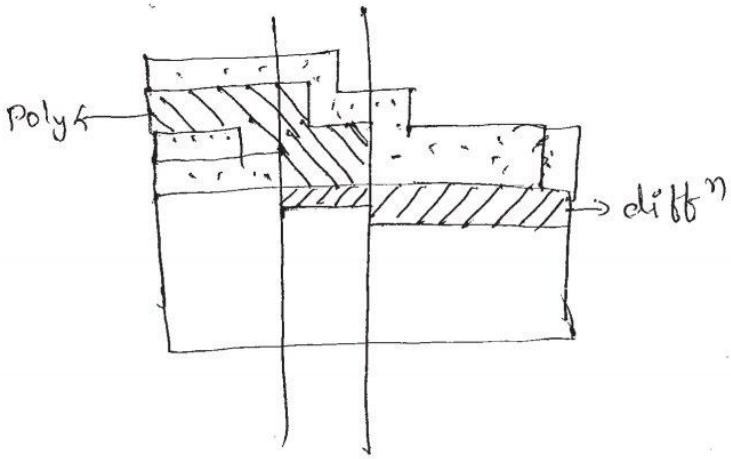
* oxide is removed from 2λ×2λ contact cut down to underlying polysi wire. Then metal is deposited. It flows thru the oxide etched area to polysi area. Then polysi is deposited on the surface, which acts as conduction path.

(b) Buried Contact

Before starting the process, there is oxide layer on Si surface, oxide is etched to expose the underlying [illegible] is deposited on the surface.

In the next step, diffⁿ is carried out and the exposed surface. When diffⁿ takes place impⁿs will diffuse into polysi as well as diffused area within the contact area.

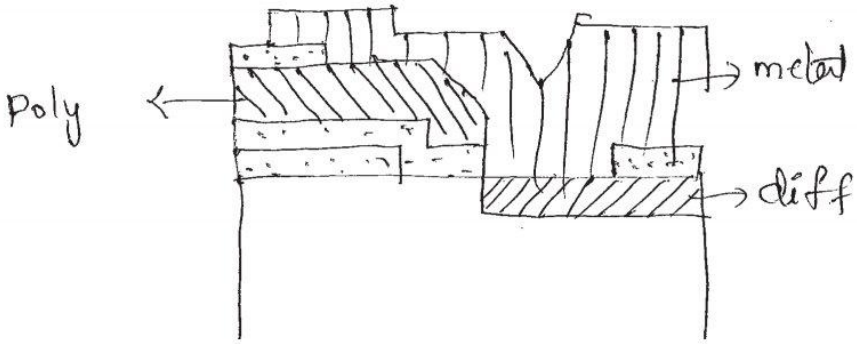
This ensures a satisfactory connecⁿ b/w polysi & diffⁿ. Buried contacts are smaller than butting contacts.



(c) Butting Contact:-

→ a complex process.

→ 2λ×2λ contact cut is made down to each layers to be joined. Layers are butted together so that two contact cuts become contiguous. The poly & diffⁿ outlines overlap & thin oxide under poly acts as mask in the diffⁿ process. Poly & diffused layers are butted together. The contact b/w two layers is then made by metal overlay.



Double metal MOS process rules

In this process a second metal layer is used so that V_{DD} & V_{SS} (gnd) rails in the system are distributed more flexibly on the chip. vias are used to establish connection blw metal 2 to other layers thru metal 1.

The first level metal can be used for local distribution of power & for signal lines.

CMOS Lambda-based design rules :-

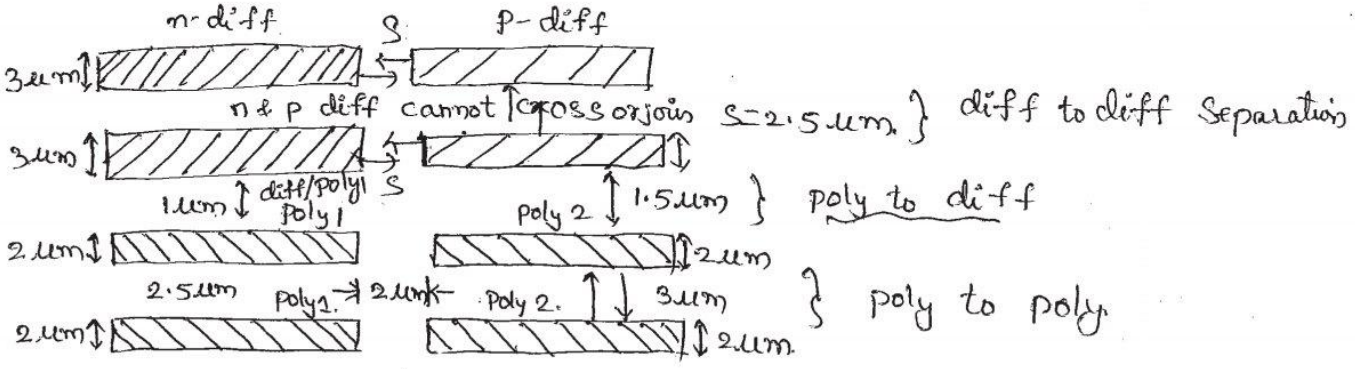
The rules of n-well (PMOS Tr), p-wires & special substrate contacts are added to the existing nMOS rules.

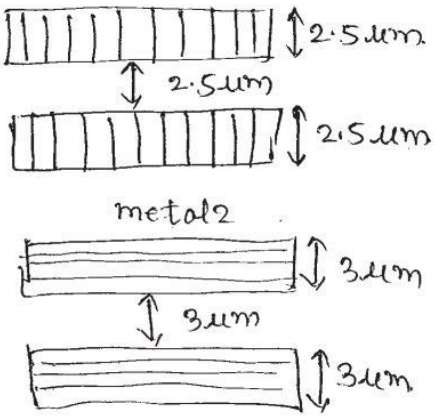
2 μm CMOS DESIGN RULES

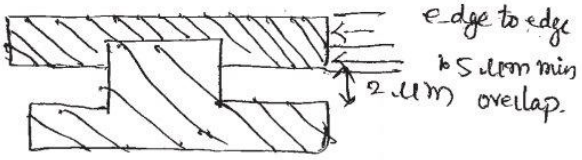
* 2 μm double metal, double poly

→ n-well : brown
Poly 1 : red
Poly 2 : Orange
n-diff : Green
P-diff : Yellow
} CMOS

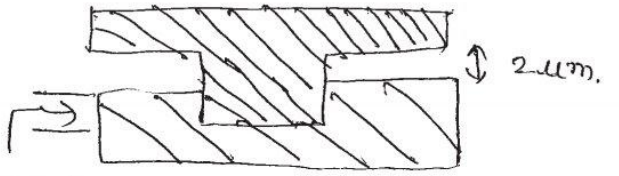
buried n+ subcoll : pale green
p-base : pink
} BiCMOS.







poly 2 overlapping poly 1.



1.5um min. overlap

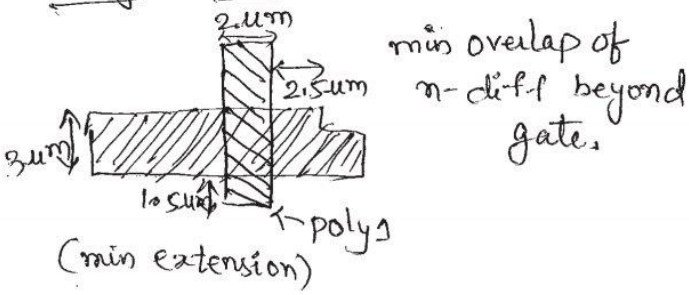
poly 1 overlapping poly 2.

fig: Design rules for wires (2 um CMOS).

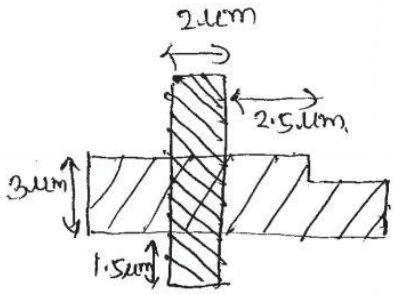
NOTE:-

For p-well CMOS, n-diff can only exist inside & p-diff wires outside p-well. For n-well CMOS, p-diff wires can only exist inside & n-diff wires outside n-well.

Design rules for transistors:-

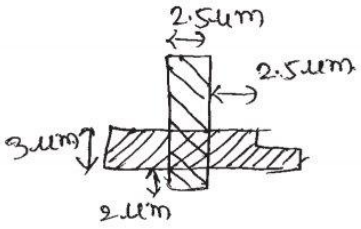


(i) n-type enhancement

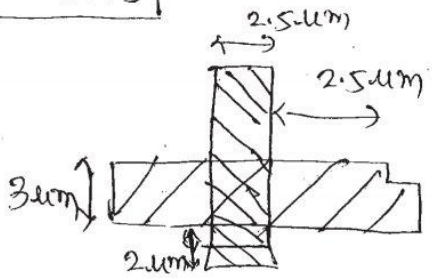


(ii) P-type Tr

fig:- PolySi Transistors.



(i) n-type Tr

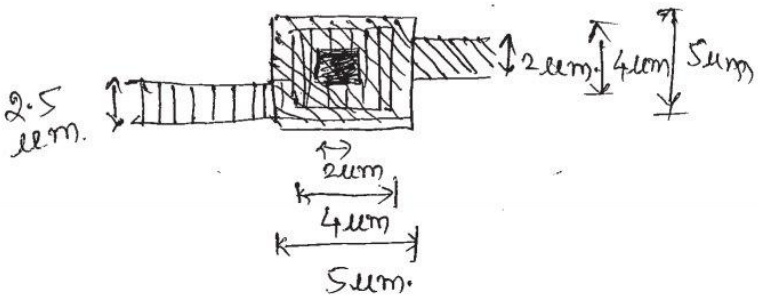


(ii) p-type Tr

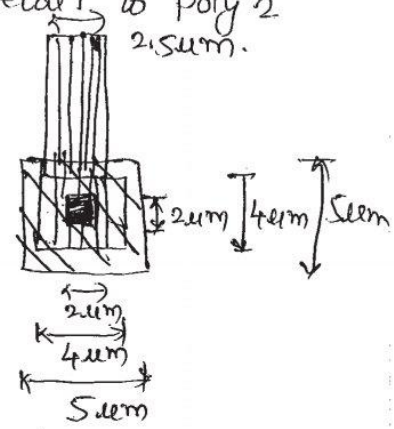
fig:- PolySi 2 Transistors.

Design rules

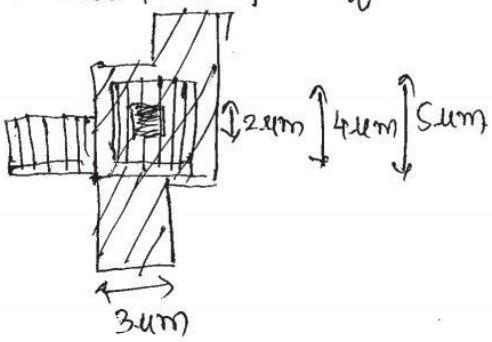
(a) Metal 1 to poly-1



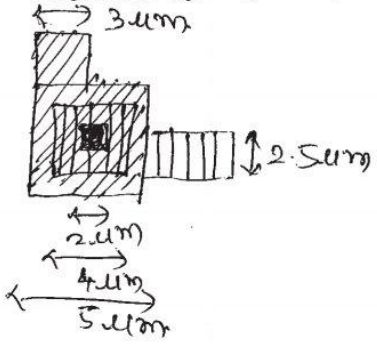
(b) Metal 1 to poly 2



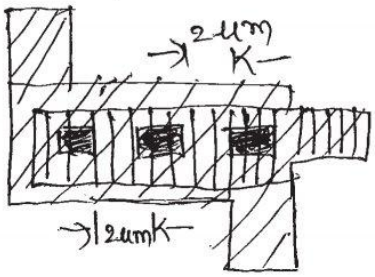
(c) Metal 1 to p diff.



(d) Metal 1 to n diff.

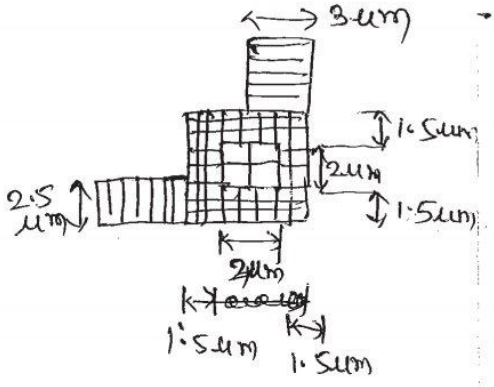


(e) Multiple contact cuts.



min spacing b/w contact cuts = 2µm

(f) Via metal 1/metal 2



Limitations of Scaling

(1) Substrate doping. $d = \sqrt{\frac{2\epsilon_{si}\epsilon_0 V}{qN_B}}$ (where $V = V_a + V_B$)

(2) Limits on miniaturization

(3) limits of interconnect & contact resistance.

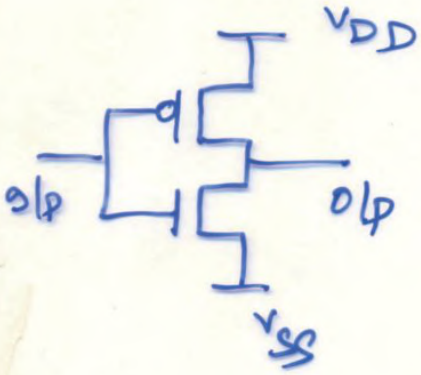
(4) Limits due to subthreshold currents.

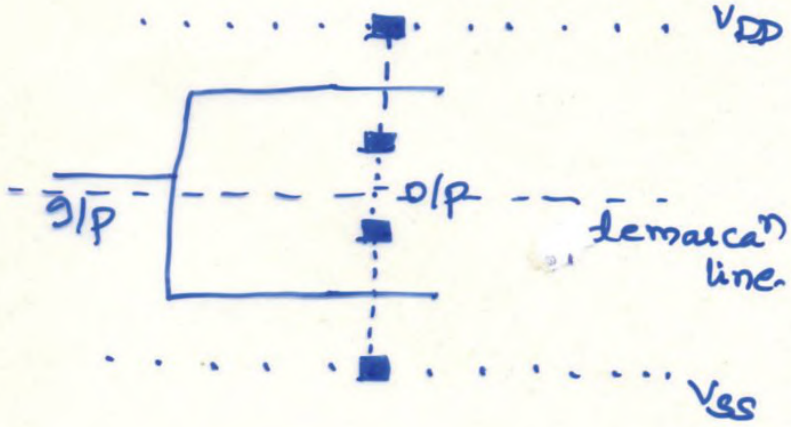
(5) Limits on logic levels & supply vtg due to noise.

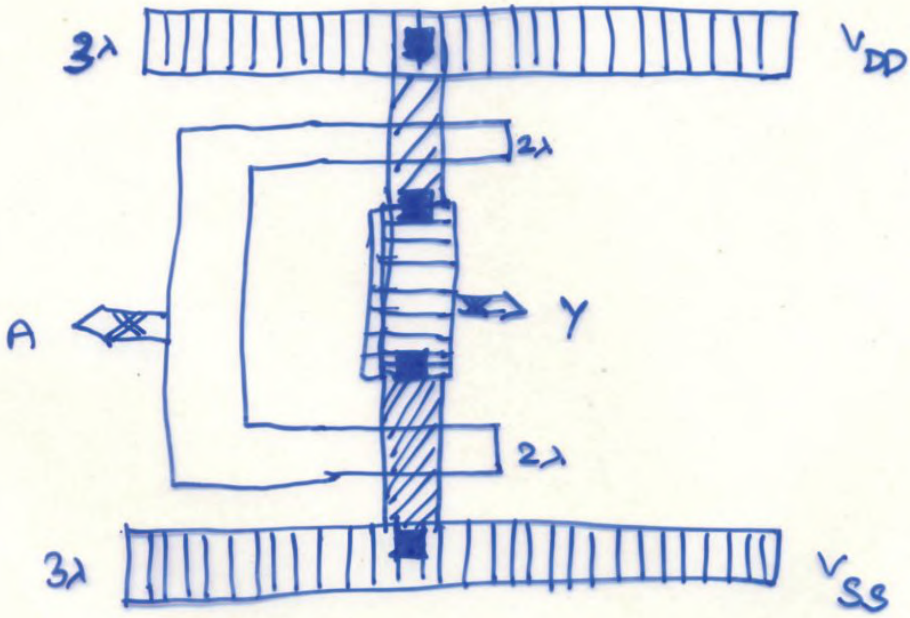
(6) limits due to current density.
[$J = 1$ to $2 mA/\mu m^2$]

Examples:

1) NOT (INVERTER)





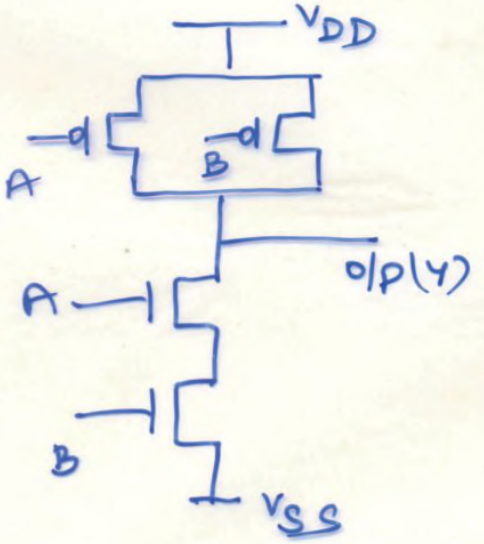


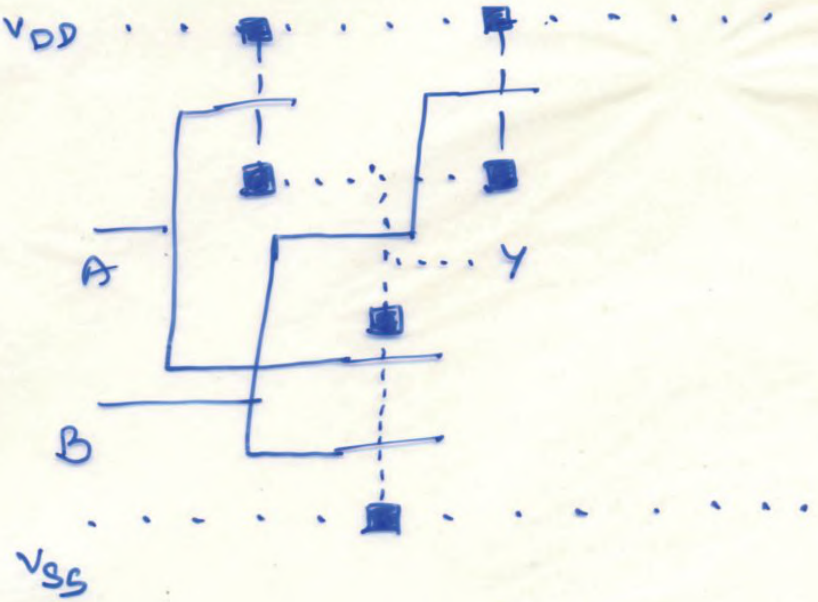
I/p: poly
O/p: Metal
V_{DD}, V_{ss}: Metal

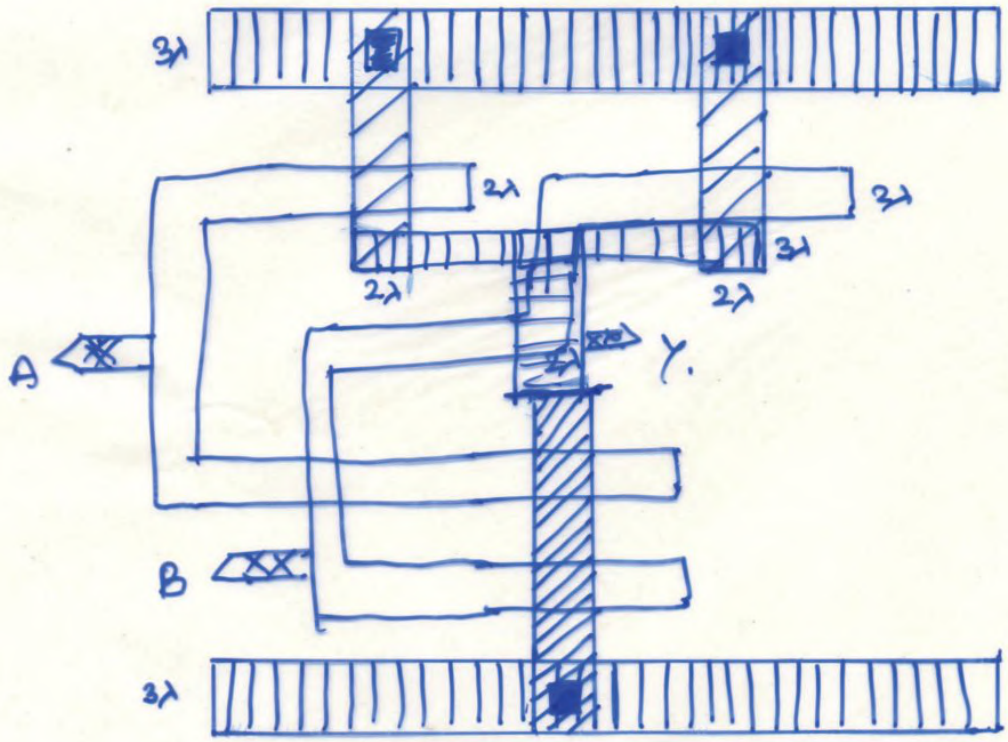
Color Codes:

Metal - Blue
Poly - Red.
n-diff - Green
P-diff - Yellow
Via - Black.

2) $Y = \overline{A \cdot B}$





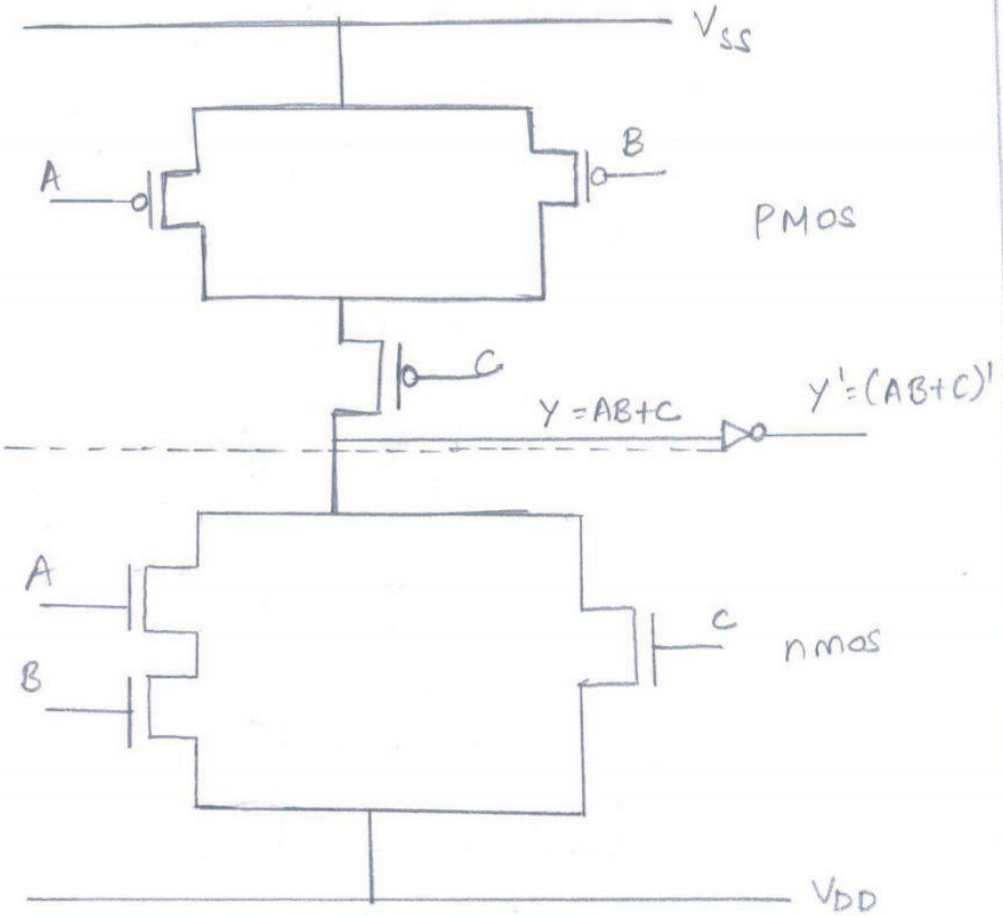


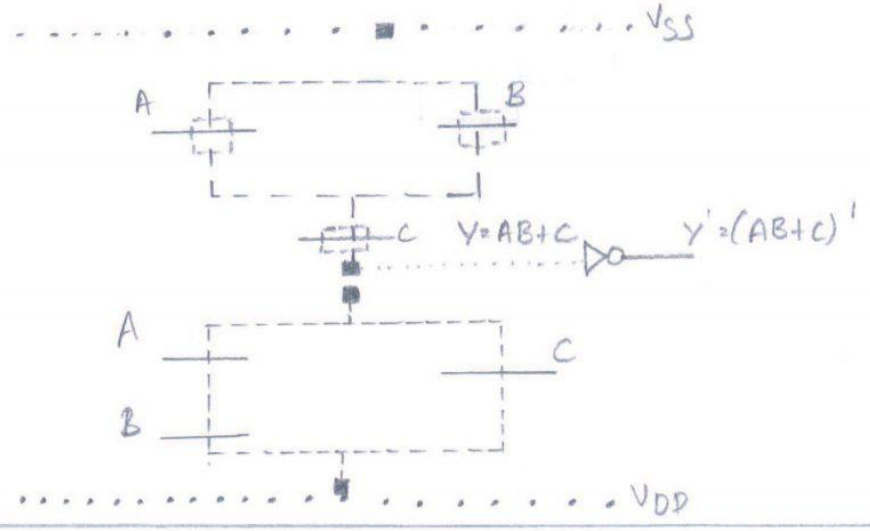
NOTE:- Via types:

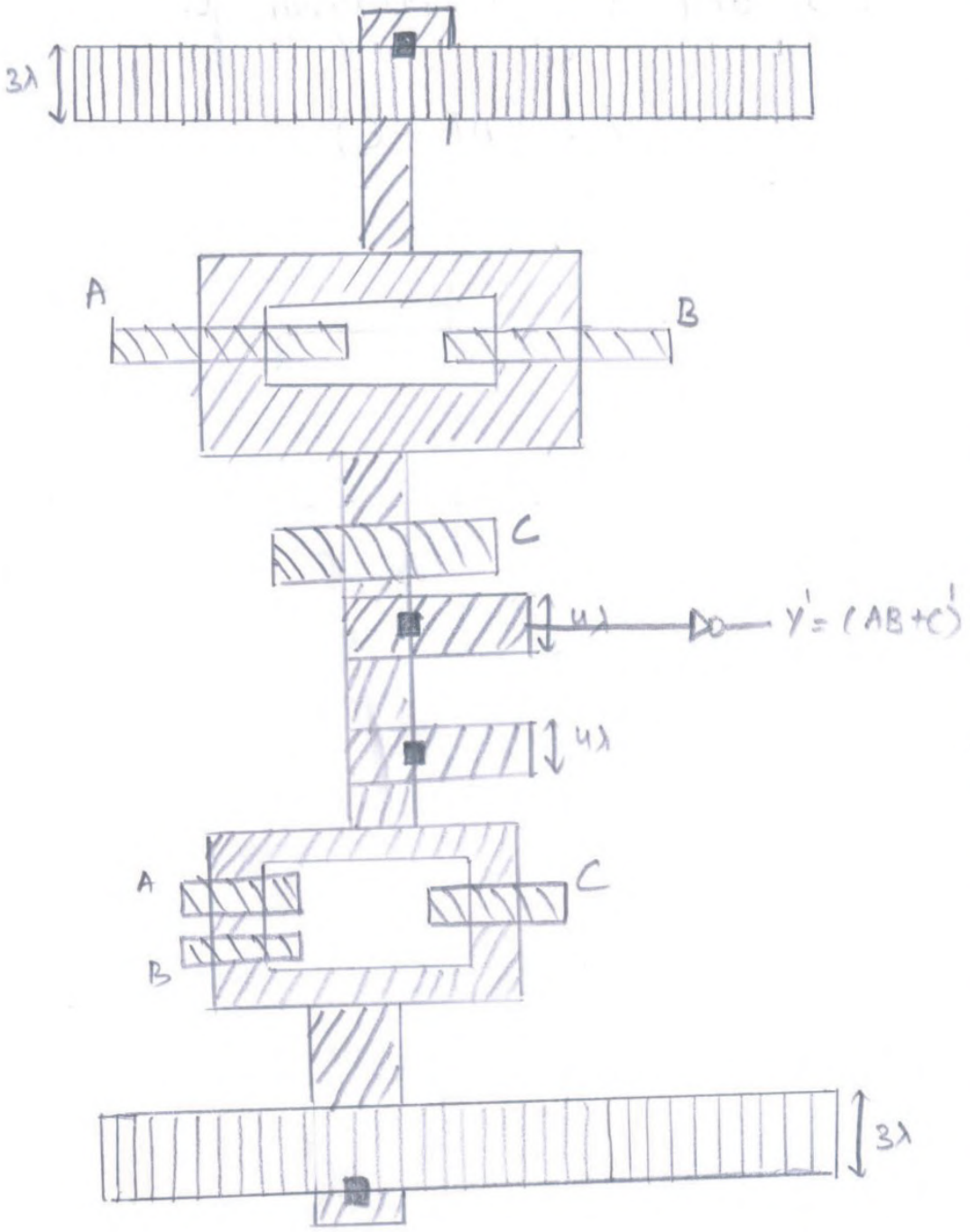
(i) n/p diff - poly
(ii) poly - metal 1
(iii) n/p diff - metal 1
(iv) metal 1 - metal 2

3) Stick and layout diagram for

$$Y = (AB + C)'$$







Scaling Factors for device Parameters:

(1) Gate Area (A_g):

$$A_g = W \cdot L$$

W & L scaled by $1/\alpha$.

$\therefore$ A_g scaled by $1/\alpha^2$

(2) Gate Cap Per Unit Area C_o or C_{ox}.

$$C_{ox} = \frac{\epsilon_{ox}}{D} = \frac{\epsilon_0 \epsilon_{ins}}{D}$$

$$\because \hat{D} = \frac{1}{\beta} D$$

$$\Rightarrow \boxed{\hat{C_{ox}} = \beta C_{ox}} \quad \text{(scaled by } \beta\text{)}$$

(3) Gate Cap C_g

$$C_g = C_{ox} \cdot W \cdot L$$

$$\hat{C_g} = \beta C_{ox} \cdot \frac{W}{\beta} \cdot \frac{L}{\alpha}$$

$$\hat{C_g} = \frac{\beta}{\alpha^2} \cdot C_{ox} \cdot W \cdot L$$

$$\boxed{\hat{C_g} = \frac{\beta}{\alpha^2} C_g.} \quad \text{(Scaled by } \frac{\beta}{\alpha^2}\text{)}.$$

(4) Parasitic Capacitance C_x:

$$C_x \propto \frac{A_x}{d}$$

where d: depletion width around S & D

$$\hat{d} = d/\alpha.$$

A_x: Area of depletion region around src or drain

$$\hat{A_x} = A_x/\alpha^2.$$

$$\therefore \hat{C_x} = \frac{A_x}{\alpha^2} \cdot \frac{1}{d/\alpha} = \frac{A_x}{\alpha \cdot d}$$

$\therefore$ C_x scaled by $1/\alpha$

(5) Carrier Density in Channel Q_{on}:

$$Q_{on} = C_{ox} \cdot V_{gs}.$$

where Q_{on}: avg charge per unit area in ch. in 'on' state.

C_{ox}: Scaled by β

V_{gs}: " " $1/\beta$

$$\therefore \hat{Q_{on}} = \beta \cdot C_{ox} \cdot \frac{1}{\beta} \cdot V_{gs} = Q_{on}$$

$\Rightarrow$ Q_{on} is scaled by 1.

(6) Channel Resistance R_{on}:

$$R_{on} = \frac{L}{W} \cdot \frac{1}{\varepsilon_{on} \cdot \mu}$$

where μ = carrier mobility (const).

R_{on} scaled by $\frac{1}{\alpha} \cdot \frac{1}{1/\alpha} \cdot 1 = 1$

(7) Gate Delay T_d.

$$T_d \propto R_{on} \cdot C_g$$

$$\hat{T_d} \propto 1 \cdot R_{on} \cdot \frac{\beta}{\alpha^2} \cdot C_g$$

$$\hat{T_d} \propto \frac{\beta}{\alpha^2} \cdot T_d$$

$\therefore$ Scaled by $\frac{\beta}{\alpha^2}$

(8) Max Operating Frequency f_o:

$$f_o = \frac{W}{L} \cdot \frac{\mu C_o V_{DD}}{C_g}$$

$$f_o \propto \frac{1}{T_d}$$

$\therefore$ f_o scaled by $\frac{\alpha^2}{\beta}$

(9) Saturation Current I_{dss}.

$$I_{dss} = \frac{C_o \mu}{2} \cdot \frac{W}{L} (v_{gs} - v_t)^2$$

$\because$ v_{gs} & v_t scaled by $1/\beta$ & C_o by β

$\Rightarrow$ I_{dss} scaled by $\beta \left(\frac{1}{\beta}\right)^2 = 1/\beta$

(10) Current Density J:

$$J = \frac{I_{dss}}{A}$$

'A' (area) of ch scaled by $1/\alpha^2$

$$\hat{I} = \frac{I_{dss}/\beta}{A/\alpha^2} = \frac{\alpha^2}{\beta} \cdot \frac{I_{dss}}{A} = \frac{\alpha^2}{\beta} J$$

$\therefore$ J is scaled by $\frac{\alpha^2}{\beta}$.

(11) Switching Egy Per Gate E_g.

$$E_g = \frac{C_g}{2} (V_{DD})^2$$

E_g scaled by $\frac{\beta}{\alpha^2} \cdot \frac{1}{\beta^2} = \frac{1}{\alpha^2 \beta}$

UNIT - IV

Subsystem Design

Subsystem Design : Subsystem Design, Shifters, Adders, ALUs, Multipliers : Array Multiplier, Serial parallel Multiplier, parity generator, comparators, zero/one Detectors, up/down counter, Memory elements : SRAM, DRAM, ROM, Serial Access Memories.

——— * ———

Subsystem Design :

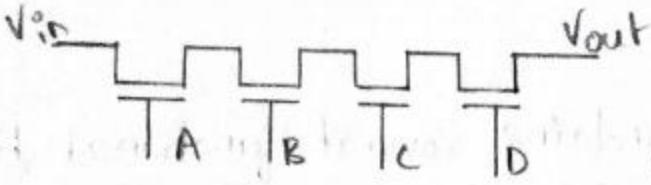
Introduction :-

* A digital System contains several functional blocks, which are known as Subsystems.
* For example, an arithmetic logic unit (ALU) contains functional blocks, or subsystems such as adders, subtractors, multipliers, dividers, comparators and shift registers.
* for designing digital systems in MOS technology there are two ways of building the circuits. They are Switch logic (pass Transistor, TG) and Gate logic (NMOS/CMOS/BiCMOS) deals with designing of subsystems, which is a small part in a larger system called leaf cell.
* The most basic leaf cell of any digital system is the logic gates and these are seen in different technologies like NMOS, CMOS and BiCMOS.
* While designing high Regularity should be maintained.

This indicates detailed designing of few leaf cells which can be replicated and interconnected to form System. (2)

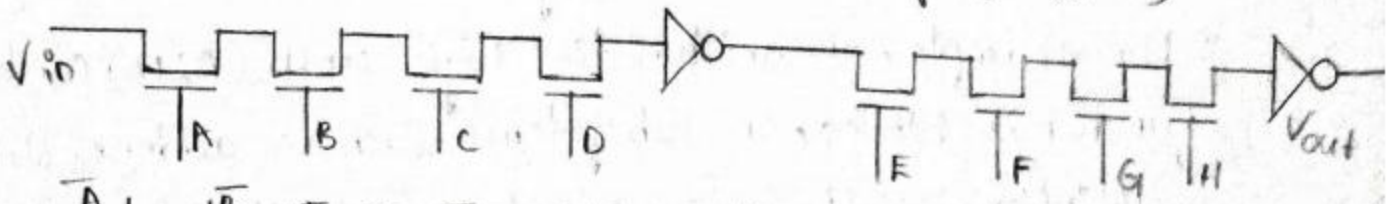
1. Switch logic :

* The Switch logic is built on 'pass transistors' & on 'transmission gates'. Switch logic is fast for small arrays and draws no static current from the supply rails. Hence power dissipation of such circuits is small because current flows only on switching.
* Pass transistor can be used as a switch in passing the signals. Switch logic arrangements using basic OR and AND connections along with other arrangements.



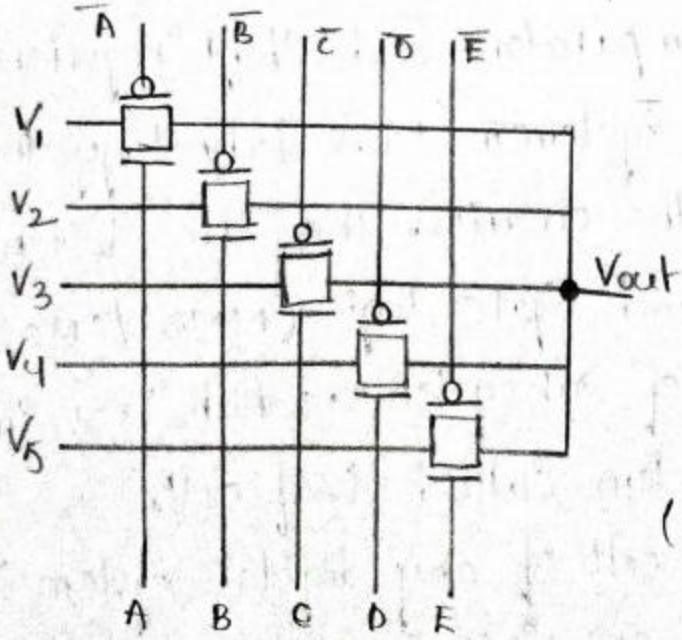
$V_{out} = V_{in}$ when $A \cdot B \cdot C \cdot D = 1$

(V_{out} logic levels will be degraded by V_t effects)



$V_{out} = V_{in}$ when $A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H = 1$

$V_{out} = ?$ when $A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \neq 1$



CMOS 5-way Selector

$V_{out} = V_1 \cdot A + V_2 \cdot B + V_3 \cdot C + V_4 \cdot D + V_5 \cdot E$

(V_{out} logic levels will not be degraded by V_t effects)

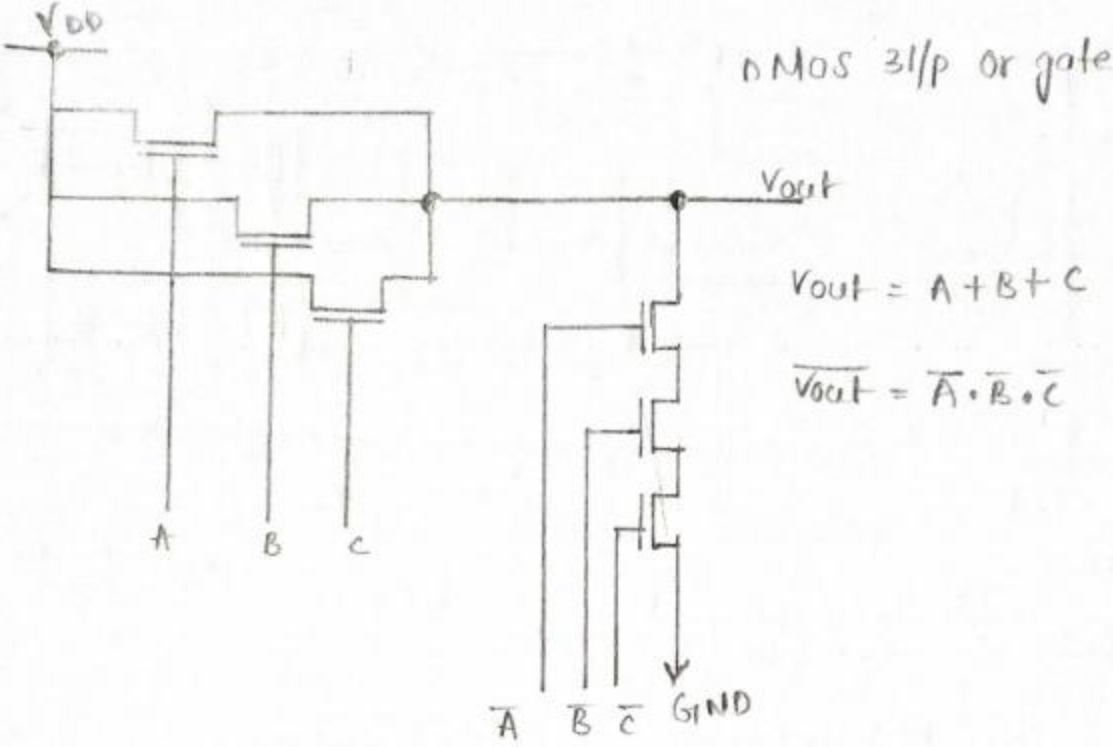
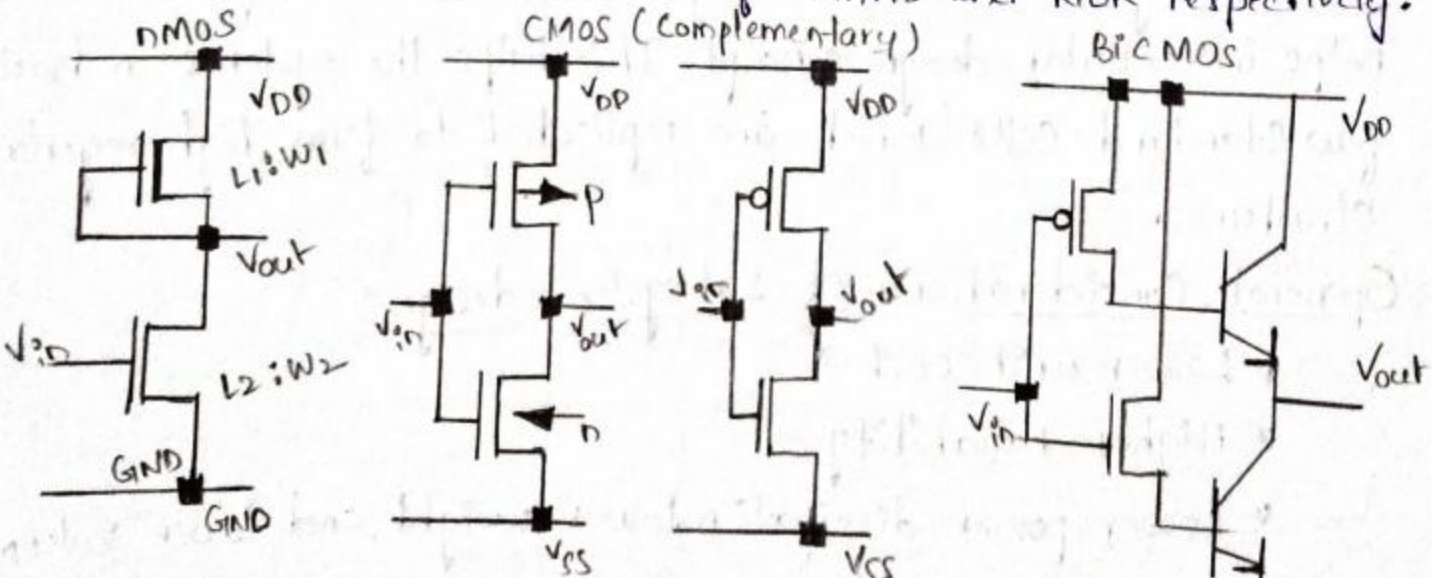


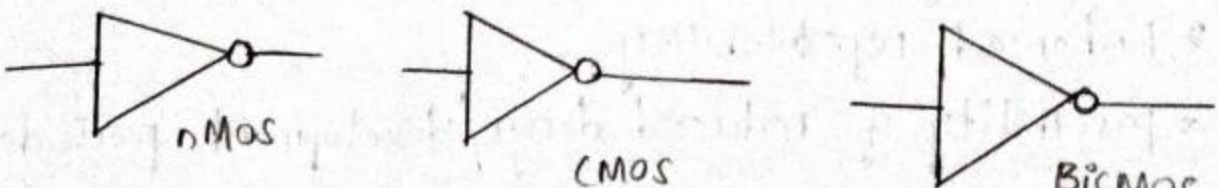
fig: Some switch logic arrangements.

2. Gate logic:

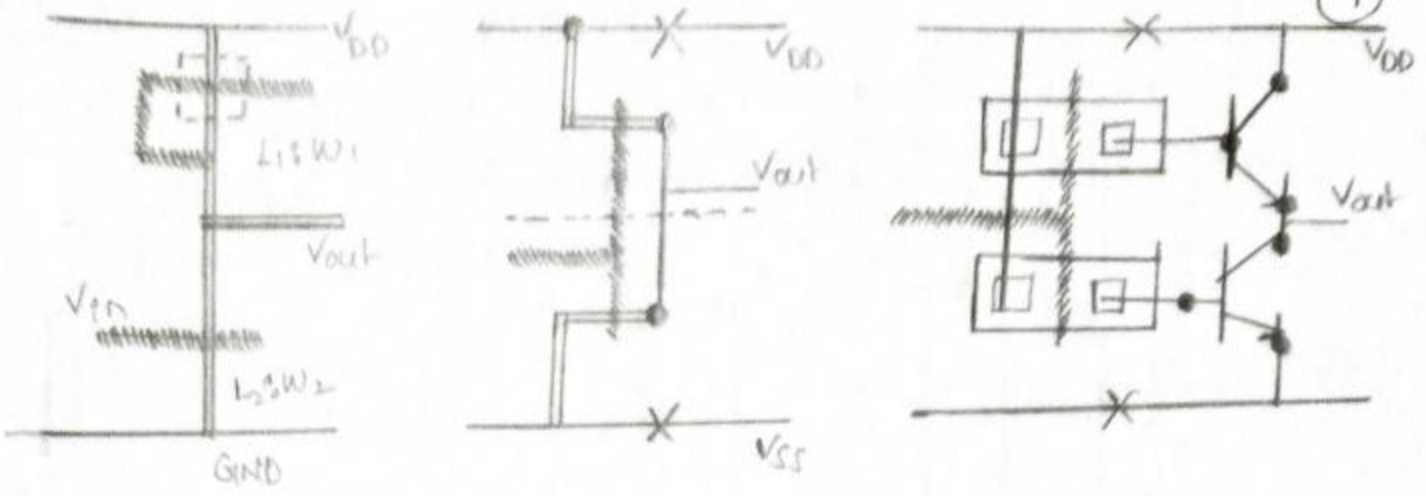
* Gate logic is based on the general arrangement of inverter as it is the simplest gate. The inverter can be constructed with nMOS, CMOS or BiCMOS technology. Similar to this NAND and NOR can be constructed. Also AND and OR can be constructed with an inverter for NAND and NOR respectively.



(a) Circuit Symbols



(b) Logic Symbols



nMOS CMOS simple BiCMOS

(c) Stick and Symbolic diagrams.

fig: nMOS, CMOS and BiCMOS inverters.

The whole design process will be associated if considerable care is taken with:

* Partitioning of the system so that there are clear subsystems with minimum interdependence and minimum complexity of interconnection between them.
* The design within the subsystems should be simple which helps in cellular design concept. This helps the systems in having few standard cells which are replicated to form high regular structures.

General Considerations of Subsystem design:

* Lower unit cost
* Higher reliability
* Lower power dissipation, lower weight and lower volume.
* Better performance
* Enhanced repeatability
* possibility of reduced design/development periods.

Architectural Issues:

* As the complexity of a system increases, the design time also increases. Thus while designing we have to adopt those design methodologies which allows handling complexity with reasonable time and reasonable amount of labor.

The following are the guidlines/architectural issues that needs to be considered while designing of the system.

1. Define the requirements carefully and properly.
2. partition the overall architecture into appropriate sub-systems.
3. Communication paths should be carefully selected in order to develop sensible interrelationships between the subsystems.
4. Draw the floor plan of how the system is to map onto the silicon.
5. Aim for regular structures so that design is largely a matter of replication.
6. Draw suitable stick or symbolic diagrams of the leaf-cells of the subsystem.
7. Convert each cell into layout.
8. Carry out design rule check carefully and thoroughly.
9. Simulate the performance of each cell/subsystem.

Shifters:

Combinational Shifters:

* Combinational shifters are useful for arithmetic operations, bit field extraction, etc.
  - Multiple shifts per clock cycle.
  - A multiple-shift shifter requires additional connectivity.