ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES::KADAPA
(AUTONOMOUS)

Utukur (Post), C.K. Dinne (V&M), Kadapa, YSR (Dist) Andhra Pradesh - 516 003
Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu
Accredited by NAAC with 'A' Grade, Bangalore

Department of Electronics & Communication Engineering
M.Tech. IN VLSI System Design
Effective for the batches admitted from 2023-24
M.Tech –I Semester

S.No	Category	Course Code	Course Title	Hours per week			Credits
				L	T	P	
1	PC	23VSDPC01	VLSI Technology	3	0	0	3
2	PC	23VSDPC02	CMOS Analog IC Design	3	0	0	3
3	PE	23VSDPE01a 23VSDPE01b 23VSDPE01c	**Program Elective – I** 1. Microchip Fabrication Techniques 2. Nano materials and Nanotechnology 3. CAD for VLSI	3	0	0	3
4	PE	23VSDPE02a 23VSDPE02b 23VSDPE02c	**Program Elective – II** 1. Device Modeling 2. FPGA Architectures and Applications 3. ASIC Design	3	0	0	3
5	MC	23VSDMC01	Research Methodology and IPR	2	0	0	2
6	PC	23VSDPC01L	VLSI Technology Lab	0	0	4	2
7	PC	23VSDPC02L	CMOS Analog IC Design Lab	0	0	4	2
8	AC	23VSDAC01a 23VSDAC01b 23VSDAC01c	**Audit Course – I** 1. English for Research paper writing 2. Disaster Management 3. Sanskrit for Technical Knowledge	2	0	0	0
Total							18

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Department of Electronics & Communication Engineering
M.Tech. IN VLSI System Design
Effective for the batches admitted from 2023-24
M.Tech –II Semester

S.No	Category	Course Code	Course Title	Hours per week			Credits
				L	T	P	
1	PC	23VSDPC03	CMOS Mixed Signal IC Design	3	0	0	3
2	PC	23VSDPC04	CMOS Digital IC Design	3	0	0	3
3	PE	23VSDPE03a 23VSDPE03b 23VSDPE03c	**Program Elective – III** 1. Physical Design Automation 2.Semiconductor Memory Design and Testing 3. Testing & Testability	3	0	0	3
4	PE	23VSDPE04a 23VSDPE04b 23VSDPE04c	**Program Elective – IV** 1. Low Power VLSI Design 2. IoT and its Applications 3. VLSI Signal Processing	3	0	0	3
5	PR	23VSDPR01	Technical seminar	0	0	4	2
6	PC	23VSDPC03L	CMOS Digital IC Design Lab	0	0	4	2
7	PC	23VSDPC04L	CMOS Mixed Signal Lab	0	0	4	2
8	AC	23VSDAC02a 23VSDAC02b 23VSDAC02c	**Audit Course – II** 1.Pedagogy Studies 2.Stress Management for Yoga 3.Personality Development through Life Enlightenment Skills	2	0	0	0
Total							18

Course Code	VLSI TECHNOLOGY	L	T	P	C
23VSDPC01		3	0	0	3
Semester		I			

Course Objectives:

1. To give exposure to different steps involved in fabrication of ICs using MOS transistor, CMOS/BICOM transistors and passive components.
2. To provide knowledge on electrical properties of MOS &BICMOS devices to analyze the Behavior of inverters designed with various loads.
3. To provide concepts to design building blocks of data path of any system using gates.
4. To teach about basic programmable logic devices and testing of CMOS circuits.

Course Outcomes (CO): Student will be able to

1. Acquire qualitative knowledge about the fabrication process of integrated circuit using MOS transistors,
2. Draw the layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit
3. Design building blocks of data path using gates.
4. Design simple memories using MOS transistors and can understand design of large memories
5. Understand the concept of testing and adding extra hardware to improve testability of system

UNIT - I		Lecture Hrs: 9

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends And Projections. Basic Electrical Properties OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds Relationships, Threshold Voltage V_t, Gm, Gds And Wo, Pass Transistor, MOS, CMOS & Bi- CMOS Inverters, Zpu/Zpd, MOS Transistor Circuit Model, Latch-Up In CMOS Circuits.

UNIT - II		Lecture Hrs: 9

LAYOUT DESIGN AND TOOLS: Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools. LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT - III		Lecture Hrs: 8

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing. SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT - IV		Lecture Hrs: 9

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

UNIT - V		Lecture Hrs: 8

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

Textbooks:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, EshraghianDougles, A. Pucknell, PHI of India Ltd.,2005.
2. Modern VLSI Design, 3rd Edition, Wayne Wolf , Pearson Education, fifth Indian Reprint, 2005.

Reference Books:

1. Principals of CMOS Design N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation Baker, Li Boyce, PHI, 2004.

Course Code	CMOS ANALOG IC DESIGN	L	T	P	C
23VSDPC02		3	0	0	3
Semester		I			

Course Objectives:

1. This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
2. Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
3. Intuitive understanding and real-life applications are emphasized throughout the course.
4. To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.
5. To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

Course Outcomes (CO): Student will be able to

1. Design MOSFET based analog integrated circuits.
2. Analyze analog circuits at least to the first order.
3. Appreciate the trade-offs involved in analog integrated circuit design.
4. Understand and appreciate the importance of noise and distortion in analog circuits.
5. Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
6. Solve engineering problems for feasible and optimal solutions in the core area

UNIT - I		Lecture Hrs:

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT - II		Lecture Hrs:

Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit

UNIT - III		Lecture Hrs:

Frequency Response of Amplifiers: General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT - IV		Lecture Hrs:

Feedback Amplifiers: General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation.

UNIT - V		Lecture Hrs:

Comparators: Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Textbooks:

1. B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition2016.
2. Paul.R.Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5thEdition, 2009.

Reference Books:

1.T.C.Carusone, D.A.Johns&K.Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012.
2. P.E.Allen&D.R.Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
3. R.Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.
4. Adel S. Sedra, Kenneth C. Smith, Arun, "Microelectronic Circuits", 6th Edition, Oxford University Press

Course Code	MICROCHIP FABRICATION TECHNIQUES	L	T	P	C
23VSDPE01a	**Program Elective – I**	3	0	0	3
Semester		I			

Course Objectives:

1. Comprehend impact of semiconductor industry on the design of development of integrated circuits.
2. Acquaint with clean room technology
3. Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
4. Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and 45nm technologies
5. Understand packaging principles

Course Outcomes (CO): Student will be able to

1. Understand various stages of fabrication
2. Understand Various packaging techniques and Design rules.
3. Classify various thin films and its characteristics.

UNIT - I		Lecture Hrs:

Introduction to Processing: Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction.

UNIT - II		Lecture Hrs:

Photolithography: Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT - III		Lecture Hrs:

Diffusion & Ion Implantation: Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT - IV		Lecture Hrs:

Film Depositions and Growth: Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT - V		Lecture Hrs:

Yield: Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.
Packaging: Chip characteristics, package functions, package operations.

Textbooks:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall, 2000.

Reference Books:

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

Course Code	NANOMATERIALS AND NANOTECHNOLOGY	L	T	P	C
23VSDPE01b	**Program Elective – I**	3	0	0	3
Semester		I			

Course Objectives:

1. To understand the basic idea behind the design and fabrication of nano scale systems.
2. To understand and frmulate new engineering solutions for current problems and technologies for future applications.
3. To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.

Course Outcomes (CO): Student will be able to

1. Understand the basic science behind the design and fabrication of nano scale systems.
2. Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. Make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
4. Gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

UNIT - I	Lecture Hrs:

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT - II	Lecture Hrs:

Fundamentals of nonmaterial's, Classification, Zero-dimensional nonmaterials, One-dimensional nonmaterials, Two-dimensional nano materials, three dimensional nonmaterials. Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.

UNIT - III	Lecture Hrs:

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT - IV	Lecture Hrs:

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT"s - Multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT"s, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs.

UNIT - V	Lecture Hrs:

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application.

Textbooks:

1. Kenneth J.Klabunde and Ryan M.Richards, "Nanoscale Materials in Chemistry", 2ndedition, John Wiley and Sons, 2009.
2. I Gusev and A Rempel, "Nanocrystalline Materials", Cambridge International Science Publishing, 1stIndian edition by Viva Books Pvt. Ltd. 2008.
3. B.S.Murty,P.Shankar,Baldev Raj, B.B.Rath, James Murday, "Nanoscience and Nanotechnology", Tata McGrawHill Education 2012.

Reference Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. Digital Integrated Circuits - A Design Perspective, Jan M.Rabaey, AnantChandrakasan, Borvivoje Nikolic, 2nd Edition, PHI.

Course Code	CAD FOR VLSI	L	T	P	C
23VSDPE01c	**Program Elective – I**	3	0	0	3
Semester		I			

Course Objectives:

1. To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
2. To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
3. To practice the application of fundamentals of VLSI technologies
4. To optimize the implemented design for area, timing and power by applying suitable constraints.

Course Outcomes (CO): Student will be able to

1. Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
2. Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
3. Practice the application of fundamentals of VLSI technologies
4. Optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT - I		Lecture Hrs:

Introduction :VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT - II		Lecture Hrs:

Partitioning : Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

UNIT - III		Lecture Hrs:

Floor Planning : Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT - IV		Lecture Hrs:

Placement and Routing :Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT - V		Lecture Hrs:

Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

Textbooks:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

Course Code	DEVICE MODELLING	L	T	P	C
23VSDPE02a	**Program Elective – II**	3	0	0	3
Semester		I			

Course Objectives:

1. To understand the physics of 2-terminal MOS operation and its characteristics
2. To understand the physics of 4-terminal MOSFET operation and its characteristics.
3. To analyze the SOI MOSFET electrical characteristics.

Course Outcomes (CO): Student will be able to

1. Understand the physics of 2-terminal MOS operation and its characteristics
2. Understand the physics of 4-terminal MOSFET operation and its characteristics.
3. Analyze the SOI MOSFET electrical characteristics.

UNIT - I		Lecture Hrs:

2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT - II		Lecture Hrs:

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit);MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit).

UNIT - III		Lecture Hrs:

4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT - IV		Lecture Hrs:

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT - V		Lecture Hrs:

SOI MOSFET: Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

Textbooks:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nanotransistors, World Scientific Publishing Co Pte Ltd 2017.

Reference Books:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.
3. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009

Course Code	FPGA ARCHITECTURES AND APPLICATIONS	L	T	P	C
23VSDPE02b	**Program Elective – II**	3	0	0	3
Semester		I			

Course Objectives:

1. To acquire knowledge about various architectures and device technologies of PLD's.
2. To comprehend FPGA Architectures.
3. To analyze System level Design and their application for Combinational and Sequential Circuits.
4. To familiarize with Anti-Fuse Programmed FPGAs.
5. To apply knowledge of this subject for various design applications.

Course Outcomes (CO): Student will be able to

1. Acquire knowledge about various architectures and device technologies of PLD's.
2. Comprehend FPGA Architectures.
3. Analyze System level Design and their application for Combinational and Sequential Circuits.
4. Familiarize with Anti-Fuse Programmed FPGAs.
5. Apply knowledge of this subject for various design applications.

UNIT - I		Lecture Hrs:

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT - II		Lecture Hrs:

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT - III		Lecture Hrs:

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT - IV		Lecture Hrs:

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT - V		Lecture Hrs:

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Textbooks:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier,Newnes.
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

Course Code	ASIC DESIGN	L	T	P	C
23VSDPE02c	**Program Elective – II**	3	0	0	3
Semester		I			

Course Objectives:

1. To understand different types of ASICs and their libraries.
2. To understand about programmable ASICs, I/O modules and their inter connects.
3. To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

Course Outcomes (CO): Student will be able to

1. Understand different types of ASICs and their libraries.
2. Understand about programmable ASICs, I/O modules and their inter connects.
3. Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT - I		Lecture Hrs:

Introduction to ASICs: Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT - II		Lecture Hrs:

Programmable ASICs and Programmable ASIC Logic Cells: The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT - III		Lecture Hrs:

I/O Cells and Interconnects & Programmable ASIC Design Software: DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT - IV		Lecture Hrs:

Low Level Design Entry and Logic Synthesis: Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT - V		Lecture Hrs:

Simulation, Test and ASIC Construction: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

Textbooks:

1. Michael John Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. L.J.Herbst, “Integrated Circuit Engineering”, Oxford Science Publications, 1996.

Reference Books:

1. HimanshuBhatnagar, “Advanced ASIC Chip Synthesis using Synopsis Design Compiler”, 2nd Edition, Kluwer Academic, 2001.

Course Code	RESEARCH METHODOLOGY AND IPR	L	T	P	C
23VSDMC01		3	0	0	3
Semester		I			

Course Objectives:

1. Identify an appropriate research problem in their interesting domain.
2. Understand ethical issues understand the Preparation of a research project thesis report.
3. Understand the Preparation of a research project thesis report
4. Understand the law of patent and copyrights.
5. Understand the Adequate knowledge on IPR

Course Outcomes (CO): Student will be able to

1. Analyze research related information
2. Follow research ethics
3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow World will be ruled by ideas, concept, and creativity.
4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among Students in general & engineering in particular.
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT - I		Lecture Hrs:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT - II		Lecture Hrs:

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT - III		Lecture Hrs:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - IV		Lecture Hrs:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT - V		Lecture Hrs:

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Textbooks:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

Reference Books:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.

4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “ Intellectual Property in New Technological Age”, 2016.

Course Code	VLSI Technology Lab	L	T	P	C
23VSDPC01L		0	0	4	2
Semester		I			

Course Objectives:

1. To explain the VLSI Design Methodologies using any VLSI design tool.
2. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

Course Outcomes (CO): Student will be able to

1. Design any logic circuit using CMOS transistor.
2. Use different software tools for analysis of circuits.
3. Design layouts to the CMOS circuits.
4. Use different software tools for analog layout

List of Experiments:

- The students are required to design the schematic diagrams using CMOS logic and to draw the layout diagrams to perform the experiments with the Industry standard EDA Tools with 180nm Technology.

1. Design and analysis of CMOS Inverter
2. Design and analysis of NAND and NOR Logic gates
3. Design and analysis of XOR and XNOR Logic gates
4. Design of AOI logic
5. Design and analysis of Full adder
6. Analysis of NMOS and PMOS characteristics
7. Design and analysis of Common source amplifier
8. Design and analysis of Common drain amplifier
9. Design of MOS differential amplifier
10. Design of two stage differential amplifier.
11. Design of Inverter Layout
12. Design of NAND/NOR Layout.

Note: Any TEN of the experiments are to be conducted

Software Required: i. Mentor Graphics/ Synopsis/ Cadence / Equivalent Industry Standard Software.
ii. Personal computer system with necessary software to run the programs and to Implement.

Course Code	CMOS ANALOG IC DESIGN LAB	L	T	P	C
23VSDPC02L		0	0	4	2
Semester		I			

Course Objectives:

1. To explain the VLSI Design Methodologies using VLSI design tool.
2. To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. To explain the Physical Verification in Layout Design
4. To fully appreciate the design and analyze of analog and mixed signal simulation
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

Course Outcomes (CO): Student will be able to

1. Explain the VLSI Design Methodologies using VLSI design tool.
2. Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
3. Explain the Physical Verification in Layout Design
4. Fully appreciate the design and analyze of analog and mixed signal simulation
5. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

List of Experiments:

- The students are required to design and implement any **TEN** Experiments using CMOS 130nm Technology.
- The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC.

Lab Requirements:

Software:

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

AUDIT COURSE-I

Course Code	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
23VSDAC01a		3	0	0	3
Semester		I			

Course Objectives:

1. Understand the essentials of writing skills and their level of readability
2. Learn about what to write in each section
3. Ensure qualitative presentation with linguistic accuracy

Course Outcomes (CO): Student will be able to

1. Understand the significance of writing skills and the level of readability
2. Analyze and write title, abstract, different sections in research paper
3. Develop the skills needed while writing a research paper

UNIT - I		Lecture Hrs:

1Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity.

UNIT - II		Lecture Hrs:

Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization.

UNIT - III		Lecture Hrs:

Introducing Review of the Literature – Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.

UNIT - IV		Lecture Hrs:

Key skills needed for writing a Title, Abstract, and Introduction.

UNIT - V		Lecture Hrs:

Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions.

Suggested Reading:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books).
Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

Course Code	DISASTER MANAGEMENT	L	T	P	C
23VSDAC01b		3	0	0	3
Semester		I			

Course Objectives:

1. Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluated are asterisk reduction and humanitarian response policy and practice from Multiple perspectives.
3. Developanunderstandingofstandardsofhumanitarianresponseandpracticalrelevanceinspecific types of disasters and conflict situations
4. Criticallyunderstandthestrengthsandweaknessesofdisastermanagementapproaches,planningand programming in different countries, particularly their home country or the countries they work in

Course Outcomes (CO): Student will be able to

UNIT - I		Lecture Hrs:

Introduction:
Disaster:Definition,FactorsandSignificance;DifferenceBetweenHazardandDisaster;Naturaland Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics.

UNIT - II		Lecture Hrs:

Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT - III		Lecture Hrs:

Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT - IV		Lecture Hrs:

Risk Assessment Disaster Risk:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT - V		Lecture Hrs:

Meaning,ConceptandStrategiesofDisasterMitigation,EmergingTrendsInMitigation.Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Suggested Reading:

1. R.Nishith,SinghAK,"DisasterManagementinIndia:Perspectives,issuesandstrategies
2. "'New Royal book Company. Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
3. GoelS.L.,DisasterAdministrationAndManagementTextAndCaseStudies",Deep&Deep Publication Pvt. Ltd., New Delhi.

Course Code	SANSKRITFOR TECHNICAL KNOWLEDGE	L	T	P	C
23VSDAC01c		3	0	0	3
Semester		I			

Course Objectives:

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. LearningofSanskrittodevelopthelogicinmathematics,science&othersubjects enhancing the memory power
4. The engineering scholars equipped with Sanskrit will be able to explore the huge
5. Knowledge from ancient literature

Course Outcomes (CO): Student will be able to

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science &technology can be understood
3. Being a logical language will help to develop logic in students

UNIT - I		Lecture Hrs:
Alphabets in Sanskrit,		
UNIT - II		Lecture Hrs:
Past/Present/Future Tense, Simple Sentences		
UNIT - III		Lecture Hrs:
Order, Introduction of roots		
UNIT - IV		Lecture Hrs:
Technical information about Sanskrit Literature		
UNIT - V		Lecture Hrs:
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics.		

Suggested Reading:

1.“Abhyaspustakam” –Dr.Vishwas, Sanskrit-Bharti Publication, New Delhi
2.“Teach Yourself Sanskrit” Prathama Deeksha- VempatiKutumbshastri, RashtriyaSanskrit Sansthanam, New Delhi Publication
3.“India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd.,New Delhi

Course Code	CMOS MIXED SIGNAL IC DESIGN	L	T	P	C
23VSDPC03		3	0	0	3
Semester		II			

Course Objectives:

1. To demonstrate first order filter with least interference
2. To extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
3. To design different A/D, D/A, modulators, demodulators and different filter for real time applications

Course Outcomes (CO): Student will be able to

1. Demonstrate first order filter with least interference
2. Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
3. Design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT - I		Lecture Hrs:

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT - II		Lecture Hrs:

Phased Lock Loop (PLL) : Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT - III		Lecture Hrs:

Data Converter: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT - IV		Lecture Hrs:

A to D Converters: Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Sigma Delta A/D coverters, Time- interleaved converters.

UNIT - V		Lecture Hrs:

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A.

Textbooks:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013.

Reference Books:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009.

Course Code	CMOS DIGITAL IC DESIGN	L	T	P	C
23VSDPC04		3	0	0	3
Semester		II			

Course Objectives:

1. To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
2. The course also involves analysis of performance metrics.
3. To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
4. To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Course Outcomes (CO): Student will be able to

1. Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,
2. Estimate Delay and Power of Adders circuits.
3. Classify different semiconductor memories.
4. Analyze, design and implement combinational and sequential MOS logic circuits.
5. Analyze complex engineering problems critically in the domain of digital IC design for conducting research.
6. Solve engineering problems for feasible and optimal solutions in the core area of digital ICs

UNIT - I		Lecture Hrs:

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT - II		Lecture Hrs:

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT - III		Lecture Hrs:

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT - IV		Lecture Hrs:

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT - V		Lecture Hrs:

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

1.Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

Course Code	PHYSICAL DESIGN AUTOMATION	L	T	P	C
23VSDPE03a	**Program Elective – III**	3	0	0	3
Semester		II			

Course Objectives:

1. To understand relation between automation algorithms and constraints posed by VLSI technology.
2. To adopt algorithms to meet critical design parameters.
3. To design area efficient logics by employing different routing algorithms and shape functions.
4. To simulate and synthesis different combinational and sequential logics.

Course Outcomes (CO): Student will be able to

1. Understand relation between automation algorithms and constraints posed by VLSI technology.
2. Adopt algorithms to meet critical design parameters.
3. Design area efficient logics by employing different routing algorithms and shape functions.
4. Simulate and synthesis different combinational and sequential logics.

UNIT - I		Lecture Hrs:

VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT - II		Lecture Hrs:

Layout: Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT - III		Lecture Hrs:

Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT - IV		Lecture Hrs:

Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis.

UNIT - V		Lecture Hrs:

High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

Textbooks:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998.
2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999.

Reference Books:

1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996.

Course Code	SEMICONDUCTOR MEMORY DESIGN AND TESTING	L	T	P	C
23VSDPE03b	**Program Elective – III**	3	0	0	3
Semester		II			

Course Objectives:

1. To understand different types of memories, their architectural and different packing techniques of memories.
2. To build fault models for memory testing.
3. To analyze different parameters that lead malfunctioning of memories.
4. To design reliable memories with efficient architecture to improve processes times and power.

Course Outcomes (CO): Student will be able to

1. Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.
2. Build fault models for memory testing.
3. Analyze different parameters that lead malfunctioning of memories.
4. Design reliable memories with efficient architecture to improve processes times and power.

UNIT - I		Lecture Hrs:

Random Access Memory Technologies :SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT - II		Lecture Hrs:

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

UNIT - III		Lecture Hrs:

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance :
RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory.

UNIT - IV		Lecture Hrs:

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.

UNIT - V		Lecture Hrs:

Advanced Memory Technologies and High-density Memory Packing Technologies
Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

Textbooks:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.

2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma, 2002, Wiley.
Reference Books:
1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, First Edition. Prentice all.

Course Code	TESTING & TESTABILITY	L	T	P	C
23VSDPE03c	**Program Elective – III**	3	0	0	3
Semester		II			

Course Objectives:

1. To understand the concepts of faults and testing in SoC
2. To implement the faults using simulation tools
3. To analyze BIST systems

Course Outcomes (CO): Student will be able to

1. Understand the concepts of faults and testing in SoC
2. Implement the faults using simulation tools
3. Analyze BIST systems

UNIT - I		Lecture Hrs:

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT - II		Lecture Hrs:

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT - III		Lecture Hrs:

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For SSF's In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

UNIT - IV		Lecture Hrs:

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan Architectures and Testing Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques Different Techniques, Syndrome Test and Signature Analysis.

UNIT - V		Lecture Hrs:

BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level. MEMORY BIST (MBIST): Memory Test Architectures and Techniques Introduction to Memory Test, JTAG Testing Features.

Textbooks:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Pulishers.

Reference Books:

1. P.K. Lala, "Digital Circuits Testing and Testability", Academic Press.
2. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
3. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs.

Course Code	LOW POWER VLSI DESIGN	L	T	P	C
23VSDPE04a	**Program Elective – IV**	3	0	0	3
Semester		II			

Course Objectives:

1. To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
2. To implement Low power design approaches for system level and circuit level measures.
3. To design low power adders, multipliers and memories for efficient design of systems.

Course Outcomes (CO): Student will be able to

1. Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
2. Implement Low power design approaches for system level and circuit level measures.
3. Design low power adders, multipliers and memories for efficient design of systems.

UNIT - I		Lecture Hrs:

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects – Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II		Lecture Hrs:

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT - III		Lecture Hrs:

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT - IV		Lecture Hrs:

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT - V		Lecture Hrs:

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbooks:

1.CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press.
2.Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000

Course Code	IOT AND ITS APPLICATIONS	L	T	P	C
23VSDPE04b	**Program Elective – IV**	3	0	0	3
Semester		II			

Course Objectives:

1. To apply the Knowledge in IOT Technologies and Data management.
2. To determine the values chains Perspective of M2M to IOT.
3. To implement the state of the Architecture of an IOT.
4. To compare IOT Applications in Industrial & real world.
5. To demonstrate knowledge and understand the security and ethical issues of an IOT.

Course Outcomes (CO): Student will be able to

1. Apply the Knowledge in IOT Technologies and Data management.
2. Determine the values chains Perspective of M2M to IOT.
3. Implement the state of the Architecture of an IOT.
4. Compare IOT Applications in Industrial & real world.
5. Demonstrate knowledge and understand the security and ethical issues of an IOT.

UNIT - I		Lecture Hrs:

Fundamentals of IoT: Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.

IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT - II		Lecture Hrs:

IoT Protocols: IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT - III		Lecture Hrs:

Design and Development: Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT - IV		Lecture Hrs:

Data Analytics and Supporting Services: Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT - V		Lecture Hrs:

Case Studies/Industrial Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino).

Textbooks:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities Press,2015

Reference Books:

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence", Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.

Course Code	VLSI SIGNAL PROCESSING	L	T	P	C
23VSDPE04c	**Program Elective – IV**	3	0	0	3
Semester		II			

Course Objectives:

1. To study the existing architectures suitable for VLSI.
2. To understand the concepts of folding and unfolding algorithms and applications.
3. To design new architectures suitable for VLSI.
4. To implement fast convolution algorithms.

Course Outcomes (CO): Student will be able to

1. Study the existing architectures suitable for VLSI.
2. Understand the concepts of folding and unfolding algorithms and applications.
3. Design new architectures suitable for VLSI.
4. Implement fast convolution algorithms.

UNIT - I		Lecture Hrs:

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT - II		Lecture Hrs:

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT - III		Lecture Hrs:

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT - IV		Lecture Hrs:

Fast Convolution: Introduction – Cook - Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT - V		Lecture Hrs:

Low Power Design: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches.

Textbooks:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998.
2. Kung S. Y, H. J. While House, T. Kailath ,VLSI and Modern Signal processing , Prentice Hall, 1985.

Reference Books:

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing , Prentice Hall, 1994.
2. Medisetti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), 1995.

Course Code	CMOS DIGITAL IC DESIGN LAB	L	T	P	C
23VSDPC03L		0	0	4	2
Semester		I			

Course Objectives:

1.To explain the VLSI Design Methodologies using any VLSI design tool.
2. To grasp the significance of various design logic Circuits in full-custom IC Design.
3. To explain the Physical Verification in Layout Extraction.
4. To fully appreciate the design and analyze of CMOS Digital Circuits.
5. To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Course Outcomes (CO): Student will be able to

1. Explain the VLSI Design Methodologies using any VLSI design tool.
2. Grasp the significance of various design logic Circuits in full-custom IC Design.
3. Explain the Physical Verification in Layout Extraction.
4. Fully appreciate the design and analyze of CMOS Digital Circuits.

Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

- The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11.Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

Course Code	CMOS Mixed Signal Lab	L	T	P	C
23VSDPC04L		0	0	4	2
Semester		I			

Course Objectives:

1. To design and simulate op-amp for given specifications
2. To design and simulate data converter for given specifications
3. To design and simulate PLL and VCO for given specifications
4. To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Course Outcomes (CO): Student will be able to

1. Design and simulate op-amp for given specifications
2. Design and simulate data converter for given specifications
3. Design and simulate PLL and VCO for given specifications
4. Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

- The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology.

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.
8. Layouts of All the circuits Designed and Simulated
9. Design of PLL
10. Fully compensated op-amp with resistor and miller compensation

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

References:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley,1986.
3. Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

AUDIT COURSE-II

Course Code	PEDAGOGY STUDIES	L	T	P	C
23VSDAC02a		3	0	0	3
Semester		II			

Course Objectives:

1. Reviewexistingevidenceonthereviewtopictoinformprogrammedesignandpolicy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Course Outcomes (CO): Student will be able to

1. Whatpedagogicalpracticesarebeingusedbyteachersinformalandinformalclassrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what
3. Conditions, and with what population of learners?
4. Howcanteachereducation (curriculumandpracticum) andtheschoolcurriculumand guidance materials best support effective pedagogy?

UNIT - I		Lecture Hrs:

Introduction and Methodology: Aims and rationale, Policy back ground, Conceptual frame work and terminology Theories oflearning,Curriculum,Teachereducation.Conceptualframework,Research questions**.** Overview of methodology and Searching.

UNIT - II		Lecture Hrs:

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT - III		Lecture Hrs:

Evidence on theeffectivenessofpedagogicalpractices,Methodologyfortheindepthstage:quality assessmen t of included studies. How can teacher education (curriculumandpracticum) andthescho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of th body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT - IV		Lecture Hrs:

Professional development: Alignment with classroom practices and follow-up support, Peer support, Support from the head eacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT - V		Lecture Hrs:

Researchgapsandfuturedirections: Researchdesign, Contexts, Pedagogy, Teachereducation**,** Curriculum and assessment**,** Dissemination and research impact.

Suggested Reading :

1. AckersJ,HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare, 31 (2): 245-261.
2. AgrawalM(2004)Curricularreforminschools:Theimportanceofevaluation,Journalof
3. Curriculum Studies, 36 (3): 361-379.
4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teachereducation research project (MUSTER) country report 1. London: DFID.
5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013)Improving teaching and learning of basic maths and reading in Africa: Does teacherpreparation count?International Journal Educational Development, 33 (3): 272–282.
6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell. Chavan M (2003)ReadIndia: A mass scale, rapid, 'learning to read'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

Course Code	**STRESSMANAGEMENT BY YOGA**	L	T	P	C
23VSDAC02b		3	0	0	3
Semester		II			

Course Objectives:

1. To achieve overall health of body and mind
2. To overcome stres

Course Outcomes (CO): Student will be able to

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency .

UNIT - I		Lecture Hrs:

Definitions of Eight parts of yog.(Ashtanga)

UNIT - II		Lecture Hrs:

Yam and Niyam.

UNIT - III		Lecture Hrs:

Do`s and Don'ts in life.
i) Ahinsa, satya ,astheya, bramhacharyaand aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT - IV		Lecture Hrs:

Asan and Pranayam

UNIT - V		Lecture Hrs:

i)Variousyogposesand theirbenefitsformind &body
ii)Regularizationofbreathingtechniques and its effects-Types ofpranayam

Suggested Reading :

1.'Yogic Asanas forGroupTarining-Part-I": Janardan SwamiYogabhyasiMandal, Nagpur
2."Rajayogaor conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata .

Course Code	PERSONALITY DEVELOPMENT THROUGHLIFE ENLIGHTENMENTSKILLS	L	T	P	C
23VSDAC02c		3	0	0	3
Semester		II			

Course Objectives:

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

Course Outcomes (CO): Student will be able to

1. StudyofShrimad-Bhagwad-Geetawillhelpthestudentindevelopinghispersonalityand achieve the highest goal in life
2. The person who has studied Geetawilllead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students.

UNIT - I		Lecture Hrs:

Neetisatakam- Holistic development of personality
Verses-19,20,21,22(wisdom)
Verses-29,31,32(pride &heroism)
Verses-26,28,63,65(virtue)

UNIT - II		Lecture Hrs:

Neetisatakam- Holistic development of personality
Verses-52,53,59(dont's)
Verses-71,73,75,78(do's)

UNIT - III		Lecture Hrs:

Approach to day to day work and duties.
ShrimadBhagwadGeeta:Chapter2-Verses41,47,48,
Chapter3-Verses13,21,27,35,Chapter6-Verses5,13,17,23,35,
Chapter18-Verses45,46,48.

UNIT - IV		Lecture Hrs:

Statements of basic knowledge.
ShrimadBhagwadGeeta:Chapter2-Verses 56,62,68
Chapter12 -Verses13,14,15,16,17,18
Personality of Rolemodel. Shrimad Bhagwad Geeta:

UNIT - V		Lecture Hrs:

Chapter2-Verses 17,Chapter3-Verses36,37,42,
Chapter4-Verses18,38,39
Chapter18– Verses37,38,63

Suggested Reading :

1."SrimadBhagavadGita"bySwamiSwarupanandaAdvaitaAshram(PublicationDepartment), Kolkata
2.Bhartrihari'sThree Satakam (Niti-sringar-vairagya) by P.Gopinath, RashtriyaSanskrit Sansthanam, Delhi.