ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES
(AUTONOMOUS)
UTUKUR, C. K. DINNE (V & M), KADAPA, YSR DIST.
Approved by AICTE, New Delhi & Affiliation to JNTUA, Anantapuramu.
Accredited by NAAC with 'A' Grade, Bangalore & NBA (EEE, ECE & CSE)

DEPARTMENT OF
ELECTRICAL AND ELECTRONICS ENGINEERING

ANALOG CIRCUITS

(23HES0403)

COURSE MATERIAL

B. TECH II YEAR II SEM

II Year B.Tech. EEE – II Semester

L	T	P	C
3	0	0	3

(23HES0403) ANALOG CIRCUITS

Course Outcomes:

CO	Statements	Blooms Level
CO1	Understand the concepts of diode clipping and clamping circuits, different amplifier configurations, operation of oscillator circuits, operational amplifiers, timers, ADC and DAC	L2
CO2	Apply the above concepts for different circuit design	L3
CO3	Analyze various circuit characteristics by using Amplifiers, Transistors, Comparators, Wave form generators, ADC and DAC	L4
CO4	Analyze various circuit characteristics by using timers, Phase locked loops and operational amplifiers	L4
CO5	Evaluate different system configurations by using various amplifier, transistor and waveform generators	L5

UNIT I

Diode clipping and clamping circuits: Diode clippers, clipping at two independent levels, Transfer characteristics of clippers, clamping circuit operation.

DC biasing of BJTs: Load lines, Operating Point, Bias Stability, Collector-to-Base Bias, Self-Bias, Stabilization against Variations in V_{BE} and β for the Self-Bias Circuit, Bias Compensation, Thermal Runaway, Thermal Stability.

UNIT II

Small Signals Modeling of BJT: Analysis of a Transistor Amplifier Circuit using h-parameters, Simplified CE Hybrid Model, Analysis of CE, CC, CB Configuration using Approximate Model, Frequency Response of CE and CC amplifiers.

Feedback Amplifiers: Classification of Amplifiers, the Feedback Concept, General Characteristics of Negative-Feedback Amplifiers, Effect of Negative Feedback upon Output and Input Resistances, Voltage-Series Feedback, Current-Series Feedback, Current-Shunt Feedback, Voltage-Shunt Feedback.

UNIT III

Oscillator Circuits: Barkhausen Criterion of oscillation, Oscillator operation, R-C phase shift oscillator, Wien bridge Oscillator, L-C Oscillators.

Operational Amplifiers: Introduction, Basic information of Op-Amp, Ideal Operational Amplifier, Block Diagram Representation of Typical Op-Amp, OP-Amps Characteristics: Introduction, DC and AC characteristics, 741 op-amp & its features.

Prof. K.Venkata Ramanaiah,
Dean Faculty of Engineering
V.S.R. Engineering College of Yi
Korrapadu Road, PRODDATUR-5163..

UNIT IV

OP-AMPS Applications: Introduction, Basic Op-Amp Applications, Instrumentation Amplifier, AC Amplifier, V to I and I to V Converter, Sample and Hold Circuit, Log and Antilog Amplifier, Differentiator, integrator.

Comparators and Waveform Generators: Introduction, Comparator, Square Wave Generator, Triangular Wave Generator, Sine Wave Generators.

UNIT V

Timers and Phase Locked Loop: Introduction to 555 timer, functional diagram, Monostable and Astable operations and applications, Schmitt Trigger, PLL block schematic, principles and description of individual blocks, 565 PLL, Applications of VCO (566).

Digital To Analog And Analog To Digital Converters: Introduction, basic DAC techniques, weighted resistor DAC, R-2R ladder DAC, inverted R-2R DAC, A-D Converters –parallel Comparator type ADC, counter type ADC, successive approximation ADC and dual slope ADC, DAC and ADC Specifications.

Textbooks:

1. Electronic Devices and Circuits- J. Millman, C.Halkias, Tata Mc-Graw Hill, 2nd Edition, 2010.
2. Linear Integrated Circuits – D. Roy Choudhury, New Age International (p) Ltd, 2nd Edition, 2003.

Reference Books:

1. Electronic Devices and Circuit Theory – Robert L.Boylestad and Lowis Nashelsky,Pearson Edition, 2021.
2. Electronic Devices and Circuits–G.K. Mithal, Khanna Publisher, 23rd Edition, 2017.
3. Electronic Devices and Circuits – David Bell, Oxford, 5thEdition, 2008.
4. Electronic Principles–Malvino, Albert Paul, and David J. Bates, McGraw-Hill/HigherEducation, 2007.
5. Operational Amplifiers and Linear Integrated Circuits– Gayakwad R.A, Prentice Hall India, 2002.
6. Operational Amplifiers and Linear Integrated Circuits –Sanjay Sharma, Kataria & Sons, 2nd Edition, 2010.
7. Design of Analog CMOS Integrated Circuits - Behzad Razavi

Web Resources:

1. https://nptel.ac.in/courses/122106025.
2. https://nptel.ac.in/courses/108102112.

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3.

UNIT I
DIODE CLIPPING AND CLAMPING CIRCUITS

DIODE CLIPPERS:

The Circuit which is used to clip off some portion of an applied input signal without distorting its remaining part is known as a clipper circuit or clipper.

A clipper is also called as limiter or slicer.

Half wave rectifier is the best example for a clipper which clips off negative half cycle from the applied input signal. By changing the orientation of the diode in the circuit of half wave rectifier positive or negative half cycle of the applied input signal can be clipped off.

Clipper circuits are mainly classified depending upon the orienta-tion of the diode in the circuit.

Clipper circuits are of two types 1. series clipper
2. parallel (or) shunt clipper.

Steps to analyse clipper circuits:

Various clipper circuits can be analysed using the following steps.

1. Replace the diodes by one of its equivalent model.
   (For forward bias replace diode with short circuit and for reverse bias replace diode with open circuit).
2. Identify ON and OFF states of the diodes and the clipping levels of input signal V_{in}.
3. Derive the equation for the transfer characteristics of the circuit
4. Plot the transfer characteristics and input output waveforms of the circuit.

Series clippers:

when the diode is connected in series with the load, such clipper circuit is called as a series clipper. A series clipper can be used to clip off the entire positive half cycle or negative half cycle of the input waveform. It can also be used to clip off the

- portion above a certain reference voltage or below a certain reference voltage by adding proper reference voltage source in the circuit.

A diode is an important element of any clipper circuit. We all know that the diode can act as a switch, it makes the circuit open when it is reverse biased while it makes the circuit closed when it is forward biased.

Series negative clipper circuit:

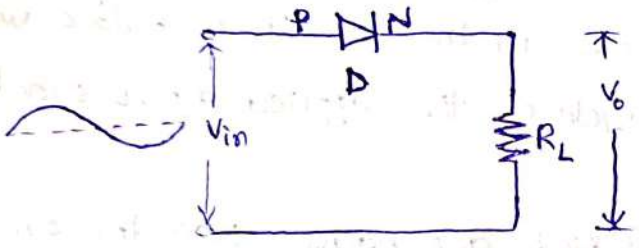


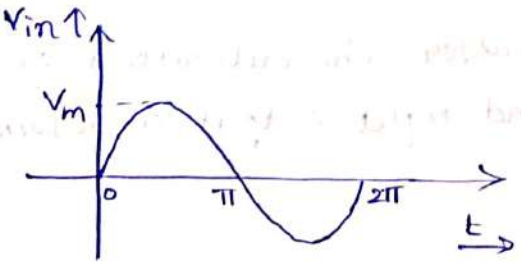
Fig: Negative clipper circuit

Operation:

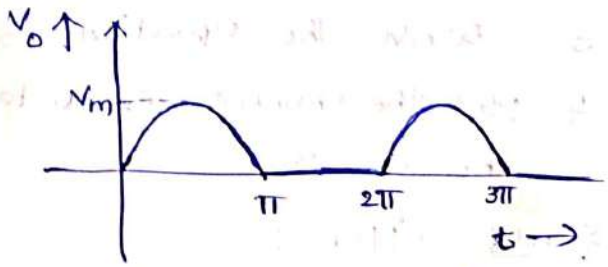
Consider the negative clipper circuit shown in figure:, in which the diode D is connected in series with the load.

During the positive half cycle in the applied input signal, the diode D is forward biased. Hence the positive half cycle can be observed in the out put V_o across R_L.

During negative half cycle the diode D is reverse biased and hence it is treated as a open circuit. Therefore no output voltage is observed across R_L during negative half cycle i.e $V_o = 0$. Hence the negative half cycle of the input voltage is clipped off from the output. The input and output waveforms of a series negative clipper circuit is as shown in below.



(a) Input waveform

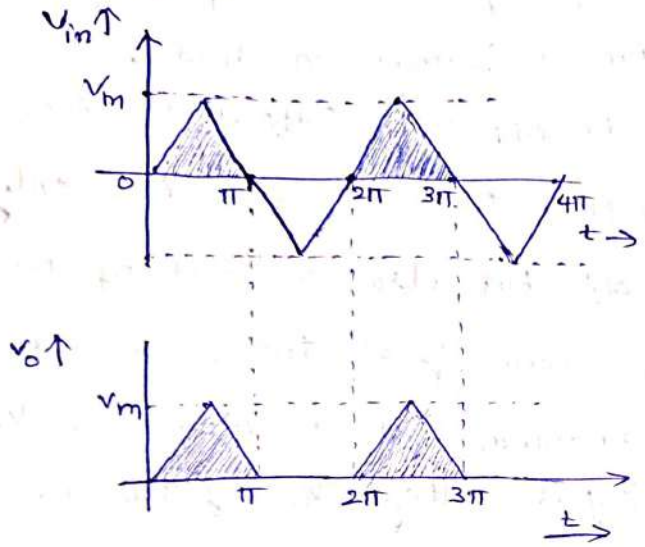


b) output waveform

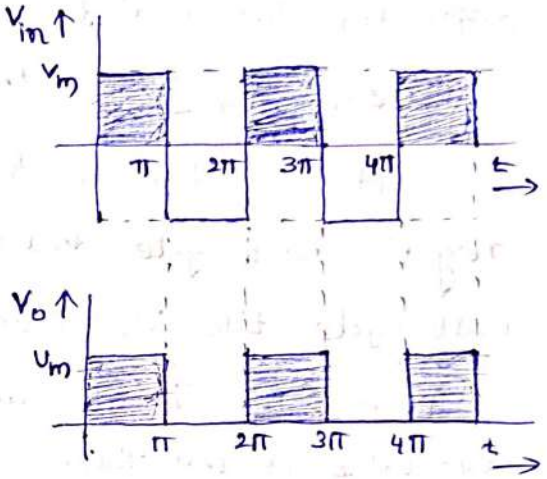
As the circuit clips off the negative half cycle of the input it is called series negative clipper.

Operation with non sinusoidal inputs :

The input to the series negative clipper circuit can be any type such as square, triangular etc. The circuit clips off the negative portion of the input waveform.



fig(a) Triangular input



fig(b) square wave input

fig: waveforms of series negative clipper.

Transfer characteristics

The working of a clipper circuit can be understood easily by using transfer characteristics. The graph between input voltage (V_{in}) and the output voltage (V_o) of the clipper circuit is called transfer characteristics of the clipper circuit.

To obtain the transfer characteristics for a clipper circuit the mathematical equation that shows the relation between V_i and V_o is to be obtained. The mathematical equation for series negative clipper is given as

$$V_o = V_{in} \quad \text{for} \quad V_{in} \geq 0$$

$$V_o = 0 \quad \text{for} \quad V_{in} < 0$$

The graph of transfer characteristics for the above mathematical equation is given here

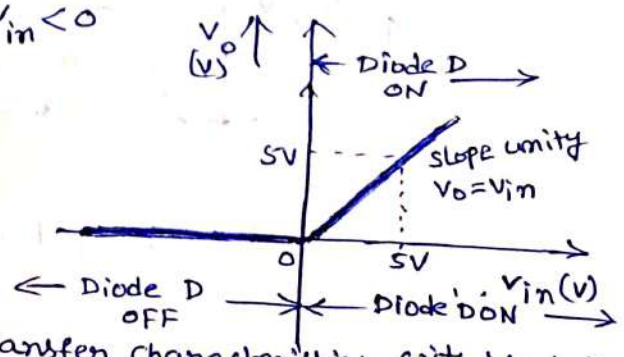


fig: Transfer characteristics with ideal diode

Transfer characteristics and input and output waveforms for series negative clipper with practical diode with a cut in voltage (V_γ)

In series negative clipper that has a diode with cut in voltage of V_γ the diode conducts when $V_{in} > V_\gamma$. where V_γ is generally 0.7V for Silicon diode and 0.3V for a Germanium diode.

when $V_{in} \leq V_\gamma$, the diode D is OFF and output $V_o = 0V$.

Hence, due to the cut in voltage of the diode not only negative half cycle does not clipped off but also a part of positive half cycle till V_{in} becomes greater than V_γ of the diode also gets clipped off. This causes the maximum output voltage of V_o available is less than maximum input voltage V_m by the amount equal to V_γ.

The mathematical equation for transfer characteristics is now becomes

$V_o = V_{in} - V_\gamma$ for $V_{in} > V_\gamma$

$V_o = 0$ for $V_{in} \leq V_\gamma$

The transfer characteristics and input and output waveforms are shown in figures below.

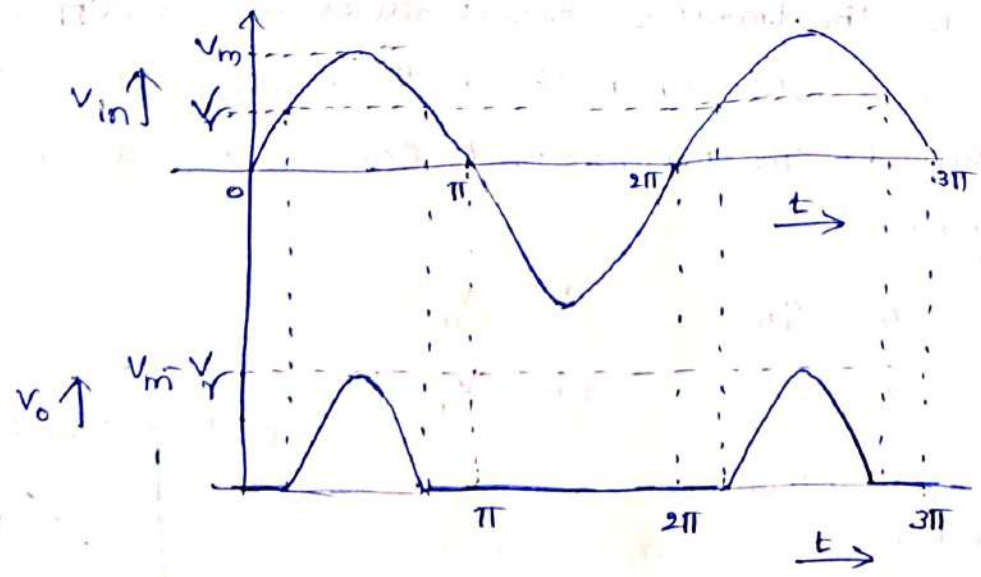
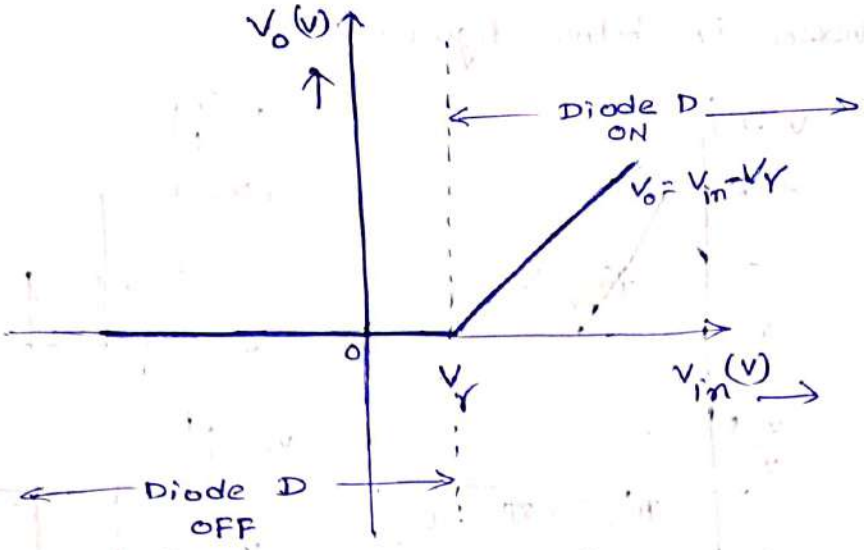


fig (a) input and output waveforms



fig(b): Transfer characteristics of series negative clipper with practical diode with a cut in voltage of V_γ

NOTE: The region in the transfer characteristics for which diode(D) is ON is called transmitting region while the region for which the diode(D) is OFF is called clipping (or) limiting region.

Series positive Clipper Circuit:

A clipper circuit in which the diode is in series with the load R_L, that clips off the positive half cycle of the applied input signal is called as a series positive clipper.

In series positive clipper circuit, the diode direction is opposite to that of the direction of diode in negative series clipper.

operation; For positive half cycle of the input i.e for $V_{in} > 0$, the diode is reverse biased. Hence the diode acts as open circuit and $V_o = 0V$. For negative half cycle of the input, when $V_{in} < 0$, the diode conducts. Assuming the diode as an ideal diode, the entire negative half cycle of the input is available at the output. The circuit diagram for a series positive clipper is shown in below figure.

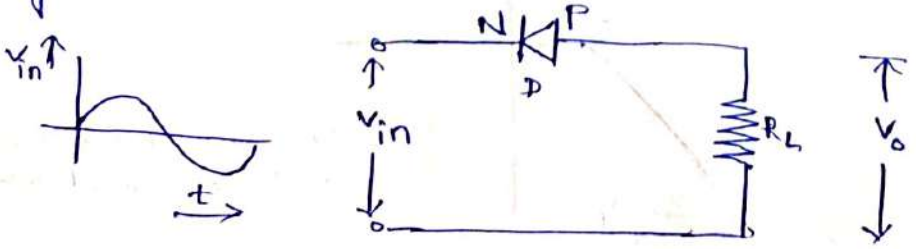
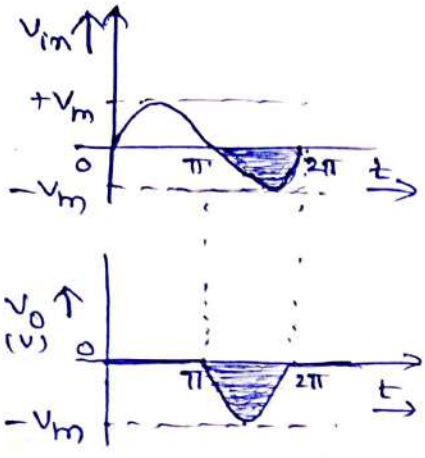
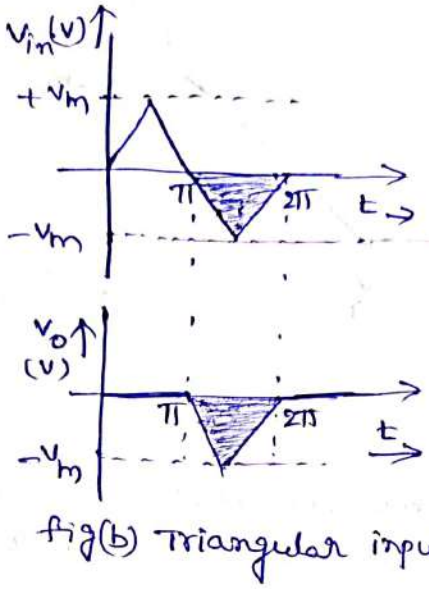


fig: series positive clipper

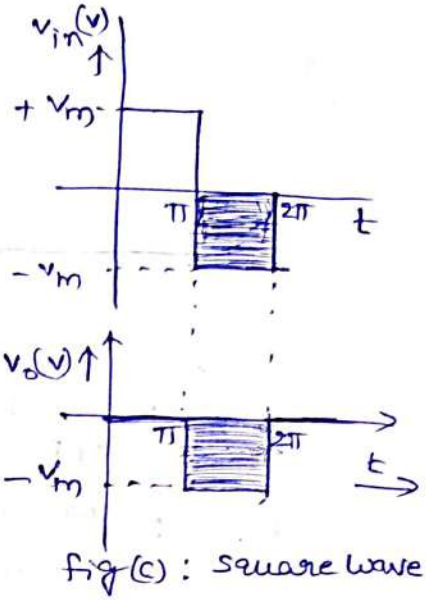
The output waveforms for a sinusoidal, non sinusoidal input waveforms are shown in below figures



fig(a) Sinusoidal i/p



fig(b) Triangular input



fig(c): square wave i/p

Transfer characteristics:

The equation for series positive clipper with an ideal diode is

$V_o = 0$ for $V_{in} > 0V$

$V_o = V_{in}$ for $V_{in} \leq 0V$

The transfer characteristics of a series positive clipper with an ideal diode is as shown in below.

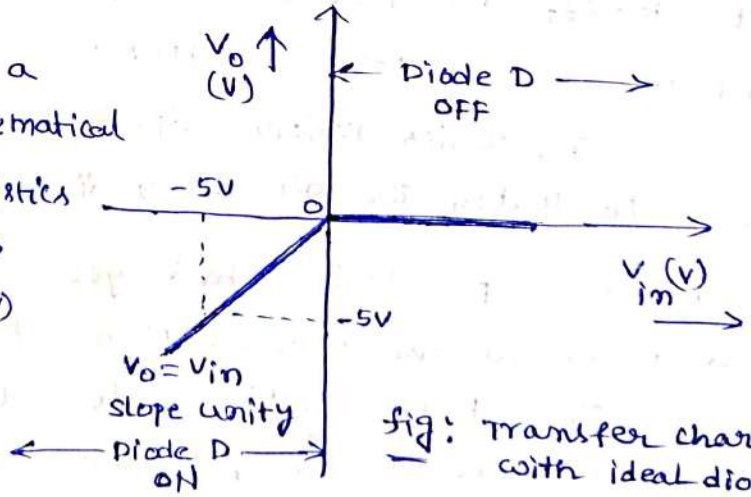


fig: Transfer characteristics with ideal diode

For a non ideal diode with a cut in voltage of $+V_\gamma$ the mathematical equation for transfer characteristics is $V_o = 0$ for $V_{in} > -V_\gamma$ Volts

$V_o = V_{in} + V_\gamma$ for $V_{in} \leq -V_\gamma$ (V)

The transfer characteristics for non ideal diode is as shown in below figure.

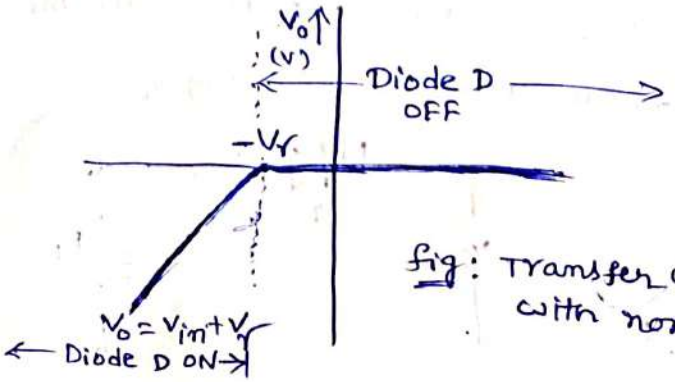


fig: Transfer characteristics with non ideal diode.

The input and output waveforms for a series positive clipper with non ideal diode with a cut in voltage V_γ is shown below.

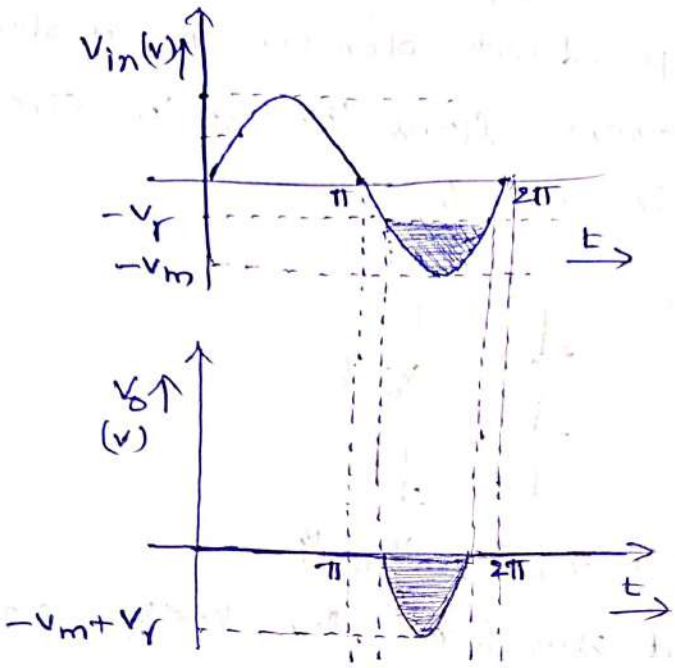


fig: Input and output waveforms for series positive clipper with non ideal diode.

Clipping above reference voltage (V_R)

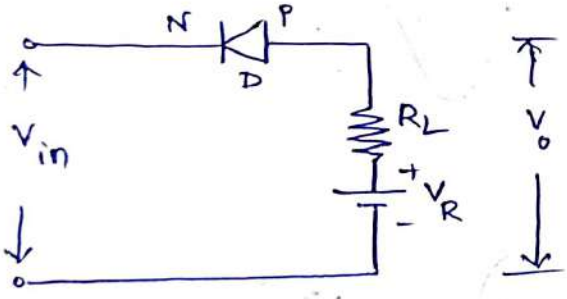


fig: clipping above V_R.

The output of a clipper circuit can be adjusted as per the requirement by adding an additional voltage source in series with the load resistance as shown in figure.

Let the diode D as an ideal diode. Hence $V_\gamma = 0$.

Operation: when V_{in} is less than V_R, the diode becomes forward biased and the circuit can be replaced with it's equivalent as shown below, in which the diode is replaced with short circuit. In this case the output voltage V_o is equal to input voltage V_{in}.

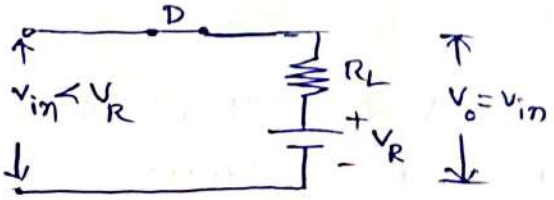


fig: output $V_o = V_{in}$ when $V_{in} < V_R$

When V_{in} is greater than V_R, the diode gets reverse biased and the circuit can be replaced with it's equivalent in which the diode 'D' is replaced with open circuit as shown in below.

In this case no current flows through the circuit and hence the output voltage V_o is equal to V_R.

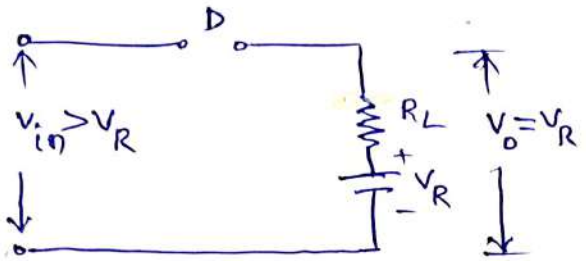


fig: output $V_o = V_R$ when $V_{in} > V_R$.

The input and output waveforms for $V_i < V_R$ and $V_i > V_R$ can be observed below.

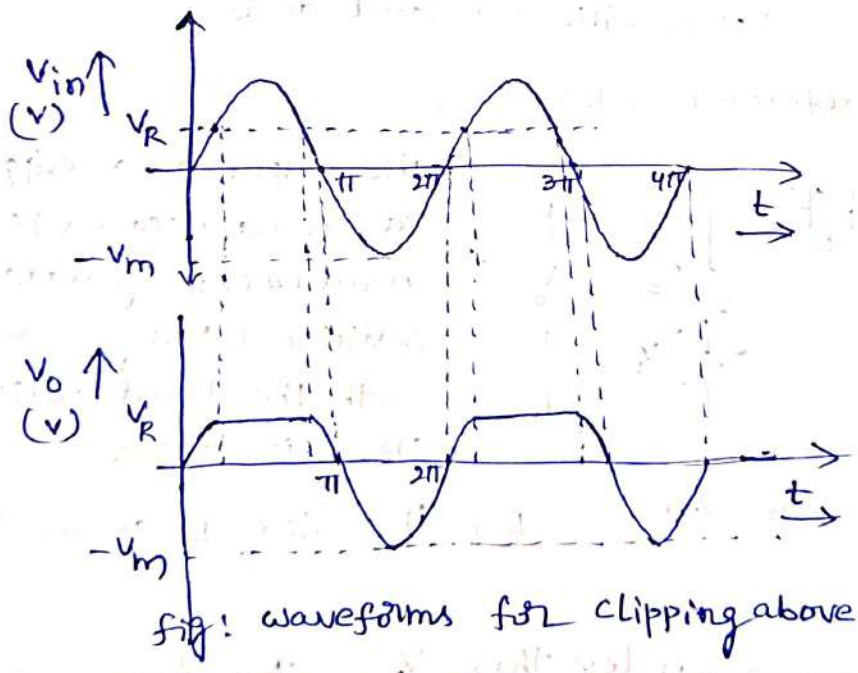


fig: waveforms for clipping above V_R

The equations for transfer characteristics of this clipper circuit for clipping above the reference voltage V_R is

$V_o = V_{in}$ for $V_{in} < V_R$

$V_o = V_R$ for $V_{in} > V_R$

The transfer characteristics of clipper circuit for clipping above reference voltage V_R is given below.

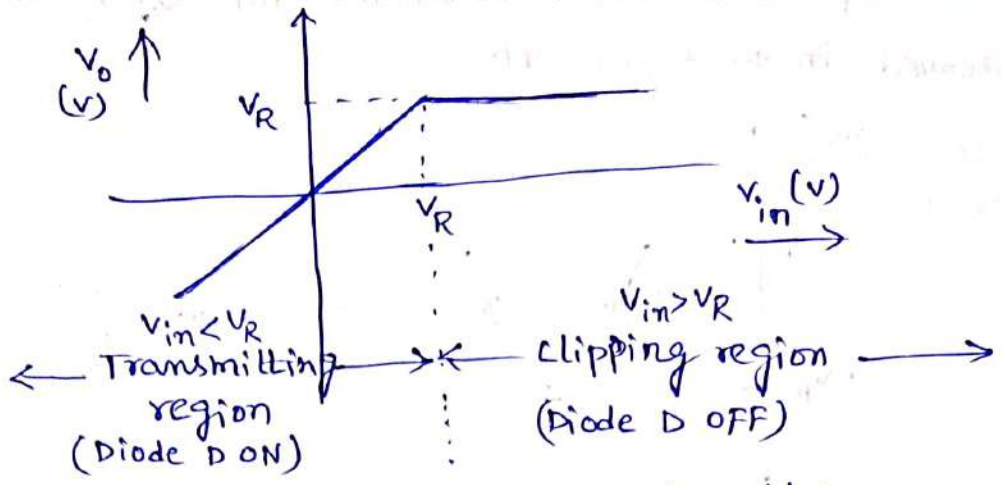
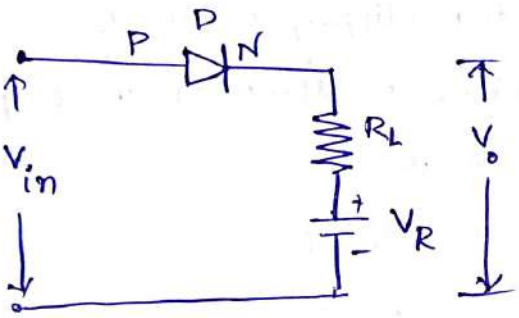


fig: Transfer characteristics

Clipping below reference voltage V_R:

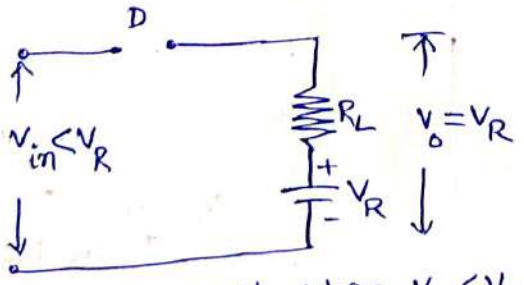
The circuit diagram that can be used for clipping below the reference voltage V_R is as shown below.



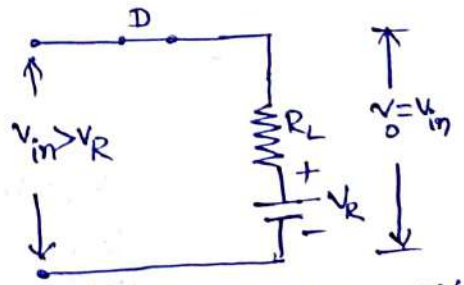
Let the Diode 'D' is an ideal diode and hence cut in voltage $V_\gamma = 0$.

fig: clipping below reference voltage V_R.

operation: when V_{in} is less than V_R, the diode 'D' is reverse biased and hence it is treated as open circuit. Therefore no current flows through the circuit. Thus the output voltage V_o is equal to V_R. The equivalent circuit for this case is as shown in below figure(a)



fig(a): output $V_o = V_R$ when $V_{in} < V_R$



fig(b): output $V_o = V_{in}$ when $V_{in} > V_R$

when V_{in} is greater than V_R, the diode 'D' is forward biased, hence it is treated as short circuit due to which the current flows through the circuit. Therefore the output $V_o = V_{in}$ when $V_{in} > V_R$. The equivalent circuit for this case is as shown in figure(b).

The input and output waveforms for $V_{in} < V_R$ and $V_{in} > V_R$ can be observed in the figure below.

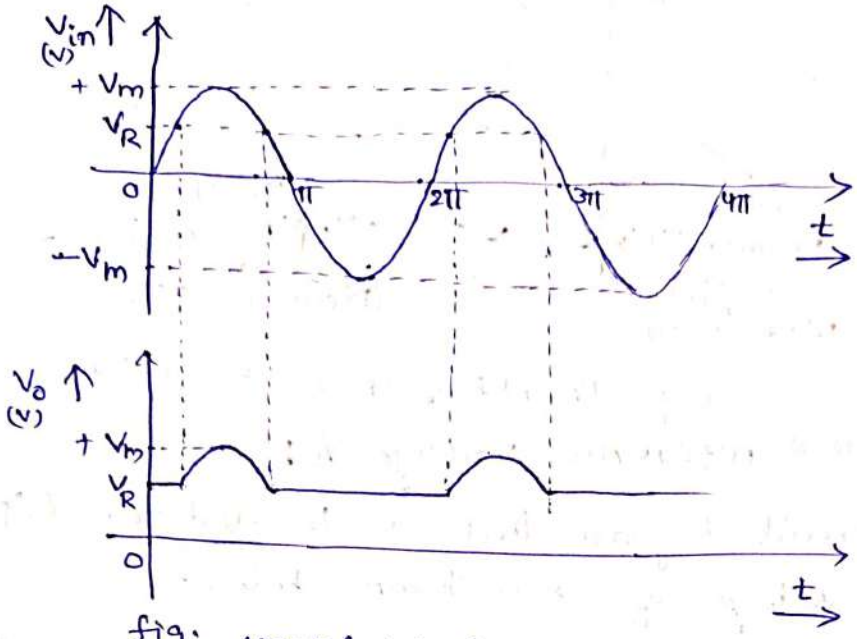


fig: waveforms for clipping below V_R.

The equations for transfer characteristics of the clipper circuit for clipping below a reference voltage V_R is

$$V_o = V_R \quad ; \text{ when } V_{in} < V_R$$

$$V_o = V_{in} \quad ; \text{ when } V_{in} > V_R$$

The transfer characteristics for this case is shown in below figure.

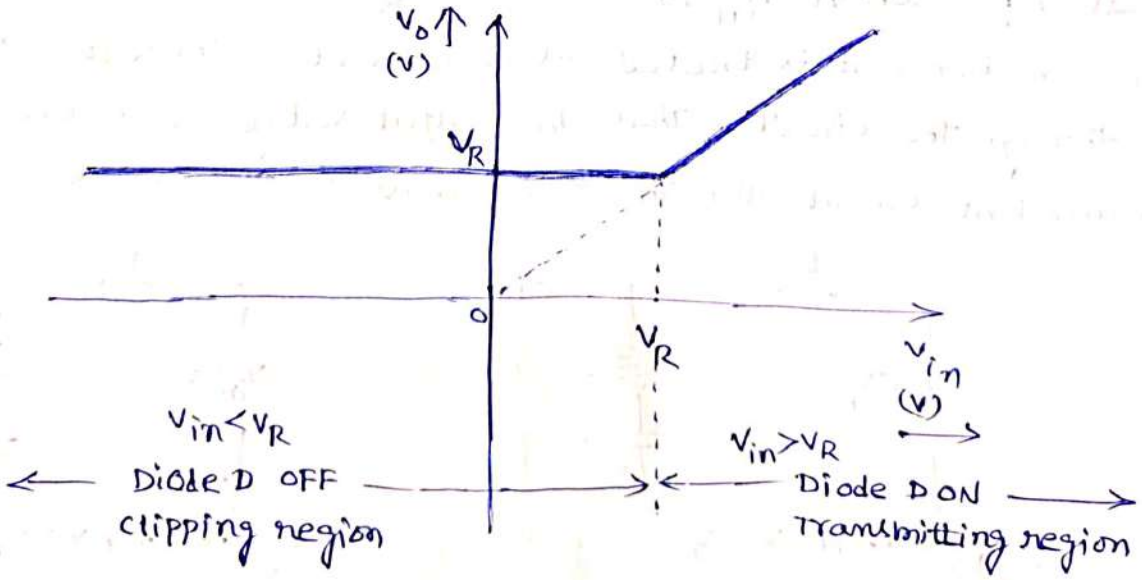


fig: Transfer characteristics

Parallel clippers (or) Shunt clippers:

The clipper circuit in which the diode is connected in a branch which is parallel to the load is called as a parallel clipper (or) Shunt-clipper. It can be used to clip off either positive or negative half-cycle of the applied input signal based on the requirement.

Basic parallel clipper with positive clipping:

The basic parallel clipper that clips off the positive half-cycle from the applied input signal is as shown in below figure. The resistance R_1 is current controlling resistance.

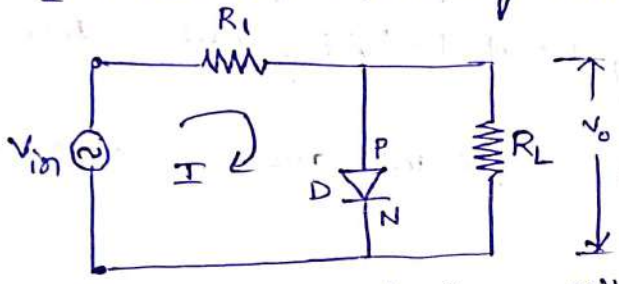


fig: Basic parallel clipper with positive clipping

Operation:

Assume the diode 'D' is an ideal diode. During positive half-cycle the diode 'D' becomes forward biased and it remains forward biased for the entire positive half cycle of the input signal. As the ideal diode acts as short circuit when forward biased, entire current I flows through the diode and voltage drop across short circuit diode is zero. As R_L is in parallel with diode and the current flows through R_L is zero, the voltage drop across R_L is zero. i.e., $V_o = 0$ V as shown in below figure.

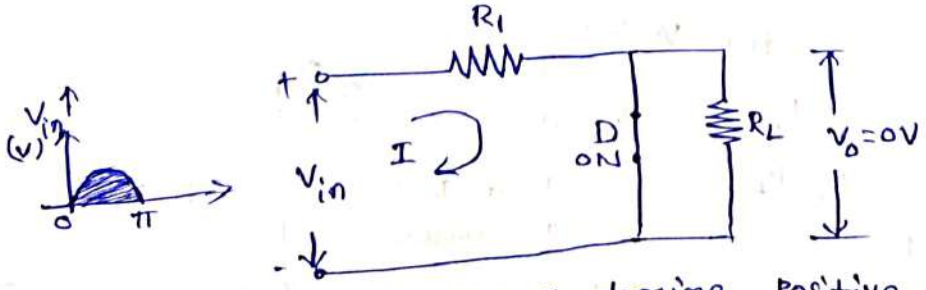


fig: Equivalent circuit during positive half cycle in the input

Therefore, the output voltage $V_o = 0$V during positive half cycle, hence positive half cycle gets clipped off in the output.

During negative half cycle of input, the diode is reverse biased and it acts as an open circuit. Hence the entire current flows through R_L as shown in below figure.

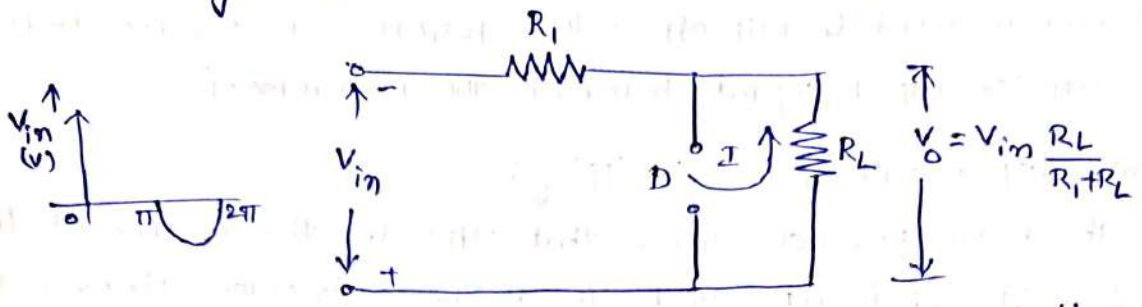


fig: Equivalent Circuit during negative half cycle in the input

Hence $V_o = \frac{V_{in} R_L}{R_1 + R_L}$ using potential divider rule. Thus $V_o \propto V_{in}$ during negative half cycle.

The input and output waveforms are shown in figure below.

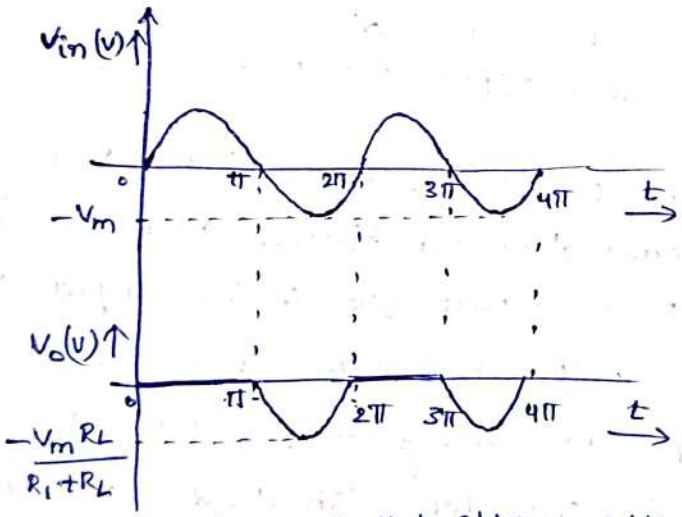


fig: waveforms for parallel clipper with positive clipping

Transfer characteristics:

The mathematical equations for transfer characteristics are

$V_o = 0$ for $V_{in} \geq 0$

$V_o = \frac{V_{in} R_L}{R_1+R_L}$ for $V_{in} < 0$

Assuming $\frac{R_L}{R_1+R_L} = K$

$V_o = K V_{in}$, therefore there exist a straight line relationship between V_{in} & V_o, making $R_1 << R_L$ $V_o = V_{in}$ can be obtained.

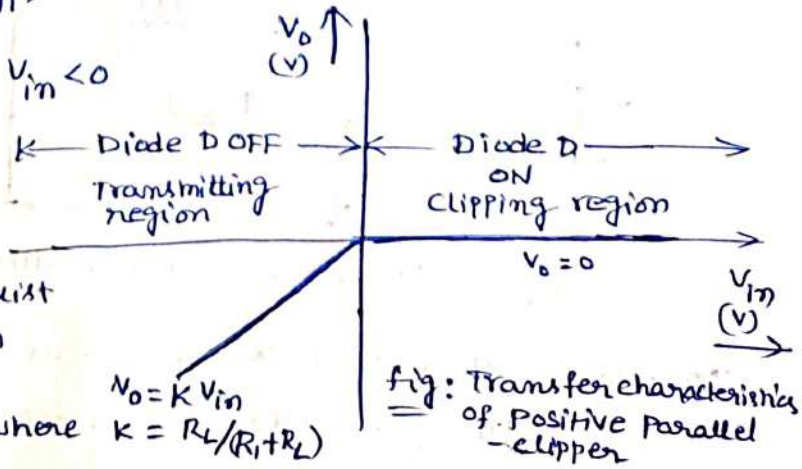
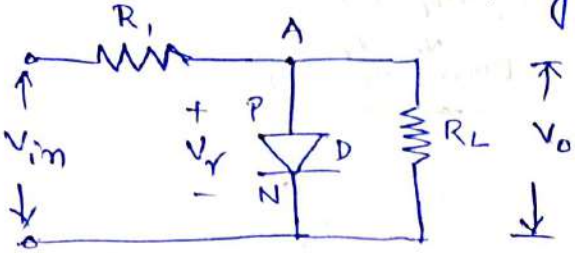


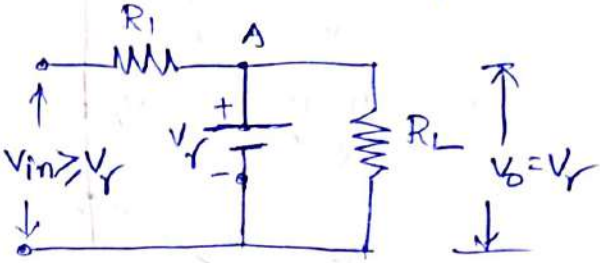
fig: Transfer characteristics of positive parallel clipper

Effect of Cut in Voltage in parallel clipper with positive clipping:

Let us consider the diode D is not an ideal diode and it has a cut in voltage of V_γ. The circuit diagram for Parallel clipper with positive clipping is shown in below figure(a).



fig(a): Parallel positive clipper

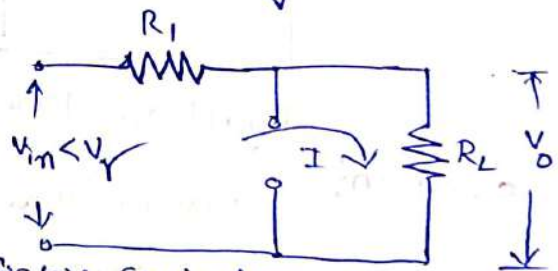


fig(b): Equivalent circuit when $V_{in} \geq V_\gamma$

When $V_{in} < V_\gamma$ the diode D is reverse biased and hence the diode is treated as open circuited due to which there will be a current flow through R_L. Hence the output voltage V_o using Potential divider rule is $V_o = V_{in} \frac{R_L}{R_1+R_L}$ for $V_{in} < V_\gamma$.

When the potential at node A becomes just equal to V_γ the diode starts conducting and it acts as a Dc voltage source of V_γ. Hence the output $V_o = V_\gamma$ for $V_{in} \geq V_\gamma$. The equivalent circuit when $V_{in} \geq V_\gamma$ is shown in the above figure (b).

The equivalent circuit for $V_{in} < V_\gamma$ is shown in figure (c).



fig(c): Equivalent circuit for $V_{in} < V_\gamma$

The input and output waveforms for this case are shown below.

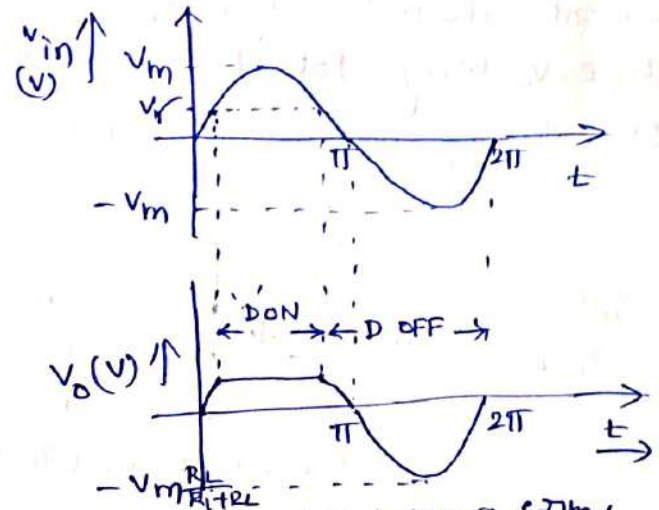


fig: Input & output wave forms

The equations for parallel positive clipper considering the effect of cut in voltage V_γ is

$V_o = V_{in} \frac{R_L}{R_1+R_L}$; $V_{in} < V_\gamma$

$V_o = V_\gamma$; $V_{in} \geq V_\gamma$

The transfer characteristics for parallel positive clipper with a non ideal diode is as shown in below figure.

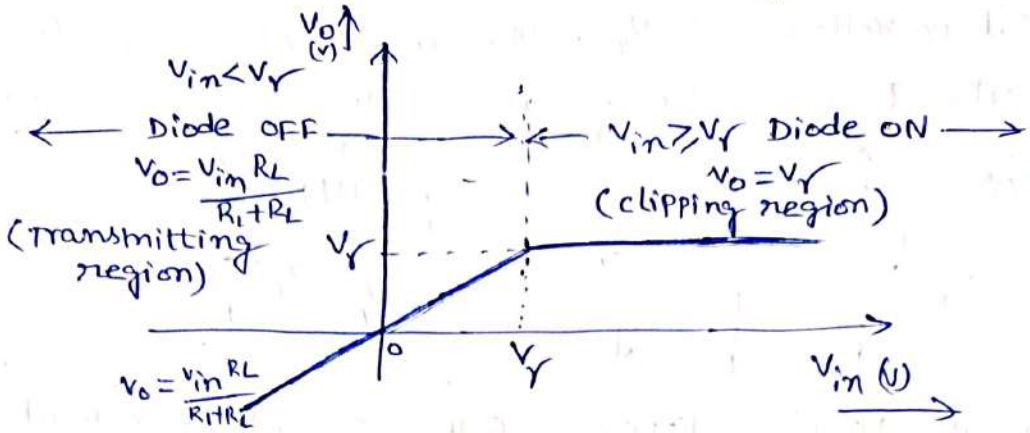
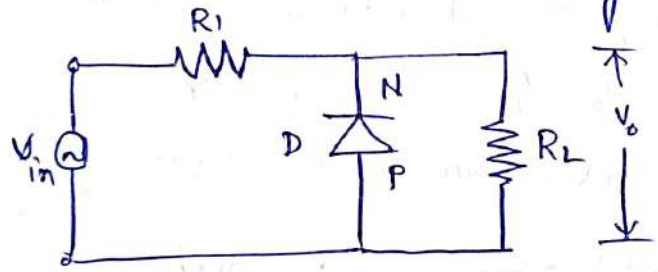


fig: Transfer characteristics

The portion for which $V_{in} < V_\gamma$ comes under transmitting region and $V_{in} \geq V_\gamma$ comes under slicing (or) clipping region.

Basic Parallel clipper with negative clipping:

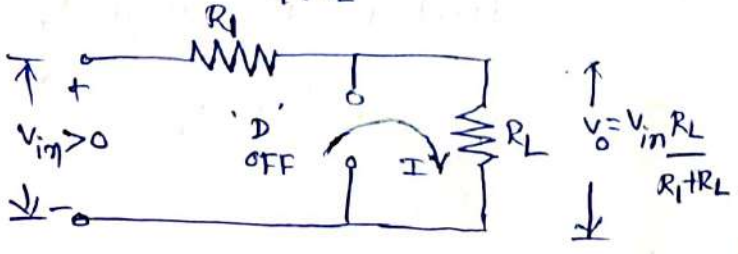
The basic parallel clipper that clips off the negative half cycle from the applied input signal is shown in below figure. The resistance R_1 is a current controlling resistance.



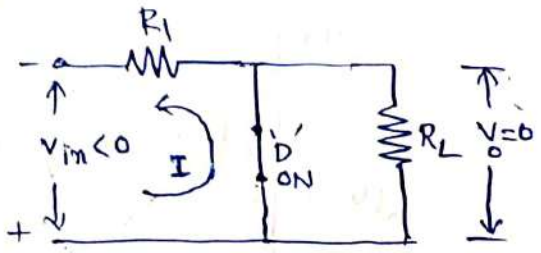
fig(a) Basic parallel clipper with negative clipping.

operation:

Assume that the diode D is an ideal diode. During positive half cycle the diode D is reverse biased and it acts as an open circuit. Hence the entire current flows through R_L as shown in figure(b) below. The output voltage V_o using potential divider rule is $V_o = V_{in} \frac{R_L}{R_1+R_L}$. Thus $V_o \propto V_{in}$ during positive half cycle.



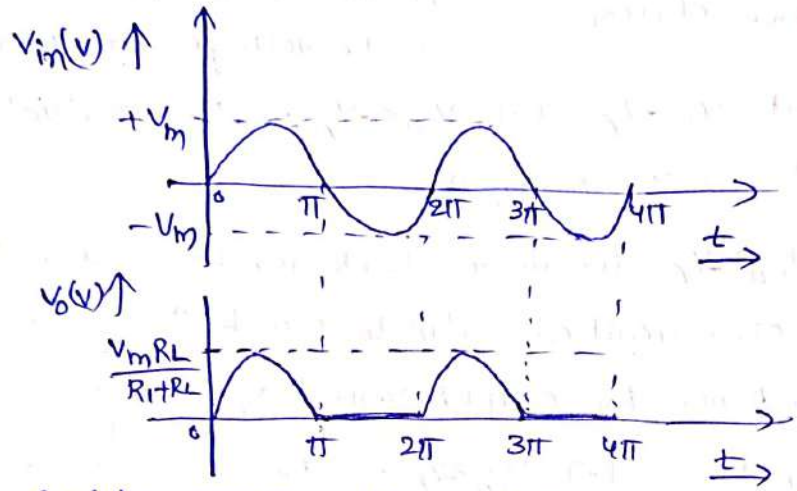
fig(b): Equivalent circuit for $V_{in} > 0$



fig(c): Equivalent circuit for $V_{in} < 0$

During negative half cycle the diode D is forward biased for the entire negative half cycle of the input V_{in}. As the ideal diode acts as short circuit when forward biased, the entire current I flows through the diode and voltage drop across short circuit diode is zero. As R_L is in parallel with the diode the voltage drop across R_L is zero. i.e $V_o = 0V$ as shown in the above fig(c).

The input and output waveforms are shown in below fig(d)



fig(d): Input and output waveforms for parallel negative clipper.

Transfer characteristics

The mathematical equations for transfer characteristics are

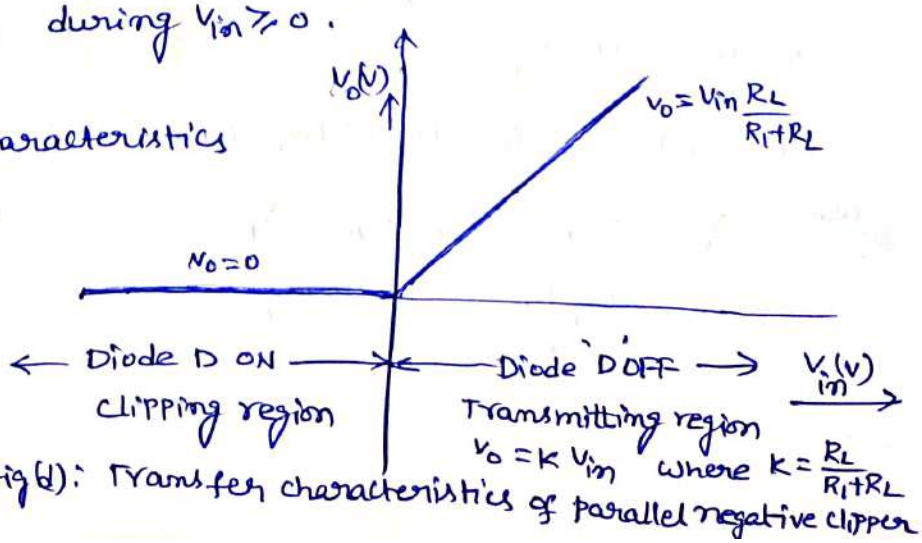
$$V_o = V_{in}\frac{R_L}{R_1+R_L} \quad ; \text{ for } V_{in} \geq 0$$

$$V_o = 0 \quad ; \text{ for } V_{in} < 0$$

Assuming $\frac{R_L}{R_1+R_L} = K$, $V_o = K V_{in}$ for $V_{in} \geq 0$. Therefore There exist a straight line relationship between V_{in} & V_o, making $R_1 << R_L$

$V_o = V_{in}$ can be obtained during $V_{in} \geq 0$.

fig(d) shows the transfer characteristics of the parallel negative clipper.



fig(d): Transfer characteristics of parallel negative clipper

Effect of Cut in Voltage in Parallel clipper with negative clipping:

Let us consider the diode D is not an ideal diode and it has a cut in voltage V_γ. The Circuit diagram for Parallel clipper with negative clipping is shown in below fig (a)

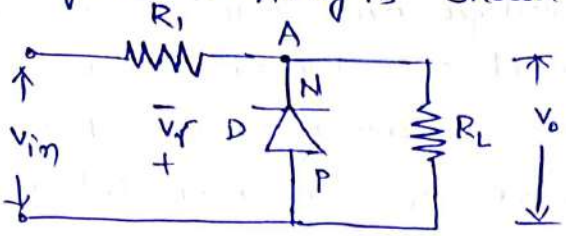


fig: Parallel negative clipper

when $V_{in} \leq -V_\gamma$ the diode D is forward biased and hence it allows the current to flow through it. In this case the diode acts as a DC voltage source of '$-V_\gamma$' volts. Hence the output $V_o = -V_\gamma$ for $V_{in} \leq -V_\gamma$. The equivalent circuit when $V_{in} \leq -V_\gamma$ is shown in fig (b).

when $V_{in} > -V_\gamma$ the diode D is reverse biased and hence it is treated as opencircuited, due to which there will be a current 'I' flows through R_L. Hence the output voltage V_o using potential divider rule is $V_o = V_{in} \frac{R_L}{R_1 + R_L}$ for $V_{in} \geq V_\gamma$. The equivalent circuit for $V_{in} > -V_\gamma$ is shown in fig (c)

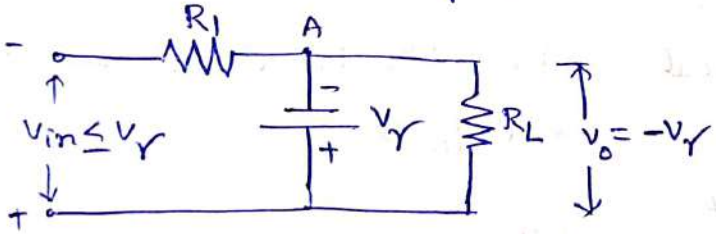


fig (b): Equivalent Circuit for $V_{in} \leq V_\gamma$

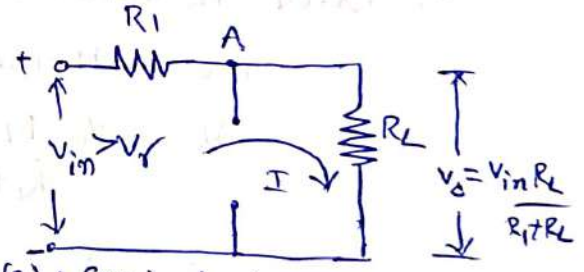
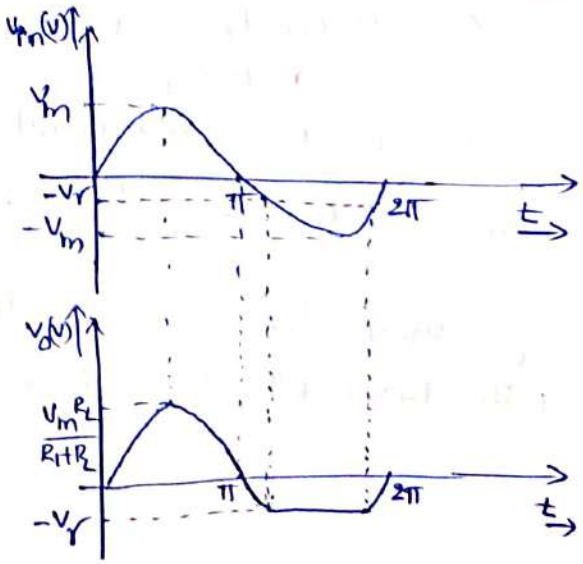


fig (c): Equivalent Circuit for $V_{in} > V_\gamma$

The input and output wave forms for parallel negative clipper with a non ideal diode with V_γ Cut in voltage is shown in fig (d).

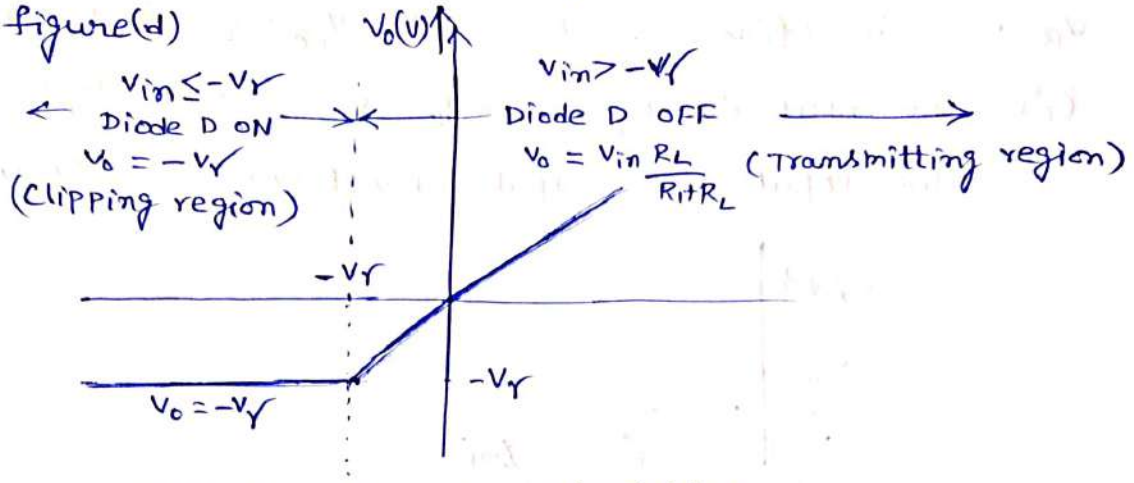


The equations for transfer characteristics are

$V_o = -V_\gamma \quad ; V_{in} \leq -V_\gamma$

$V_o = V_{in} \frac{R_L}{R_1 + R_L} \quad ; V_{in} > -V_\gamma$

The transfer characteristics for parallel negative clipper with non ideal diode of cut in voltage of V_γ volts is as shown in below figure(d)

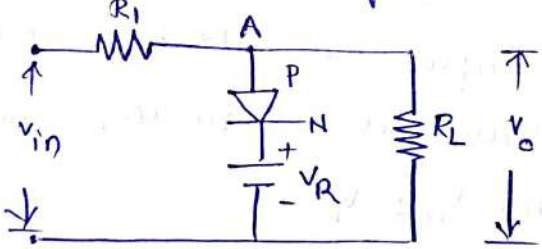


fig(d): Transfer characteristics.

Parallel clipper circuits with reference voltage (V_R)

Parallel positive clipper with positive reference voltage V_R

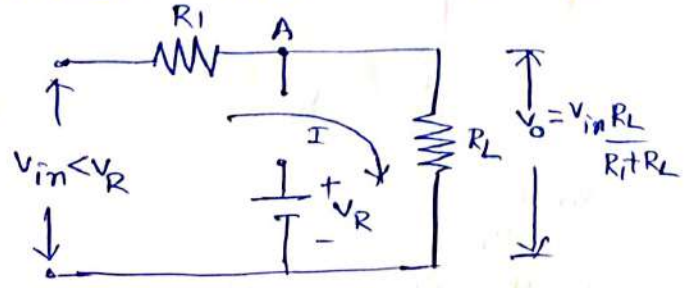
The circuit diagram for positive clipper with positive reference voltage V_R is shown in below figure. Assume Diode D is ideal diode.



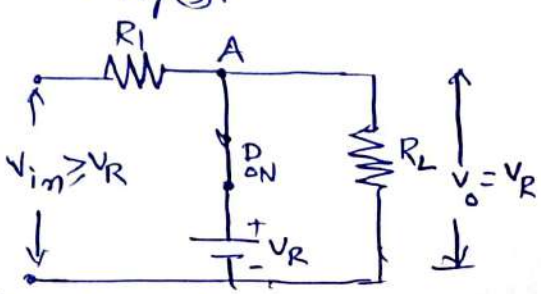
fig(a): Parallel positive clipper with positive reference voltage

operation: During $V_{in} < V_R$ the diode is reverse biased and acts as open circuit. Hence the current 'I' flows through R_L. The output voltage V_o, using voltage divider rule is $V_o = V_{in} \frac{R_L}{R_1+R_L}$ for $V_{in} < V_R$

The equivalent circuit for $V_{in} < V_R$ is shown in fig(b).



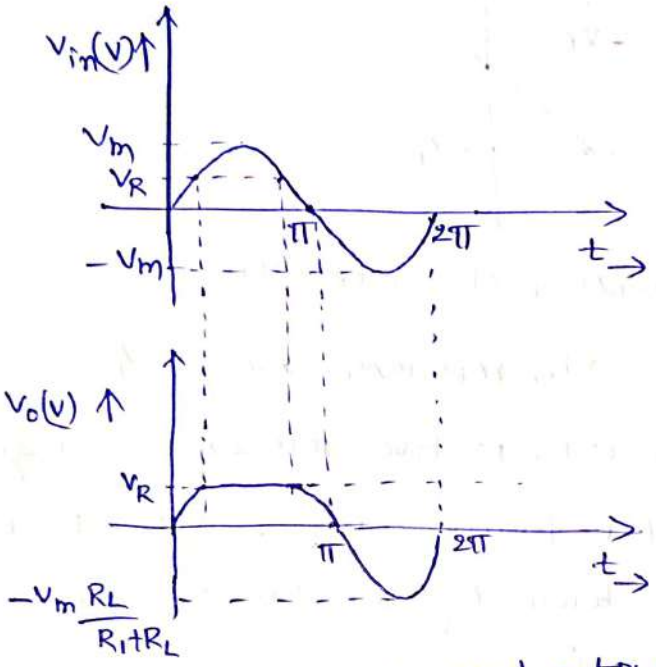
fig(b): Equivalent circuit for $V_{in} < V_R$



fig(c): Equivalent circuit for $V_{in} \geq V_R$

During $V_{in} \geq V_R$ the diode D is forward biased. The output voltage V_o for this case is same as the voltage at Node A which is V_R. Therefore $V_o = V_R$ for $V_{in} \geq V_R$. The equivalent circuit for the input during $V_{in} \geq V_R$ is shown in fig(c) above.

The input and output wave forms are shown in below fig(d)



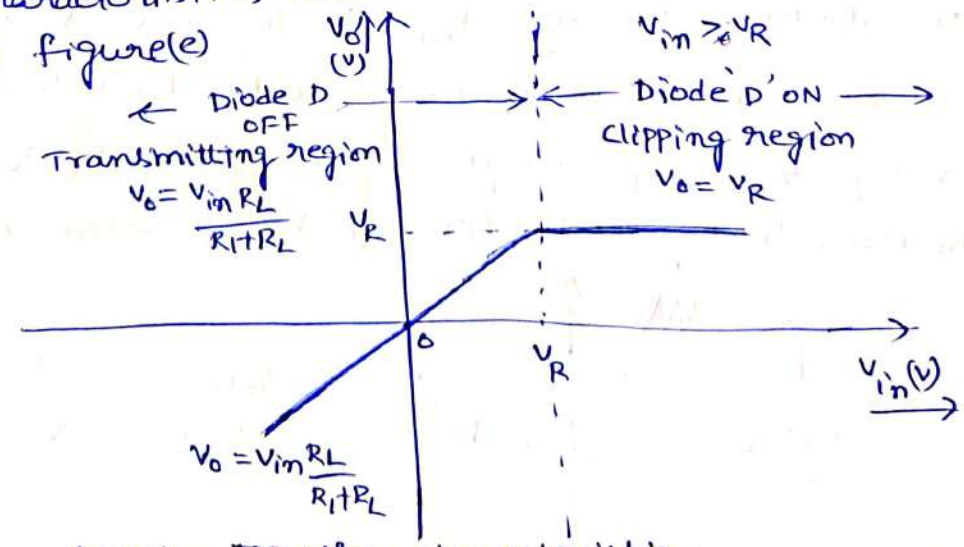
fig(d): Input and output wave forms

The mathematical equations for transfer characteristics are

$V_o = V_{in} \frac{R_L}{R_1+R_L}$; for $V_{in} \leq V_R$

$V_o = V_R$; for $V_{in} > V_R$

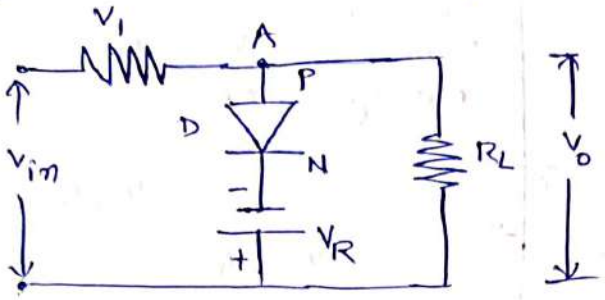
The transfer characteristics are shown in below figure(e)



fig(e): Transfer characteristics.

Parallel Positive clipper with negative reference voltage:

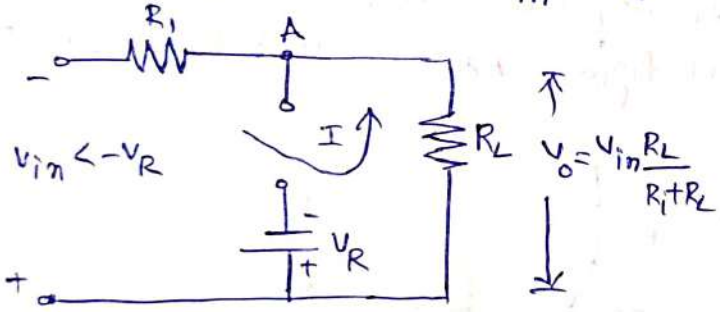
The circuit diagram for positive clipper with negative reference voltage V_R is shown in below fig(a). Assume diode D is ideal diode.



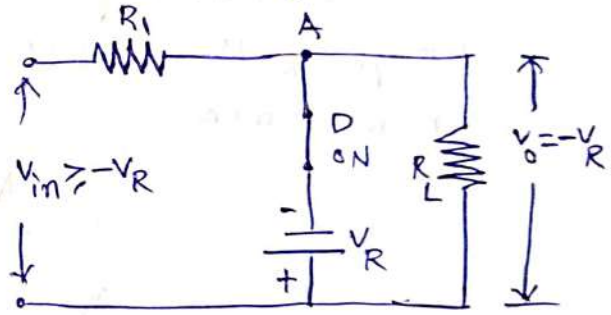
fig(a) Parallel Positive clipper with negative reference voltage

Operation: During $V_{in} < -V_R$ the diode D is reverse biased and it acts as an open circuit. Hence the current flows through the load R_L. The output voltage V_o using the voltage divider rule is $V_o = V_{in}\frac{R_L}{R_i+R_L}$ for $V_{in} < -V_R$

The equivalent circuit when $V_{in} < -V_R$ is shown in below fig(b).



fig(b): Equivalent circuit for $V_{in} < -V_R$



fig(c): Equivalent circuit for $V_{in} \geq -V_R$

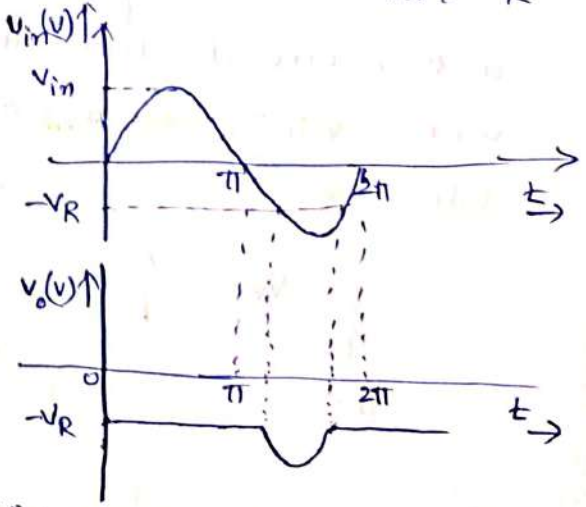
During $V_{in} \geq -V_R$ the diode D is forward biased. The output voltage V_o for this case is same as the voltage at node A which is equal to $-V_R$. Therefore $V_o = V_R$ for $V_{in} \geq -V_R$. The equivalent circuit for $V_{in} \geq -V_R$ is shown in fig(c).

The input and output waveforms are shown in figure(d).

The mathematical equations for transfer characteristics are

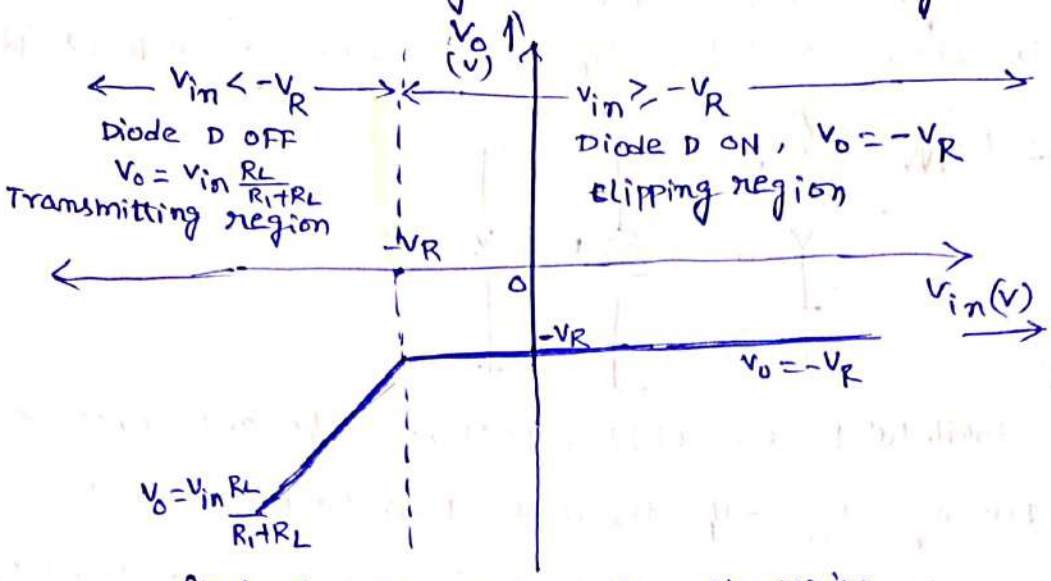
$$V_o = V_{in}\frac{R_L}{R_i+R_L} \quad ; \text{ for } V_{in} \leq -V_R$$

$$V_o = -V_R \quad ; \text{ for } V_{in} > -V_R$$



fig(d): Input and output waveforms

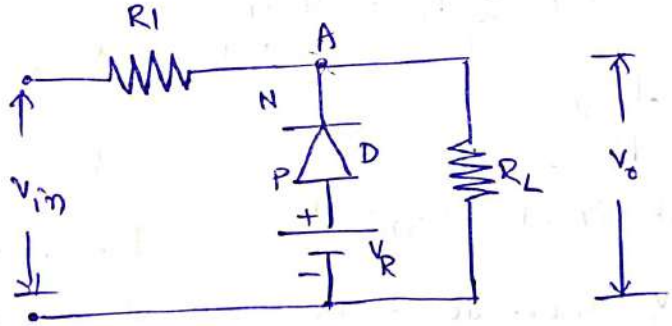
The transfer characteristics are shown in fig(e) for a Parallel Positive clipper with negative reference voltage.



fig(e): Transfer characteristics

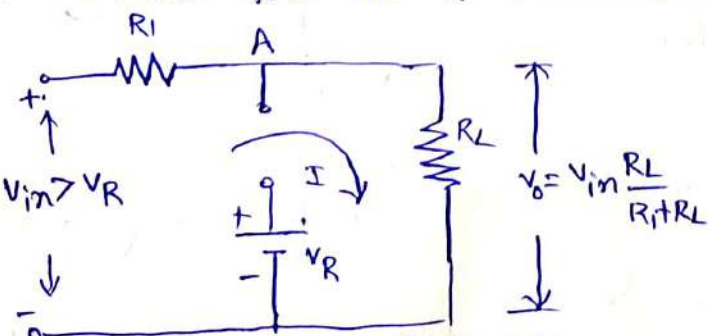
Parallel Negative clipper with Positive reference voltage:

The circuit diagram for negative clipper with Positive reference voltage V_R is shown in below fig(a). Assume that the diode D is an ideal diode.

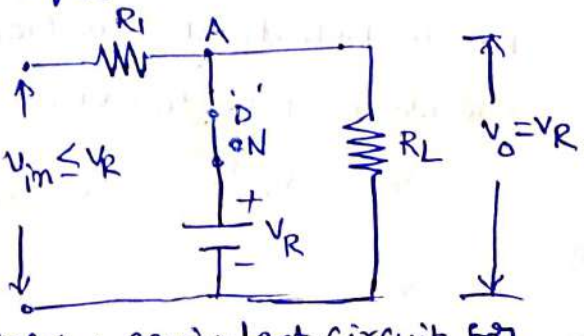


fig(a): Parallel Negative clipper with Positive reference voltage

operation: During $V_{in} > V_R$ the diode D is reverse biased and it acts as a open circuit. Hence the current flows through R_L. The output V_o using voltage divider rule is $V_o = V_{in} \frac{R_L}{R_1+R_L}$. for $V_{in} > V_R$. The equivalent circuit for $V_{in} > V_R$ is shown in fig(b).



fig(b) Equivalent circuit for $V_{in} > V_R$



fig(c): Equivalent circuit for $V_{in} < V_R$.

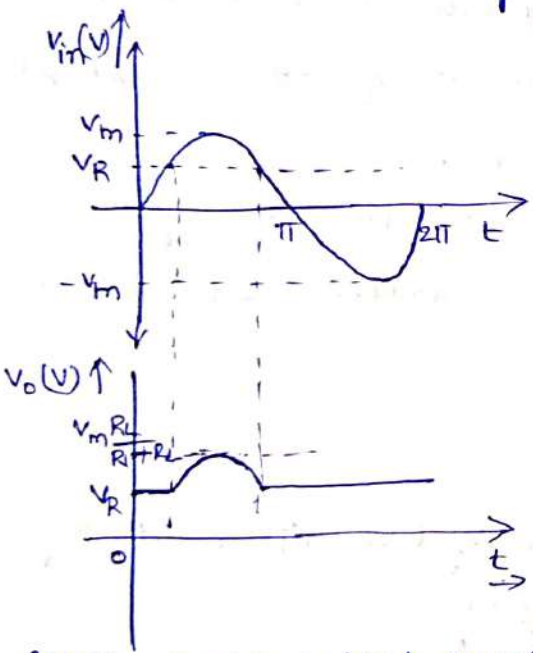
During $V_{in} \leq V_R$ the diode D is forward biased and it acts a short circuit. For this case the voltage across R_L is same as the voltage at node A, which is equal to V_R. i.e $V_o = V_R$ for $V_{in} \leq V_R$. The Equivalent circuit for $V_{in} \leq V_R$ is as shown in fig(c). The input and output waveforms are shown in below fig(d).

The mathematical equations for obtaining the transfer characteristics are

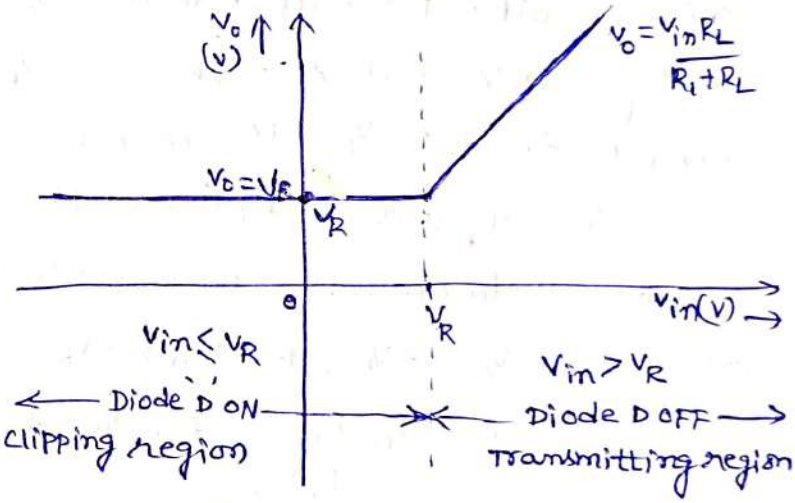
$$V_o = V_R \quad \text{for } V_{in} \leq V_R$$

$$V_o = V_{in} \frac{R_L}{R_1 + R_L} \quad \text{for } V_{in} > V_R.$$

The transfer characteristics for parallel negative clipper with positive reference voltage is shown in below fig(e).



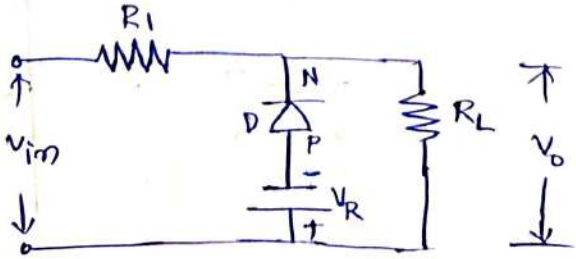
fig(d): Input-output waveforms



fig(e): Transfer characteristics

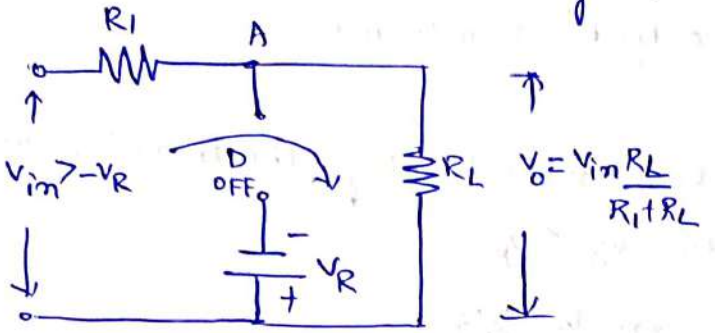
Parallel Negative clipper with Negative reference Voltage:

The circuit diagram for parallel negative clipper with negative reference voltage is shown in below fig(a). Assume that the diode is an ideal diode.

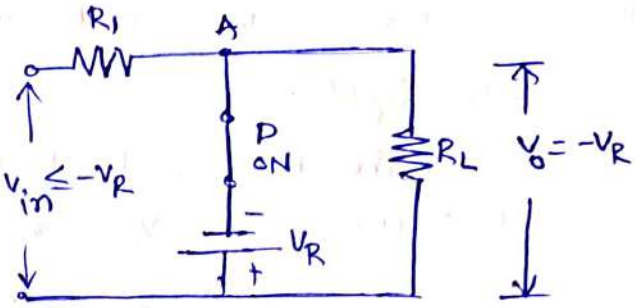


fig(a) Parallel negative clipper with negative reference voltage

operation: During $V_{in} > -V_R$ the diode D is reverse biased and it acts as an open circuit. Hence the current flows through R_L. The output V_o using voltage divider rule is $V_o = V_{in}\frac{R_L}{R_1+R_L}$ for $V_{in} > -V_R$. The equivalent circuit during $V_{in} > -V_R$ is shown in below fig(b).



fig(b): Equivalent circuit for $V_{in} > -V_R$



fig(c): Equivalent circuit for $V_{in} \geq -V_R$

During $V_{in} \leq -V_R$, the diode D is forward biased and it acts as short circuit. The output voltage V_o for this case is same as the voltage across node A. i.e $V_o = -V_R$ for $V_{in} \leq -V_R$. The equivalent circuit for $V_{in} \leq -V_R$ is shown in above fig(c).

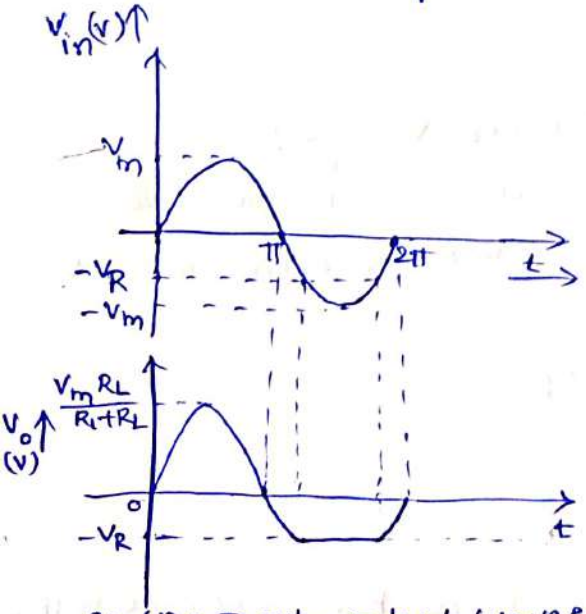
The input and output waveforms are shown in below fig(d).

The mathematical equations for obtaining transfer characteristics are

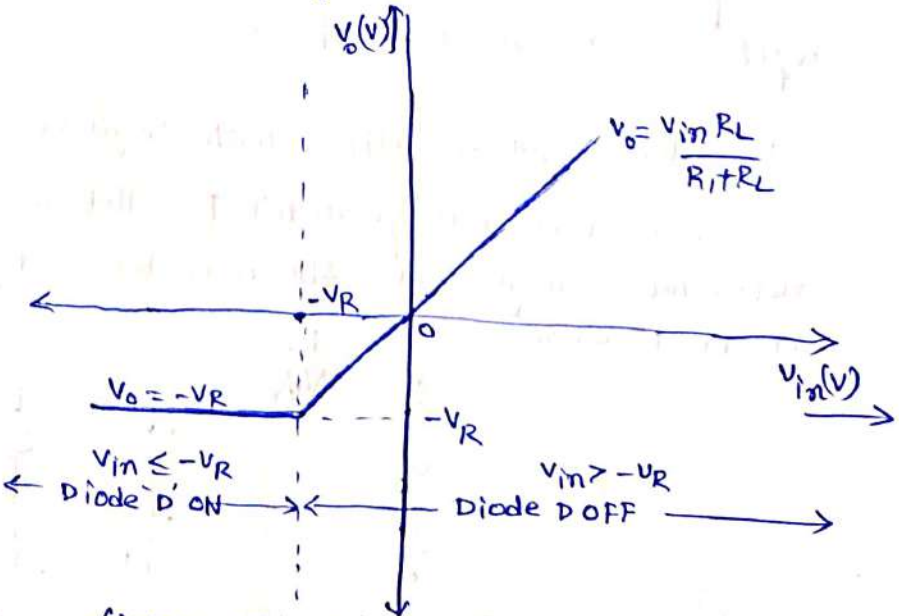
$$V_o = -V_R \text{ ; for } V_{in} \leq -V_R$$

$$V_o = V_{in}\frac{R_L}{R_1+R_L} \text{ ; for } V_{in} > -V_R$$

The transfer characteristics for parallel negative clipper with negative reference voltage is as shown in below fig(e)



fig(d): Input - output waveforms

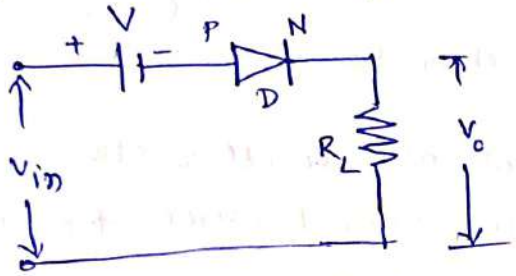


fig(e): Transfer characteristics

Additional DC supply in series with the diode

The output of the clipper circuits can be adjusted as per the requirement by adding an additional voltage source in series with the diode. Let us see some circuits of this category, their output wave-forms and transfer characteristics.

1) Determine the output waveform, equations for the transfer characteristics for the following circuit and derive its transfer characteristics.



Assume diode D is ideal.

Sol) Assuming the diode 'D' is an ideal diode, when it is forward biased applying KVL to the circuit replacing the diode D with short circuit we get $V_o = V_{in} - V$

when the diode is reverse biased replacing it with open circuit we get $V_o = 0$.

As long as $V_{in} < V$ the diode will not start conducting Hence the output $V_o = 0$ for $V_{in} < V$.

When V_{in} increases above V, the diode gets forward biased and we get the output $V_o = V_{in} - V$

for peak value of V_{in} i.e for $V_{in} = V_m$ the output V_o will give Peak value $V_o = V_m - V$.

During negative half cycle the diode will be in reverse bias. Hence the negative half cycle will be clipped off from the output.

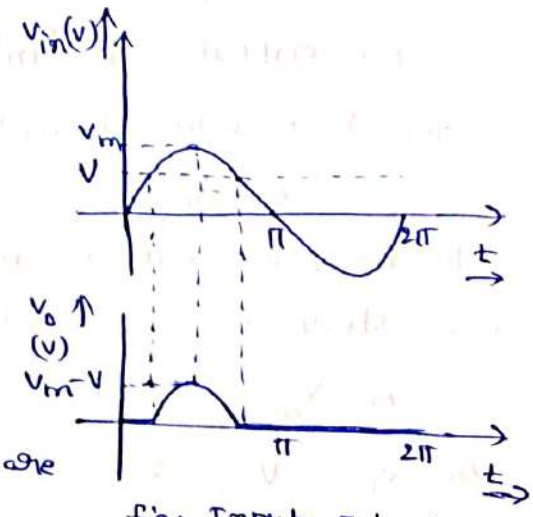


fig: Input-output waveforms

Transfer characteristics:

The equations for transfer characteristics are

$V_o = V_{in} - V$ for $V_{in} > V$

$V_o = 0$ for $V_{in} \leq V$

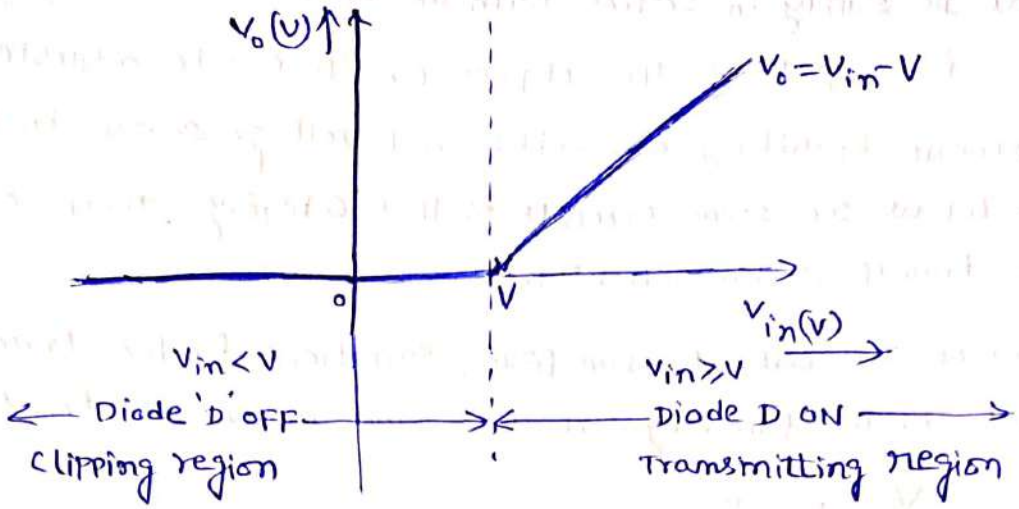
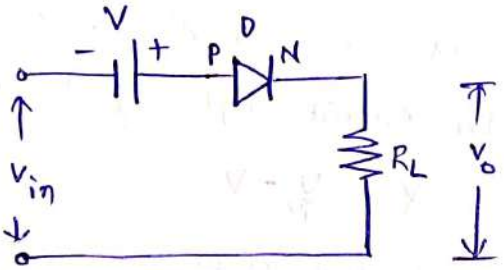


fig: Transfer characteristics

2) Determine the output wave forms and transfer characteristics by obtaining the equations for transfer characteristics for the circuit given below.



Assume diode D as an ideal.

Sol) Assuming diode D is an ideal diode and replacing it with short circuit when it is in forward bias, applying KVL to the circuit we get

$$V_o = V_{in} + (V)$$

$$\Rightarrow V_o = V_{in} + V$$

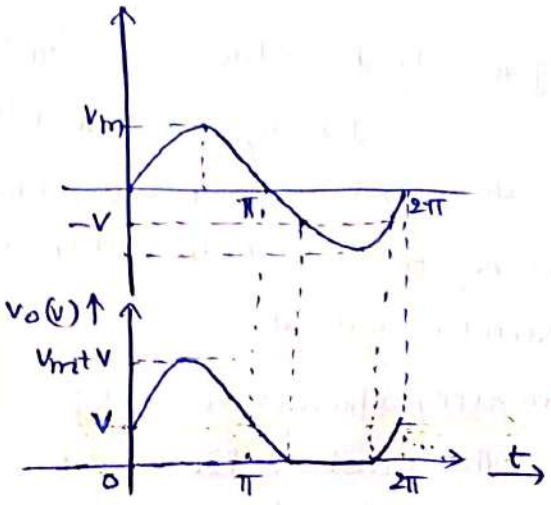
As long as $V_{in} < -V$ the diode D is reverse biased during that the output $V_o = 0$

when $V_{in} \geq -V$ the diode D is forward biased hence we get the output $V_o = V_{in} + V$

for peak value of V_{in} i.e $V_{in} = V_m$

$$V_o = V_m + V$$

The input and output waveforms are shown in figure below



At $V_{in} = 0$, $V_o = 0 + V = V$

At $V_{in} = -V$, $V_o = -V + V = 0$

Transfer characteristics:

To obtain the transfer characteristics the mathematical equations for output voltage V_o are

$V_o = V_{in} + V$ for $V_{in} \geq -V$

$V_o = 0$ for $V_{in} < -V$

The transfer characteristics are shown in below figure

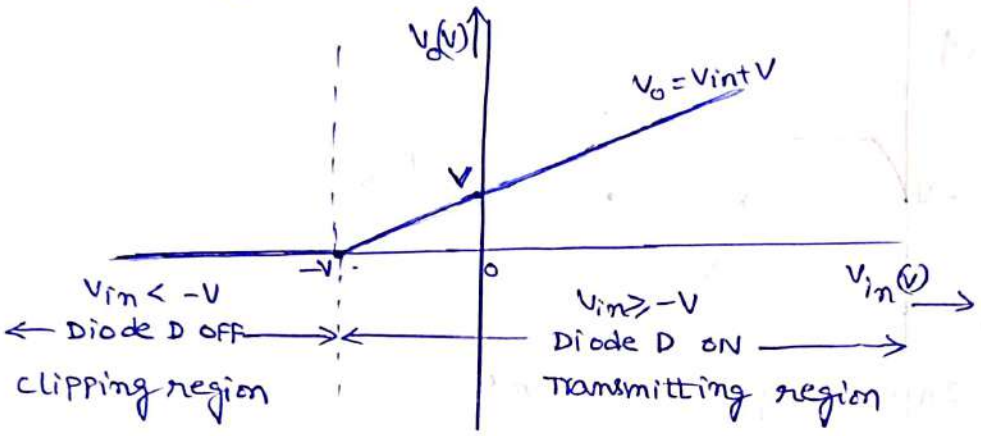
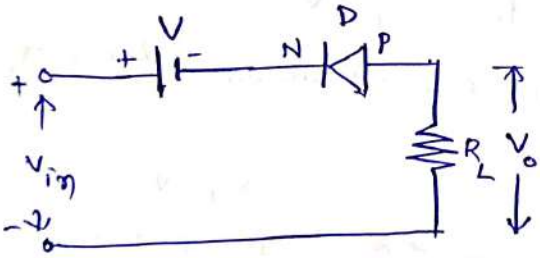


fig: Transfer characteristics.

3) Determine the output waveform and transfer characteristics by obtaining the equations for transfer characteristics for the circuit given below.



Assume the diode 'D' is an ideal diode.

Sol) Assuming the diode D as an ideal diode, when it is forward biased replacing it with short circuit we get the expression for V_o by applying KVL to the circuit as $V_o = V_{in} - V$

As long as $V_{in} \leq V$ the diode is forward biased and the output $V_o = V_{in} - V$

for $V_{in} > V$ the diode gets reverse biased and hence $V_o = 0$

At $V_{in} = 0$, $V_o = -V$

At $V_{in} = -V_m$, $V_o = -V_m - V$

The input and output waveforms are as shown in below figure

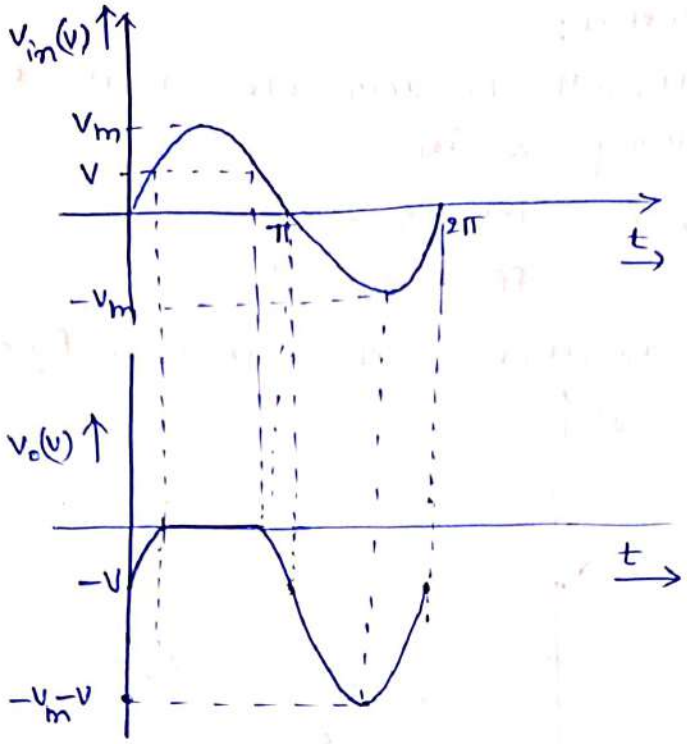


fig: Input-output waveforms

Transfer characteristics:

The equations for transfer characteristics are given as

$V_o = V_{in} - V$ for $V_{in} \leq V$

$V_o = 0$ for $V_{in} > V$

The transfer characteristics are as shown in below figure.

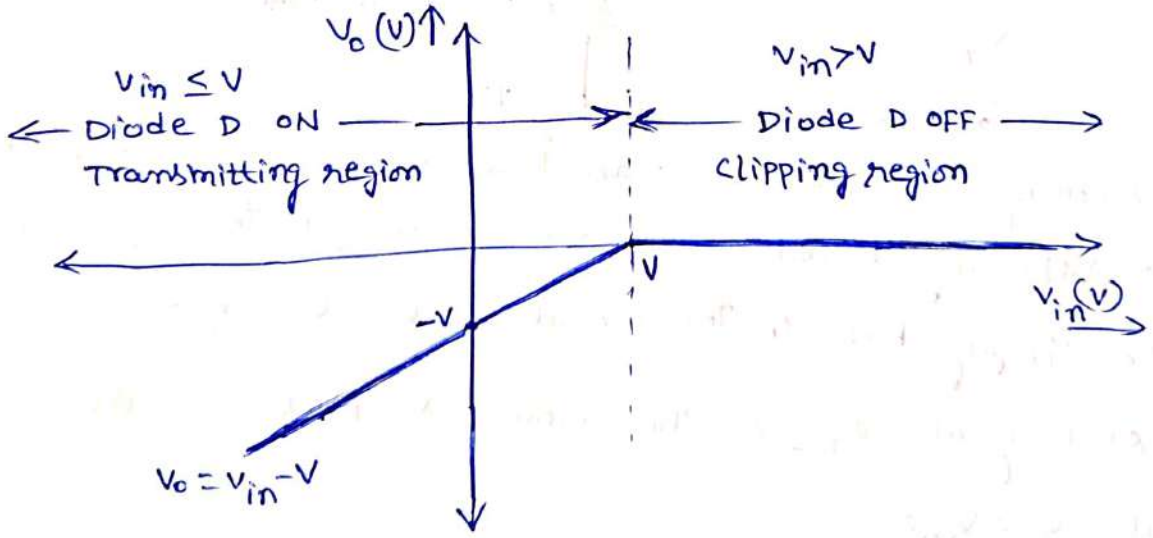
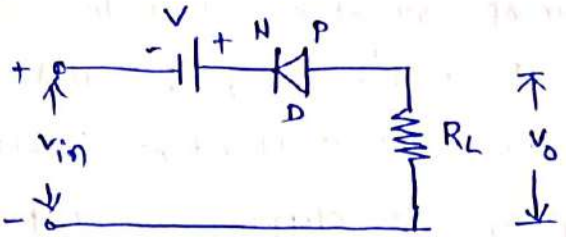


fig: Transfer characteristics.

(4) Determine the output waveform and transfer characteristics by obtaining the equations for transfer characteristics for the circuit given below. Assume the Diode 'D' is an ideal diode.



Sol) Assuming the diode D as an ideal diode, when it is forward biased, replacing it with short circuit we get the expression for V_o by applying KVL to the circuit as $V_o = V_{in} - (-V)$

$$V_o = V_{in} + V$$

As long as V_{in} is less than $-V$ the diode D is forward biased and the output $V_o = V_{in} + V$ for $V_{in} \leq -V$

when $V_{in} > -V$ the diode is reverse biased and hence $V_o = 0$ for $V_{in} > -V$.

for $V_{in} = -V$, $V_o = -V + V = 0$

for $V_{in} = -V_m$, $V_o = -V_m + V$

The input and output waveforms are shown in below figure.

The equations for transfer characteristics are $V_o = V_{in} + V$; $V_{in} \leq -V$

$V_o = 0$; $V_{in} > -V$

The transfer characteristics are shown in figure below.

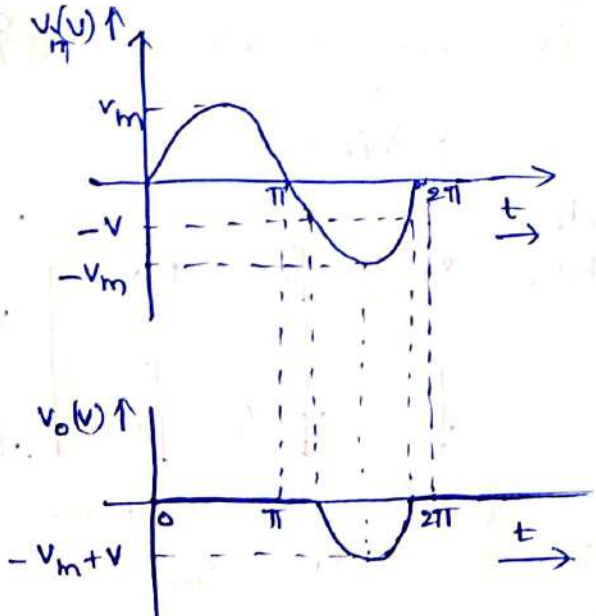


fig: Input - output wave forms

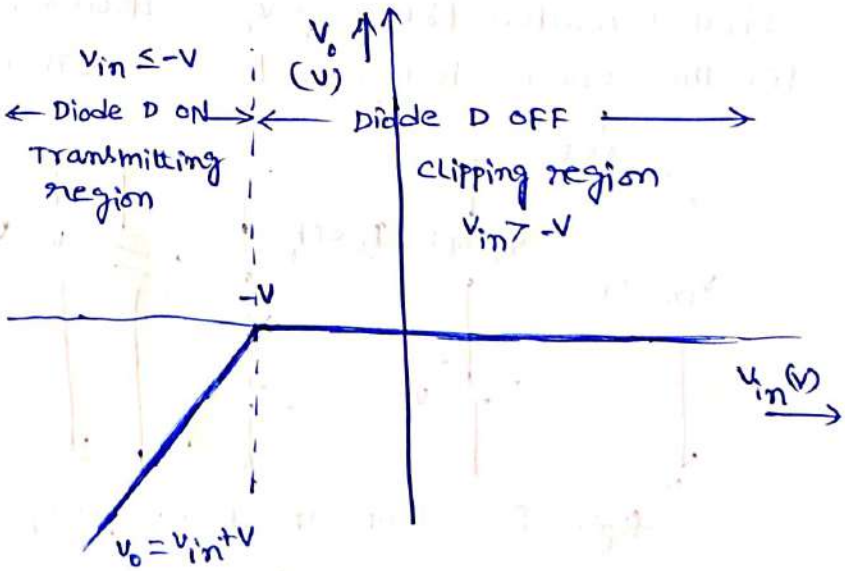
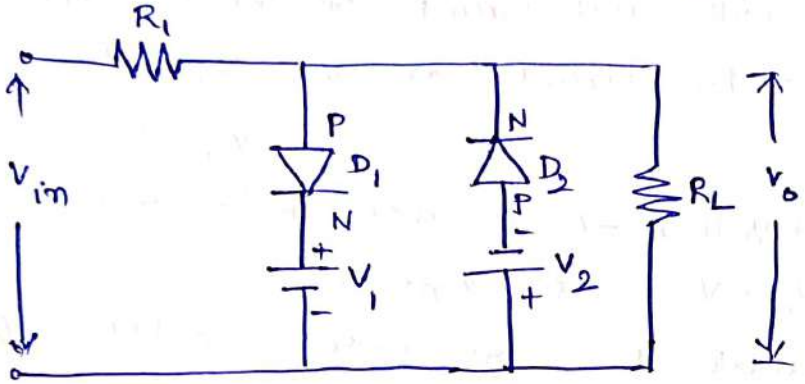


fig: Transfer characteristics.

Clipping at two independent levels (or) Two way parallel clipper:

A clipper circuit that can clip off some portion of positive half cycle and some portion of negative half cycle from the applied input signal is called as a two way parallel clipper.

It requires two diodes and two independent levels of reference voltages. The circuit diagram for clipping an input signal at two independent levels is shown in figure below.

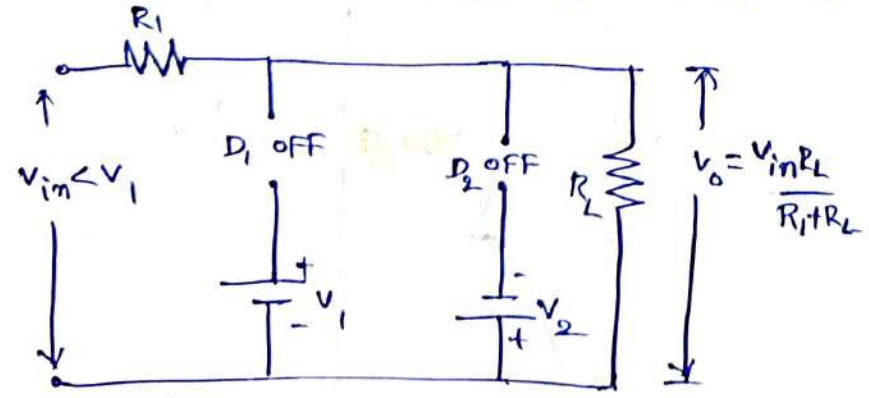


fig(a): Two way parallel clipper circuit.

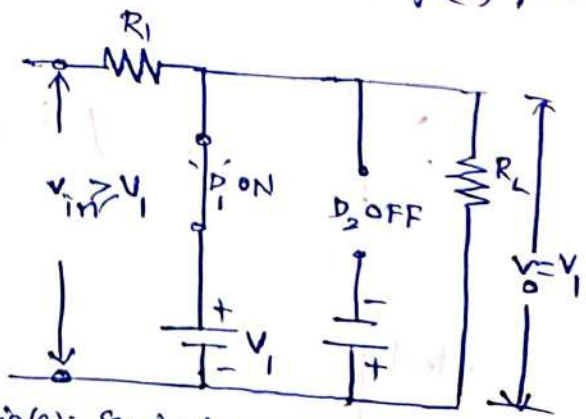
Assume that the diodes D_1 and D_2 are ideal diodes

operation:

During positive half cycle till $V_{in} < V_1$ the diode D_1 is reverse biased and hence D_1 is open circuited for $V_{in} < V_1$. For $V_{in} \geq V_1$ the diode D_1 is forward biased and conducts for $V_{in} \geq V_1$ hence it is short circuited for $V_{in} \geq V_1$. However D_2 is reverse biased (open circuited) for the entire positive half cycle. This is shown in below fig(b) & (c)



fig(b) Equivalent circuit for $V_{in} < V_1$



fig(c): Equivalent circuit for $V_{in} \geq V_1$

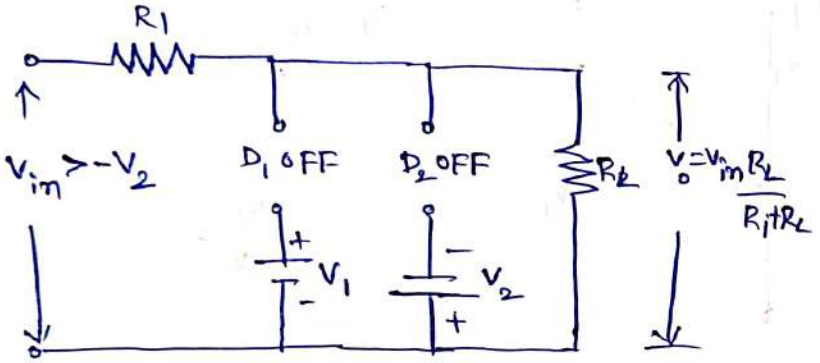
Thus for $V_{in} < V_1$, D_1 is OFF and D_2 is OFF and $V_o = V_{in} \frac{R_L}{R_1 + R_L}$

for $V_{in} \geq V_1$, D_1 is ON and D_2 is OFF and $V_o = V_1$

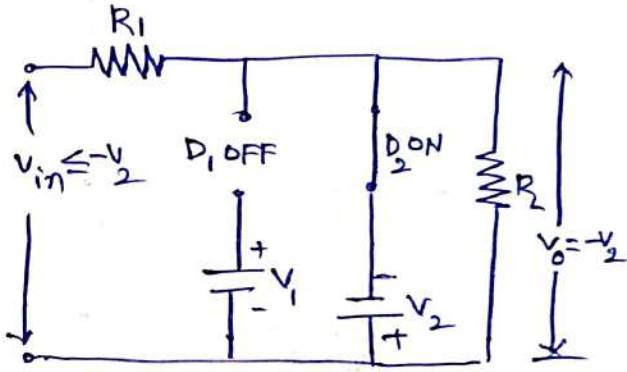
During negative half cycle as long as $V_{in} > -V_2$ the diode D_2 remains reverse biased, hence it is open circuit for $V_{in} > -V_2$. For $V_{in} \leq -V_2$ the diode D_2 is forward biased hence it conducts. during which D_2 is short circuited. However diode D_1 is reverse biased (open circuited) for the entire negative half cycle. Thus

- for $V_{in} > -V_2$, D_1 is OFF and D_2 is OFF and $V_o = V_{in} \frac{R_L}{R_1 + R_L}$
  for $V_{in} \leq -V_2$ D_1 is OFF and D_2 is ON. and $V_o = -V_2$.

This is shown in below fig(d) and fig(e)

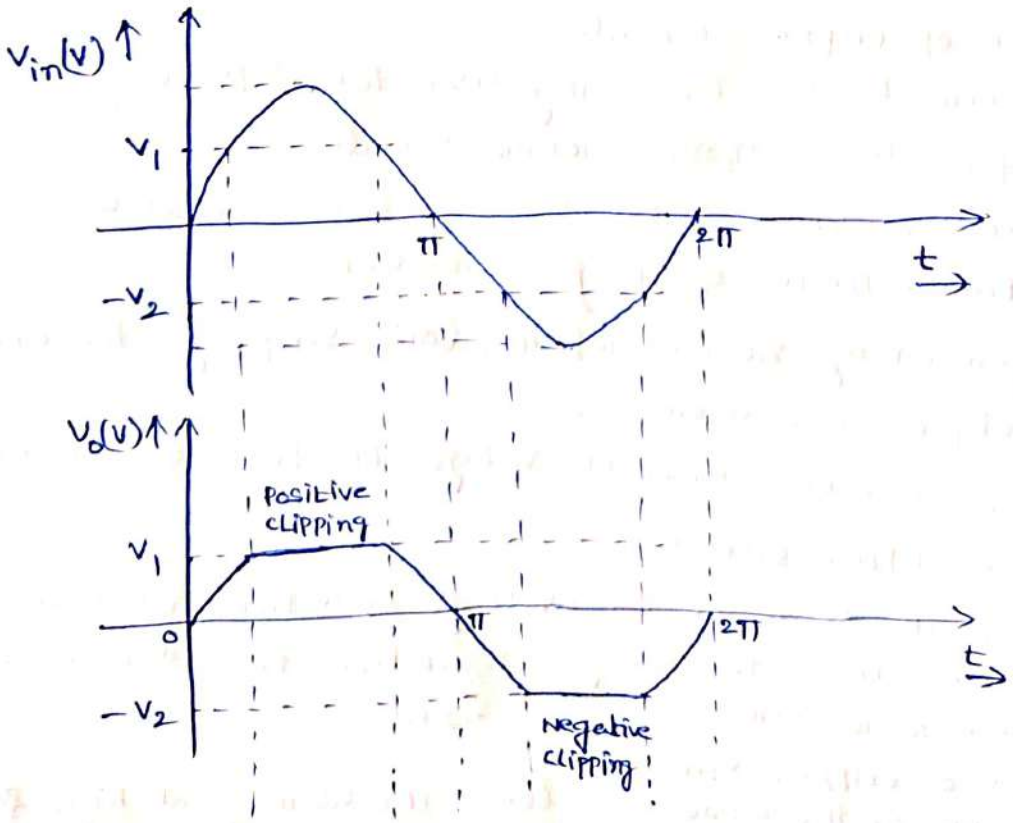


fig(d): Equivalent circuit for $V_{in} > -V_2$



fig(e): Equivalent circuit for $V_{in} \leq -V_2$

The input and output waveforms for a two way clipper are shown in below fig(f).



Transfer characteristics:

The mathematical equations for the two way parallel clipper are

$V_o = V_{in} \frac{R_L}{R_1+R_L}$; for $V_{in} < V_1$
$V_o = V_1$; for $V_{in} \geq V_1$
} During Positive Half cycle

$V_o = -V_2$; for $V_{in} \leq V_2$
$V_o = V_{in} \frac{R_L}{R_1+R_L}$; for $V_{in} > V_2$
} During Negative half cycle.

The transfer characteristics are shown in below fig (g).

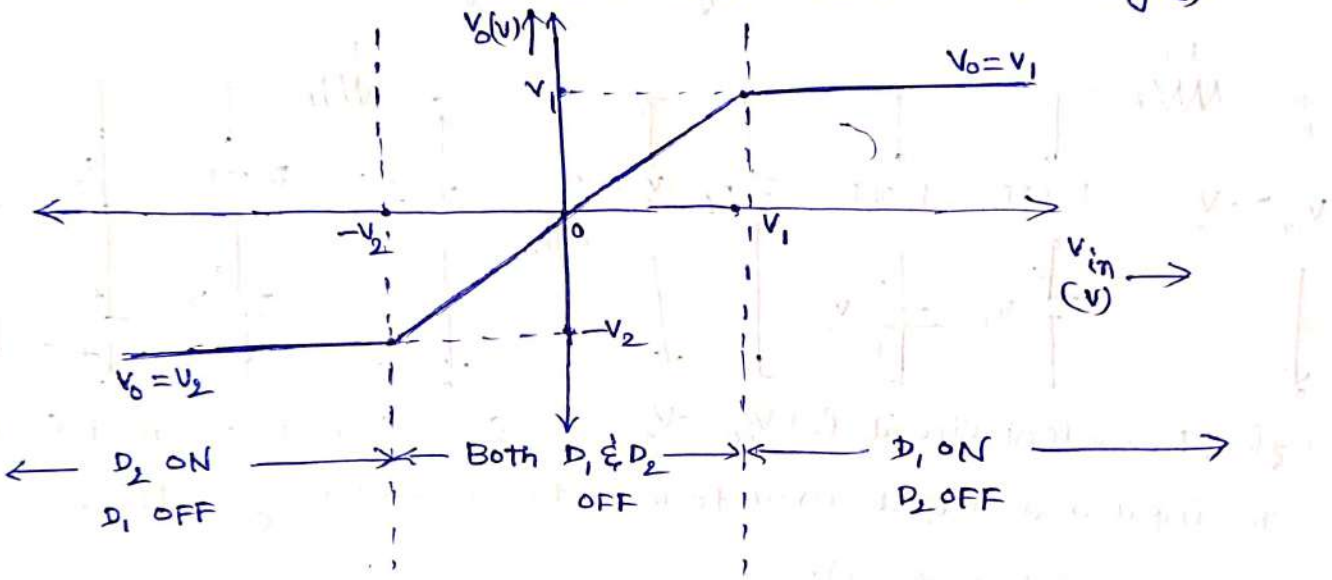


fig: Transfer characteristics of Two way parallel clipper

Applications of clipper circuits

1) Clipper circuits are frequently used for seperating the synchronizing signals from the composite picture signals
2) The excessive noise spikes above a certain level can be clipped off in FM transmitters by using series clippers
3) For generating new waveforms (or) shaping the existing wave-form clippers are used.
4) Clippers can be used as voltage limiters & amplitude selectors.

Advantages of clipper circuits:

1) Clipper circuits serve as over voltage protection for sensitive devices
2) they can be used for voltage regulation for sensitive devices
3) They can reduce the noise in a signal

Disadvantages of clipper circuits:

1) The capacitance of the diode can affect its working at high frequencies
2) The signal may get distorted if potential across the diode drops drastically

Clamper Circuits

Some times it may be necessary to add a DC level to an AC input signal.

The Circuits that are used to add a DC level to the AC input signal as per the requirements, are called as clamper Circuits.

The capacitor, diode and resistor are three basic elements of a clamper Circuit. The clamper Circuits are also called as DC restorer or DC inserter Circuits.

Depending upon whether positive DC level or negative DC level is to be introduced in the applied AC input signal, the clamper Circuits are classified into two types. such as

1) Negative clamper Circuit
2) Positive clamper Circuit.

Negative clamper Circuit

A simple negative clamper which adds a negative DC level to the AC input signal is shown in figure below. It consists of a capacitor C, a diode D and a Load resistor R_L

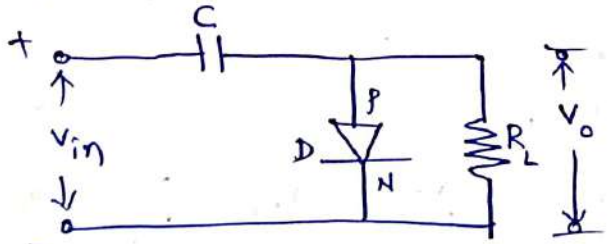


fig: Negative clamper

Let the diode D is an ideal diode and the time Constant $\tau = R_L C$ is very large by selecting large values of R_L and C.

Operation: During the first quarter of the positive half cycle in V_{in}, the capacitor gets charged through the forward biased diode 'D' upto the peak value V_m of the input signal V_{in}. The capacitor charging is almost instantaneous, which is possible by selecting proper values of R_L and C in the circuit. once the capacitor charges to V_m it acts as

a battery of voltage V_m.

As the input voltage decreases after attaining its maximum value V_m, the capacitor remains charged to V_m and the diode D becomes reverse biased. Due to large time constant the capacitor voltage remains $V_c = V_m$.

The output voltage $V_o = V_{in} - V_c = V_{in} - V_m$.

During negative half cycle of V_{in}, the diode D will remain in reverse bias. As the diode D is open circuited, the capacitor will get a path to discharge through R_L. But the large time constant of $R_L C$ causes capacitor to hold its charge to V_m during negative half cycle also as shown in below fig(c)

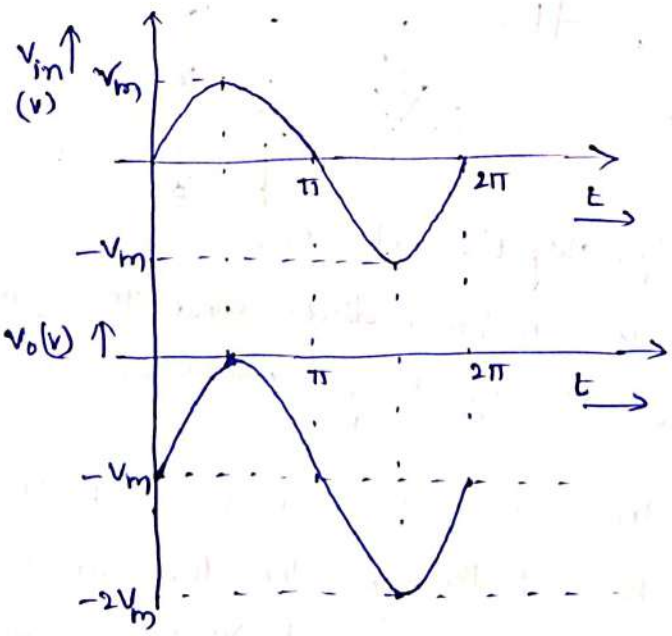
The output voltage $V_o = V_{in} - V_c = V_{in} - V_m$ ⟶ (1)

when $V_{in} = 0$, $V_o = 0 - V_m = -V_m$

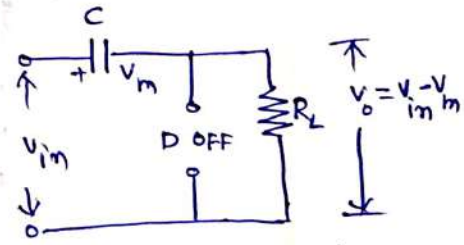
when $V_{in} = V_m$, $V_o = V_m - V_m = 0$

when $V_{in} = -V_m$, $V_o = -V_m - V_m = -2V_m$.

The input and output waveforms of negative clamper are shown below.



fig(b) Input and output waveforms of negative clamper



fig(c): Negative clamper during negative half-cycle of V_{in}

Square wave input for a negative clamper:

If a square wave input is applied to a negative clamper the capacitor charges to peak value (V_m) of the input voltage almost instantaneously and the net output voltage (V_o) during positive half cycle of the applied input signal remains zero.

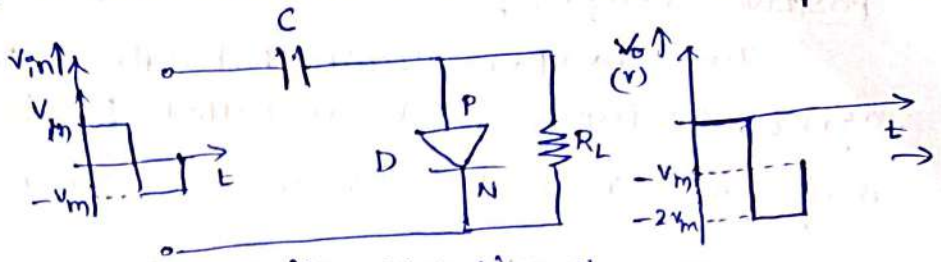


fig: Negative clamper

During negative half cycle the output swings to twice the peak value of the voltage (ie $-2V_m$) and remains constant during the entire negative half cycle of V_{in}. The input and output wave forms are as shown in below figure.

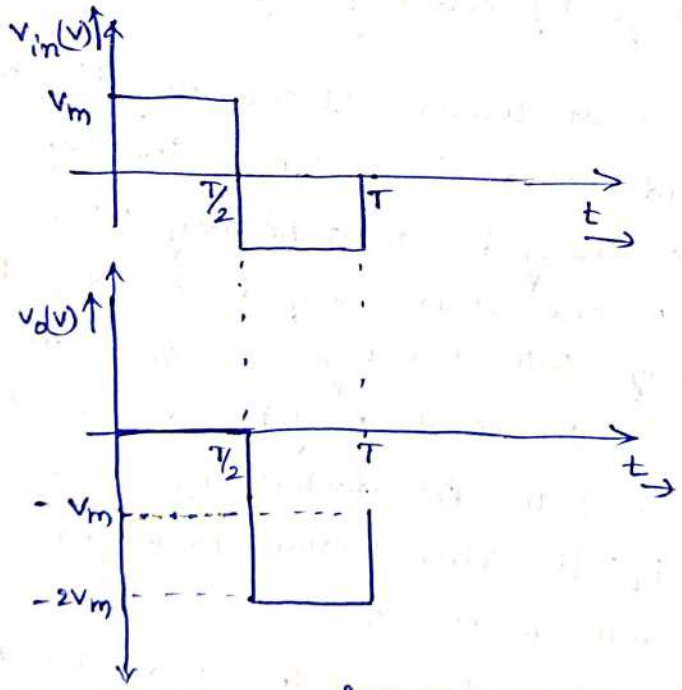


fig: waveforms for square wave input in negative clamper

Steps to analyze a clamper circuit

To analyse the given clamper circuit the following steps are useful.

1) Start the analysis of the clamper circuit by considering that part of the input signal for which the diode is forward biased.
2) when the diode is conducting, assume that the capacitor charges instantaneously to a voltage level determined by the input
3) When the diode is not conducting, due to large time constant the capacitor maintains its charge which is stored during forward biased condition of diode.

4) Analyse the output for different values of input and sketch the output waveform.

Positive clamper:

The clamper circuit that adds a positive DC level to the applied AC input signal is called positive clamper. The circuit diagram for positive clamper is shown in figure below

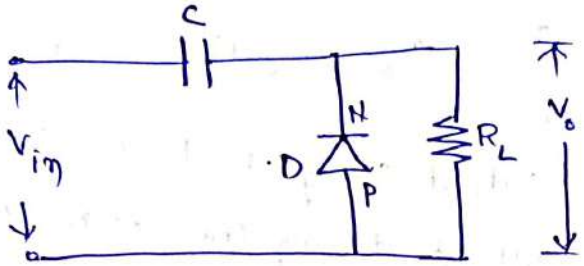


fig: Positive clamper Circuit

Let the diode D is an ideal diode and the time constant $\tau = R_L C$ is very large by selecting large values of R_L and C.

Operation: During first quarter of the negative half cycle the diode 'D' gets forward biased due to which the capacitor starts charging and it is charged instantaneously up to the peak value $-V_m$ of the input signal. once it is charged to $-V_m$ the capacitor behaves like a battery with a voltage of $-V_m$. As the input V_{in} increases after $-V_m$, the diode D gets reverse biased hence the capacitor gets a path for discharging through R_L, but the large value of $R_L C$ (i.e Time constant is large) causes the voltage across capacitor to remain as $-V_m$.

During positive half cycle the diode will remain in reverse bias. As large time constant $\tau = R_L C$ is present in the circuit, the capacitor maintains the voltage of $-V_m$ during positive half cycle also. The output V_o during positive half cycle of V_{in} is

$$V_o = V_{in} - V_C = V_{in} - (-V_m)$$

$$\Rightarrow V_o = V_{in} + V_m$$

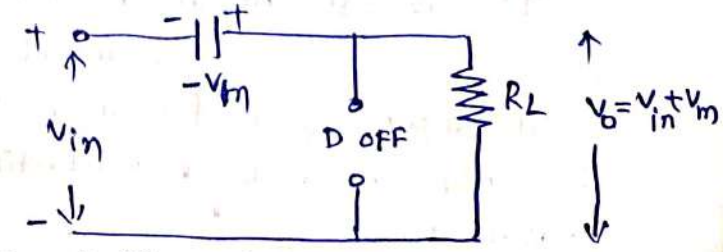


fig: Positive clamper during Positive half cycle of V_{in}

when $V_{in} = 0$, $V_o = 0 + V_m = V_m$

when $V_{in} = V_m$, $V_o = V_m + V_m = 2V_m$

when $V_{in} = -V_m$, $V_o = -V_m + V_m = 0$

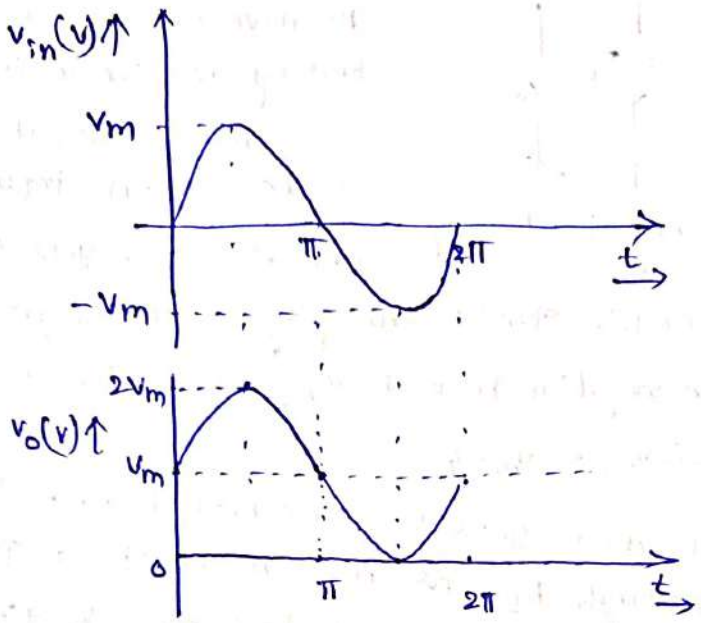


fig: Input and output waveforms of positive clamper.

Square wave input for a positive Clamper

If a square wave input is applied to a positive clamper, the capacitor charges to peak value $-V_m$ of the input instantaneously and the net output voltage V_o during the negative half cycle of V_{in} remains zero.

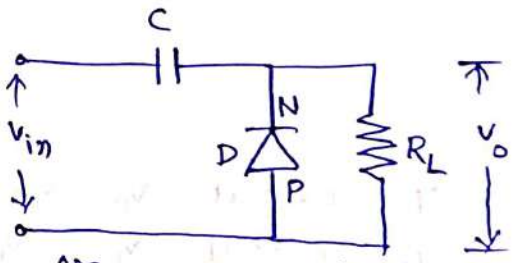
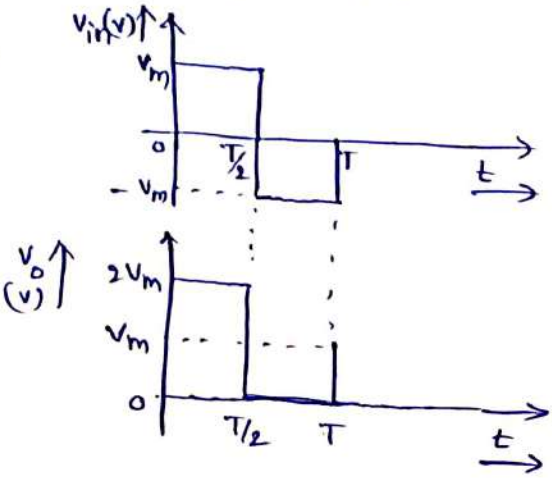


fig: positive clamper

During positive half cycle the output swings twice the peak value of the input voltage i.e $2V_m$ and remains constant during the entire positive half cycle of V_{in}.

The input and output waveforms are shown in figure.



Clamper circuits with biasing:

Positive clamper with negative biasing:

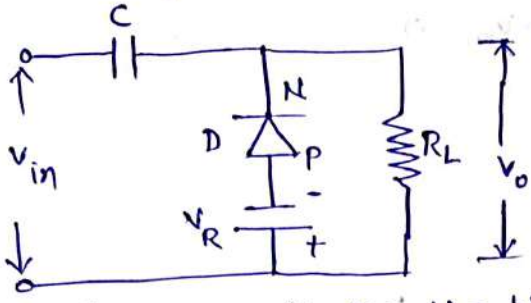


fig: Positive clamper with negative biasing

The circuit diagram for positive clamper with negative biasing is shown in figure.

During negative half - cycle when input $V_{in} < -V_R$ the diode D gets into forward - bias during which the capacitor starts charging. The capacitor charges till V_{in} reaches $-V_m$ (i.e the negative peak of V_{in}) and the capacitor holds the voltage of $-V_m-(-V_R) = -V_m+V_R$.

when $V_{in} > -V_R$ the diode gets reverse biased and the capacitor gets a path to discharge through R_L. As the time constant $\tau = R_L C$ is very large the capacitor maintains the voltage of $-V_m+V_R$ during the reverse biased condition of the diode also.

The output voltage $V_o = V_{in} - V_c$

$$V_o = V_{in} - (-V_m + V_R)$$

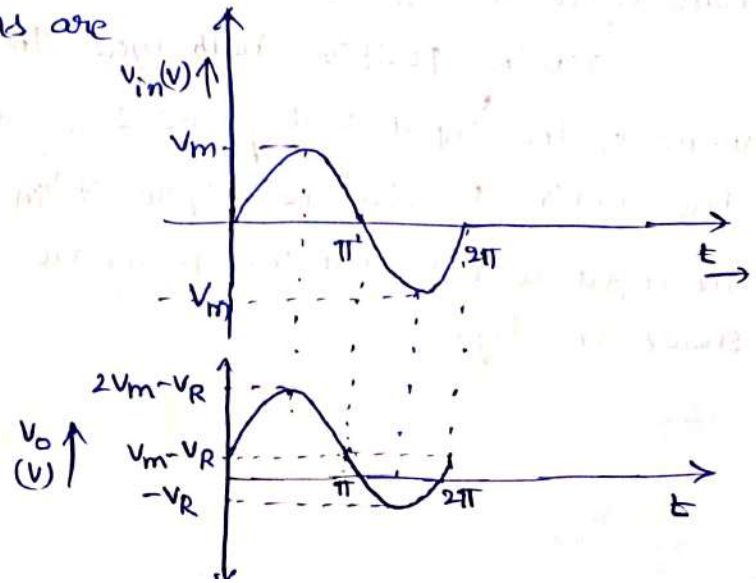
$$V_o = V_{in} + V_m - V_R \quad \text{---------} \quad (1)$$

The output $V_o = V_m - V_R$ for $V_{in} = 0$

The output $V_o = 2V_m - V_R$ for $V_{in} = V_m$

The output $V_o = -V_R$ for $V_{in} = -V_m$

The input and output waveforms are shown in figure below.



Positive clamper with positive biasing:

The circuit diagram for positive clamper with positive biasing is as shown in figure.

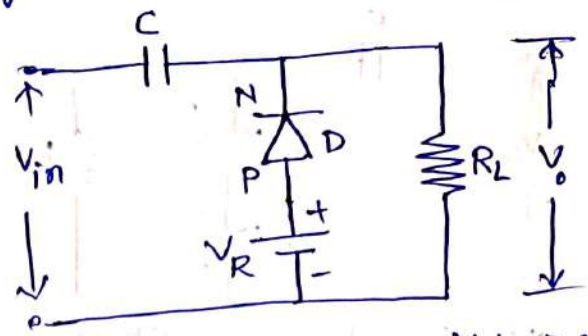


fig: Positive clamper with positive -biasing.

During negative half cycle of V_{in} the diode gets into forward bias and the capacitor charges instantaneously till V_{in} reaches $-V_m$. Therefore the voltage across capacitor is $V_C = -V_m$.

During positive half cycle when $V_{in} > V_m$ the diode gets into reverse bias and the capacitor gets a path to discharge through R_L. As R_LC is very large the capacitor maintains the voltage of $-V_m$ during the reverse biased condition of the diode also.

The output voltage $V_o = V_{in} - V_C + V_R$

$\Rightarrow V_o = V_{in} - (-V_m) + V_R$

$\Rightarrow V_o = V_{in} + V_m + V_R$

for $V_{in} = 0$, $V_o = V_m + V_R$

for $V_{in} = V_m$, $V_o = 2V_m + V_R$

for $V_{in} = -V_m$, $V_o = V_R$

The input and output waveforms for positive clamper with positive biasing is shown in figure

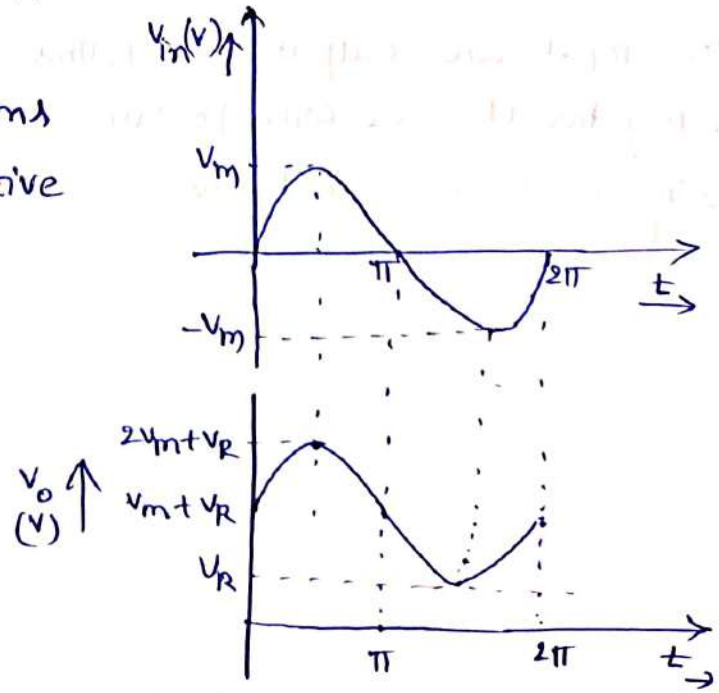


fig: Input and output wave forms

Negative Clamper with positive biasing:

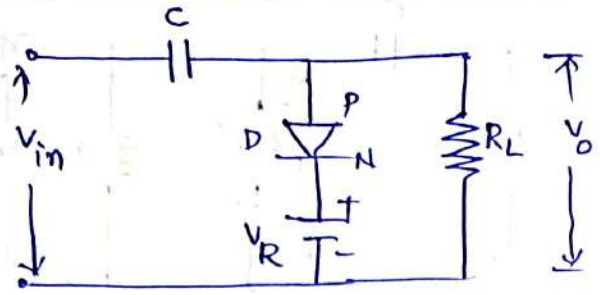


fig: Negative clamper with positive biasing

The circuit diagram for negative-clamper with positive biasing is as shown in figure.

During positive half cycle, when $V_{in} > V_R$ the diode D gets forward biased and the capacitor starts charging instantaneously till V_{in} reaches $+V_m$. The voltage across the capacitor $V_c = V_m - V_R$.

During $V_{in} < V_R$ the diode gets into reverse bias, and the capacitor gets a path to discharge through the load R_L. As $R_L C$ is very high, the capacitor maintains the voltage of $V_m - V_R$ during the reverse biased condition of the diode also

the output $V_o = V_{in} - V_c$

$$V_o = V_{in} - (V_m - V_R)$$

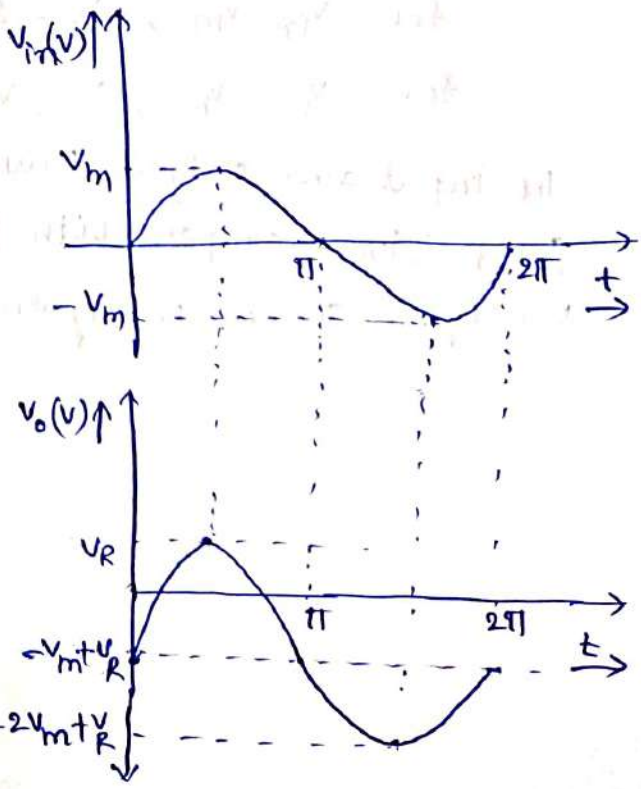
$$V_o = V_{in} - V_m + V_R$$

for $V_{in} = 0$, $V_o = -V_m + V_R$

for $V_{in} = V_m$, $V_o = V_R$

for $V_{in} = -V_m$, $V_o = -2V_m + V_R$

The input and output waveforms for negative clamper with positive biasing is as shown in figure.



Negative clamper with negative biasing:

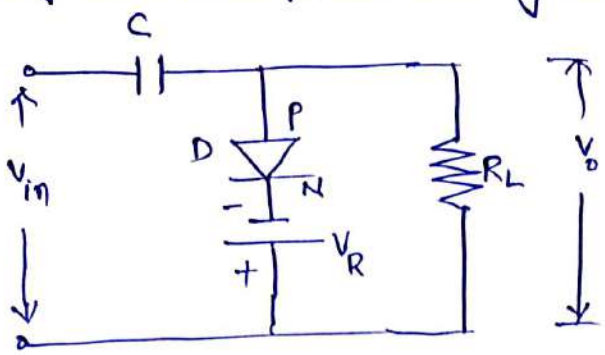


fig: Negative clamper with negative biasing.

The circuit diagram for negative clamper with negative biasing is as shown in figure.

During positive half cycle the diode D is forward biased and hence the capacitor gets charged till V_{in} reaches $+V_m$. Therefore the capacitor holds the voltage of V_m.

when $V_{in} < -V_R$, the diode gets into reverse bias and the capacitor gets a path to discharge through R_L. As R_LC is very large the capacitor maintains the voltage of V_m during the reverse biased condition of the diode also.

The output voltage $V_o = V_{in} - V_C - V_R$

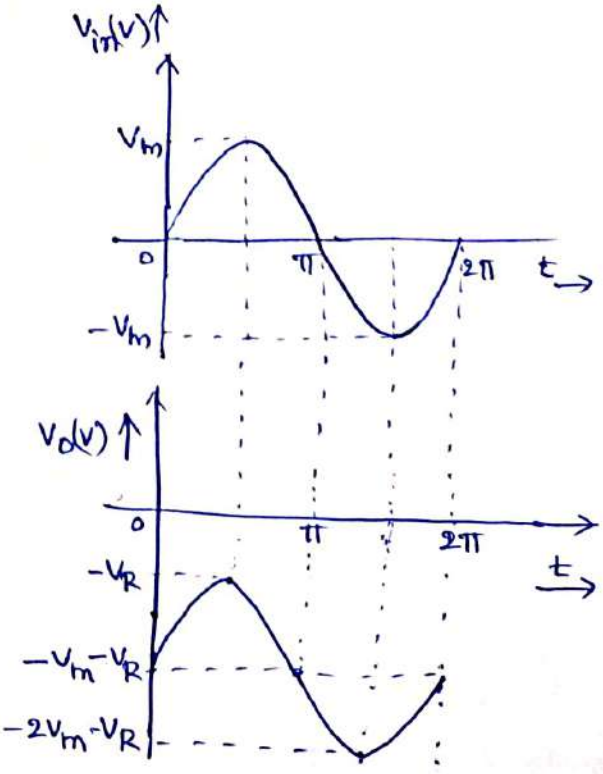
$$V_o = V_{in} - V_m - V_R$$

for $V_{in} = 0$, $V_o = -V_m - V_R$

for $V_{in} = V_m$, $V_o = -V_R$

for $V_{in} = -V_m$ $V_o = -2V_m - V_R$

The input and output waveforms for a negative clamper with negative biasing are as shown in figure below.



Advantages & disadvantages of clampers:

Advantages:

1) It is used to shift DC level of input signal
2) It is easy to implement
3) clampers are cost effective
4) Design is flexible

Disadvantages:

1) Design of biased clampers is complex
2) It has limited frequency response

UNIT-I

TRANSISTOR BIASING & THERMAL STABILIZATION

Need for Biasing :

* Inorder to produce the distortion free output in amplifier circuits the supply voltages and resistances in the circuit must be properly chosen. These voltages and resistances establish a set of d.c voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region. These voltages and currents are called Quiescent values which determine the operating point or Q-point for the transistor.

* The process of giving proper supply voltages and resistances to an amplifier circuit for obtaining the desired Q-point is called as 'biasing'. The circuits that are used for getting the desired and proper operating point are known as biasing circuits.

Load line Analysis :

i) DC Load Line :

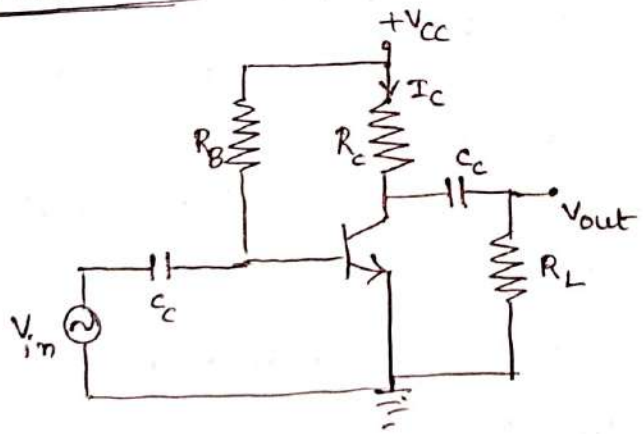


fig a: Biasing Circuit

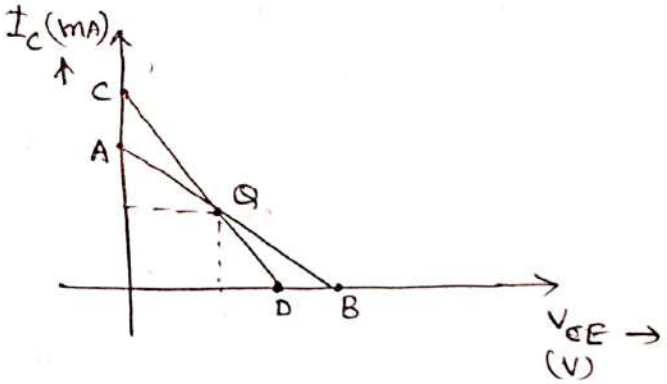


fig b : Load line analysis.

The load line can be a DC Load Line or an AC Load Line, that is drawn to a biasing circuit.

By applying KVL to the collector (output) circuit of the circuit shown in figure(a) we get $V_{cc} = I_c R_c + V_{CE}$ → (1)

The straight line AB in fig(b) represents the DC Load line.

* The coordinates of point 'A' are obtained by substituting $V_{CE}=0$ in equation ①. Then $I_C = I_{C_{max}} = \frac{V_{CC}}{R_C}$. Therefore the co-ordinates of Point 'A' are $V_{CE}=0$ and $I_C = \frac{V_{CC}}{R_C}$

* The coordinates of point 'B' are obtained by substituting $I_C = 0$ in equation ①. Then $V_{CE} = V_{CEmax} = V_{CC}$. Therefore the co-ordinates of Point 'B' are $V_{CE} = V_{CC}$ and $I_C = 0$.

Thus the DC Load line AB is drawn, if the values of V_{CC} and R_C are known.

* The optimum Q-point is located at the mid point of the DC load line AB i.e Q is exactly midway between A and B.

In order to get faithful amplification the operating point 'Q' must be in the middle of the active region.

Q) What are the factors that cause the Q-point to shift it's position. Explain in detail.

Ans) Even though the operating point 'Q' is fixed in the middle of the active region, it is very important to ensure that it remains stable where it is originally fixed. If the operating point shifts nearer to either A or B, the output signal may get clipped off i.e the output gets distorted.

In practice the Q-point tends to shift its position due to the following three main factors. We know that $I_C = \beta I_B + (1+\beta) I_{C_0}$.

i) Reverse saturation current, I_{CO}, which doubles for every 10°C increase in temperature.

ii) Base-emitter voltage V_{BE}, which decreases by 2.5 mV for 1°C increase in temperature. I_C is dependent on I_B which is decided by V_{BE}

iii) Transistor current gain β i.e h_{FE} which increases with increase in temperature.

If the transistor is replaced by another one, we cannot ensure that the new transistor will have the same transistor parameters as that of the first one. The parameters such as β may be differed. This results in the variation of collector current I_C. Hence the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which is either saturation region or cutoff region. This is completely unsatisfactory.

ii) AC Load line:

The DC load line is drawn under zero input ac conditions and the operating point is located in the middle of the dc load line. The Ac load line should also pass through the operating point Q. In this case the effective load resistance $R_{ac} = R_C \| R_L$.

To draw the ac load line, two end points are required with respect to maximum V_{CE} and maximum I_C when the ac input signal is applied.

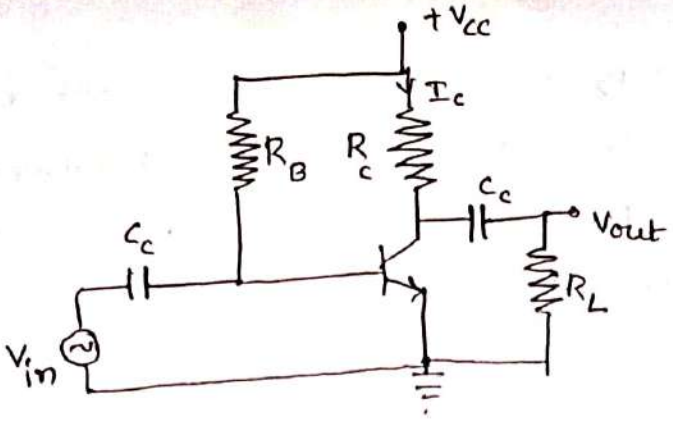
Maximum $V_{CE} = V_{CE_Q} + I_{CQ} R_{ac}$ which locates the point 'D' on the V_{CE} axis.

Maximum $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$ which locates the point 'C' on the I_C axis.

By joining these points C and D, the ac load line is formed. As $R_C > R_{ac}$ the DC load line is less steeper than the ac load line.

From the above figure (b) it is clear that the intersection of DC and Ac load lines is the operating point.

Problem: In the transistor shown in below figure (a) $R_C = 8\,k\Omega$ $R_L = 24\,k\Omega$ and $V_{CC} = 24V$. Draw the dc load line and determine the optimum operating point. Also draw the ac load line.



solution: i) DC load line: To draw this $V_{in} = 0$.

Applying KVL to the output (collector) circuit

$$V_{CC} = V_{CE} + I_c R_c \Rightarrow V_{CC} - V_{CE} - I_c R_c = 0 \rightarrow (1)$$

To draw the dc load line, the two end points i.e maximum V_{CE} (at $I_c = 0$) and maximum I_c (at $V_{CE} = 0$) are required.

Maximum $V_{CE} = V_{CC}$ [∵ From eq(1) when $I_c = 0$]

$\therefore V_{CE\,max} = 24V$, Point A = $V_{CE\,max} = 24V$, $I_c = 0$.

Maximum $I_c = \frac{V_{CC}}{R_c}$ [∵ from eq(1) when $V_{CE} = 0$]

$\therefore I_{cmax} = \frac{V_{CC}}{R_c} = \frac{24}{8 \times 10^3} = 3mA$.

Point B is $V_{CE} = 0$, $I_{cmax} = 3mA$.

The DC load line is drawn by joining the points A and B.

ii) For optimum operating point, mark the middle of the dc load line and corresponding V_{CE} and I_c are known.

$$V_{CEQ} = \frac{V_{CE\,max}}{2} = \frac{24}{2} = 12V,$$

$$I_{CQ} = \frac{I_{c\,max}}{2} = \frac{3 \times 10^{-3}}{2} = 1.5mA.$$

iii) **AC Load line:**

To draw the AC load line two end points i.e maximum V_{CE} and maximum I_C when the signal is applied are required.

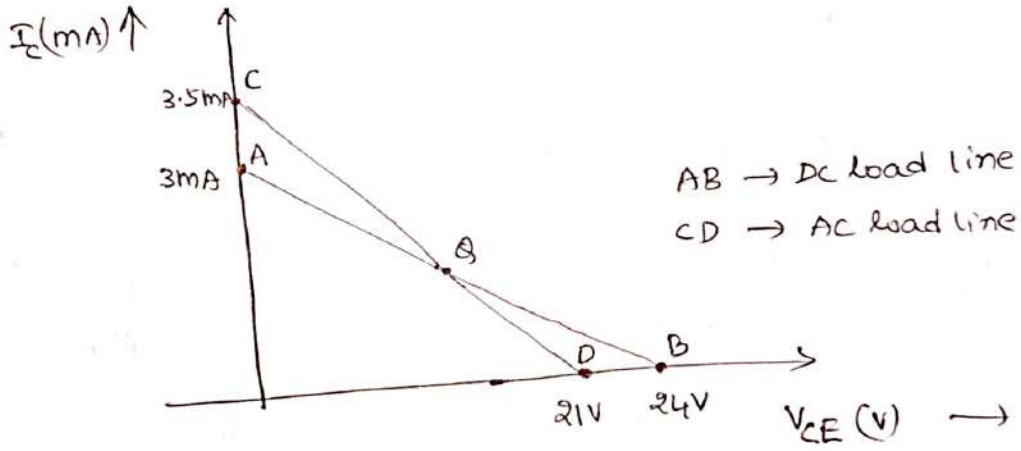
$$R_{ac} = R_c \| R_L = \frac{R_c R_L}{R_c + R_L} = \frac{8 \times 24}{8+24} = 6\,k\Omega$$

Maximum $V_{CE} = V_{CEQ} + I_{CQ} R_c = 12 + (1.5 \times 10^{-3} \times 6 \times 10^3) = 21\,V$.

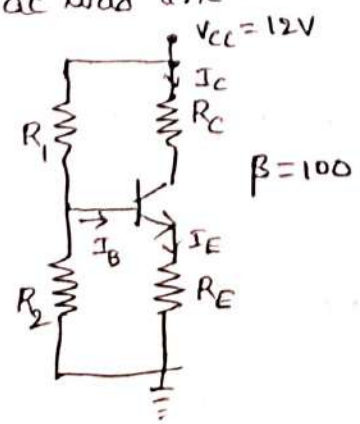
This locates the point 'D' on V_{CE} axis.

Maximum $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 1.5 \times 10^{-3} + \frac{12}{6 \times 10^3} = 3.5\,mA$.

This locates the point C on the I_C axis. By joining these points C and D, ac load line is formed.



(2) For the transistor amplifier shown in below figure, $V_{CC} = 12V$, $R_1 = 8k\Omega$, $R_2 = 4k\Omega$, $R_C = 1k\Omega$, $R_E = 1k\Omega$ and $R_L = 1.5k\Omega$. Assume $V_{BE} = 0.7\,V$ i) Draw the dc load line ii) Determine the operating point iii) Draw the ac load line.



Sol) i) DC load line :

Applying KVL to the output circuit

$$V_{CC} = V_{CE} + I_C R_C + I_E R_E$$

$I_C \simeq I_E$, Therefore $V_{CC} = V_{CE} + I_C(R_C + R_E) \rightarrow (1)$

To draw the dc load line we require two end points i.e maximum V_{CE} (at $I_C = 0$) and maximum I_C (at $V_{CE} = 0$).

Maximum $V_{CE} = V_{CC}$ ($\because$ From eq (1) when $I_C = 0$)

This locates the point B on the V_{CE} axis.

Maximum $I_C = \frac{V_{CC}}{R_C + R_E} = \frac{12}{(1+1)10^3} = 6mA$ ($\because$ from eq (1) when $V_{CE} = 0$)

This locates the point A on the I_C axis.

Joining these two points A and B, the DC load line is formed.

ii) operating point (Q) :

$$V_T = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

$$= 12 \times \frac{4}{8+4}$$

$$V_T = 4V.$$

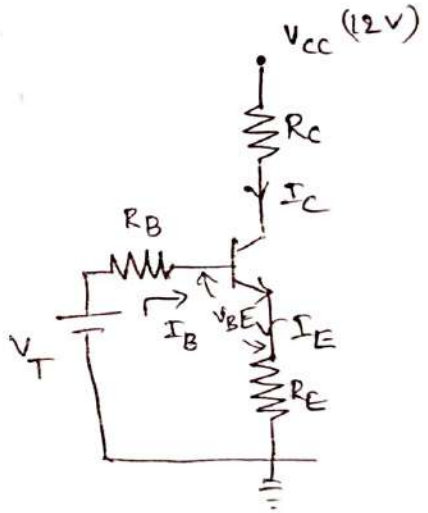


fig:- Thevenin equivalent circuit

$$R_B = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$R_B = \frac{8 \times 4}{8+4} = 2.6666 k\Omega$$

Applying KVL to the input circuit

$$V_T - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_T - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0$$

$$V_T - I_B R_B - V_{BE} - (\beta I_B + I_B) R_E = 0$$

$$V_T - I_B\left[R_B + (1+\beta)R_E\right] - V_{BE} = 0$$

$$I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta)R_E} = \frac{4 - 0.7}{2.6666\times10^3 + (1+100)(1\times10^3)}$$

$$\therefore I_B = 31.8\ \mu A$$

$$\therefore I_C = \beta I_B = 100\times 31.8\times10^{-6} = 3.1833\ mA$$

$$I_E = I_B + I_C = 31.8\times10^{-6} + 3.1833\times10^{-3} = 3.2118\ mA$$

Applying KVL to the output circuit

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$12 - 3.1833\times10^{-3}\times1\times10^3 - V_{CE} - 3.2118\times10^{-3}\times1\times10^3 = 0$$

$$\Rightarrow V_{CE} = 5.60487\ V.$$

$$\therefore \text{operating point } (V_{CEQ}, I_{CQ}) = (5.6049\ V,\ 3.1833\ mA)$$

iii) AC load line:

To draw the AC load line we need two end points ie maximum V_{CE} and maximum I_C when input AC signal is applied.

$$R_{ac} = R_C \| R_L = \frac{R_C R_L}{R_C + R_L} = \frac{10\times1.5\times10^3}{(1+1.5)10^3} = 0.6\ k\Omega$$

$$\text{Maximum } V_{CE} = V_{CEQ} + I_{CQ}R_{ac} = 5.60487 + (3.1833\times10^{-3}\times0.6\times10^3)$$

$$\therefore V_{CE\,max} = 7.51485\ V$$

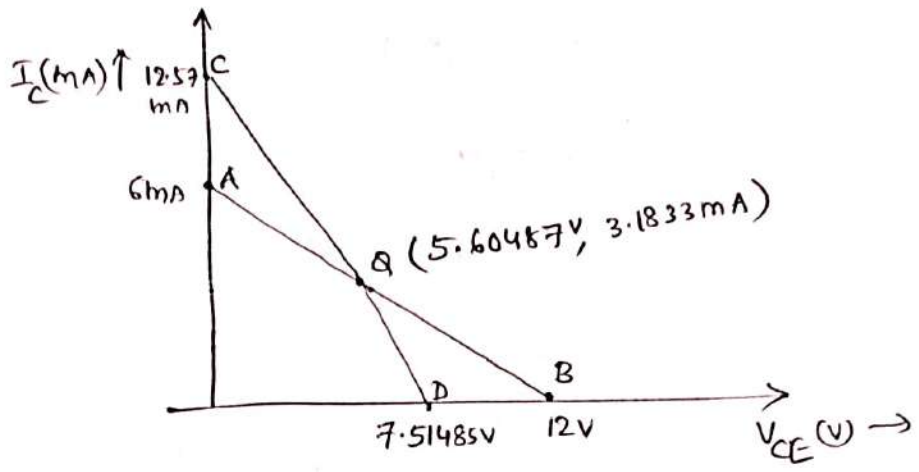
This locates the point D on V_{CE} axis.

$$\text{Maximum } I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = (3.1833\times10^{-3}) + \frac{5.60487}{0.6\times10^3}$$

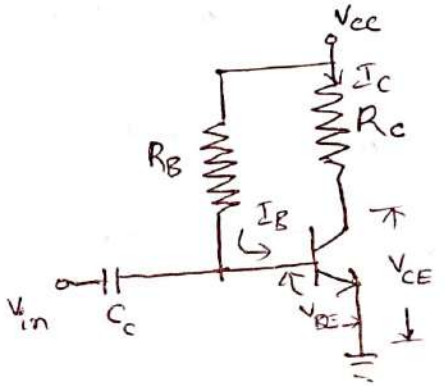
$$\therefore I_{C\,max} = (3.1833\times10^{-3}) + (9.34145\times10^{-3})$$

$$\therefore I_{C\,max} = 12.52475.$$

This locates a point 'C' on I_C axis. Joining the points C and D, the AC load line is formed.



Problem 3: Design the circuit shown below. Given Q-point values to be $I_{CQ} = 1mA$ and $V_{CEQ} = 6V$. Assume that $V_{CC} = 10V$, $\beta = 100$ and $V_{BE} = 0.7V$



Sol) Applying KVL to the output circuit $V_{CC} - I_C R_C - V_{CE} = 0$

$$\Rightarrow R_c = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10-6}{1\times10^{-3}} = 4K\Omega$$

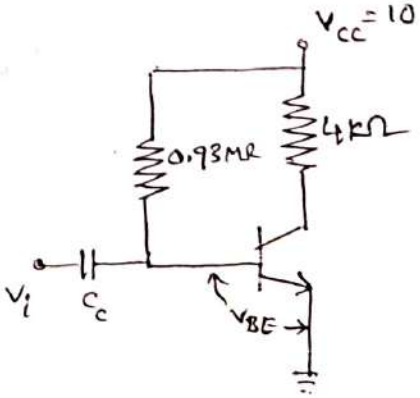
$$I_B = \frac{I_C}{\beta} = \frac{1\times10^{-3}}{100} = 10\mu A.$$

Applying KVL to i/p ckt

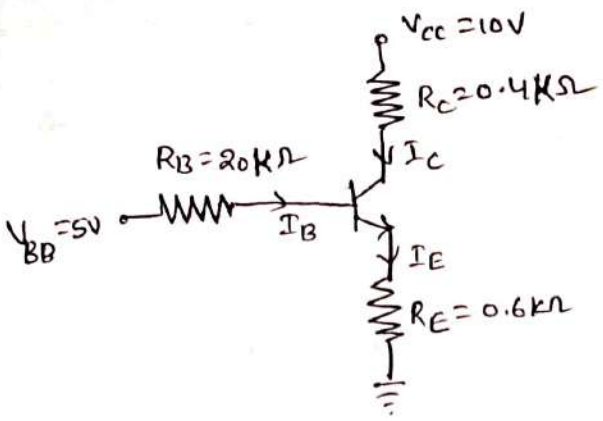
$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$10 - 10\times10^{-6} \times R_B - 0.7 = 0$$

$$\Rightarrow R_B = 0.93 M\Omega$$



Problem 4: Determine the Q-point for the circuit shown in below Assume that $\beta = 100$ and $V_{BE} = 0.7\ V$



Sol: Applying KVL to the input circuit

$$V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0 \quad \rightarrow (1)$$

we know that $I_E = I_B + I_C = I_B + \beta I_B = I_B(1+\beta) \rightarrow (2)$

$\therefore$ substituting eq (2) in eq (1)

$$V_{BB} - I_B R_B - V_{BE} - I_B(1+\beta) R_E = 0$$

$$\Rightarrow I_B = \frac{V_{BB} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{5 - 0.7}{20\times10^3 + (1+100)(0.6\times10^3)}$$

$$\therefore I_B = 53.3499\ \mu A$$

W.K.T $I_C = \beta I_B = 100 \times 53.3499 \times 10^{-6} = 5.335\ mA$

$$I_E = I_C + I_B = 5.335\times10^{-3} + (53.3499\times10^{-6})$$

$$\therefore I_E = 5.3883\ mA$$

Applying KVL to o/p circuit

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$10 - (5.335\times10^{-3} \times 0.4\times10^3) - V_{CE} - (5.3883\times10^{-3} \times 0.6\times10^3) = 0$$

$$\Rightarrow V_{CE} = 4.633\ V$$

$\therefore$ operating point $(V_{CE}, I_C) = (4.633\ V,\ 5.335\ mA)$

Biasing stability :

Designing the biasing circuit of the transistor to stabilize the Q-point is called the biasing stability.

stability factor:

The extent to which the collector current I_C is stabilized with varying I_{C_0}, V_{BE} and β is measured by using stability factors S, S' and S'' respectively.

Stability factor (S):

It is defined as the rate of change of collector current I_C with respect to the collector junction reverse saturation current I_{C_0}, keeping V_{BE} and β as constant.

$$\text{i.e } S = \frac{\partial I_C}{\partial I_{C_0}} \simeq \frac{dI_C}{dI_{C_0}} \simeq \frac{\Delta I_C}{\Delta I_{C_0}}, \quad V_{BE} \text{ and } \beta \text{ Constant.}$$

The collector current for a C.E amplifier is given by

$$I_C = \beta I_B + I_{CE_0}.$$

where $I_{CE_0} = (1+\beta) I_{C_0}$.

$$\therefore I_C = \beta I_B + (1+\beta) I_{C_0}.$$

Differentiating the above equation with respect to I_C, we get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{C_0}}{dI_C}$$

$$\Rightarrow \frac{dI_{C_0}}{dI_C} = \frac{1 - \beta \frac{dI_B}{dI_C}}{1+\beta}$$

$$\Rightarrow \boxed{S = \frac{dI_C}{dI_{C_0}} = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}}$$

To have a better thermal stability 'S' should be as small as possible.

Stability factor (s') :

It is defined as the rate of change of collector current I_C with respect to the base to emitter voltage V_{BE}, keeping I_{C_0} and β as constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \simeq \frac{dI_C}{dV_{BE}} \simeq \frac{\Delta I_C}{\Delta V_{BE}} \quad , \; I_{C_0} \text{ and } \beta \text{ Constant}$$

stability factor (s''):

It is defined as the rate of change of collector current I_C with respect to the current amplification factor β, keeping I_{C_0} and V_{BE} as constant.

$$S'' = \frac{\partial I_C}{\partial \beta} \simeq \frac{dI_C}{d\beta} \simeq \frac{\Delta I_C}{\Delta \beta} \quad , \; I_{C_0} \text{ and } V_{BE} \text{ Constant.}$$

BJT biasing :

Methods of BJT biasing :

The commonly used biasing methods are

1) Fixed bias (or) base resistor method.
2) Collector to base bias (or) Biasing with feed back resistor
3) Self bias (or) Emitter bias (or) voltage (potential) divider - bias

1) Fixed bias (or) Base resistor method :

A common emitter amplifier using fixed bias circuit is as shown in below figure.

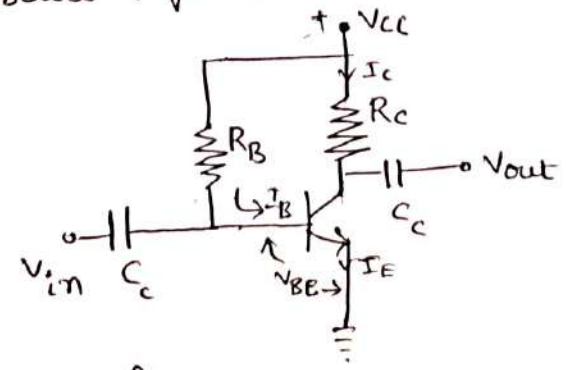


fig:- Fixed biasing Circuit.

In this method a high resistance R_B is connected between Positive terminal of V_{cc} and the base terminal of the transistor.

To get the DC analysis the input signal V_{in} should be zero and capacitors are short circuited.

Now by applying KVL to the input circuit, we get

$$V_{cc} - I_B R_B - V_{BE} = 0 \longrightarrow (1)$$

$$\Rightarrow I_B = \frac{V_{cc} - V_{BE}}{R_B} \longrightarrow (2)$$

Since the above equation is independent of 'I_c', we get

$$\frac{dI_B}{dI_c} = 0.$$

We know that the stability factor $S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_c}}$

$$\Rightarrow S = \frac{1+\beta}{1-\beta(0)} = 1+\beta$$

$$\therefore \boxed{S = 1+\beta}$$

Advantages of fixed bias method:

1) Circuit is very simple.
2) It requires less number of components.
3) If the supply voltage V_{cc} is very large compared to V_{BE}, the base current becomes largely independent of V_{BE}.

Disadvantages of fixed bias:

1) The stability factor for fixed bias $S = 1+\beta$. since 'β' is a large quantity, fixed bias has the poor stability.

Stability factor S' for fixed bias circuit:-

We know that stability factor $S' = \frac{\partial I_c}{\partial V_{BE}}$, I_{c_0} and β are Constant.

We know that $I_c = \beta I_B + (1+\beta) I_{c_0}$.

$$\Rightarrow I_B = \frac{I_C - (1+\beta) I_{C_0}}{\beta}$$

Substituting the above equation in equation (1) we get

$$V_{CC} - \left(\frac{I_C - (1+\beta) I_{C_0}}{\beta}\right) R_B - V_{BE} = 0 \quad \longrightarrow (3)$$

differentiating the equation (3) with respect to V_{BE} we get

$$0 - \frac{1}{\beta}\left[\frac{dI_C}{dV_{BE}} - 0\right] R_B - 1 = 0$$

$$\Rightarrow -\frac{1}{\beta}\frac{dI_C}{dV_{BE}} \cdot R_B = 1$$

$$\Rightarrow \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B}$$

$$\therefore \boxed{S' = \frac{-\beta}{R_B}}$$

Stability factor (S''):

we know that stability factor $S'' = \frac{dI_C}{d\beta}$, I_{C_0} and V_{BE} constant

Differentiating equation (3) with respect to β we get

$$0 - \frac{\left[\beta\left(\frac{dI_C}{d\beta} - I_{C_0}\right) - \left[I_C - (1+\beta) I_{C_0}\right]\right] R_B}{\beta^2} - 0 = 0$$

$$\Rightarrow \beta \frac{dI_C}{d\beta} - \cancel{\beta I_{C_0}} - I_C + I_{C_0} + \cancel{\beta I_{C_0}} = 0$$

Neglecting I_{C_0} we get

$$\beta \frac{dI_C}{d\beta} = I_C \Rightarrow \frac{dI_C}{d\beta} = \frac{I_C}{\beta}$$

$$\therefore \boxed{S'' = \frac{I_C}{\beta}}$$

2) Collector to Base bias (or) Biasing with feedback resistor:

The Collector to base bias circuit is same as that of fixed bias except the base resistor 'R_B' is connected to the collector rather than V_{cc} supply. The resistor 'R_B' acts as a feed back resistor. Hence this method can also be called as biasing with feed back resistor.

If the collector current I_c tends to increase due to either increase in temperature or the transistor has been replaced by the one with higher β, then the voltage drop across R_c increases. This causes V_{CE} to decrease.

From the collector to base bias circuit shown below

$V_{CE} = I_B R_B + V_{BE}$, as V_{CE} decreases I_B should be decreased. so, this compensates the increase in I_c due to the temperature increase.

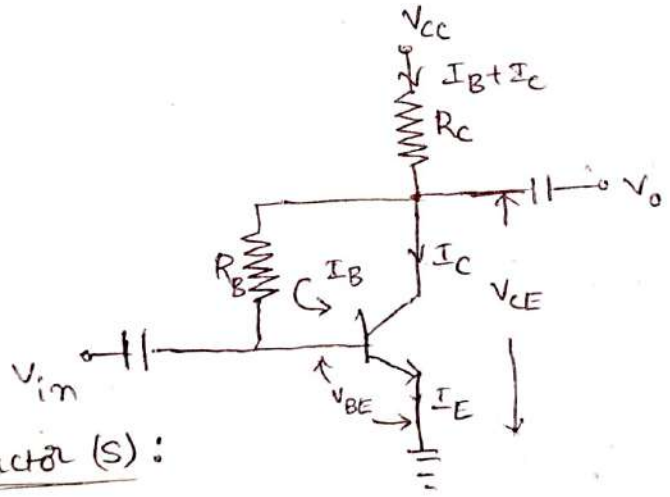


fig:- Collector to base bias

i) Stability factor (S):

Applying KVL to the input circuit

$$V_{cc} - (I_B + I_c)R_c - I_B R_B - V_{BE} = 0$$

$$V_{cc} - I_B (R_B + R_c) - I_c R_c - V_{BE} = 0 \longrightarrow (1)$$

Differentiating the above equation with respect to 'I_c' we get

$$0 - \frac{dI_B}{dI_c}(R_B + R_c) - R_c (1) - 0 = 0$$

$$\Rightarrow \frac{dI_B}{dI_c} = -\frac{R_c}{R_B + R_c} \longrightarrow (2)$$

we know that the stability factor $S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$ → ③

Substituting the equation ② in equation ③ we get

$$S = \frac{1+\beta}{1-\beta\left(\frac{-R_C}{R_B+R_C}\right)}$$

$$\therefore \boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}}$$

If R_C is very much larger than R_B, then $S=1$. Then we can say that the value of stability factor (S) in collector to base bias is smaller than the value obtained by fixed bias circuit.

If R_C is very much smaller than R_B then the stability factor $S = 1+\beta$, i.e the stabity is very poor. Thus the collector to base bias arrangement is not satisfactory for the amplifier circuits such as Transformer coupled amplifiers.

ii) Stability factor (S'):

we know that the stability factor $S' = \frac{\partial I_C}{\partial V_{BE}}$, I_{C_0} and β are constant

we know that $I_C = \beta I_B + (1+\beta) I_{C_0}$

$$\Rightarrow I_B = \frac{I_C - (1+\beta) I_{C_0}}{\beta}$$

Substituting the above equation in equation ①, we get

$$V_{CC} - \left[\frac{I_C - (1+\beta)I_{C_0}}{\beta}\right](R_B+R_C) - I_C R_C - V_{BE} = 0 \rightarrow ④$$

Differentiating equation ④ with respect to V_{BE}, we get

$$0 - \left(\frac{R_B+R_C}{\beta}\right)\frac{dI_C}{dV_{BE}} - \frac{dI_C}{dV_{BE}} \cdot R_C - 1 = 0$$

$$-\frac{dI_C}{dV_{BE}}\left[\frac{R_B+R_C}{\beta}+R_C\right]=1$$

$$-\frac{dI_C}{dV_{BE}}\left[\frac{R_B+R_C+\beta R_C}{\beta}\right]=1$$

$$\Rightarrow \quad \frac{dI_C}{dV_{BE}}=\frac{-\beta}{R_B+(1+\beta)R_C}$$

$$\therefore \quad \boxed{S'=\frac{-\beta}{R_B+(1+\beta)R_C}}$$

iii) stability factor S'' :

we know that the stability factor $S''=\frac{dI_C}{d\beta}$, I_{C_0} and V_{BE} are constant

Differentiating Equation (4) with respect to β, we get

$$0-\frac{\left[\beta\left(\frac{dI_C}{d\beta}-I_{C_0}\right)-\left(I_C-(1+\beta)I_{C_0}\right)\cdot 1\right]}{\beta^2}(R_B+R_C)-R_C\frac{dI_C}{d\beta}-0=0$$

$$-\left[\frac{\beta S''-\cancel{I_{C_0}\beta}-I_C+I_{C_0}+\cancel{I_{C_0}\beta}}{\beta^2}\right](R_B+R_C)-R_C S''=0$$

Neglecting I_{C_0}, as I_{C_0} is a very small value

$$-\left[\frac{(\beta S''-I_C)(R_B+R_C)+R_C S''\beta^2}{\beta^2}\right]=0$$

$$S''\beta\left[\frac{R_B+R_C}{\beta}\right]-I_C(R_B+R_C)+S''R_C\beta^2=0$$

$$S''\beta\left[R_B+R_C+\beta R_C\right]=I_C(R_B+R_C)$$

$$\therefore \quad S''=\frac{I_C(R_B+R_C)}{\beta\left(R_B+(1+\beta)R_C\right)}$$

Since $I_B = \frac{I_c}{\beta}$

$$\therefore \quad \boxed{S'' = \frac{I_B (R_B + R_c)}{R_B + (1+\beta) R_c}}$$

Advantages of Collector to base bias :

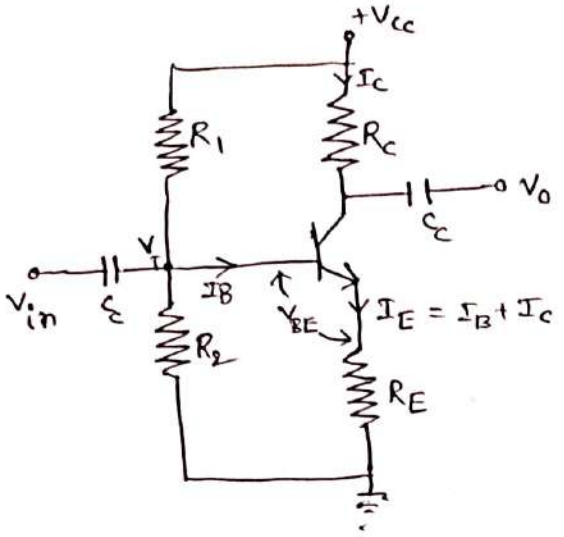
1) circuit is simple
2) Less number of components are required.
3) Stability factor is better compared to fixed bias
4) Increase in I_c due to increase in temperature & large β -value gets compensated as the drop across R_c is increased and V_{CE} is decreased due to which I_B is decreased and I_c is also decreased.

Disadvantages of Collector to base bias :

1) The stability factor $S = \frac{1+\beta}{1+\beta\left(\frac{R_c}{R_B+R_c}\right)}$, if R_c is very small compared to R_B then $S = 1+\beta$, which is nothing but the stability factor of fixed bias.
2) Collector to base biasing is not suitable for the amplifier circuits like transformer coupled amplifier.

3) Selb bias (or) Emitter bias (or) Voltage (potential) divider bias :

Selb biasing circuit is a simple circuit used to establish a stable operating point. The selb biasing circuit and it's thevenin's equivalent circuit are as shown in below.



fig(a) selb bias circuit

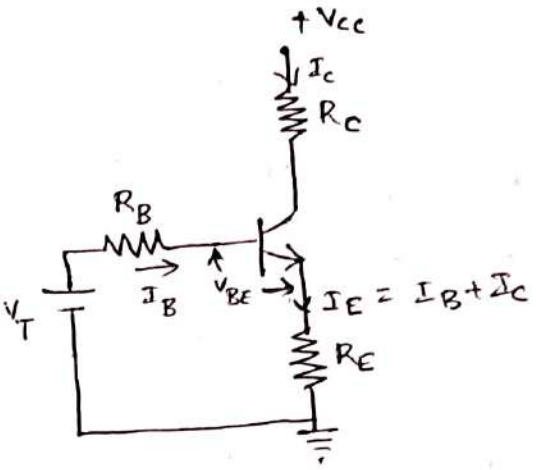


fig (b) : Thevenin's equivalent circuit.

The current in emitter resistor R_E causes a voltage drop which makes the emitter base junction to be reverse biased. But, to remain in the active region, the emitter base junction has to be forward biased. The required base bias is obtained from the power supply through the potential divider network of the resistances R_1 and R_2.

If I_c tends to increase, say due to increase in I_{co} with temperature, the current in I_E increases. Hence the voltage drop across R_E increases, which causes the base current I_B to be decreased, due to which I_c is also decreased. Thus the collector current I_c is maintained almost constant.

i) Stability factor (S) :

The thevenin's equivalent voltage $V_T = \frac{V_{cc} R_2}{R_1 + R_2}$

The base resistance $R_B = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$.

Applying KVL to the input circuit of figure (b) we get

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$\Rightarrow \quad V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$V_T = I_B (R_B + R_E) + V_{BE} + I_C R_E \longrightarrow (1)$$

Differentiating the above equation with respect to I_C we get

$$0 = \frac{dI_B}{dI_C} (R_B + R_E) + 0 + (1) R_E$$

$$\Rightarrow \quad \frac{dI_B}{dI_C} = -\frac{R_E}{R_B + R_E} \longrightarrow (2)$$

we know that stability factor $S = \dfrac{1+\beta}{1 - \beta \dfrac{dI_B}{dI_C}}$

substituting the equation (2) in the above equation we get

$$\boxed{S = \frac{1+\beta}{1 + \beta \dfrac{R_E}{R_B + R_E}}}$$

ii) Stability factor (S'):

we know that the stability factor $S' = \dfrac{dI_C}{dV_{BE}}$, I_{C_0} and β are constant.

we know that $I_C = \beta I_B + (1+\beta) I_{C_0}$.

$$\Rightarrow \quad I_B = \frac{I_C - (1+\beta) I_{C_0}}{\beta} \longrightarrow (3)$$

Substituting the above equation in equation (1) we get

$$V_T = \frac{\left[I_C - (1+\beta) I_{C_0}\right]}{\beta} (R_B + R_E) + V_{BE} + I_C R_E \longrightarrow (4)$$

Differentiating the above equation (4) with respect to V_{BE}, we get

$$0 = \left(\frac{R_B + R_E}{\beta}\right) \left[\frac{dI_C}{dV_{BE}} - 0\right] + 1 + \frac{dI_C}{dV_{BE}} R_E$$

$$\Rightarrow \quad 0 = \frac{dI_C}{dV_{BE}} \left[\frac{R_B + R_E}{\beta} + R_E\right] + 1$$

$$\Rightarrow \quad \frac{dI_c}{dV_{BE}} \left[\frac{R_B + R_E + \beta R_E}{\beta} \right] = -1$$

$$\Rightarrow \quad \frac{dI_c}{dV_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_E}$$

$$\therefore \quad \boxed{S' = \frac{-\beta}{R_B + (1+\beta) R_E}}$$

iii) Stability factor (S'') :

We know that the stability factor $S'' = \frac{\partial I_c}{\partial \beta}$, I_{C_0} and V_{BE} are constant

Differentiating the equation (4) with respect to 'β' we get

$$0 = \frac{\left[\beta \left(\frac{dI_c}{d\beta} - 1 \cdot I_{C_0} \right) - \left(I_C - (1+\beta) I_{C_0} \right) \cdot 1 \right] (R_B + R_E)}{\beta^2} + 0 + \frac{dI_c}{d\beta} \cdot R_E$$

$$\Rightarrow \quad 0 = \frac{\left[\beta \left(S'' - I_{C_0} \right) - I_C + I_{C_0} + \beta I_{C_0} \right] (R_B + R_E)}{\beta^2} + S'' R_E$$

$$\Rightarrow \quad 0 = \frac{\left(\beta S'' - \cancel{\beta I_{C_0}} - I_C + I_{C_0} + \cancel{\beta I_{C_0}} \right) (R_B + R_E)}{\beta^2} + S'' R_E \beta^2$$

Neglecting I_{C_0} we get

$$\Rightarrow \quad 0 = \left(\beta S'' - I_C \right) \cdot \left(R_B + R_E \right) + S'' R_E \beta^2$$

$$\Rightarrow \quad S'' \beta \left(R_B + R_E + \beta R_E \right) - I_C \left(R_B + R_E \right) = 0$$

$$\Rightarrow \quad S'' \beta \left(R_B + (1+\beta) R_E \right) = I_C \left(R_B + R_E \right)$$

$$\Rightarrow \quad S'' = \frac{I_C (R_B + R_E)}{\beta \left(R_B + (1+\beta) R_E \right)} = \frac{I_B (R_B + R_E)}{R_B + (1+\beta) R_E}$$

$$\therefore \quad \boxed{S'' = \frac{I_B (R_B + R_E)}{R_B + (1+\beta) R_E}} \quad (\text{or}) \quad S'' = \frac{S I_C}{\beta (1+\beta)} = \frac{S I_B}{1+\beta}$$

Advantages of Self biasing circuits:

1) If R_E is very high, then the stability factor $S \simeq 1$

2) stability factor is independent of R_c.

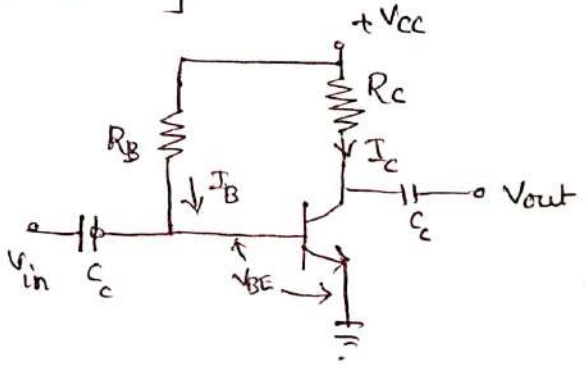
3) High stability when compared to fixed bias and collector to base bias.

Draw back:

More components are required.

Problems:

1) In the fixed bias method as shown in below figure, A silicon transistor with $\beta = 100$ is used, $V_{cc} = 6V$, $R_c = 3k\Omega$, $R_B = 530k\Omega$. Draw the DC load line and determine the operating point. Also find the stability factor (S).



Sol) i) DC load line:

Applying KVL to the output circuit, we get

$$V_{cc} - I_c R_c - V_{CE} = 0 \quad \rightarrow (1)$$

Put $I_c = 0$ to get V_{CE} max.

Then $V_{CE\,max} = V_{cc} = 6V$

$\therefore$ Point B on V_{CE} - axis is $= B(6V, 0)$

put $V_{CE} = 0$ to get I_c max in equation (1),

$$\text{Then } I_{c\,max} = \frac{V_{cc}}{R_c} = \frac{6}{3\times10^3} = 2mA$$

$\therefore$ Point A on I_c - axis is $= A(0, 2mA)$

The DC load line is drawn by joining the points A and B.

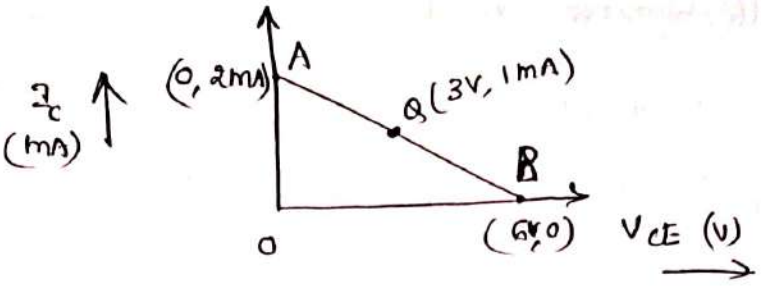


fig: DC load line

ii) operating point :

Applying KVL to the input circuit we get

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$6 - I_B (530 \times 10^3) - 0.7 = 0$$

$$\Rightarrow I_B = \frac{5.3}{530 \times 10^3} = 10\mu A$$

(∵ given transistor is a silicon transistor. So $V_{BE} = 0.7V$)

we know that $I_C = \beta I_B = 100 \times 10 \times 10^{-6} = 1mA$

Applying KVL to the output circuit we get

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$6 - (1 \times 10^{-3} \times 3 \times 10^3) - V_{CE} = 0$$

$$\therefore V_{CE} = 3V$$

$\therefore$ operating point $(V_{CEQ}, I_{CQ}) = (3V, 1mA)$

iii) stability factor $S = 1 + \beta$ (for fixed bias)

$$= 1 + 100$$

$$\therefore S = 101.$$

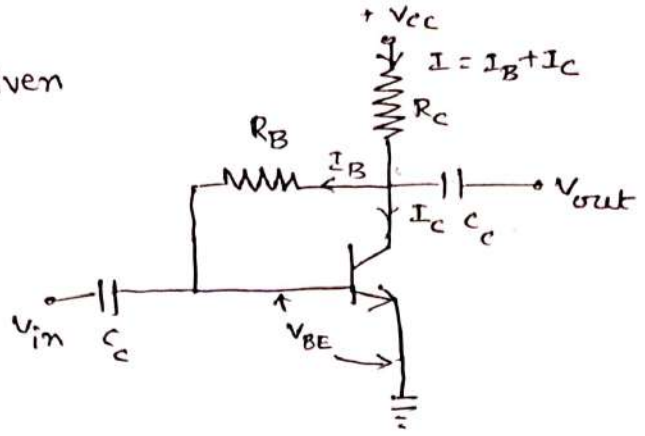
2) In the biasing with feedback resistor method, a silicon - transistor with feed back resistor is used. The operating point is at (7V, 1mA) and $V_{CC} = 12V$. Assume $\beta = 100$.

a) Determine the value of R_B b) calculate the stability factor.

c) what will be the new operating point if $\beta = 50$ with all the circuit values are same.

Sol)

Given



$\beta = 100$, $V_{CC} = 12V$, $Q = (7V, 1mA)$ i.e $V_{CEQ} = 7V$

$I_{CQ} = 1mA$

$I_C = 1mA$

$$I_B = \frac{I_C}{\beta} = \frac{1mA}{100} = 10\mu A.$$

$$I_B + I_C = 10\times10^{-6} + 1\times10^{-3} = 1.01\ mA$$

Applying KVL to the output circuit

$$V_{CC} - (I_B + I_C)R_C - V_{CE} = 0$$

$$12 - (1.01\times10^{-3})R_C - 7 = 0$$

$$\Rightarrow \quad R_C = \frac{5}{1.01\times10^{-3}} = 4.9504\ K\Omega$$

a) R_B :

Applying KVL to the input circuit

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0$$

$$12 - (1.01\times10^{-3}\times 4.9504\times10^{3}) - 10\times10^{-6}\times R_B - 0.7 = 0$$

$$\Rightarrow \quad 10^{-5} R_B = 6.3$$

$$R_B = 6.3\times10^{5} = 630\ K\Omega$$

b) Stability factor (S) :

For Feedback resistor biasing $S = \dfrac{1+\beta}{1+\beta\dfrac{R_C}{R_B+R_C}} = \dfrac{1+100}{1+100\dfrac{4.9504\times10^{3}}{(630+4.9504)\times10^{3}}}$

$$\Rightarrow \quad S = 56.7546$$

c) New operating point if $\beta = 50$:

Applying KVL to the input circuit, we get

$$V_{cc} - (I_c + I_B) R_c - I_B R_B - V_{BE} = 0$$

$$12 - (\beta I_B + I_B)(4.9504 \times 10^3) - I_B \times 630 \times 10^3 - 0.7 = 0$$

$$11.3 - I_B (\beta + 1)(4.9504 \times 10^3) - I_B \times 630 \times 10^3 = 0$$

$$11.3 - I_B (50+1)(4.9504 \times 10^3) - I_B\, 630 \times 10^3 = 0$$

$$11.3 - I_B [8.8247 \times 10^5]$$

$$\Rightarrow I_B = 12.805\ \mu A$$

$$\therefore I_C = \beta I_B = 50 \times 12.805 \times 10^{-6} = 0.64025\ mA$$

$$I_C + I_B = 0.64025 \times 10^{-3} + 12.805 \times 10^{-6} = 0.6530555\ mA$$

Applying KVL to the output circuit

$$V_{cc} - (I_c + I_B) R_c - V_{CE} = 0$$

$$12 - 0.6530555 \times 10^{-3} \times 4.9504 \times 10^3 - V_{CE} = 0$$

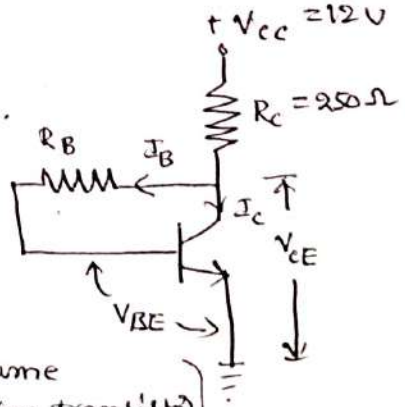
$$\therefore V_{CE} = 8.76711\ V.$$

$\therefore$ New operating point $(V_{CE}, I_c) = (8.76711\ V,\ 0.6530\ mA)$

3) In a collector to base CE amplifier circuit having $V_{cc} = 12V$, $R_c = 250\ \Omega$, $I_B = 0.25mA$, $\beta = 100$ and $V_{CEQ} = 8V$. Calculate R_B and stability factor.

Sol)

Given $V_{CEQ} = 8V$, $R_c = 250\Omega$, $I_B = 0.25mA$. $\beta = 100$.



From the circuit

$$V_{CE} = I_B R_B + V_{BE}$$

$$8 = 0.25 \times 10^{-3} R_B + 0.7V \quad (\because \text{Assume silicon transistor } V_{BE} = 0.7V)$$

$$\Rightarrow R_B = 29.2\ k\Omega$$

The stability factor $S = \dfrac{1+\beta}{1+\beta \dfrac{R_c}{R_c + R_B}} = \dfrac{1+100}{1+100 \dfrac{250}{(250+29200)}} = 54.627$

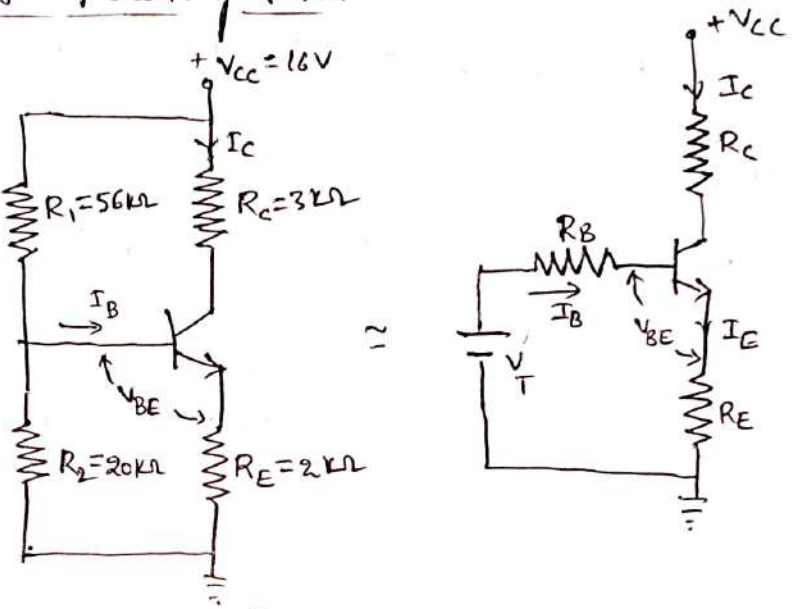
4) A CE Germanium transistor amplifier circuit has been provided by Self bias. i.e emitter resistor and potential divider arrangement. The various parameters are $V_{CC} = 16V$, $R_C = 3K\Omega$, $R_E = 2K\Omega$, $R_1 = 56K\Omega$, $R_2 = 20K\Omega$ and $\alpha = 0.985$ Determine a) The co-ordinates of the operating Point b) Stability factor (S).

Sol) For Ge transistor, $V_{BE} = 0.3V$, $V_{CC} = 16V$, $R_C = 3K\Omega$, $R_E = 2K\Omega$,

Given $\alpha = 0.985$, $\Rightarrow \beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1-0.985} = 65.66667$

a) Co-ordinates of operating point :

Given Self bias.



$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{12 \times 20 \times 10^3}{(56 \times 10^3) + (20 \times 10^3)} = 4.2105V$$

$$R_B = R_1 \| R_2 = \frac{56 \times 10^3 \times 20 \times 10^3}{(56 \times 10^3) + (20 \times 10^3)} = 14.7368\ K\Omega$$

Applying KVL to the input circuit of thevenin's equivalent circuit

$$V_T - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_T - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_T - I_B R_B - V_{BE} - (I_B + \beta I_B) R_E = 0$$

$$V_T - I_B (R_B + (1+\beta) R_E) - V_{BE} = 0$$

$$\Rightarrow I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta) R_E} = \frac{4.2105 - 0.3}{[14.7368 + (1+65.6666)2]10^3}$$

$I_B = 26.41\ \mu A$

$\therefore I_c = \beta I_B = 65.6667 \times 26.41 \times 10^{-6} = 1.7342\ mA$

$I_E = I_B + I_c = 26.41 \times 10^{-6} + 1.7342 \times 10^{-3} = 1.76061\ mA$

Applying KVL to the output circuit of thevenin's equivalent circuit we get $V_{CC} - I_c R_c - V_{CE} - I_E R_E = 0$

$16 - 1.7342 \times 10^{-3} \times 3 \times 10^3 - V_{CE} - 1.76061 \times 10^{-3} \times 2 \times 10^3 = 0$

$\Rightarrow V_{CE} = 7.27618\ V.$

$\therefore$ Co-ordinates of operating point $(V_{CE}, I_c) = (7.27618\ V, 1.7342\ mA)$

b) <u>stability factor</u> (S) :

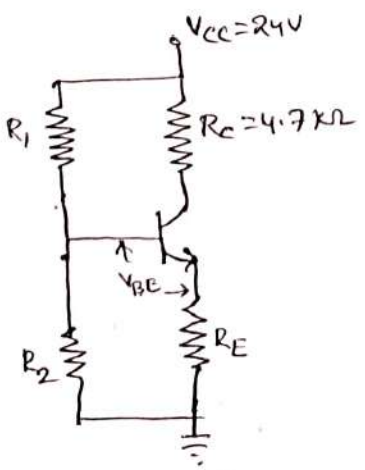
For self bias circuit stability factor $S = \dfrac{1+\beta}{1+\beta \dfrac{R_E}{R_B + R_E}}$

$\Rightarrow S = \dfrac{1+65.66667}{1+65.66667 \times \dfrac{2 \times 10^3}{(14.7368+2) \times 10^3}}$

$S = 7.5355$

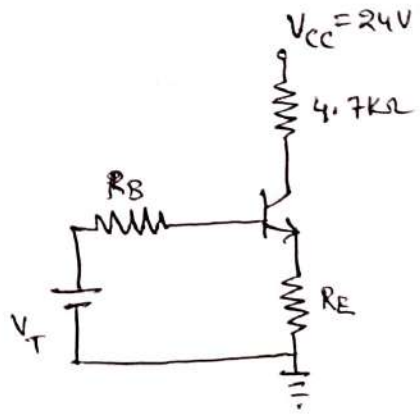
5) A C.E transistor amplifier with voltage divider bias circuit of quiescent point at $V_{CE} = 12V$, $I_c = 2mA$, and stability factor ≤ 5.1. If $V_{CC} = 24V$, $V_{BE} = 0.7V$, $\beta = 50$ and $R_c = 4.7\ k\Omega$. Determine the values of resistors R_E, R_1 and R_2.

Sol)



self bias circuit

$\simeq$



Thevenin's equivalent ckt

a) R_E :

Applying KVL to the output circuit of thevenin's equivalent ckt

$$V_{cc} - I_c R_c - V_{CE} - I_E R_E = 0 \quad \rightarrow (1)$$

Given $I_c = 2mA$, $I_E = I_B + I_C = \frac{I_c}{\beta} + I_c = \frac{2\times10^{-3}}{50} + 2\times10^{-3}$

$$\Rightarrow \quad I_E = 2.04mA$$

$\therefore$ From eq (1), on substituting values

$$24 - 2\times10^{-3}\times4.7\times10^{3} - 12 - 2.04\times10^{-3} R_E = 0$$

$$R_E = 1.27451\ k\Omega$$

b) R_1 and R_2 :

Given stability factor $S \leq 5.1$

we know that $S = \frac{1+\beta}{1+\beta\frac{R_E}{R_B+R_E}}$ for self bias

$$5.1 = \frac{1+50}{1+50\times\frac{1.27451}{R_B+(1.27451\times10^{3})}}$$

$$\Rightarrow \quad 5.1\left[1+\frac{63.7255\times10^{3}}{R_B+(1.27451\times10^{3})}\right] = 51$$

$$\Rightarrow \quad \frac{63.7255\times10^{3}}{R_B+(1.27451\times10^{3})} = 9$$

$$\Rightarrow \quad 9R_B + 11.47705\times10^{3} = 63.7255\times10^{3}$$

$$R_B = 5.806\ k\Omega$$

For a good voltage divider circuit $R_2 = 0.1\beta R_E$

$$\therefore R_2 = 0.1\times50\times1.27451\times10^{3}$$

$$R_2 = 6.3725\ k\Omega$$

$$R_B = \frac{R_1 R_2}{R_1+R_2} \Rightarrow 5.806\times10^{3} = \frac{R_1\times6.3725\times10^{3}}{R_1+(6.3725\times10^{3})}$$

$$\Rightarrow R_1 = 65.311\ k\Omega$$

(6) Given a voltage divider bias circuit. Determine Q-point. Let R_1 value is 56kΩ, $R_2 = 12.2kΩ$, $R_C = 2kΩ$, $R_E = 400Ω$, $V_{CC} = 10V$, $V_{BE} = 0.7V$ and $\beta = 150$.

sol)

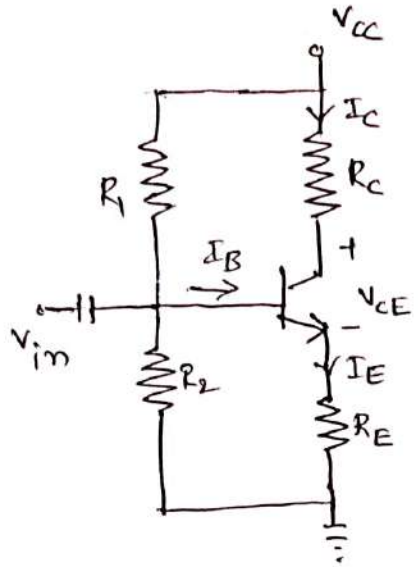
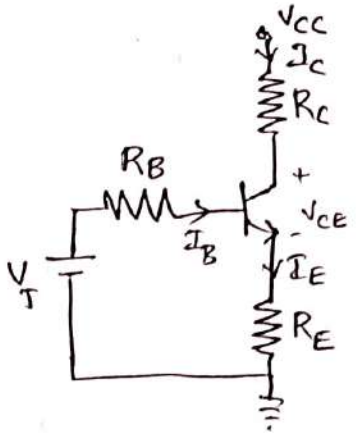


fig: Voltage divider bias

$\simeq$



Thevenin's equivalent circuit

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{56\times10^3 \times 12.2\times10^3}{(56+12.2)10^3} = 10.017\ k\Omega$$

$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{10 \times 12.2\times10^3}{(56+12.2)10^3} = 1.78885\ V, \quad R_B = 10.017\ k\Omega$$

Applying KVL to the input circuit of thevenin's equivalent circuit we get

$$V_T - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_T - I_B R_B - V_{BE} - \left(\frac{I_C}{} + I_B\right) R_E = 0$$

$$V_T - I_B R_B - V_{BE} - (\beta I_B + I_B) R_E = 0$$

$$V_T - I_B R_B - V_{BE} - I_B(\beta+1) R_E = 0$$

$$\Rightarrow I_B \left[R_B + (\beta+1)R_E\right] = V_T - V_{BE}$$

$$\Rightarrow I_B = \frac{V_T - V_{BE}}{R_B + (\beta+1)R_E} = \frac{1.78885 - 0.7}{10.017\times10^3 + (150+1)\,400}$$

$$\Rightarrow I_B = 15.46289\,\mu A$$

$$\therefore I_C = \beta I_B = 150 \times 15.46289\times10^{-6} = 2.3194\ mA$$

$$I_E = I_B + I_C = 15.46289\times10^{-6} + 2.3194\times10^{-3} = 2.33486\ mA$$

Applying KVL to the output circuit of thevenin's equivalent ckt

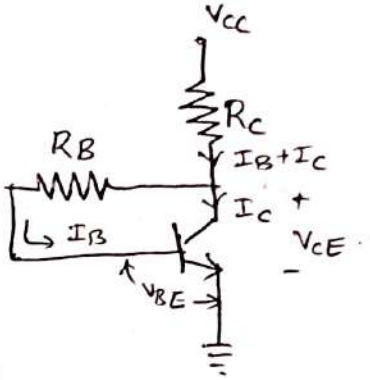
we get $V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$10 - 2.3194\times10^{-3} \times 2\times10^{3} - V_{CE} - 2.33486\times10^{-3}\times400 = 0$

$\Rightarrow V_{CE} = 4.4272V$.

$\therefore$ operating point $(V_{CE}, I_C) = (4.4272V,\ 2.3194mA)$

(7) An npn transistor if $\beta = 50$ is used in CE amplifier with $V_{CC}=10V$ and $R_C = 2K\Omega$, the bias is obtained by connecting $100K\Omega$ resistor from collector to base. Find the quiescent point and stability factor.



Sol) Given $\beta = 50$, $V_{CC} = 10V$, $R_C = 2K\Omega$

$R_B = 100K\Omega$, Assume $V_{BE} = 0.7V$

Applying KVL to the input circuit

we get, $V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$

$V_{CC} - (I_B + \beta I_B) R_C - I_B R_B - V_{BE} = 0$

$\Rightarrow I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C} = \dfrac{10 - 0.7}{[100 + (1+50)2]10^3}$

$\therefore I_B = 46.0396\,\mu A$

$I_C = \beta I_B = 50 \times 46.0396\times10^{-6} = 2.3019\ mA$

$I_B + I_C = 46.0396\times10^{-6} + 2.3019\times10^{-3} = 2.3479\ mA$

Applying KVL to the o/p circuit we get

$V_{CC} - (I_B + R_C) R_C - V_{CE} = 0$

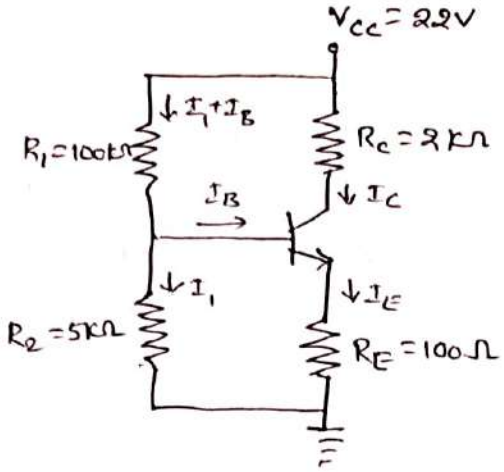
$10 - 2.3479\times10^{-3} \times 2\times10^{3} - V_{CE} = 0$

$V_{CE} = 5.3042V$.

$\therefore$ Quiescent point $(V_{CE}, I_C) = (5.3042V,\ 2.3019mA)$

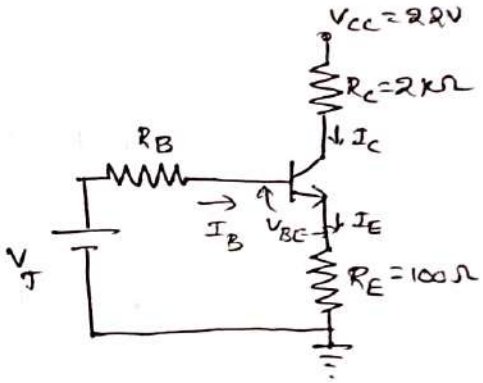
Stability factor $S = \dfrac{1+\beta}{1+\beta\left(\dfrac{R_C}{R_B + R_C}\right)} = \dfrac{1+50}{1+50\,\dfrac{2\times10^3}{(100+2)10^3}} = 25.75$

8) For the circuit shown below $V_{cc} = 22V$, $R_c = 2K\Omega$, $\beta = 60$, $V_{BE} = 0.6V$ $R_1 = 100K\Omega$, Calculate I_B, V_{CE}, I_c and Stability factor S.



Sol)

The thevenin equivalent circuit for the given circuit is



$$V_T = \frac{V_{cc} R_2}{R_1 + R_2}$$

$$V_T = \frac{22 \times 5 \times 10^3}{100 \times 10^3 + 5 \times 10^3} = 1.047619\,V$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 10^3 \times 5 \times 10^3}{100 \times 10^3 + 5 \times 10^3}$$

$$R_B = 4.7619\,K\Omega$$

Applying KVL to the input circuit of thevenin's equivalent ckt we get

$$V_T - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_T - I_B R_B - V_{BE} - (I_B + I_c) R_E = 0$$

$$V_T - I_B R_B - V_{BE} - (I_B + \beta I_B) R_E = 0$$

$$\Rightarrow I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta) R_E} = \frac{1.047619 - 0.6}{4.7619 \times 10^3 + (1+60)\,100}$$

$$\Rightarrow I_B = 41.2\,\mu A$$

$$\therefore I_c = \beta I_B = 60 \times 41.2 \times 10^{-6} = 2.4726\,mA$$

$$I_E = I_B + I_c = 41.2 \times 10^{-6} + 2.4726 \times 10^{-3} = 2.5138\,mA$$

Applying KVL to the output circuit of thevenin's equivalent circuit we get $V_{cc} - I_c R_c - V_{CE} - I_E R_E = 0$

$$\Rightarrow 22 - 2.4726\times10^{-3}\times 2\times10^{3} - V_{CE} - 2.5138\times10^{-3}\times 100 = 0$$

$$\Rightarrow V_{CE} = 16.8034\ V$$

Stability factor $S = \dfrac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_E+R_B}\right)} = \dfrac{1+60}{1+60\times\dfrac{100}{100+(4.7619\times10^{3})}}$

$$\Rightarrow S = 27.304$$

9) For a self bias circuit $V_{cc} = 20V$, $R_C = 2K\Omega$, $\beta = 50$, $R_1 = 100K\Omega$ $R_2 = 10K\Omega$, $R_E = 100\Omega$. Calculate the stability factor (S). Assume $V_{BE} = 0.2V$.

Sol). Given $V_{cc} = 20V$, $R_C = 2K\Omega$, $\beta = 50$

$R_1 = 100K\Omega$ $R_2 = 10K\Omega$

$R_E = 100\Omega$.

We know that the stability factor (S) for self bias ckt is

$$S = \frac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_E+R_B}\right)} \rightarrow (1)$$

where $R_B = R_1 \| R_2 = \dfrac{100\times10^{3}\times10\times10^{3}}{100\times10^{3}+10\times10^{3}} = 9.0909K\Omega$

$\therefore R_B = 9.0909K\Omega$. substituting values in eq (1)

$$\therefore S = \frac{1+50}{1+50\left(\dfrac{100}{100+9.0909K\Omega}\right)}$$

$$= \frac{51}{1.54401}$$

$$S = 33.0308$$

$\therefore$ The stability factor $S \simeq 33$

Bias Compensation Techniques:

The change in temperature may cause a change in the parameters like I_{C_0}, β and V_{BE} which causes the collector current I_C to be changed. There are some techniques which are used to compensate the variations in collector current I_C. They are

1. Diode Compensation
2. Thermistor Compensation
3. Sensistor Compensation.

1. Diode Compensation:

The following figure shows the transistor amplifier with a diode 'D' connected between the base and emitter terminals of the transistor such that it is reversebiased by the base to emitter voltage V_{BE}. Hence the diode 'D' allows a small reverse saturation current I_o to flow through it.

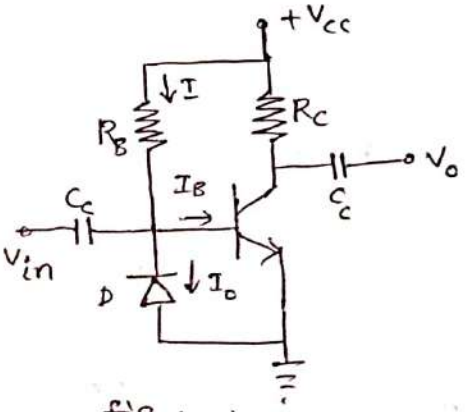


fig: Diode bias Compensation.

From the figure $I_B = I - I_o$

In this method, the diode 'D' is made of the same material with which the transistor is made.

As long as the temperature is constant the diode operates as a resistor.

When the temperature increases the reverse saturation current I_{C_0} increases, due to which I_C increases.

The increase in temperature will also cause the reverse saturation current of the diode i.e I_o to increase. This causes I_B to decrease, because $I_B = I - I_o$. The decrease in I_B causes I_C to decrease.

Hence collector current variations are compensated to keep I_C constant.

NOTE: In this method, as both the diode and transistor are made of the same material both I_o and I_{C_0} changes equally according to the change in temperature.

2) Thermistor Compensation :

* A thermistor is a negative temperature coefficient device. The resistance of thermistor decreases exponentially with increase in temperature.

* In thermistor compensation technique, the thermistor is connected in parallel to the resistor R_2 as shown in figure below.

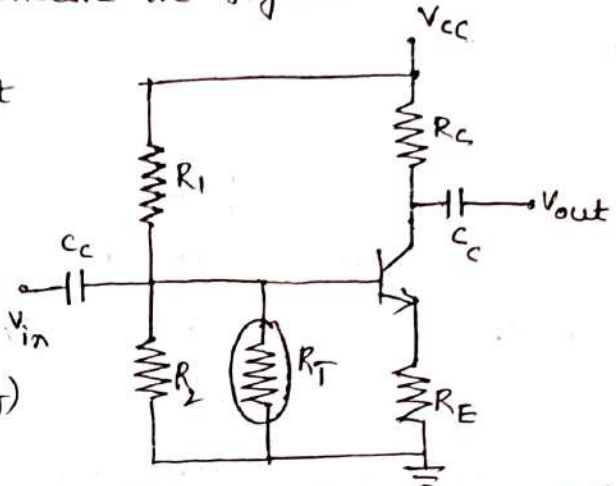


fig: Thermistor compensation

* When the temperature increases, that may cause a change in the parameters such as I_{C_0}, V_{BE} and β. Due to this the collector current I_c increases.

* At the same time the resistance (R_T) of the thermistor decreases with the increase in temperature due to which the voltage drop across the thermistor decreases. This causes the base current I_B to be decreased due to which the collector current I_c is also decreased. Hence the variations in the collector current are compensated to keep I_c constant.

3) Sensistor Compensation :

* A sensistor is a positive temperature coefficient device. The resistance of sensistor increases exponentially with the increase in temperature.

* In sensistor compensation technique, the sensistor is connected in parallel to R_1 resistor as shown in figure below.

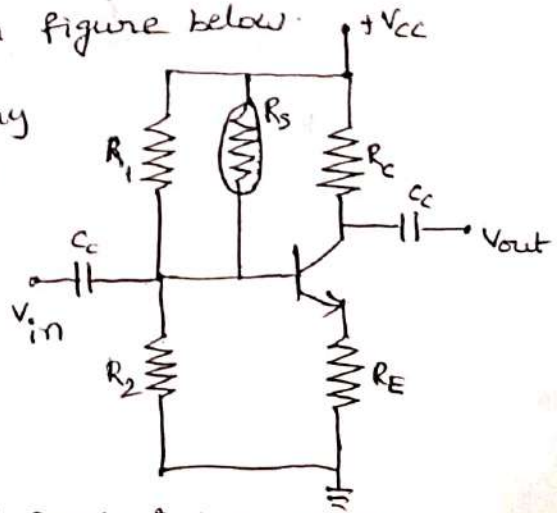


fig: sensistor Compensation.

* When the temperature increases, that may cause a change in the parameters such as I_{C_0}, V_{BE} and β. Due to this the collector current I_c increases.

* At the same time the resistance 'R_S' of the sensistor increases with the increase in temperature. Hence the equivalent -

-resistance of $R_1 \| R_2$ also increases due to which the voltage drop across it increases. This causes decrease in V_{BE}, due to which I_B gets decreased, thereby decreasing I_C. Hence the variations in Collector Current I_C are compensated to keep I_C Constant.

Thermal run away and thermal stability:

Thermal run away:

The Collector current for Common Emitter amplifier is expressed by

$$I_C = \beta I_B + I_{CE_0} = \beta I_B + (1+\beta) I_{C_0}.$$

The three variables β, I_B and I_{C_0} in the equation, increase with the rise in temperature. In particular, the reverse saturation current I_{C_0} changes significantly with temperature. I_{C_0} doubles for every 10°C rise in temperature. when I_{C_0} increases, I_C increases. This causes the power dissipation at collector - base junction to be increased, due to which the collector base junction temperature is increased. This inturn increases I_{C_0}, as a result I_C will increase still further, which will further rise the temperature at the collector base junction. This process is cumulative and leads to Thermal run away that will destroy the transistor.

NOTE:

1) The Collector is normally made larger in size than the emitter region in order to help the dissipation of heat developed at the collector - base junction.

2) In power transistors, the heat developed at the collector junction may be removed using heat sink.

Thermal resistance (Θ) :

* Consider a transistor used in a circuit where the ambient temperature of the air around the transistor is $T_A^\circ C$ and the temperature of the collector-base junction is $T_J^\circ C$. Due to the heat with in the transistor T_J is greater than T_A.

* As the temperature difference $T_J - T_A$ is greater, the power dissipated in the transistor P_D will also be greater.

i.e $T_J - T_A \propto P_D$.

$\Rightarrow T_J - T_A = \Theta P_D$, where '$\Theta$' is the proportionality constant called as thermal resistance.

* Thermal resistance is given by $\Theta = \dfrac{T_J - T_A}{P_D}$.

Hence Θ is measured in $^\circ C/W$.

* The thermal resistance Θ some times referred as Θ_{J-A}, i.e the thermal resistance from junction to the ambient temperature.

* The thermal resistance from junction to ambience is considered to be two parts.

$$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A}$$

Θ_{J-C} = Thermal resistance from junction to case. Here case is nothing but the equipment in which the transistor is present.

Θ_{C-A} = Thermal resistance from case to ambience.

* The heat sink is a relatively large heat conducting device which is placed closer to the transistor case. The thermal resistance from heat sink to ambience is Θ_{HS-A}. Larger the heat sink smaller the value for Θ_{HS-A}.

* Θ_{HS-A} is not added in series with Θ_{C-A} but in parallel to it.

$$\text{i.e} \quad \Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} \parallel \Theta_{HS-A}$$

Problems

1) For a given transistor, the thermal resistance is 8°c/Watts and ambient temperature T_A is 27°c. If the transistor dissipates 3W of power. Calculate the junction temperature.

Sol) we know that $T_J - T_A = \Theta P_D$

$$\Rightarrow T_J = T_A + \Theta P_D = 27 + 8 \times 3 = 51^\circ c$$

2) For a transistor $T_J = 160^\circ c$, $T_A = 40^\circ c$ and $\Theta_{J-A} = 80^\circ c/W$ calculate the power that the transistor can safely dissipate in free air.

Sol) we know that $T_J - T_A = \Theta P_D$

$$\Rightarrow P_D = \frac{T_J - T_A}{\Theta} = \frac{160 - 40}{80} = 1.5 \text{ watts}$$

3) Determine the power dissipation capability of a transistor which has been mounted with a heat sink having thermal resistance $\Theta_{HS-A} = 8^\circ c/W$. $T_A = 40^\circ c$, $T_J = 160^\circ c$, $\Theta_{J-C} = 5^\circ c/W$ and $\Theta_{C-A} = 85^\circ c/W$

Sol) we know that $\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} \parallel \Theta_{HS-A}$

$$\Rightarrow \theta_{J-A} = 5 + (85 \parallel 8) = 5 + \frac{85 \times 8}{85 + 8}$$

$$\therefore \Theta_{J-A} = 5 + 7.311 = 12.31^\circ c/W$$

Power dissipation $P_D = \frac{T_J - T_A}{\Theta_{J-A}} = \frac{160 - 40}{12.31} = 9.75 \text{ Watts}$

Thermal Stability:

To prevent a transistor from thermal run away, the required condition is that the rate at which the heat is released at the collector junction should not exceed the rate at which the heat is dissipated under steady state condition.

conditions for thermal stability:

1) To prevent the transistor from thermal run away the condition is

$$\frac{\partial P_C}{\partial T_J} < \frac{1}{\Theta} \longrightarrow (1)$$

2) The condition to prevent a transistor from thermal run-away can be re written as

$$\left(\frac{\partial P_C}{\partial I_C}\right) \cdot \left(\frac{\partial I_C}{\partial T_J}\right) < \frac{1}{\Theta} \longrightarrow (2)$$

considering a self bias C.E amplifier circuit, the power generated at the collector junction without any input ac signal is

$$P_C = V_{CE} I_C \longrightarrow (3)$$

Applying KVL to the output circuit of self bias we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

If I_B is very small $I_E \simeq I_C$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Multiplying both sides by I_C we get

$$V_{CE} \cdot I_C = \left[V_{CC} - I_C (R_C + R_E)\right] I_C$$

$$\Rightarrow V_{CE} \cdot I_C = V_{CC} I_C - I_C^2 (R_C + R_E)$$

$$\Rightarrow P_C = V_{CC} I_C - I_C^2 (R_C + R_E)$$

Differentiating both sides with respect to I_C

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2 I_C (R_C + R_E) \longrightarrow (4)$$

To avoid thermal run away it is necessary that

$$I_C > \frac{V_{CC}}{2(R_E + R_C)}$$

we know that the stability factor $S = \frac{\partial I_C}{\partial I_{C_0}}$

$$\Rightarrow \quad \partial I_C = S \cdot \partial I_{C_0}.$$

$$\therefore \quad \frac{\partial I_C}{\partial T_J} = S \cdot \frac{\partial I_{C_0}}{\partial T_J} \longrightarrow (5)$$

Since the reverse saturation current increases by 7% per degree centegrade either for Si (or) Ge.

$$\text{i.e} \quad \frac{\partial I_{C_0}}{\partial T_J} = 0.07\, I_{C_0}. \longrightarrow (6)$$

Substituting (6) in (5) we get

$$\frac{\partial I_C}{\partial T_J} = S(0.07\, I_{C_0}) \longrightarrow (7)$$

Substituting equations (4) and (7) in equation (2) we get

$$\left[V_{CC} - 2I_C(R_E + R_C)\right] S(0.07\, I_{C_0}) < \frac{1}{2}$$

3) To avoid thermal run away, a heat sink may be attached to the collector of the power transistor.

FET Biasing Methods and Stabilization :

FET biasing is of two types.

1) JFET biasing
2) MOSFET biasing.

JFET biasing is in turn categorised into three types.

1) Fixed bias circuit for JFET
2) Self bias circuit for JFET
3) Voltage divider bias circuit for JFET.

Amplifier:

An Amplifier is an electronic circuit that increases the amplitude of a given input signal. i.e the amplifier is used to obtain a larger ac signal output from the small given input signal.

In general BJTs and FETs are commonly used as amplifying elements.

The frequency of the amplifier output must be same as that of the frequency of the amplifier input. If we assume the sinusoidal signal as an input of the amplifier, the output should also be a sinusoidal with the same frequency as that of the input signal.

Classification of Amplifiers:

The Amplifiers can be classified in different ways as discussed below.

1) Based on frequency range:
   - i) Audio frequency Amplifiers (20HZ - 20KHZ)
   - ii) Radio frequency Amplifiers (>20KHZ)
   - iii) Video Frequency Amplifiers (5-8 MHz)
   - iv) Very Low Frequency Amplifiers (VLF) (10KHZ - 30KHZ)
   - v) Low Frequency Amplifiers (LF) (30KHZ - 300KHZ)
   - vi) Medium Frequency Amplifiers (300KHZ - 3000KHZ)
   - vii) High Frequency Amplifiers (3MHZ - 30MHZ)
   - viii) Very High Frequency Amplifiers (30MHZ - 300MHZ)
   - ix) Ultra High Frequency Amplifiers (300MHZ - 3000MHZ)
   - x) Super High Frequency Amplifiers (3000MHZ - 30,000MHZ)

2) Based on the method of operation:

i) Class A Amplifier: An amplifier is said to be Class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for full input signal.

For this amplifier the position of the Q-point is approximately at the middle of the dc load line.

ii) Class B amplifier: An amplifier is said to be class B amplifier if the Q-point and input signal are selected such that the output signal is obtained for only one half cycle of the full input cycle.

iii) Class-AB Amplifier: An amplifier is said to be class AB amplifier if the Q-point and the input signal are selected such that the output signal is obtained for more than 180° and less than 360° of the full input cycle.

iv) Class-C Amplifier: An Amplifier is said to be class-c amplifier if the Q-Point and the input signal are selected such that the output signal is obtained for less than half cycle of full input cycle.

3) Based on the method of Coupling:

i) RC Coupled Amplifier: Resistors and Capacitors are used as Coupling Components. They block DC and gives flat response at mid frequencies.

ii) Transformer Coupled Amplifier: Transformer is used as a Coupling Component. It provides impedance matching.

iii) Direct Coupled Amplifier: If the output of the first stage is directly connected to the input of the next stage without using any component, that amplifier is known as direct coupled amplifier It does not block DC signal components.

4) Based on the type of the Load:

i) Resistive Load Amplifier ii) Inductive Load Amplifier

5) Based on the type of the signal being handled:

Based on the level of the signal, signals are two types. They are small signal and large signal. So the amplifiers are categorised as i) Small signal amplifier ii) Large signal Amplifier.

6) Based on the type of application:

i) voltage amplifier: Amplifies voltage of the input signal.

ii) Current amplifier: Amplifies current of the input signal.

iii) power amplifier: Amplifies both voltage and current of the input signal.

iv) Tuned amplifier: Amplifier of this kind is used for impedance matching.

7) Based on the type of active device used:

i) BJT amplifier ii) FET Amplifier

8) Based on the transistor configuration: a) under BJT

i) Common Emitter Amplifier ii) Common Base Amplifier

iii) Common Collector Amplifier.

b) under FET

i) Common source amplifier ii) Common drain amplifier

iii) Common Gate amplifier.

9) According to the number of stages:

i) Single stage Amplifier ii) Multistage Amplifier

Hybrid model (or) h-parameter model for a general two port network:

The h-parameter equations for a general two port network are given as

$$V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

The h-parameter model that satisfies the above two equations can be verified by applying KVL in the input loop and KCL at the output node, for the following figure.

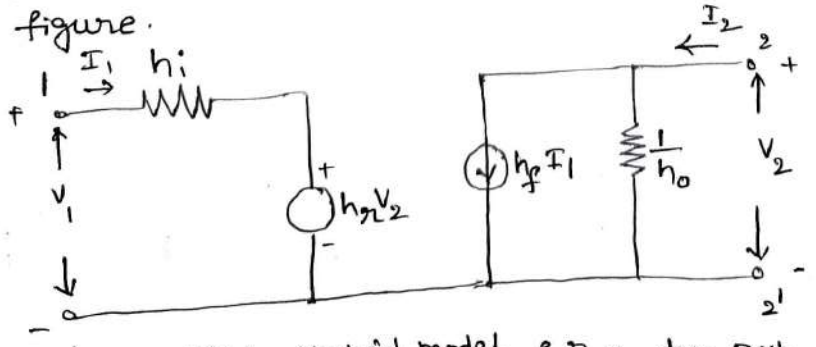


fig: Hybrid model for a two port network.

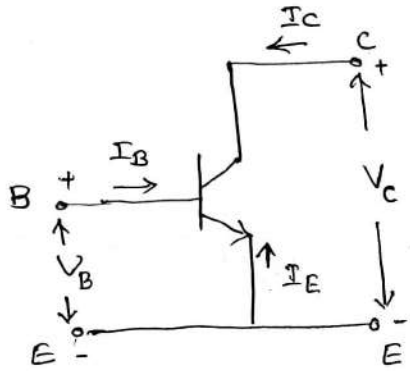
NOTE: Transistor is a type of two port network. So the H-parameter model given in the above figure can be applied for a transistor also. The notations for V_1, I_1 and V_2, I_2 will be changed based on the configuration in which the transistor is connected in. And also h_i, h_r, h_f and h_o notations are changed based on the configurations.

Hybrid model for the transistor in three different Configurations:

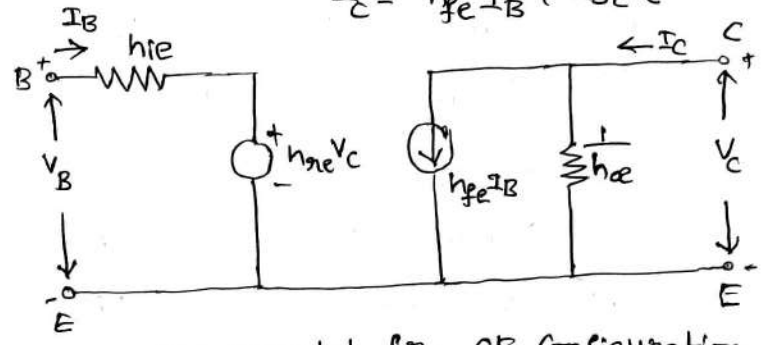
a) Common Emitter Configuration:

For common emitter the H-parameter equations are $V_B = h_{ie} I_B + h_{re} V_C$

$I_C = h_{fe} I_B + h_{oe} V_C$



fig(a) CE configuration

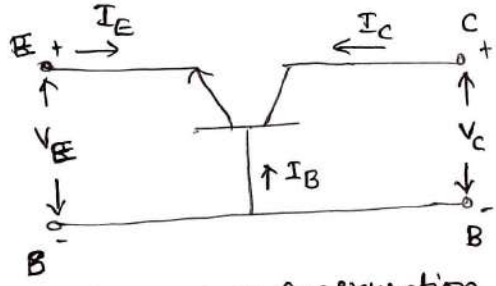


fig(b): Hybrid model for CE configuration

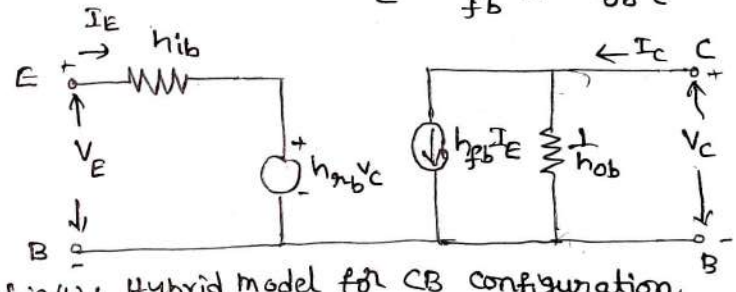
b) Common Base Configuration:

For common base the H-parameter equations are $V_E = h_{ib} I_E + h_{rb} V_C$

$I_C = h_{fb} I_E + h_{ob} V_C$



fig(a) Common base configuration

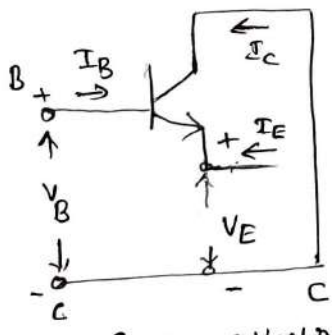


fig(b): Hybrid model for CB configuration.

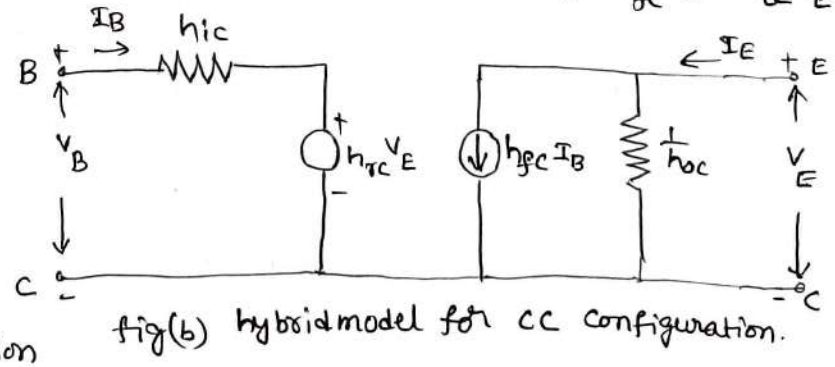
c) Common collector configuration:

For common collector the H-parameter equations are $V_B = h_{ic} I_B + h_{rc} V_E$

$I_E = h_{fc} I_B + h_{oc} V_E$



fig(a) Common collector configuration



fig(b) hybrid model for CC configuration.

Small signal Analysis of a generalized transistor amplifier:

To form a transistor amplifier it is necessary to connect an external load, source of a signal along with proper biasing for transistor network. The transistor can be connected in any one of the three possible configurations.

The basic transistor amplifier and it's generalized h-parameter model are shown in below using exact model.

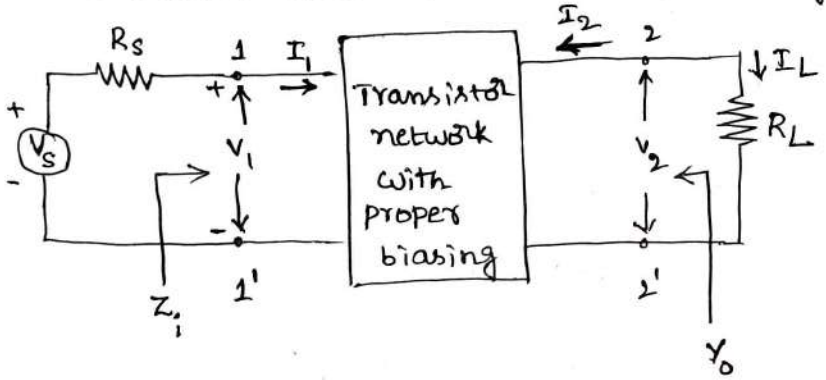


fig: Basic Amplifier using transistor

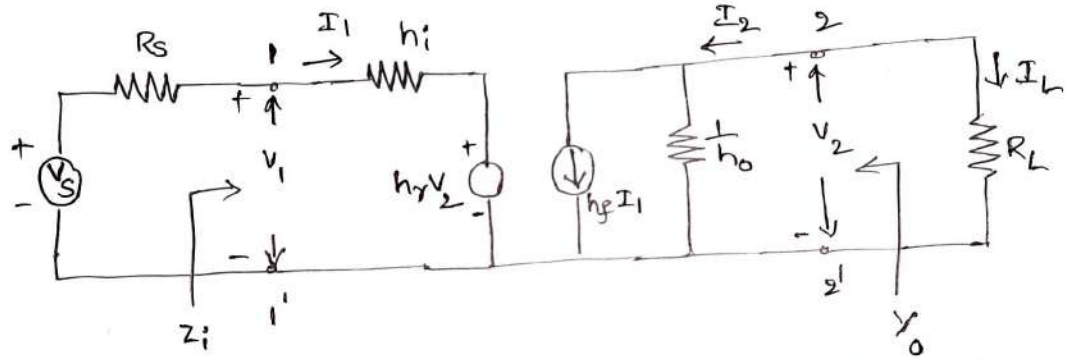


fig: Generalized h-parameter model for a transistor amplifier

To analyse the hybrid model we need to find the parameters such as Current Gain (A_I), Input Impedance (Z_i), Voltage Gain (A_V), output Admittance (Y_o), current Gain with Source (A_{IS}), voltage gain with source (A_{VS}) and power gain. Let us derive them one by one.

Current Gain (A_I):

$$\text{current Gain } (A_I) = \frac{I_L}{I_1} = -\frac{I_2}{I_1} \qquad \left(\because \text{from the figure } I_L = -I_2\right)$$

we know that $I_2 = h_f I_1 + h_o V_2$

$$\Rightarrow I_2 = h_f I_1 + h_o(-I_2 R_L) \qquad \left(\because \text{from figure } V_2 = I_L R_L = -I_2 R_L\right)$$

$$\Rightarrow I_2 (1 + h_o R_L) = h_f I_1$$

$$\Rightarrow \frac{I_2}{I_1} = \frac{h_f}{1+h_o R_L}$$

$$\Rightarrow \frac{-I_2}{I_1} = \frac{-h_f}{1+h_o R_L}$$

$$\therefore \boxed{A_I = \frac{-h_f}{1+h_o R_L}}$$

Input Impedance (Z_i):

Input Impedance $z_i = \frac{V_1}{I_1}$

we know that $V_1 = h_i I_1 + h_r V_2$

$$\Rightarrow V_1 = h_i I_1 + h_r(-I_2 R_L)$$

$$\Rightarrow V_1 = h_i I_1 + h_r(A_I I_1) R_L \qquad \left(\because \frac{-I_2}{I_1} = A_I \Rightarrow -I_2 = A_I I_1\right)$$

$$\Rightarrow V_1 = I_1(h_i + h_r A_I R_L)$$

$$\Rightarrow \frac{V_1}{I_1} = h_i + h_r A_I R_L$$

$$\therefore \boxed{Z_i = h_i + h_r A_I R_L}$$

Replacing $A_I = \frac{-h_f}{1+h_o R_L}$ we get $Z_i = h_i + h_r\left(\frac{-h_f}{1+h_o R_L}\right) R_L$

$$\therefore \boxed{Z_i = h_i - \frac{h_r h_f R_L}{1+h_o R_L}}$$

Voltage Gain (A_V):

Voltage Gain $A_V = \frac{V_2}{V_1}$

$$= \frac{-I_2 R_L}{V_1}$$

$$= \frac{(A_I I_1) R_L}{V_1} \qquad \left(\because A_I = \frac{-I_2}{I_1} \Rightarrow -I_2 = A_I I_1\right)$$

$$\therefore \boxed{A_V = \frac{A_I R_L}{Z_i}} \qquad \left(\because \frac{V_1}{I_1} = Z_i\right)$$

Output Admittance (Y_o):

output admittance $(Y_o) = \frac{I_2}{V_2}$ with $V_s = 0$

we know that $I_2 = h_f I_1 + h_o V_2$

$$\Rightarrow \frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o$$

$$\Rightarrow Y_o = h_f \frac{I_1}{V_2} + h_o \longrightarrow (1)$$

with $V_s = 0$, applying KVL in the input circuit of hybrid model

$$I_1 R_s + I_1 h_i + h_r V_2 = 0$$

$$I_1 (R_s + h_i) = -h_r V_2$$

$$\Rightarrow \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i} \longrightarrow (2)$$

substituting equation (2) in equation (1) we get

$$Y_o = h_f \left(\frac{-h_r}{R_s + h_i}\right) + h_o$$

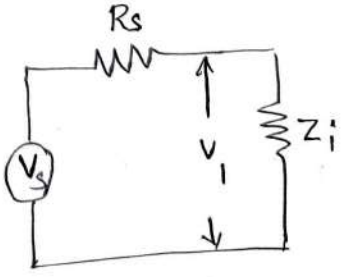
$$\Rightarrow \boxed{Y_o = h_o - \frac{h_f h_r}{R_s + h_i}}$$

and output impedance $Z_o = \frac{1}{Y_o} = \frac{1}{h_o - \frac{h_f h_r}{R_s + h_i}}$

Voltage Gain with source : (A_{VS})

Voltage Gain with source $(A_{VS}) = \frac{V_2}{V_s} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_s}$

$$\Rightarrow A_{VS} = A_V \cdot \frac{V_1}{V_s} \longrightarrow (3)$$



from the figure $V_1 = \frac{V_s Z_i}{R_s + Z_i}$

$$\Rightarrow \frac{V_1}{V_s} = \frac{Z_i}{R_s + Z_i} \longrightarrow (4)$$

substituting equation (4) in equation (3) we get

$$\boxed{A_{VS} = \frac{A_V \cdot Z_i}{R_s + Z_i}}$$

$$A_{VS} = \frac{\left(\frac{A_I R_L}{Z_i}\right) \cdot Z_i}{R_S + Z_i}$$

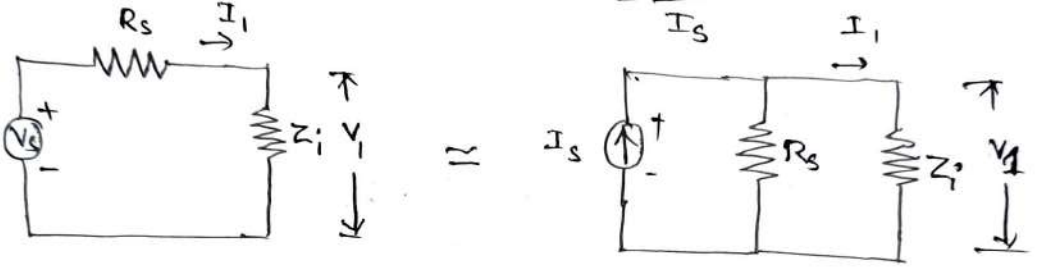
$$\therefore \boxed{A_{VS} = \frac{A_I R_L}{R_S + Z_i}}$$

Current Gain with source (A_{IS}):

Current Gain with source $(A_{IS}) = \frac{I_L}{I_S} = \frac{-I_2}{I_S}$

$$\Rightarrow A_{IS} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_S}$$

$$\Rightarrow A_{IS} = A_I \frac{I_1}{I_S} \longrightarrow (5)$$



From the above figure $I_1 = \frac{I_S \cdot R_S}{R_S + Z_i} \Rightarrow \frac{I_1}{I_S} = \frac{R_S}{R_S + Z_i} \longrightarrow (6)$

substituting equation (6) in equation (5) we get

$$\boxed{A_{IS} = \frac{A_I R_S}{R_S + Z_i}}$$

Power Gain: (A_P)

Power Gain $(A_P) = A_V \cdot A_I = \frac{A_I R_L}{Z_i} \cdot A_I$

$$\therefore \boxed{\text{Power Gain } (A_P) = \frac{A_I^2 R_L}{Z_i}}$$

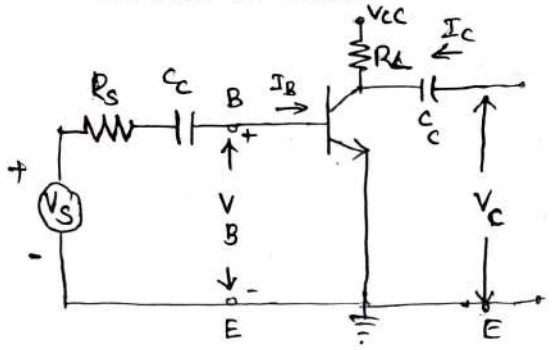
1) $A_I = \frac{-h_f}{1 + h_o R_L}$ 2) $Z_i = h_i + h_r A_I R_L = h_i - \frac{h_r h_f R_L}{1 + h_o R_L}$

3) $A_V = \frac{A_I R_L}{Z_i}$ 4) $Y_o = h_o - \frac{h_r h_f}{R_S + h_i}$ 5) $A_{IS} = \frac{A_I R_S}{R_S + Z_i}$

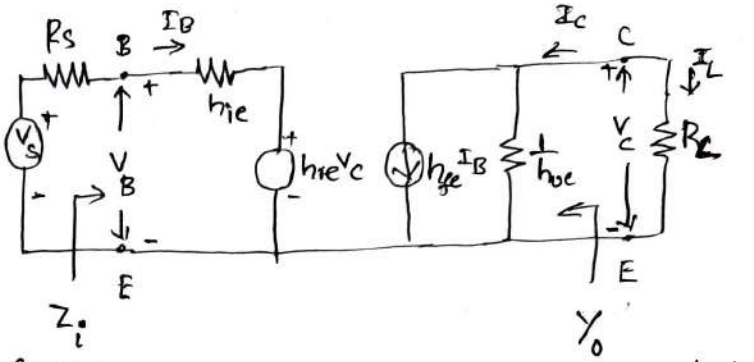
6) $A_{VS} = \frac{A_V Z_i}{R_S + Z_i} = \frac{A_I R_L}{R_S + Z_i}$ 7) $A_P = \frac{A_I^2 R_L}{Z_i}$

Small signal analysis of a Common Emitter Amplifier using exact h-Parameter model:

The Common Emitter Amplifier and it's equivalent h-parameter model are shown in below.



fig(a) CE amplifier



fig(b): CE amplifier h-parameter equivalent model. (Exact model)

To analyse the CE amplifier using h-parameter model, the following parameters are to be derived.

Current Gain (A_I):

Current Gain $A_I = \frac{I_L}{I_B} = \frac{-I_C}{I_B}$

we know that $I_C = h_{fe} I_B + h_{oe} V_C$ $\left(\because V_C = -I_C R_L \text{ From fig}\right)$

$$I_C = h_{fe} I_B + h_{oe}(-I_C R_L)$$

$$\Rightarrow I_C (1 + h_{oe} R_L) = h_{fe} I_B$$

$$\Rightarrow \frac{I_C}{I_B} = \frac{h_{fe}}{1 + h_{oe} R_L}$$

$$\therefore \boxed{A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}}$$

Input impedance: (Z_i)

Input Impedance $(Z_i) = \frac{V_B}{I_B}$

we know that $V_B = h_{ie} I_B + h_{re} V_C$

$$V_B = h_{ie} I_B + h_{re}(-I_C R_L)$$

$$V_B = h_{ie} I_B + h_{re}(A_I I_B) R_L \quad \left(\because \frac{-I_C}{I_B} = A_I\right)$$

$$\therefore \quad V_B = I_B (h_{ie} + h_{re} A_I R_L)$$

$$\Rightarrow \quad \frac{V_B}{I_B} = h_{ie} + h_{re} A_I R_L$$

$$\therefore \quad \boxed{Z_i = h_{ie} + h_{re} A_I R_L}$$

$$\boxed{Z_i = h_{ie} - \frac{h_{re} h_{fe} R_L}{1 + h_{oe} R_L}} \qquad \left(\because A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}\right)$$

Voltage Gain (A_V):

$$\text{Voltage Gain } (A_V) = \frac{V_c}{V_B} = \frac{-I_c R_L}{V_B} \qquad \left(\because \frac{-I_c}{I_B} = A_I\right)$$

$$\Rightarrow \quad A_V = \frac{A_I I_B R_L}{V_B}$$

$$\Rightarrow \quad \boxed{A_V = \frac{A_I R_L}{Z_i}} \qquad \left(\because \frac{V_B}{I_B} = Z_i\right)$$

output Admittance (Y_o):

$$\text{output admittance } (Y_o) = \frac{I_c}{V_c} = \frac{h_{fe} I_B + h_{oe} V_c}{V_c} \qquad \text{with } V_s = 0$$

$$\Rightarrow \quad Y_o = h_{fe} \frac{I_B}{V_c} + h_{oe} \longrightarrow (1)$$

when $V_s = 0$, applying KVL in the input circuit we get

$$I_B R_s + I_B h_{ie} + h_{re} V_c = 0$$

$$\Rightarrow \quad I_B (R_s + h_{ie}) = -h_{re} V_c$$

$$\Rightarrow \quad \frac{I_B}{V_c} = \frac{-h_{re}}{R_s + h_{ie}} \longrightarrow (2)$$

Substituting equation (2) in equation (1) we get

$$Y_o = h_{fe} \left(\frac{-h_{re}}{R_s + h_{ie}}\right) + h_{oe}$$

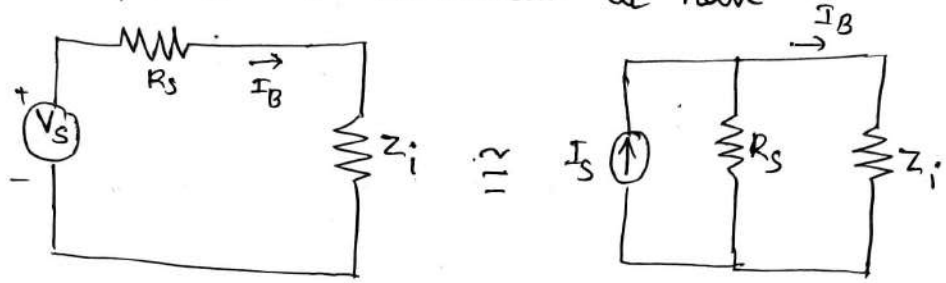
$$\therefore \quad \boxed{Y_o = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}}$$

Current Gain with source (A_{IS}):

$$\text{Current Gain with source } (A_{IS}) = \frac{-I_C}{I_S} = \frac{-I_C}{I_B} \cdot \frac{I_B}{I_S}$$

$$\Rightarrow A_{IS} = A_I \cdot \frac{I_B}{I_S} \longrightarrow (3)$$

From the input side of the circuit we have



From the above figure $I_B = \frac{I_S R_S}{R_S + Z_i}$

$$\Rightarrow \frac{I_B}{I_S} = \frac{R_S}{R_S + Z_i} \longrightarrow (4)$$

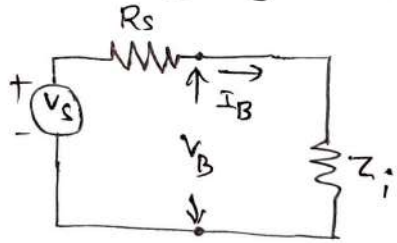
substituting equation (4) in equation (3) we get

$$\boxed{A_{IS} = \frac{A_I R_S}{R_S + Z_i}}$$

Voltage Gain with source (A_{VS}):

$$\text{Voltage Gain with source } (A_{VS}) = \frac{V_C}{V_S} = \frac{V_C}{V_B} \cdot \frac{V_B}{V_S} = A_V \cdot \frac{V_B}{V_S} \longrightarrow (5)$$

From the figure $V_B = \frac{V_S Z_i}{R_S + Z_i}$



$$\therefore \frac{V_B}{V_S} = \frac{Z_i}{R_S + Z_i} \longrightarrow (6)$$

substituting equation (6) in equation (5) we get

$$\boxed{A_{VS} = \frac{A_V Z_i}{R_S + Z_i}} \longrightarrow (7)$$

we know that $A_V = \frac{A_I R_L}{Z_i}$ substituting this in eq (7) we get

$$\boxed{A_{VS} = \frac{A_I R_L}{R_S + Z_i}} \longrightarrow (8)$$

Equation (8) $\Rightarrow$ $A_{VS} = \dfrac{A_I R_L}{R_S + Z_i}$

$$A_{VS} = \frac{A_I R_S}{R_S + Z_i} \cdot \frac{R_L}{R_S}$$

$$\therefore \boxed{A_{VS} = \frac{A_{IS} R_L}{R_S}}$$

Power Gain (A_p) :

Power Gain (A_p) = Voltage Gain (A_V) $\times$ Current Gain (A_I)

$$= A_V \cdot A_I$$

$$A_p = \frac{A_I R_L}{Z_i} A_I$$

$$\therefore \boxed{A_p = \frac{A_I^2 R_L}{Z_i}}$$

1) current Gain (A_I) = $\dfrac{-h_{fe}}{1 + h_{oe} R_L}$

2) Input Impedance (Z_i) = $h_{ie} + h_{re} A_I R_L$

and $Z_i = h_{ie} - \dfrac{h_{re} h_{fe}}{1 + h_{oe} R_L} R_L$

3) Voltage Gain (A_V) = $\dfrac{A_I R_L}{Z_i}$

4) output admittance $Y_o = h_{oe} - \dfrac{h_{re} h_{fe}}{R_S + h_{ie}}$

and output impedance (Z_o) = $\dfrac{1}{h_{oe} - \dfrac{h_{re} h_{fe}}{R_S + h_{ie}}}$

5) current Gain with source (A_{IS}) = $\dfrac{A_I R_S}{R_S + Z_i}$

6) Voltage Gain with source (A_{VS}) = $\dfrac{A_V Z_i}{R_S + Z_i}$

(or) $A_{VS} = \dfrac{A_I R_L}{R_S + Z_i} = \dfrac{A_{IS} R_L}{R_S}$

7) Power Gain $A_p = \dfrac{A_I^2 R_L}{Z_i}$

Analysis of a common collector amplifier (Emitter follower) using exact h-parameter model :

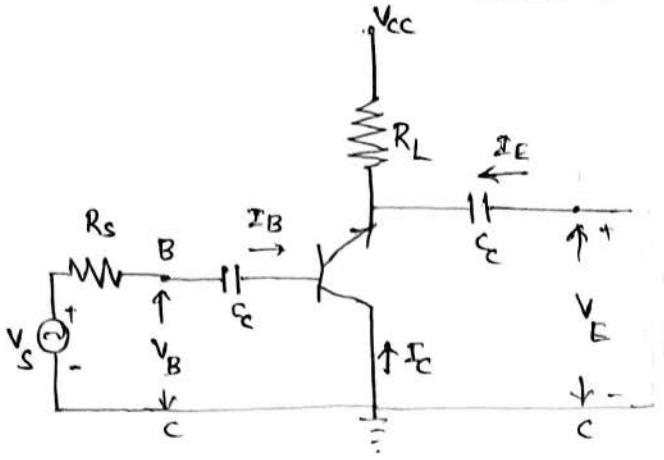
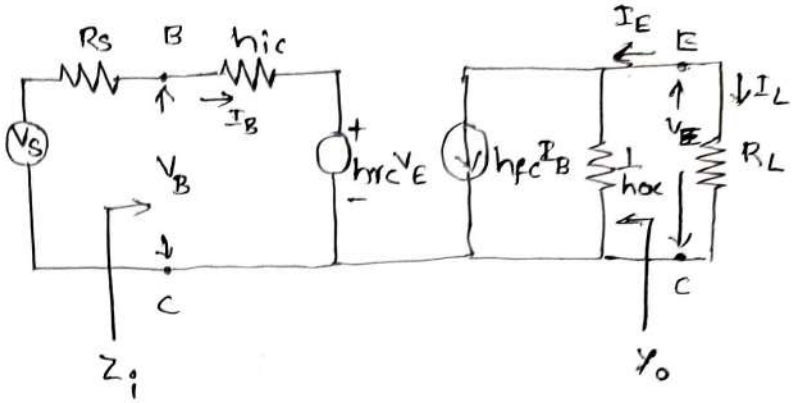


fig: (a) common collector Amplifier



fig(b): Exact h-parameter model of a common collector amplifier.

To analyse the common collector amplifier using h-parameter model, the following parameters are to be derived.

Current Gain (A_I) :

$$\text{Current Gain } (A_I) = \frac{I_L}{I_B} = \frac{-I_E}{I_B}$$

we know that $I_E = h_{fc} I_B + h_{oc} V_E$

$$I_E = h_{fc} I_B + h_{oc}(-I_E R_L)$$

$$\Rightarrow I_E(1 + h_{oc} R_L) = h_{fc} I_B$$

$$\therefore \frac{I_E}{I_B} = \frac{h_{fc}}{1 + h_{oc} R_L}$$

but $A_I = \frac{-I_E}{I_B}$ so $\boxed{A_I = -\frac{h_{fc}}{1 + h_{oc} R_L}}$

Input impedance (Z_i) :

$$\text{Input impedance } (Z_i) = \frac{V_B}{I_B}$$

we know that $V_B = h_{ic} I_B + h_{rc} V_E$

$$\Rightarrow V_B = h_{ic} I_B + h_{rc}(-I_E R_L)$$

$$\Rightarrow V_B = h_{ic} I_B + h_{rc}(A_I I_B) R_L \quad \left(\because A_I = \frac{-I_E}{I_B}\right)$$

$$\Rightarrow \quad \frac{V_B}{I_B} = h_{ic} + h_{rc} A_I R_L$$

$$\therefore \boxed{Z_i = h_{ic} + h_{rc} A_I R_L}$$

substituting $A_I = \frac{-h_{fc}}{1 + h_{oc} R_L}$ in the above equation, we get

$$\boxed{Z_i = h_{ic} - \frac{h_{rc} h_{fc} R_L}{1 + h_{oc} R_L}}$$

Voltage Gain (A_V):

$$\text{Voltage Gain } (A_V) = \frac{V_E}{V_B} = \frac{-I_E R_L}{V_B}$$

$$\Rightarrow \quad A_V = \frac{(A_I I_B) R_L}{V_B} \qquad \left(\because A_I = \frac{-I_E}{I_B}\right)$$

$$\Rightarrow \quad \boxed{A_V = \frac{A_I R_L}{Z_i}} \qquad \left(\because Z_i = \frac{V_B}{I_B}\right)$$

output Admittance (Y_o):

output admittance $Y_o = \frac{I_E}{V_E}$ with $V_s = 0$.

we know that $I_E = h_{fc} I_B + h_{oc} V_E$

$$\therefore \quad Y_o = \frac{h_{fc} I_B + h_{oc} V_E}{V_E}$$

$$Y_o = h_{fc}\left(\frac{I_B}{V_E}\right) + h_{oc} \longrightarrow (1)$$

From fig(b) when $V_s = 0$ we can write

$$I_B R_s + \frac{I_B}{} \cdot h_{ic} + h_{rc} V_E = 0$$

$$\Rightarrow \quad I_B (R_s + h_{ic}) = -h_{rc} V_E$$

$$\therefore \quad \frac{I_B}{V_E} = -\frac{h_{rc}}{R_s + h_{ic}} \longrightarrow (2)$$

Substituting eq(2) in eq(1)

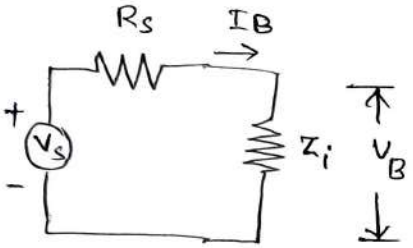
we get $$Y_o = h_{oc} - \frac{h_{fc}\, h_{rc}}{R_s + h_{ic}}$$

The output Impedance $$Z_o = \frac{1}{Y_o} = \frac{1}{h_{oc} - \frac{h_{fc}\, h_{rc}}{R_s + h_{ic}}}$$

Current Gain with source (A_{IS}):

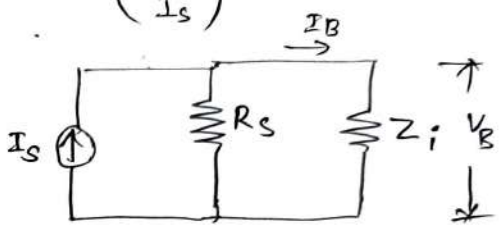
Current Gain with source $(A_{IS}) = \frac{-I_E}{I_S} = \frac{-I_E}{I_B} \cdot \frac{I_B}{I_S}$

$$\Rightarrow A_{IS} = A_I \cdot \left(\frac{I_B}{I_S}\right) \longrightarrow (3)$$



Input section of hybrid model

$\equiv$



Input section of hybrid model with Current Source instead of voltage source

From the figure $$I_B = \frac{I_S R_S}{R_S + Z_i}$$

$$\Rightarrow \frac{I_B}{I_S} = \frac{R_S}{R_S + Z_i} \longrightarrow (4)$$

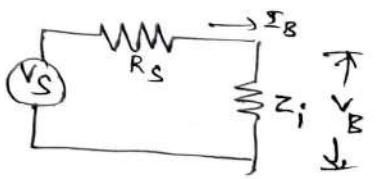
Substituting equation (4) in eq(3) we get

$$A_{IS} = \frac{A_I R_S}{R_S + Z_i}$$

Voltage Gain with source (A_{VS}):

Voltage Gain with source $A_{VS} = \frac{V_E}{V_S} = \frac{V_E}{V_B} \cdot \frac{V_B}{V_S}$

$$\Rightarrow A_{VS} = A_V \cdot \frac{V_B}{V_S} \longrightarrow (5)$$



from the figure $$V_B = \frac{V_S \cdot Z_i}{R_S + Z_i}$$

$$\Rightarrow \frac{V_B}{V_S} = \frac{Z_i}{R_S + Z_i} \longrightarrow (6)$$

Substituting equation (6) in (5) we get

$$\boxed{A_{VS} = \frac{A_V Z_i}{R_S + Z_i}}$$

substituting $A_V = \frac{A_I R_L}{Z_i}$ in the above equation we get

$$\boxed{A_{VS} = \frac{A_I R_L}{R_S + Z_i}}$$

$$\Rightarrow \quad A_{VS} = \left(\frac{A_I R_S}{R_S + Z_i}\right) \frac{R_L}{R_S}$$

$$\boxed{A_{VS} = \frac{A_{IS} R_L}{R_S}}$$

Power Gain (A_P):

Power Gain (A_P) = Voltagain x Current Gain

$$= A_V \cdot A_I$$

$$= \left(\frac{A_I R_L}{Z_i}\right) A_I$$

$$\therefore \quad \boxed{A_P = \frac{A_I^2 R_L}{Z_i}}$$

1) Current Gain $A_I = \frac{-h_{fc}}{1 + h_{oc} R_L}$

2) Input impedance $Z_i = h_{ic} + h_{rc} A_I R_L$

$$Z_i = h_{ic} - \frac{h_{rc} h_{fc} R_L}{1 + h_{oc} R_L}$$

3) voltage Gain $A_V = \frac{A_I R_L}{Z_i}$

4) output admittance $Y_o = h_{oc} - \frac{h_{rc} h_{fc}}{R_S + h_{ic}}$

output impedance $Z_o = \frac{1}{Y_o} = \frac{1}{h_{oc} - \frac{h_{rc} h_{fc}}{R_S + h_{ic}}}$

5) voltage with source (A_{VS})

$$A_{VS} = \frac{A_V Z_i}{R_S + Z_i}$$

(or) $$A_{VS} = \frac{A_I R_L}{R_S + Z_i}$$

(or) $$A_{VS} = \frac{A_{IS} \cdot R_L}{R_S}$$

6) Current gain with source

$$A_{IS} = \frac{A_I R_S}{R_S + Z_i}$$

7) Power Gain (A_P) = $\frac{A_I^2 R_L}{Z_i}$

Exact Analysis of a Common base amplifier using h-parameter model:

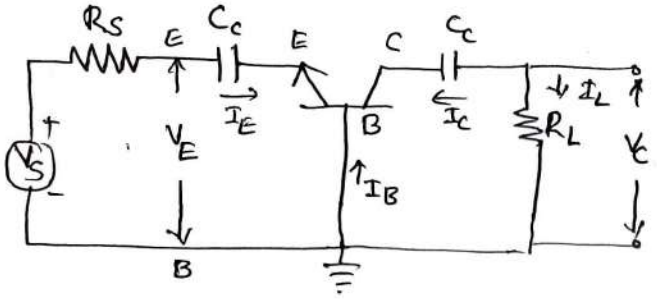


fig a) CB amplifier

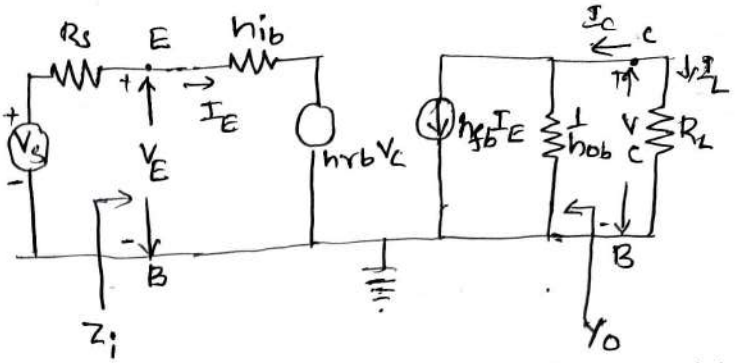


fig b) CB amplifier h-parameter model.

To analyse CB amplifier the following parameters are to be derived.

1) Current Gain (A_I):

$$\text{Current gain } (A_I) = \frac{I_L}{I_E} = \frac{-I_C}{I_E}$$

we know that $I_C = h_{fb} I_E + h_{ob} V_C$

$$I_C = h_{fb} I_E + h_{ob}(-I_C R_L)$$

$$I_C (1 + h_{ob} R_L) = h_{fb} I_E$$

$$\frac{I_C}{I_E} = \frac{h_{fb}}{1 + h_{ob} R_L}$$

but $A_I = -\frac{I_C}{I_E}$ so $\boxed{A_I = -\frac{h_{fb}}{1 + h_{ob} R_L}}$

2) Input Impedance (Z_i):

$$\text{Input impedance } (Z_i) = \frac{V_E}{I_E}$$

we know that $V_E = h_{ib} I_E + h_{rb} V_C$

$$V_E = h_{ib} I_E + h_{rb}(-I_C R_L) \qquad \left(\because \frac{-I_C}{I_E} = A_I\right)$$

$$V_E = h_{ib} I_E + h_{rb} A_I I_E R_L$$

$$\Rightarrow \frac{V_E}{I_E} = h_{ib} + h_{rb} A_I R_L$$

$$\therefore \boxed{Z_i = h_{ib} + h_{rb} A_I R_L}$$

Substituting $A_I = \frac{-h_{fb}}{1+h_{ob}R_L}$ in the above equation we get

$$\boxed{Z_i = h_{ib} - \frac{h_{rb}h_{fb}.R_L}{1+h_{ob}R_L}}$$

3) Voltage Gain (A_V): Voltage Gain $A_V = \frac{V_C}{V_E}$

$$A_V = \frac{-I_C R_L}{V_E}$$

$$= \frac{(A_I I_E)R_L}{V_E} \quad \left(\because A_I = -\frac{I_C}{I_E}\right)$$

$$\therefore \boxed{A_V = \frac{A_I R_L}{Z_i}} \quad \left(\because Z_i = \frac{V_E}{I_E}\right)$$

4) output admittance (Y_o):

output admittance $Y_o = \frac{I_C}{V_C}$ with $R_S = 0$

$$= \frac{h_{fb}I_E + h_{ob}V_C}{V_C}$$

$$Y_o = h_{ob} + h_{fb}\left(\frac{I_E}{V_C}\right) \longrightarrow (1)$$

when $V_S = 0$, Applying KVL to the input circuit we get

$$I_E R_S + I_E h_{ib} + h_{rb}V_C = 0$$

$$\Rightarrow \frac{I_E}{V_C} = \frac{-h_{rb}}{R_S + h_{ib}} \longrightarrow (2)$$

Substituting eq(2) in eq(1) we get

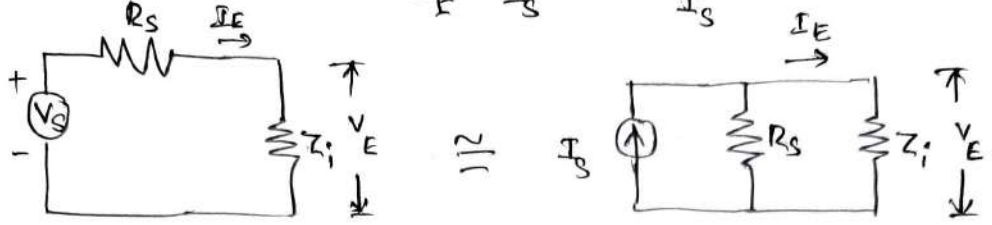
$$\boxed{Y_o = h_{ob} - \frac{h_{fb}h_{rb}}{R_S + h_{ib}}}$$

output impedance $Z_o = \frac{1}{Y_o} = \frac{1}{h_{ob} - \frac{h_{fb}h_{rb}}{R_S + h_{ib}}}$

5) Current Gain with source (A_{IS}):

Current Gain with source $A_{IS} = \frac{I_L}{I_S} = -\frac{I_C}{I_S}$

$$\Rightarrow A_{IS} = -\frac{I_C}{I_E}\frac{I_E}{I_S} = A_I \cdot \frac{I_E}{I_S} \longrightarrow (3)$$



From the above figure $I_E = \frac{I_S R_S}{R_S + Z_i}$

$$\Rightarrow \frac{I_E}{I_S} = \frac{R_S}{R_S + Z_i} \longrightarrow (4)$$

substituting eq (4) in eq (3) we get

$$\boxed{A_{IS} = \frac{A_I R_S}{R_S + Z_i}}$$

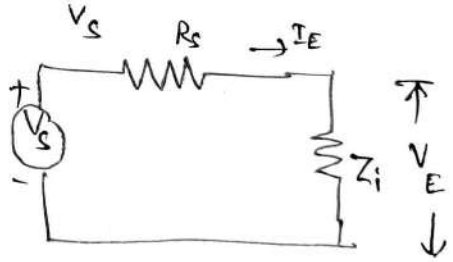
6) Voltage Gain with Source (A_{VS}):

Voltage Gain with source $(A_{VS}) = \frac{V_C}{V_S} = \frac{V_C}{V_E}\cdot\frac{V_E}{V_S}$

$$\Rightarrow A_{VS} = A_V \cdot \frac{V_E}{V_S} \longrightarrow (5)$$

From the figure

$$V_E = \frac{V_S Z_i}{R_S + Z_i} \longrightarrow (6)$$



Substi $\frac{V_E}{V_S} = \frac{Z_i}{R_S + Z_i}$ in eq (5) we get

$$\boxed{A_{VS} = \frac{A_V Z_i}{R_S + Z_i}}$$

Substituting $A_V = \frac{A_I R_L}{Z_i}$ in the above eq we get $\boxed{A_{VS} = \frac{A_I R_L}{R_S + Z_i}}$

$$\Rightarrow \quad A_{VS} = \frac{A_I R_S}{R_S + Z_i} \frac{R_L}{R_S}$$

$$\therefore \boxed{A_{VS} = \frac{A_{IS} R_L}{R_S}}$$

7) **Power Gain (A_P):** Power Gain $(A_P) = A_V \cdot A_I$

$$= \frac{A_I R_L}{Z_i} A_I$$

$$\therefore \boxed{A_P = \frac{A_I^2 R_L}{Z_i}}$$

---

1) Current Gain $A_I = \frac{-h_{fb}}{1 + h_{ob} R_L}$

2) Input Impedance $Z_i = h_{ib} + h_{rb} A_I R_L$

$$Z_i = h_{ib} - \frac{h_{rb} h_{fb} R_L}{1 + h_{ob} R_L}$$

3) Voltage Gain $A_V = \frac{A_I R_L}{Z_i}$

4) Output Admittance $Y_o = h_{ob} - \frac{h_{rb} h_{fb}}{R_S + h_{ib}}$

Output Impedance $Z_o = \frac{1}{Y_o} = \frac{1}{h_{ob} - \frac{h_{rb} h_{fb}}{R_S + h_{ib}}}$

5) Current Gain with source $(A_{IS}) = \frac{A_I R_S}{R_S + Z_i}$

6) Voltage Gain with source $(A_{VS}) = \frac{A_V Z_i}{R_S + Z_i}$

(or) $A_{VS} = \frac{A_I R_L}{R_S + Z_i}$

(or) $A_{VS} = \frac{A_{IS} R_L}{R_S}$

7) Power Gain $(A_P) = \frac{A_I^2 R_L}{Z_i}$

Approximate (or) Simplified h-parameter model for a transistor amplifier:

In most of the practical cases it may be required to obtain the approximate values of current gain, input impedance, voltage gain, output admittance etc rather than their exact values which require lengthy calculations.

But All the times we cannot go for simplified h-parameter model. Since common Emitter is most widely used amplifier, it is taken into consideration. The exact model for CE amplifier using h-parameters is as shown in below.

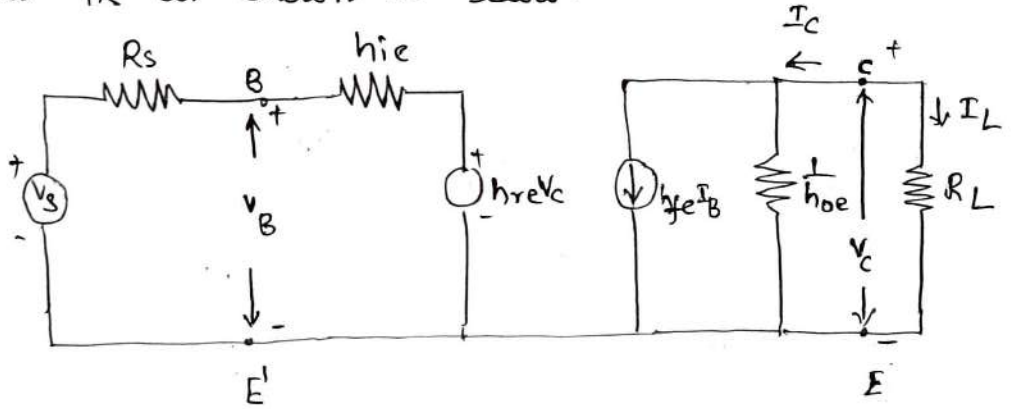


fig: Exact h-parameter model for CE amplifier

Here $\frac{1}{h_{oe}}$ is in parallel with R_L. The parallel combination of two unequal impedances i.e $\frac{1}{h_{oe}}$ and R_L is approximately equal to Lower value i.e R_L. Hence if $\frac{1}{h_{oe}} >> R_L$, then h_{oe} may be neglected provided $h_{oe}R_L < 0.1$.

If h_{oe} is neglected, Collector current I_C becomes $I_C = h_{fe}I_B$

under this condition $h_{re}|V_C| \simeq h_{re}I_C R_L = h_{re}h_{fe}I_B R_L$

Since $h_{re}h_{fe} \simeq 0.01$, $h_{re}V_C$ can be neglected, provided R_L is not too large.

As a conclusion, if R_L is small it is possible to neglect the parameters h_{re} and h_{oe} and we can obtain the approximate h-parameter model.

It can be shown that if $h_{oe}R_L \leq 0.1$ the error in calculating A_I, A_V, Z_i and Y_o for CE configuration is less than 10%.

Analysis of CE configuration using approximate h-parameter model: The approximate hybrid model for CE configuration is as shown in below.

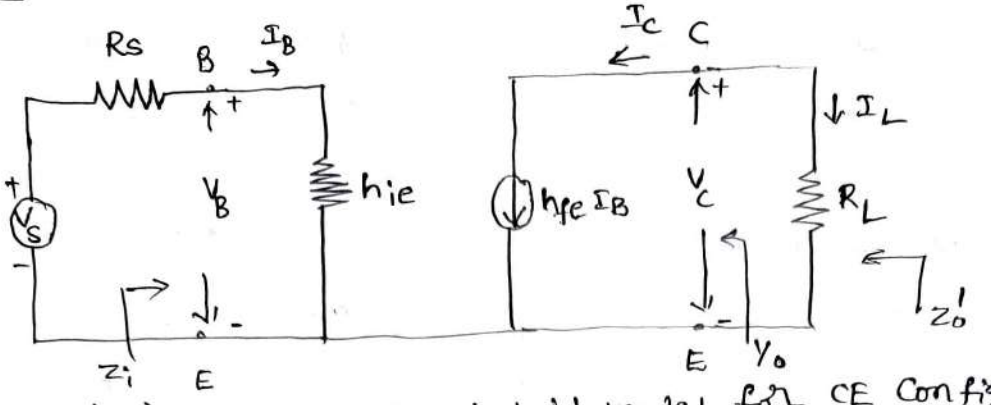


fig a) Approximate hybrid model for CE Configuration

The approximate hybrid model, which is valid for all types of Configurations of a transistor is shown in figure (b).

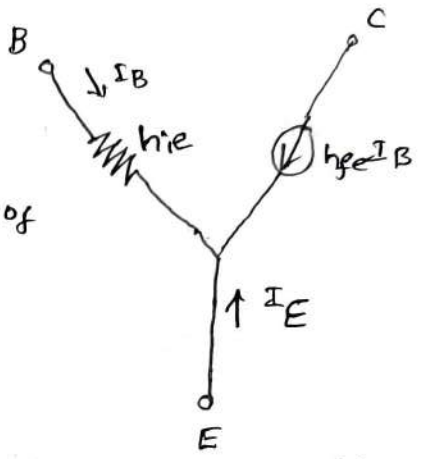


fig b): Approximate hybrid model valid for all configurations.

The parameters for an approximated hybrid model of CE are derived below.

Current Gain (A_I):

The Current Gain (A_I) for CE configuration using exact h-parameter model is $$\text{Current Gain } (A_I) = \frac{-h_{fe}}{1+h_{oe}R_L}$$

If $h_{oe}R_L < 0.1$, $A_I = -h_{fe}$

$$\therefore \boxed{\text{Current Gain } (A_I) \simeq -h_{fe}}$$

Input Impedance (Z_i):

The input impedance (Z_i) for Common Emitter using exact h-parameter model is $$Z_i = h_{ie} + h_{re} \cdot A_I R_L$$

$$Z_i = h_{ie} + h_{re} \cdot (-h_{fe}) R_L$$

$$= h_{ie} - (h_{re} \cdot h_{fe} R_L)$$

since $h_{re} \cdot h_{fe} \simeq 0.01$ if R_L value is not too large we can -

neglect $h_{re} \cdot h_{fe} \cdot R_L$.

$\therefore$ **Input impedance $z_i \simeq h_{ie}$**

Voltage Gain (A_v):

we know that the voltage gain (A_v) $= \frac{A_I R_L}{z_i}$

$\Rightarrow$ **$A_V = -\frac{h_{fe} R_L}{h_{ie}}$**

output admittance: (Y_o)

we know that the output admittance (Y_o) $= h_{oe} - \frac{h_{fe} h_{re}}{R_s + h_{ie}}$

Neglecting h_{oe}, h_{re} we get $Y_o = 0$

$\therefore$ output admittance **$Y_o = 0$**

The output Impedance $Z_o = \frac{1}{Y_o} = \frac{1}{0} = \infty$.

$\therefore$ **$Z_o = \infty$**

$z_o' = z_o \| R_L \simeq R_L$ where z_o' = o/p impedance along with R_L

Analysis of CC configuration using approximate h-parameter model:

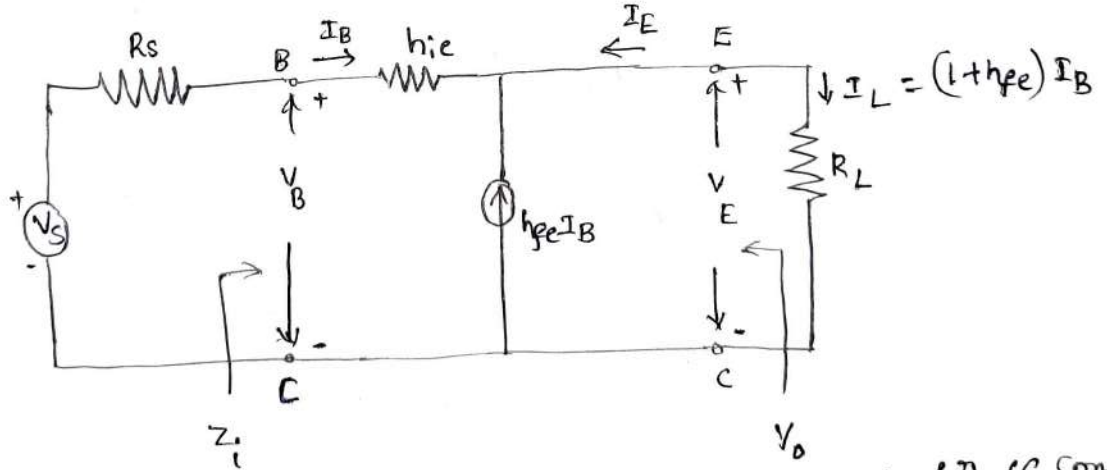


fig: simplified (a) approximated hybrid model for CC Configuration

The above figure shows the approximated hybrid model for CC amplifier using which we derive the following parameters such as current-gain (A_I), voltage Gain (A_V), Input impedance (Z_i) and output admittance (Y_o) etc. Common Collector amplifier is also known as Emitter follower.

Current Gain (A_I):

$$\text{Current Gain } (A_I) = \frac{I_L}{I_B} = \frac{(1+h_{fe})I_B}{I_B} = 1+h_{fe}$$

$$\therefore \quad \boxed{A_I = 1+h_{fe}}$$

(∵ From figure $I_L = (1+h_{fe})I_B$)

Input impedance (Z_i):

From the figure $Z_i = \frac{V_B}{I_B}$

Applying KVL we have (at the input side of the circuit)

$$V_B = I_B h_{ie} + I_L R_L$$

$$V_B = I_B h_{ie} + (1+h_{fe}) I_B R_L$$

$$\Rightarrow \quad \frac{V_B}{I_B} = h_{ie} + (1+h_{fe}) R_L$$

$$\therefore \quad \boxed{Z_i = h_{ie} + (1+h_{fe}) R_L}$$

From this equation the input impedance of CC amplifier is clearly observed to be greater than that of CE amplifier.

Voltage Gain (A_V):

$$\text{The voltage Gain } (A_V) = \frac{V_E}{V_B} = \frac{I_L R_L}{h_{ie} I_B + I_L R_L}$$

$$\Rightarrow \quad A_V = \frac{(1+h_{fe}) I_B \cdot R_L}{h_{ie} I_B + (1+h_{fe}) I_B R_L}$$

$$\Rightarrow \quad \boxed{A_V = \frac{(1+h_{fe}) R_L}{h_{ie} + (1+h_{fe}) R_L}}$$

we know that $(1+h_{fe})R_L >> h_{ie}$ neglecting h_{ie} in the denominator we get

$$A_V \simeq \frac{(1+h_{fe})R_L}{(1+h_{fe})R_L} \simeq 1$$

$$\therefore \quad \boxed{A_V \simeq 1}$$

The output admittance (Y_o) :

The output admittance $Y_o = \frac{I_E}{V_E}$ with $V_s = 0$. $\longrightarrow$ (1)

Applying KVL to the above circuit assuming $V_s = 0$ we get

$$I_B R_s + I_B h_{ie} + V_E = 0$$

$$V_E = -I_B (R_s + h_{ie}) \longrightarrow (2)$$

From the figure $I_E = -I_L = -(1 + h_{fe}) I_B \longrightarrow (3)$

substituting eq (2) and eq (3) in eq (1) we get

$$Y_o = \frac{-(1+h_{fe})I_B}{-I_B(R_s + h_{ie})} = \frac{1+h_{fe}}{R_s + h_{ie}}$$

$$\therefore \boxed{Y_o = \frac{1 + h_{fe}}{R_s + h_{ie}}}$$

The output impedance $\boxed{Z_o = \frac{1}{Y_o} = \frac{R_s + h_{ie}}{1 + h_{fe}}}$

The output impedance along with $R_L = Z_o' = Z_o \| R_L$.

Analysis of common base configuration using approximate h-parameter model;

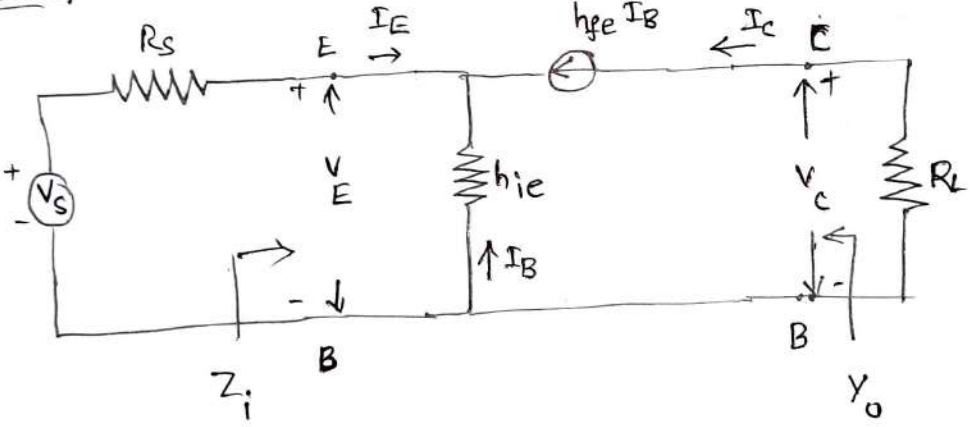


fig: Simplified hybrid model for common base amplifier.

To analyse the common base amplifier using approximate h-parameter model, we have to derive the parameters such as current gain (A_I), input impedance (Z_i), voltage gain (A_V) and output admittance (Y_o) etc.

Current Gain: (A_I)

$$\text{Current Gain } A_I = \frac{-I_C}{I_E} = \frac{I_L}{I_E} \longrightarrow (1)$$

From the figure $I_C = h_{fe} I_B$ and $I_E = -(h_{fe} I_B + I_B)$

substituting these equations in equation (1) we get

$$A_I = \frac{-h_{fe} I_B}{-(h_{fe} I_B + I_B)}$$

$$\therefore \boxed{A_I = \frac{h_{fe}}{1+h_{fe}} = -h_{fb}}$$

Input impedance (Z_i):

$$\text{Input impedance } Z_i = \frac{V_E}{I_E} = \frac{-h_{ie} I_B}{-(I_B + h_{fe} I_B)}$$

$$\Rightarrow Z_i = \frac{h_{ie} I_B}{(1+h_{fe}) I_B} = \frac{h_{ie}}{1+h_{fe}}$$

$$\therefore \boxed{Z_i = \frac{h_{ie}}{1+h_{fe}} = h_{ib}}$$

Voltage Gain (A_V):

$$\text{Voltage Gain } A_V = \frac{V_C}{V_E} = \frac{-I_C R_L}{-h_{ie} I_B}$$

$$\Rightarrow A_V = \frac{-h_{fe} I_B R_L}{-h_{ie} I_B} = \frac{h_{fe} R_L}{h_{ie}}$$

$$\therefore \boxed{A_V = \frac{h_{fe} R_L}{h_{ie}}}$$

output admittance (Y_o):

$$Y_o = \frac{I_C}{V_C} \text{ with } V_s = 0$$

From the figure when $V_s = 0$, $I_b = 0$ and $I_E = 0$ and hence $I_c = 0$

$\therefore \boxed{Y_o = 0}$ Therefore $\boxed{\text{output Impedance } Z_o = \infty}$

o/p impedance along with R_L, $Z_o' = Z_o \| R_L = R_L$

NOTE: The typical values of h-parameters when the transistor is connected in CE Configuration are $h_{ie} = 1.1K\Omega$, $h_{fe} = 50$, $h_{re} = 2.5 \times 10^{-4}$ and $h_{oe} = 25\mu A/V$

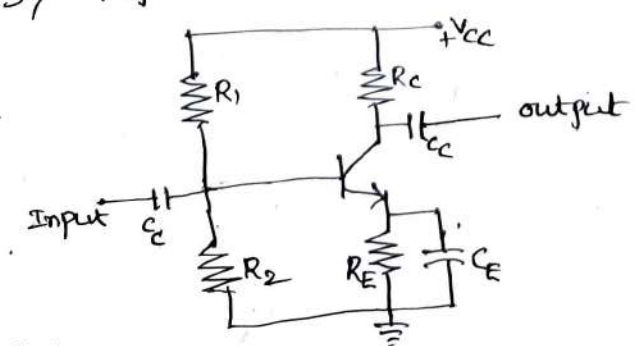
Conversion formulae for h-parameters

Common Collector	Common Base
1) $h_{ic} = h_{ie}$	1) $h_{ib} = \frac{h_{ie}}{1+h_{fe}}$
2) $h_{rc} \simeq 1$	2) $h_{rb} = \frac{h_{ie} h_{oe}}{1+h_{fe}} - h_{re}$
3) $h_{fc} = -(1+h_{fe})$	3) $h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$
4) $h_{oc} = h_{oe}$	4) $h_{ob} = \frac{h_{oe}}{1+h_{fe}}$

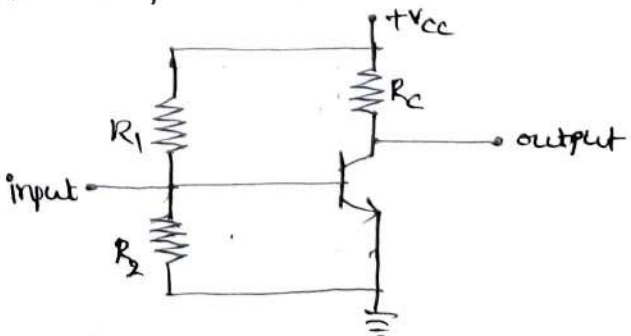
Guidelines for the analysis of a transistor amplifier:

There are different biasing techniques, different Configurations and so on. The analysis of such transistor circuits can be done by following the simple guidelines given below.

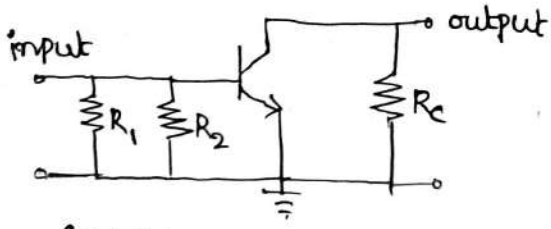
1) Draw the actual circuit diagram
2) Replace the coupling capacitors and emitter bypass capacitor by short circuit
3) Replace DC source by short circuit. In other words short V_{cc} and ground lines
4) Mark the points B (base), C (collector) and Emitter E on the Circuit diagram
5) Replace the transistor by it's h-parameter model.



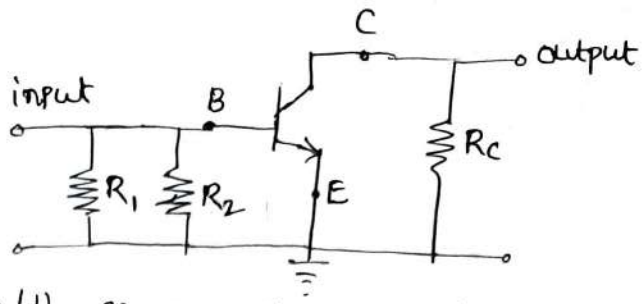
fig(a) Actual circuit



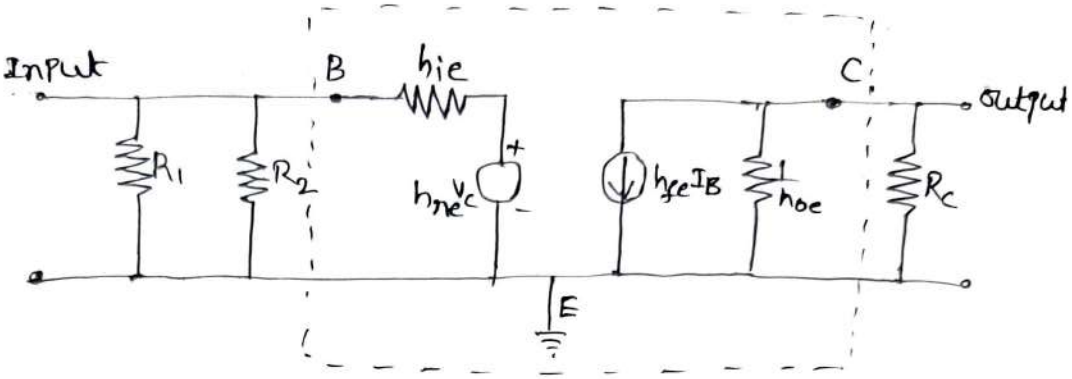
fig(b): Circuit with capacitors as a short - Circuit



fig(c): Circuit with V_{cc} and Ground - Short Circuit.

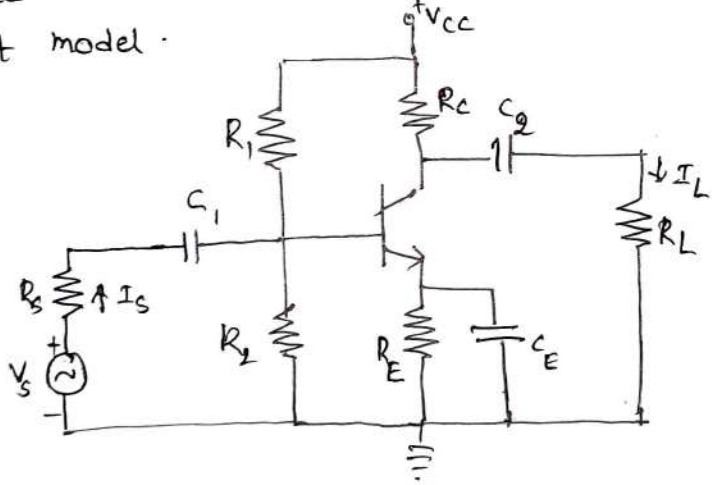


fig(d) Circuit with B, C, and E points located.



fig(e) Circuit with transistor replaced by h-parameter equivalent.

Problem: Consider a single stage CE amplifier with $R_s = 1k\Omega$, $R_1 = 50k\Omega$, $R_2 = 2k\Omega$, $R_c = 1k\Omega$, $R_L = 1.2k\Omega$, $h_{fe} = 50$, $h_{ie} = 1.1k\Omega$, $h_{oe} = 25\mu A/V$ and $h_{re} = 2.5 \times 10^{-4}$ as shown in below. Find $A_i, Z_i, A_V, Y_o, A_{IS}$ and A_{Vs} use Exact model.



NOTE: This circuit is a common Emitter Amplifier with Emitter bypass capacitor C_E in parallel with the Emitter resistance R_E

Sol)

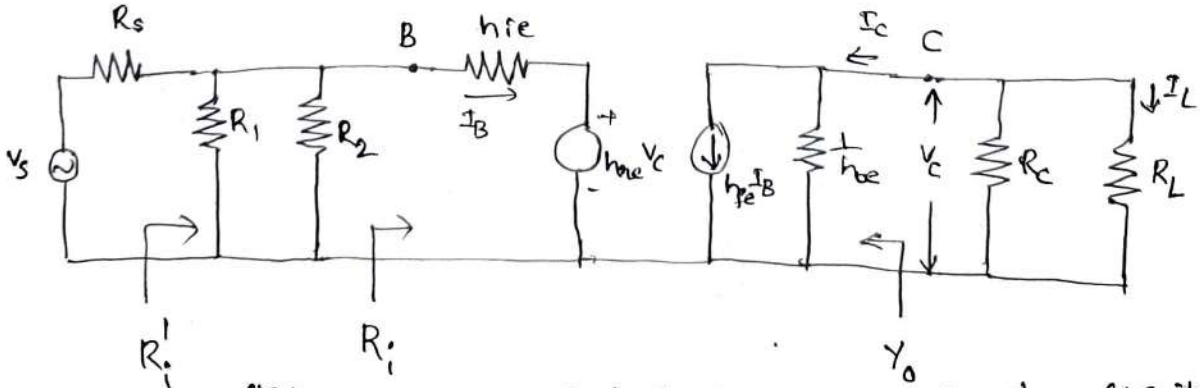


fig: H-Parameter equivalent circuit for the given circuit

Current Gain $(A_I) = \frac{-I_c}{I_B} = \frac{-h_{fe}}{1+h_{oe}R_L'}$

where $R_L' = R_c \| R_L = 1k\Omega \| 1.2k\Omega$

$R_L' = \frac{(1\times10^3)\times(1.2\times10^3)}{(1\times10^3)+(1.2\times10^3)} = \frac{1.2\times10^6}{2.2\times10^3} = 545.45\Omega$

$\therefore A_I = \frac{-50}{1+(25\times10^{-6}\times 545.45)} = -49.32$

Input Impedance $Z_i = h_{ie} + h_{re}A_I R_L'$

$= 1100 + (2.5\times10^{-4}\times(-49.32)\times 545.45)$

$\therefore Z_i = 1093.27\Omega$

Voltage Gain $A_V = \frac{A_I R_L'}{Z_i} = \frac{-49.32\times 545.45}{1093.27}$

$\therefore A_V = -24.606$

output admittance $Y_o = h_{oe} - \frac{h_{re}h_{fe}}{R_S'+h_{ie}}$

$\left(\because R_S' = R_S \| R_1 \| R_2 = 1k\Omega \| 50k\Omega \| 2k\Omega = 657.5\Omega\right)$

$= 25\times10^{-6} - \frac{2.5\times10^{-4}\times 50}{657.5+1100}$

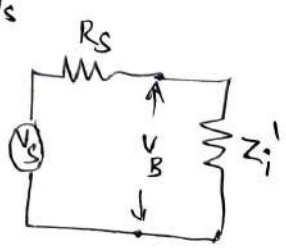
$= 25\times10^{-6} - 7.112\times10^{-6}$

$\therefore Y_o = 17.88\times10^{-6}\ \mho$

output Impedance $Z_o = \frac{1}{Y_o} = \frac{1}{17.88\times10^{-6}} = 55.9\ k\Omega$

Voltage Gain with source $A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_B}\cdot\frac{V_B}{V_s}$

$\Rightarrow A_{VS} = A_V \cdot \frac{\left(\frac{V_s\cdot Z_i'}{Z_i'+R_S}\right)}{V_s}$



$\Rightarrow A_{VS} = \frac{A_V Z_i'}{Z_i'+R_S}$

where $Z_i' = Z_i \| R_1 \| R_2 = 1093.27 \| 50k\Omega \| 2k\Omega$

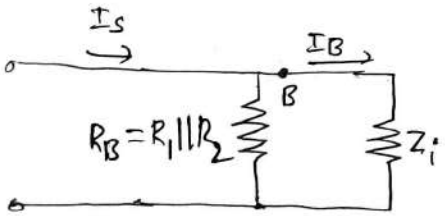
$= 1093.27 \| 1.92k\Omega$

$Z_i' = 696.61\ \Omega$

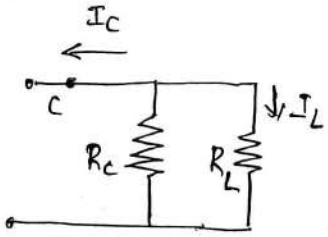
$\therefore A_{VS} = \frac{A_V Z_i'}{R_S + Z_i'} = \frac{-24.606 \times 696.61}{1000 + 696.61}$

$\therefore A_{VS} = -10.102$

Current Gain with source (A_{IS}):



fig(a)



fig(b)

$A_{IS} = \frac{I_L'}{I_S} = \frac{I_L}{I_C} \cdot \frac{I_C}{I_B} \cdot \frac{I_B}{I_S}$ → eq (A)

$\Rightarrow A_{IS} = \frac{I_L}{I_C}(-A_I) \cdot \frac{I_B}{I_S}$ → (1)

From above fig(b) $I_L = \frac{-I_C \cdot R_C}{R_C + R_L} \Rightarrow \frac{I_L}{I_C} = -\frac{R_C}{R_C + R_L}$ → (2)

From fig(a) $I_B = \frac{I_S R_B}{R_B + Z_i} \Rightarrow \frac{I_B}{I_S} = \frac{R_B}{R_B + Z_i}$ → (3)

where $R_B = R_1 \| R_2 = 50k\Omega \| 2k\Omega = 1.923k\Omega$

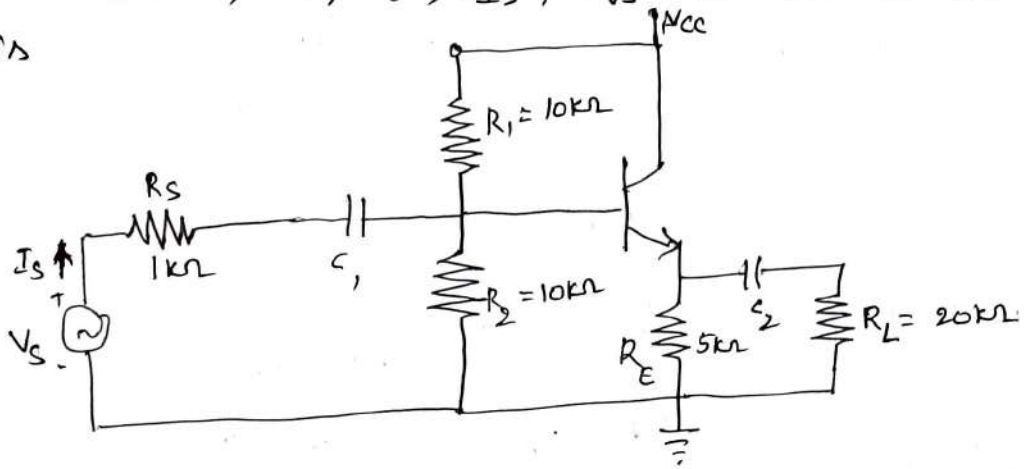
Substituting eq (3), eq (2) together in eq (1) we get

$A_{IS} = \frac{-R_C}{R_C + R_L} \cdot (-A_I) \cdot \frac{R_B}{R_B + Z_i}$

$A_{IS} = \frac{-1 \times 10^3}{(1 \times 10^3) + (1.2 \times 10^3)} \times 49.32 \times \frac{1.923 \times 10^3}{(1.923 \times 10^3) + (1.093 \times 10^3)}$

$\therefore A_{IS} = -14.29$

⇒ In the common collector amplifier shown in below, the transistor parameters are $h_{ic} = 1.2k\Omega$, $h_{fc} = -101$, $h_{rc} = 1$, $h_{oc} = 25\mu A/V$, Calculate A_I, Z_i, A_V, Y_o, A_{IS}, A_{VS} for the circuit using exact analysis



sol⇒ Given $h_{ic} = 1.2k\Omega$, $h_{fc} = -101$, $h_{rc} = 1$, $h_{oc} = 25\times10^{-6}$ ℧

$R_1 = 10k\Omega$, $R_2 = 10k\Omega$, $R_E = 5k\Omega$, $R_L = 20k\Omega$

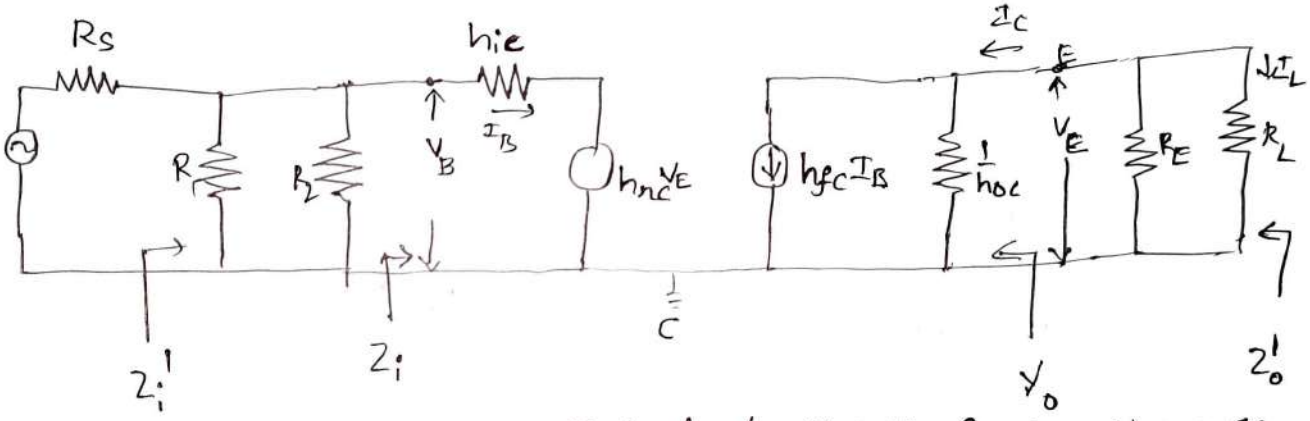


fig: H-parameter equivalent circuit for the given CC amplifier

↳ Current Gain $A_I = \dfrac{-h_{fc}}{1 + h_{oc} R_L'}$ where $R_L' = R_E \| R_L$

$R_L' = 5k\Omega \| 20k\Omega$

$R_L' = 4k\Omega$

$= \dfrac{-(-101)}{1 + (25\times10^{-6} \times 4\times10^{3})}$

$= 91.81$

↳ Input Impedance $Z_i = h_{ic} + h_{rc} A_I R_L'$

$= 1200 + (1)(91.81)(4000)$

$Z_i = 368.472\ k\Omega$

overall input impedance $Z_i' = Z_i \| R_1 \| R_2$

$= 368.472\ k\Omega \| 10k\Omega \| 10k\Omega$

$= 368.472\text{k}\Omega \parallel 5\text{k}\Omega$

$\therefore Z_i' = 4.933\ \text{k}\Omega$

↳ voltage Gain $A_V = \dfrac{A_I R_L'}{Z_i} = \dfrac{(91.81)(4000)}{368.472 \times 10^3}$

$\therefore A_V = 0.9967$

↳ output admittance $Y_o = h_{oc} - \dfrac{h_{rc} h_{fc}}{R_S' + h_{ie}}$

where $R_S' = R_S \parallel R_1 \parallel R_2 = 1\text{k}\Omega \parallel 10\text{k}\Omega \parallel 10\text{k}\Omega$

$\Rightarrow R_S' = 833.33\Omega$

$\therefore Y_o = 25 \times 10^{-6} - \dfrac{1.(-101)}{833.33 + 1200}$

$Y_o = 0.0497\ \mho$

output Impedance $Z_o = \dfrac{1}{Y_o} = \dfrac{1}{0.0497} = 20.1219\Omega$

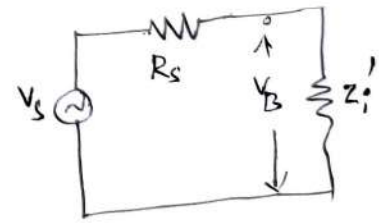
overall output Impedance $Z_o' = Z_o \parallel R_E \parallel R_L = Z_o \parallel R_L'$

$\Rightarrow Z_o' = 20.1219 \parallel 4000$

$\Rightarrow Z_o' = 20.02\Omega$

↳ Voltage Gain with source $(A_{VS}) = \dfrac{V_E}{V_S} = \dfrac{V_E}{V_B} \cdot \dfrac{V_B}{V_S} = A_V \cdot \dfrac{V_B}{V_S}$

$\Rightarrow A_{VS} = A_V \cdot \dfrac{\left(\dfrac{V_S \cdot Z_i'}{R_S + Z_i'}\right)}{V_S}$



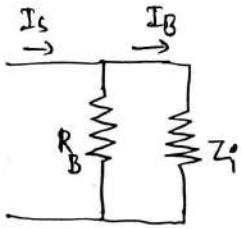
$\Rightarrow A_{VS} = \dfrac{A_V Z_i'}{R_S + Z_i'}$

$= \dfrac{0.9967 \times 4.933 \times 10^3}{1000 + 4933}$

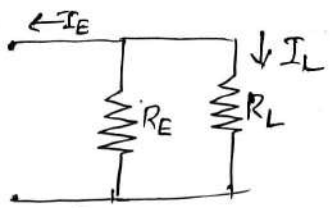
$\therefore A_{VS} = 0.8287$

∴ voltage Gain with source (A_{VS}) = 0.8287

→ Current Gain with source $(A_{IS}) = \frac{I_L}{I_S}$



fig(a)



fig(b)

$$A_{IS} = \frac{I_L}{I_E} \cdot \frac{I_E}{I_B} \cdot \frac{I_B}{I_S}$$

$$A_{IS} = \frac{I_L}{I_E} \cdot (-A_I) \cdot \frac{I_B}{I_S} \rightarrow (1) \qquad \left(\because A_I = \frac{-I_E}{I_B}\right)$$

From fig(a) $I_B = \frac{I_S R_B}{R_B + Z_i}$

$$\Rightarrow \frac{I_B}{I_S} = \frac{R_B}{R_B + Z_i} = \frac{5\times10^3}{5\times10^3 + (368.44\times10^3)} \qquad \left(\begin{array}{l} R_B = R_1 \| R_2 \\ = 10k\Omega \| 10k\Omega \\ = 5k\Omega \end{array}\right)$$

$$\Rightarrow \frac{I_B}{I_S} = 0.0134 \rightarrow (2)$$

From fig(b) $I_L = \frac{-I_E \cdot R_E}{R_E + R_L}$

$$\Rightarrow \frac{I_L}{I_E} = \frac{-R_E}{R_E + R_L} = \frac{-5\times10^3}{5\times10^3 + 20\times10^3}$$

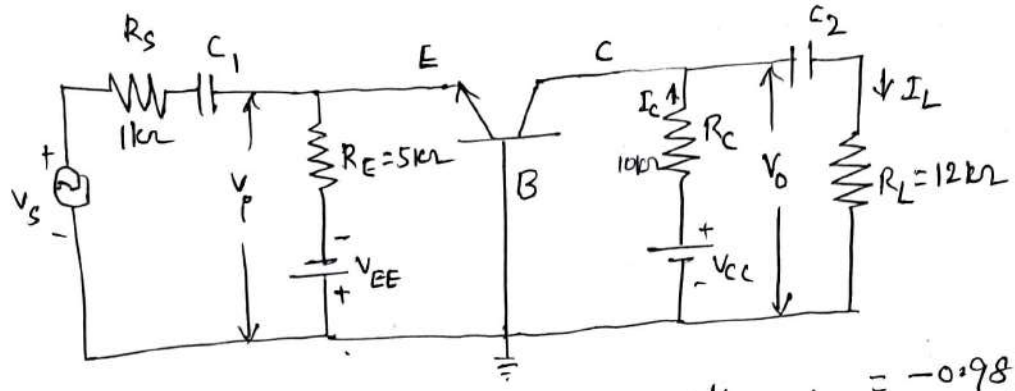
$$\Rightarrow \frac{I_L}{I_E} = -0.2 \rightarrow (3)$$

substitute eq (3), (2) in eq (1) along with $A_I = 91.81$

we get $A_{IS} = (-0.2)(-91.81)\cdot(0.0134)$

$\therefore A_{IS} = 0.2461$

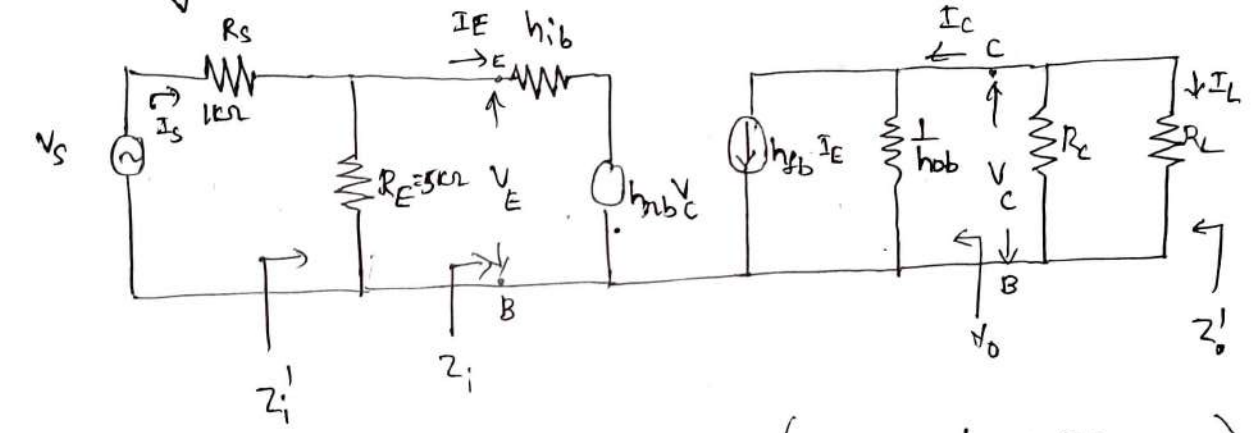
3) From the common base amplifier the transistor parameters are $h_{ib} = 22\Omega$, $h_{fb} = -0.98$, $h_{ob} = 0.49\,\mu A/V$, $h_{rb} = 2.9\times10^{-4}$. Calculate the values of Current gain, input impedance, voltage gain output admittance, voltage gain with source and Current gain with source using exact analysis



Sol) Given $h_{ib} = 22\Omega$, $h_{rb} = 2.9\times10^{-4}$, $h_{fb} = -0.98$, $h_{ob} = 0.49\,\mu A/V$

$R_S = 1k\Omega$, $R_E = 5k\Omega$, $R_C = 10k\Omega$, $R_L = 12k\Omega$.

The H-parameter equivalent circuit for the given circuit is given in below figure.



↳ Current Gain $(A_I) = \dfrac{-h_{fb}}{1+h_{ob}R_L'}$ (where $R_L' = R_C \| R_L$)

$= 10k\Omega \| 12k\Omega$

$R_L' = 5.4545k\Omega$

$$= \frac{-(-0.98)}{1+(0.49\times10^{-6}\times5.4545\times10^{3})}$$

$$= +0.9774$$

$\therefore A_I = 0.9774$

↳ Input Impedance $(Z_i) = h_{ib} + h_{rb}A_I R_L'$

$$= 22 + (2.9\times10^{-4}\times0.9774\times5.4545\times10^{3})$$

$Z_i = 23.5448\Omega$

Overall input Impedance $Z_i' = R_E \| Z_i$

$= 5k\Omega \| 23.5448$

$\therefore Z_i' = 23.4344\Omega$

↳ voltage Gain $(A_V) = \dfrac{A_I R_L'}{Z_i}$

$$= \frac{0.9774 \times (5.4545 \times 10^{3})}{23.5448}$$

$$\therefore A_V = 226.4291$$

↳ output admittance $Y_o = h_{ob} - \dfrac{h_{rb} h_{fb}}{R_S' + h_{ib}}$

where $R_S' = R_S \| R_E = 1K\Omega \| 5K\Omega = 833.33\Omega$

$$\therefore Y_o = 0.49 \times 10^{-6} - \frac{2.9 \times 10^{-4} \times (-0.98)}{833.3 + 22}$$

$$= 0.49 \times 10^{-6} + 0.33 \times 10^{-6}$$

$$Y_o = 0.82 \times 10^{-6} \, \mho$$

The output Impedance $Z_o = \dfrac{1}{Y_o} = \dfrac{1}{0.82 \times 10^{-6}} = 1.21 M\Omega$

over all output impedance $(Z_o') = Z_o \| R_C \| R_L = 1.21 \times 10^{6} \| R_L'$

$(\because R_C \| R_L = R_L')$

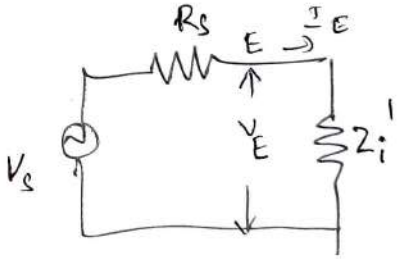
$$= 1.21 \times 10^{6} \| 5.4545 \times 10^{3}$$

$$= 5.43 K\Omega$$

↳ Voltage Gain with source (A_{VS})

$$A_{VS} = \frac{V_C}{V_S} = \frac{V_C}{V_E} \cdot \frac{V_E}{V_S}$$

$$\Rightarrow A_{VS} = A_V \cdot \frac{V_E}{V_S}$$



from this figure $V_E = \dfrac{V_S \cdot Z_i'}{R_S + Z_i'}$

$$\Rightarrow \frac{V_E}{V_S} = \frac{Z_i'}{R_S + Z_i'} = \frac{23.4344}{1000 + 23.4344} = 0.0229$$

$$\therefore A_{VS} = A_V \cdot \frac{V_E}{V_S} = 226.4291 \times 0.0229 = 5.1847$$

∴ Voltage Gain with source $(A_{VS}) = 5.1847$

Current Gain with source (A_{IS}) :

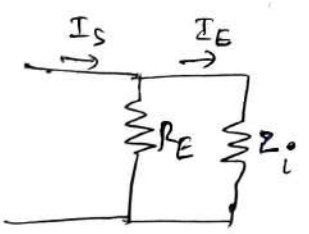


fig (a):

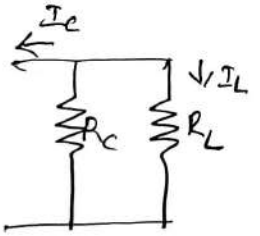


fig (b)

$$A_{IS} = \frac{I_L}{I_S} = \frac{I_L}{I_C} \cdot \frac{I_C}{I_E} \cdot \frac{I_E}{I_S}$$

$$= \frac{I_L}{I_C}\left[\left(\frac{-I_C}{I_E}\right)\right]\frac{I_E}{I_S} \qquad \left(\because \frac{-I_C}{I_E} = A_I\right)$$

$$A_{IS} = -\frac{I_L}{I_C}(A_I)\frac{I_E}{I_S} \longrightarrow (1)$$

from fig (b) $I_L = -\dfrac{I_C R_C}{R_C + R_L} \Rightarrow \dfrac{-I_L}{I_C} = \dfrac{R_C}{R_C + R_L}$

$$\Rightarrow -\frac{I_L}{I_C} = \frac{10k\Omega}{10k\Omega + 12k\Omega} = 0.4545 \longrightarrow (2)$$

from fig (a) $I_E = \dfrac{I_S \cdot R_E}{R_E + Z_i} \Rightarrow \dfrac{I_E}{I_S} = \dfrac{R_E}{R_E + Z_i}$

$$= \frac{5\times10^3}{(5\times10^3) + 23.5448}$$

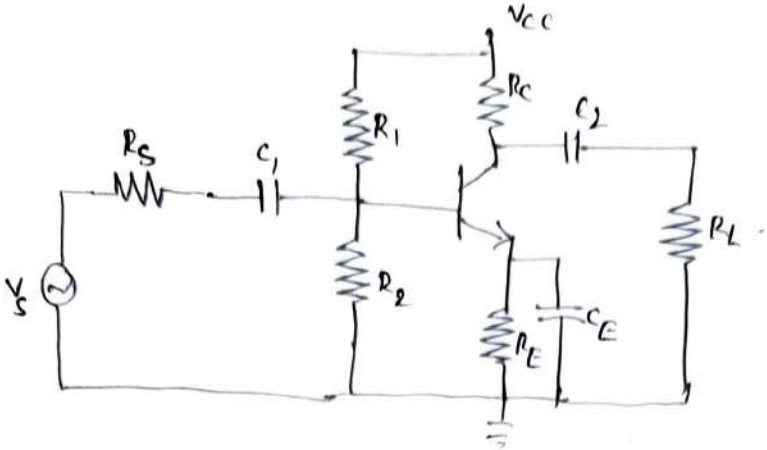
$$\frac{I_E}{I_S} = 0.9953 \longrightarrow (3)$$

Substitute $A_I = 0.9774$, eq (2), eq (3) in eq (1) we get

$$A_{IS} = 0.4545 \times 0.9774 \times 0.9953$$

$$\therefore A_{IS} = 0.4421$$

4) Consider a single stage CE amplifier with $R_S = 1k\Omega$, $R_1 = 50k\Omega$, $R_2 = 2k\Omega$, $R_C = 2k\Omega$, $R_L = 2k\Omega$, $h_{fe} = 50$, $h_{ie} = 1.1k\Omega$, $h_{oe} = 25\times10^{-6}$ A/V $h_{re} = 2.5\times10^{-4}$ as shown in below figure. Find A_I, Z_I, A_V, Y_o and R_o



Sol) Given $R_S = 1k\Omega$, $R_1 = 50k\Omega$, $R_2 = 2k\Omega$, $R_C = 2k\Omega$, $R_E = 2k\Omega$, $h_{ie} = 1.1k\Omega$, $h_{fe} = 50$, $h_{re} = 2.5\times10^{-4}$ $h_{oe} = 25\times10^{-6}$ A/V

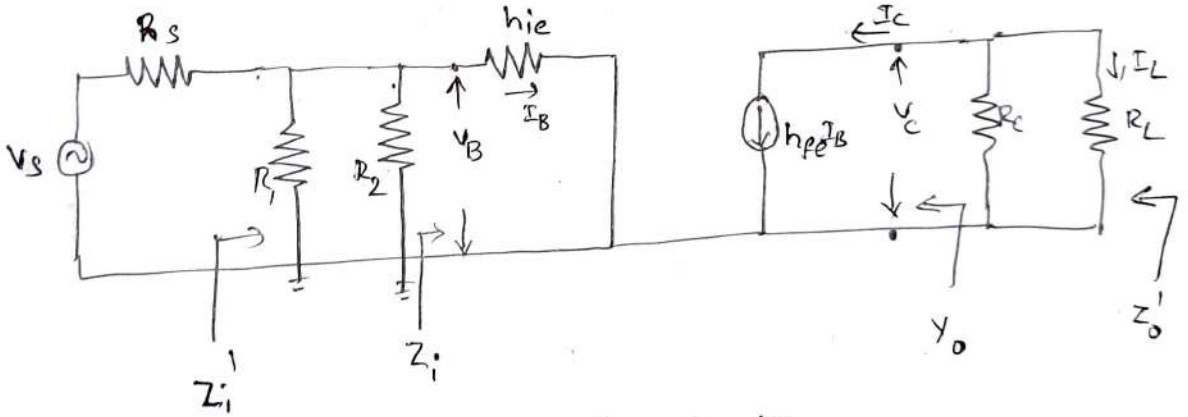
The given circuit has a transistor with $h_{oe} = 25\times10^{-6}$ A/V and $R_L = 2k\Omega$,

$$h_{oe}\cdot R_L' = 25\times10^{-6}\times\left(2\times10^3 \,||\, 2/10^3\right)$$

$$= 25\times10^{-6}\times 1\times10^3$$

$$= 0.025$$

$\therefore h_{oe} R_L' < 0.1$ so we go for approximate analysis



↳ The current gain $(A_I) = -h_{fe} = -50$

↳ Input impedance $Z_i = h_{ie} = 1.1k\Omega$

↳ voltage gain $(A_V) = \dfrac{A_I R_L'}{Z_i} = \dfrac{(-50)(1k\times10^3)}{1.1\times10^3}$ $\left(\because R_L' = R_C \,||\, R_L = 2k\Omega \,||\, 2k\Omega = 1k\Omega\right)$

$\Rightarrow A_V = -45.45$

↳ overall input impedance $Z_i' = Z_i \,||\, R_1 \,||\, R_2$

$= 1.1\times10^3 \,||\, 50\times10^3 \,||\, 2\times10^3$

$$\Rightarrow \quad Z_i' = 1.1\times10^3 \,||\, 1.923\times10^3$$

$$Z_i' = 699.7\ \Omega$$

↳ output admittance $(Y_o) = 0$

output impedance $(Z_o) = \frac{1}{Y_o} = \frac{1}{0} = \infty$

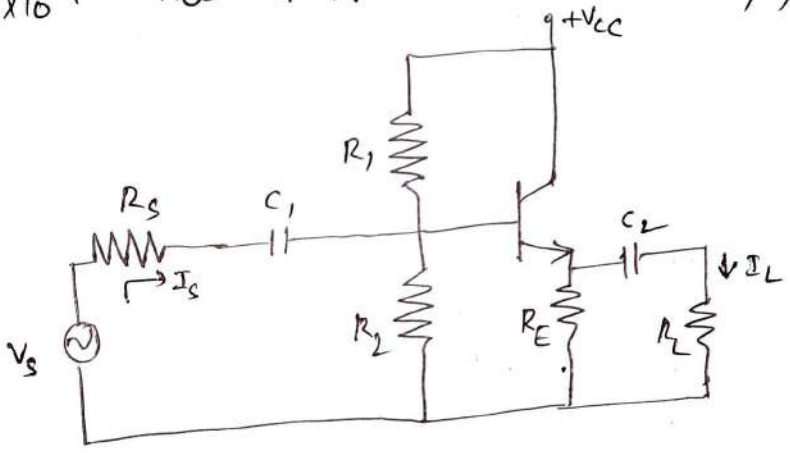
overall output impedance $Z_o' = Z_o \,||\, R_C \,||\, R_L$

$$= \infty \,||\, 2k\Omega \,||\, 2k\Omega$$

$$= \infty \,||\, 1k\Omega$$

$$\therefore Z_o' = 1k\Omega$$

5) Consider a common collector amplifier that has $R_1 = 27k\Omega$, $R_2 = 27k\Omega$, $R_E = 5.6k\Omega$, $R_L = 47k\Omega$, $R_S = 600\Omega$, $h_{ie} = 1k\Omega$, $h_{fe} = 85$ $h_{re} = 2.5\times10^{-4}$ $h_{oe} = 2\mu A/V$ Calculate A_I, R_i, A_V, Y_o



Sol) Given $R_1 = 27k\Omega$, $R_2 = 27k\Omega$, $R_E = 5.6k\Omega$, $R_L = 47k\Omega$, $R_S = 600\Omega$, $h_{ie} = 1k\Omega$, $h_{fe} = 85$, $h_{oe} = 2\mu A/V$, $h_{re} = 2.5\times10^{-4}$

$$h_{oe} R_L' = 2\times10^{-6} \times (R_E \,||\, R_L)$$

$$= 2\times10^{-6} \times (5.6\times10^3 \,||\, 47\times10^3)$$

$$= 2\times10^{-6} \times 5.003\times10^3$$

$$= 0.01$$

$h_{oe} R_L' < 0.1$ so we go for approximate analysis

Current Gain $(A_I) = 1 + h_{fe} = 1 + 85 = 86$

Input Impedance $Z_i = h_{ie} + (1 + h_{fe}) R_L'$

$$= 1\times10^{3} + (1+85)(5.003\times10^{3})$$

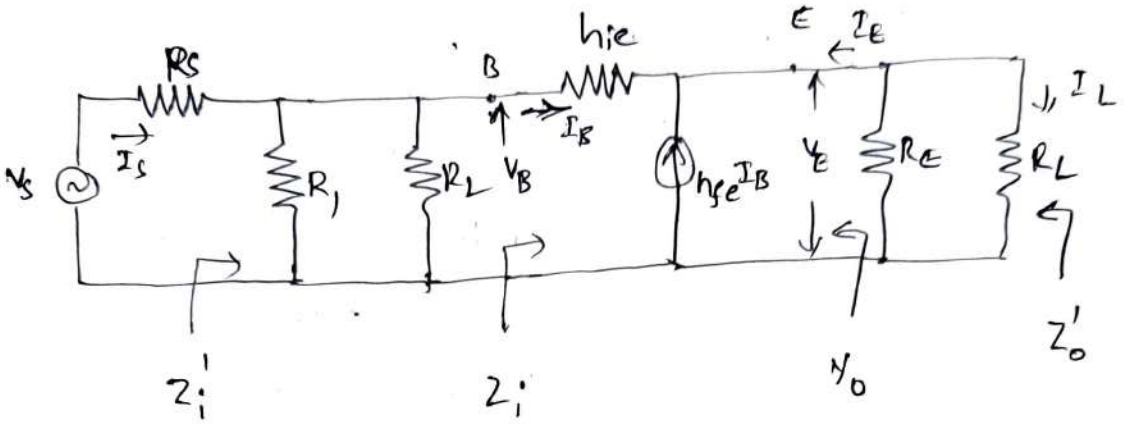
$$= 431.258\ k\Omega$$

overall input impedance $Z_i' = R_1 \| R_2 \| Z_i$

$$= 27\times10^{3} \| 27\times10^{3} \| 431.258\times10^{3}$$

$$= 13.5\times10^{3} \| 431.258\times10^{3}$$

$$Z_i' = 13.09\ k\Omega$$



↳ voltage Gain $(A_v) = \dfrac{(1+h_{fe})R_L'}{h_{ie} + (1+h_{fe})R_L'}$

$$= \frac{(1+85)(5.003\times10^{3})}{1000 + (1+85)(5.003\times10^{3})}$$

$$A_v = 0.9977$$

↳ output Admittance $Y_o = \dfrac{1+h_{fe}}{R_s' + h_{ie}} = \dfrac{1+85}{(R_s \| R_1 \| R_2) + (1\times10^{3})}$ (where $R_s' = R_1 \| R_2 \| R_s$)

$R_s = 600\ \Omega$, $R_1 = 27k\Omega$, $R_2 = 27k\Omega$, $R_1 \| R_L = 13.5k\Omega$

$\therefore R_s' = 13.5\ k\Omega \| 600 = 574.468\ \Omega$

$$\therefore Y_o = \frac{1+85}{574.468 + 1000} = 0.0546$$

output Impedance $z_o = \dfrac{1}{Y_o} = \dfrac{1}{0.0546} = 18.30\ \Omega$

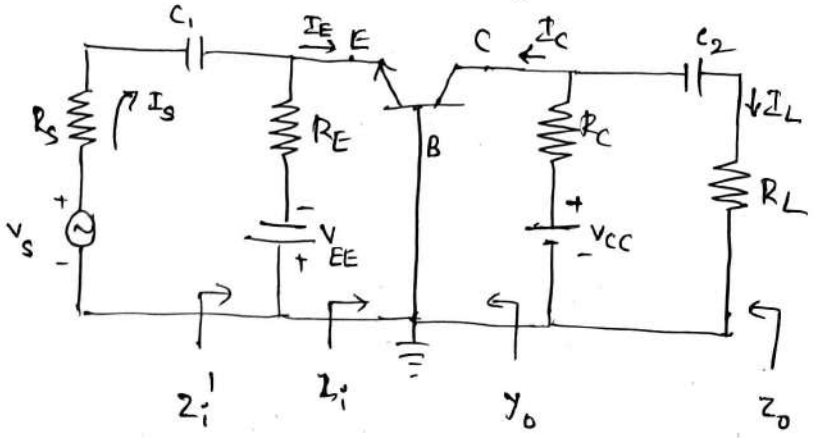
overall output Impedance $Z_o' = Z_o \| R_E \| R_L$

$$= 18.3 \| 5.6\times10^{3} \| 47\times10^{3}$$

$$\therefore Z_o' = 18.233\ \Omega$$

c) A common base amplifier has the components $R_s = 600\,\Omega$, $R_E = 5.6\,k\Omega$, $R_E = 5.6\,k\Omega$, $R_L = 39\,k\Omega$, $h_{ie} = 1k\Omega$ $h_{fe} = 85$, $h_{oe} = 2\mu A/V$

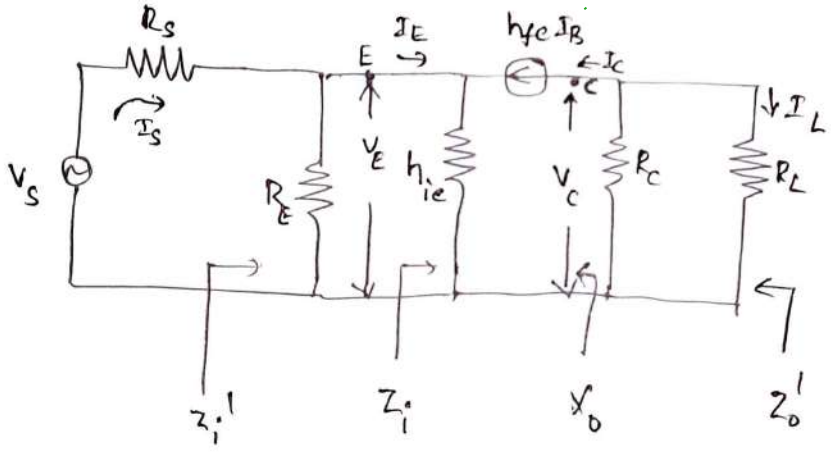
Calculate A_I, Z_i, A_v, Y_o



Sol) Since $h_{oe} R_L' = 2\times10^{-6} \times (R_C \| R_E) = 2\times10^{-6} \times (5.6k\Omega \| 39.k\Omega)$

$= 9.79\times10^{-3}$

$\Rightarrow h_{oe} R_L' = 0.00979 < 0.1$ we go for approximate analysis



↳ Current Gain $A_I = \frac{h_{fe}}{1+h_{fe}} = \frac{85}{1+85} = 0.9884$

↳ Input impedance $(Z_i) = \frac{h_{ie}}{1+h_{fe}} = \frac{1\times10^3}{1+85} = 11.6279\,\Omega$

overall input impedance $(Z_i') = Z_i \| R_E = 11.6279 \| 5.6\times10^3$

$\therefore Z_i' = 11.60\,\Omega$

↳ voltage Gain $(A_v) = \frac{h_{fe} R_L'}{h_{ie}} = \frac{85 \times (39\times10^3 \| 5.6\times10^3)}{1\times10^3} = 416.23\,\Omega$

$(\because R_L' = R_L \| R_C)$

↳ output admittance $Y_0 = 0$

output impedance $Z_0 = \frac{1}{Y_0} = \frac{1}{0} = \infty$

overall output impedance $Z_0' = Z_0 \| R_L' = Z_0 \| R_c \| R_L$

$\Rightarrow Z_0' = \infty \| 5.6k\Omega \| 39k\Omega = 4.896k\Omega$

Miller's Theorem:

In general, the miller's theorem is used for converting any circuit having the configuration shown in figure(a) to another configuration shown in figure(b).

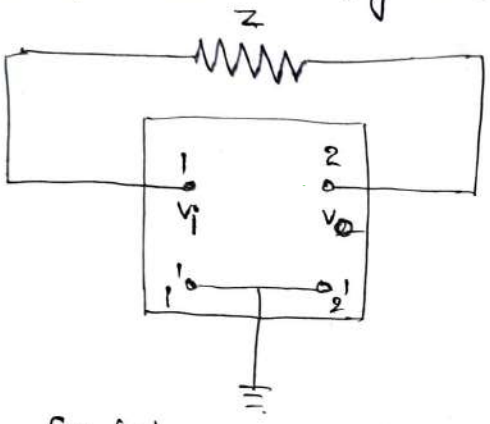
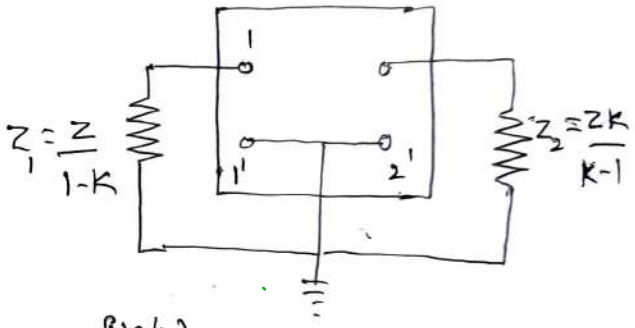


fig (a)



fig(b)

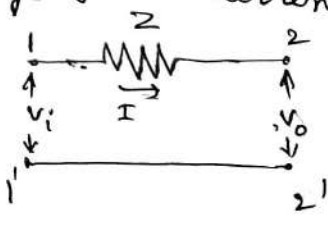
The above figures shows that, if the impedance 'Z' is connected between two nodes, node1 and node 2 it can be replaced by two seperate impedances Z_1 and Z_2 where Z_1 is connected between node 1 and ground and Z_2 is connected between Node 2 and Ground.

V_i and V_o are the voltages at node1 and node 2 with respect to Ground respectively. The values of Z_1 and Z_2 are derived from the ratio of V_o and V_i. Thus it is important to know the values of V_i and V_o to calculate Z_1 and Z_2.

proof:

Miller's theorem states that the effect of impedance 'Z' on the input circuit is a ratio of input voltage to the current I which flows from input to output

$\therefore Z_1 = \frac{V_i}{I} \Rightarrow Z_1 = \frac{V_i}{\left(\frac{V_i - V_o}{Z}\right)}$

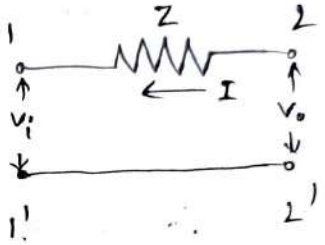


$$\Rightarrow \quad Z_1 = \frac{Z V_i}{V_i - V_o}$$

$$= \frac{Z V_i}{V_i \left(1 - \frac{V_o}{V_i}\right)}$$

$$\Rightarrow \boxed{Z_1 = \frac{Z}{1-K}} \qquad \text{where } K = \frac{V_o}{V_i}$$

Miller's theorem states that the effect of impedance on the output circuit is the ratio of the output voltage to the current flows from the output to the input.



$$Z_2 = \frac{V_o}{I}$$

$$\Rightarrow Z_2 = \frac{V_o}{\left(\frac{V_o - V_i}{Z}\right)}$$

$$\Rightarrow Z_2 = \frac{Z V_o}{V_o - V_i} = \frac{Z V_o}{V_o\left(\frac{V_o}{V_o} - \frac{V_i}{V_o}\right)} = \frac{Z}{1 - \frac{1}{(V_o/V_i)}}$$

$$\Rightarrow \quad Z_2 = \frac{Z}{1 - \frac{1}{K}} = \frac{ZK}{K-1}$$

$$\therefore \quad \boxed{Z_2 = \frac{ZK}{K-1}}$$

NOTE:

In the place of Z if we have R, (or) $j\omega L$ (or) $\frac{1}{j\omega C}$ then the following changes will occur

i) If $Z = R$, then $Z_1 = R_1 = \frac{R}{1-K}$ and $Z_2 = R_2 = \frac{RK}{K-1}$

ii) If $Z = j\omega L$ then $Z_1 = L_1 = \frac{L}{1-K}$ and $Z_2 = L_2 = \frac{LK}{K-1}$

iii) If $Z = \frac{1}{j\omega C}$ then $Z_1 = C_1 = C(1-K)$ & $Z_2 = C_2 = \frac{C(K-1)}{K}$

UNIT - II

FEEDBACK AMPLIFIERS

Introduction:

Feedback plays a very important role in electronic circuits and the parameters such as input impedance, current gain, voltage gain, output impedance and bandwidth may be altered considerably by the use of feedback for a given amplifier.

In large signal amplifiers and electronic measuring instruments the major problem of distortion should be avoided as far as possible. And also the gain must be independent of external factors such as variation in dc supply voltage and the values of the circuit components. All this can be achieved with the help of feedback.

A portion of the output signal is taken from the output of the amplifier and is combined with the normal input signal to accomplish the feed-back for an amplifier.

Classification of Basic amplifiers:

The basic amplifiers are classified into four categories as voltage amplifier, current amplifier, transconductance amplifier and trans resistance amplifier based on the magnitudes of input and output resistances of an amplifier with respect to the source and load resistances. These basic amplifiers are used in feed-back amplifiers.

Voltage Amplifier:

The figure shows a thevenin's equivalent circuit of a voltage-amplifier.

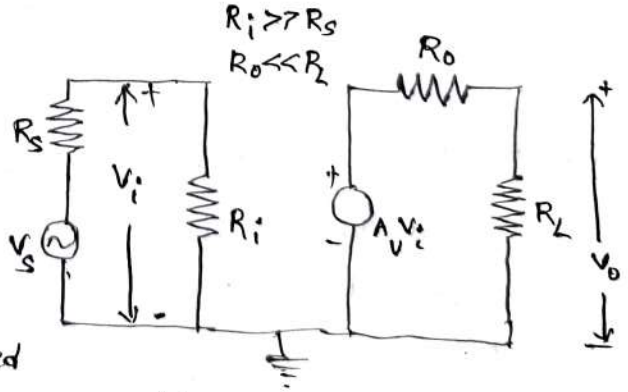


fig: voltage amplifier

An Ideal voltage amplifier is defined as an amplifier which provides the output voltage proportional to the input voltage and the proportionality factor doesnot depend on the magnitude of source and load resistances. An ideal voltage amplifier has

$V_o \simeq A_v V_s$

infinite input resistance (R_i) and zero output resistance (R_o). But a practical voltage amplifier has $R_i >> R_s$ and $R_o << R_L$.

The output voltage $V_o \simeq A_v V_i \simeq A_v V_s$ where A_v is the open circuit voltage gain with $R_L = \infty$.

Current Amplifier:

Figure shows the Norton's equivalent circuit for current amplifier. An ideal current amplifier is defined as an amplifier which provides the output current proportional to the input current and the proportionality factor is independent of R_s and R_L.

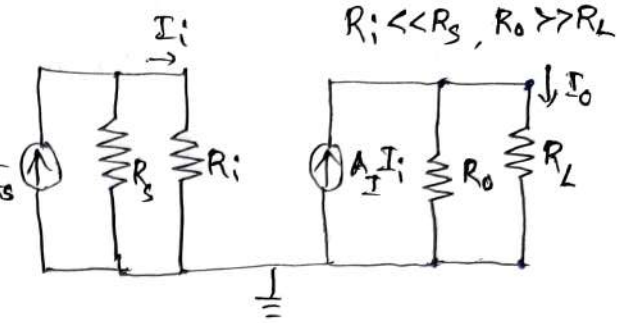


fig: Current amplifier

$I_o \simeq A_I I_s$

An ideal current amplifier has zero input resistance (R_i) and infinite output resistance (R_o). But practical current-amplifier has $R_i << R_s$ and $R_o >> R_L$.

The output current $I_o \simeq A_I \cdot I_i$, where A_I is the short circuit current gain with $R_L = 0$.

Transconductance amplifier:

Figure shows the transconductance amplifier in which the input circuit is thevenin and output circuit is norton.

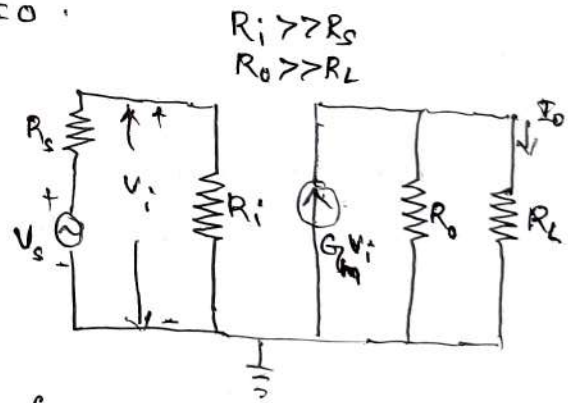


fig: Transconductance Amplifier

$I_o \simeq G_m V_s$

An Ideal transconductance amplifier is defined as an amplifier in which the output current is proportional to the input voltage and the proportionality factor is independent of R_s and R_L.

An ideal transconductance amplifier has $R_i = \infty$ and $R_o = \infty$. But practical transconductance amplifier has $R_i >> R_s$, $R_o >> R_L$.

The output current $I_o \simeq G_m V_i$, where G_m is short circuit transconductance with $R_L = 0$

Transresistance Amplifier:

Figure shows the transresistance amplifier in which the input is Norton and output is thevenin.

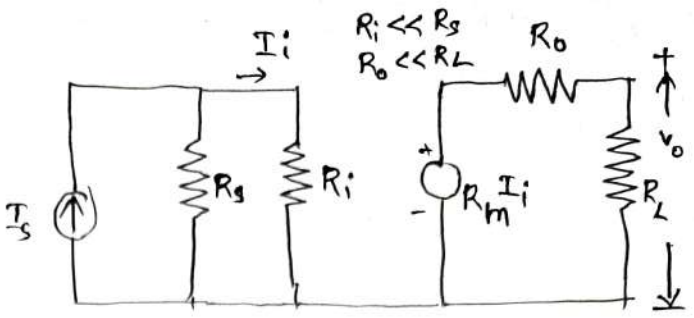


fig: Transresistance amplifier

$V_o \simeq R_m I_s$

An Ideal transresistance amplifier is defined as an amplifier the output voltage is proportional to the input current and proportionality factor is independent of the values of R_s and R_L.

For an ideal transresistance amplifier $R_i = 0$ and $R_o = 0$. But in practical transresistance amplifier $R_i \ll R_s$ and $R_o \ll R_L$.

The output voltage $V_o = R_m \cdot I_i$ where R_m is opencircuit transfer resistance with $R_L = \infty$.

Basic Concept of feedback:

The block diagram of an amplifier with feedback is shown in below figure

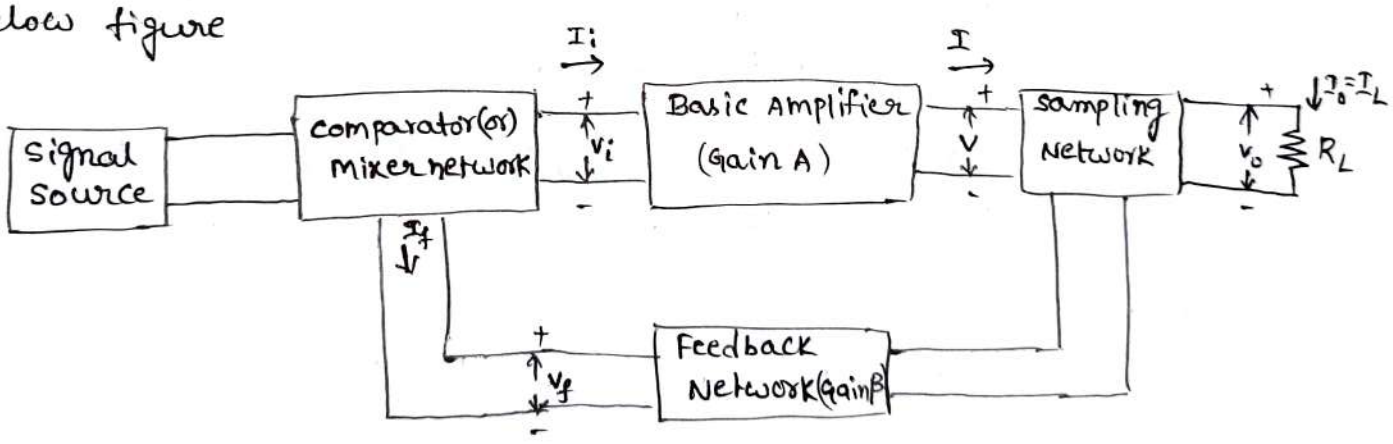


fig: Blockdiagram of an amplifier with feedback

In a feedback amplifier a basic amplifier is used that can be a voltage amplifier (or) a current amplifier (or) transconductance (or) transresistance amplifier. In each one of these circuits we may sample the output voltage (or) output current by means of a suitable sampling network which is of two types, namely, voltage sampler and current sampler. and apply the sampled signal to the

feed back network. The output of the feedback network is combined with the source signal through a mixer and fed to the basic amplifier.

Mixers are also known as comparators which are of two types series mixer and shunt mixer.

In the block diagram shown above we have

A = Gain of the basic amplifier = $\frac{V}{V_i}$

β = feed back ratio (or) reverse transmission factor

$= \frac{V_f}{V_o}$

A_f = gain of the feed back amplifier = $\frac{V_o}{V_s}$

V_s = signal voltage from the source.

V_f = feedback signal voltage.

The signal source in a feed back amplifier can be either a signal voltage V_s in series with a resistor R_s (or) a signal current I_s in parallel with a resistor R_s.

The feedback network may contain resistors, capacitors and inductors. Most often it is simply a resistive configuration.

If sampling network is a voltage sampler, the output voltage is sampled by connecting the feedback network in shunt across the o/p. If it is a current sampler the output current is sampled by connecting the o/p to feedback network in series.

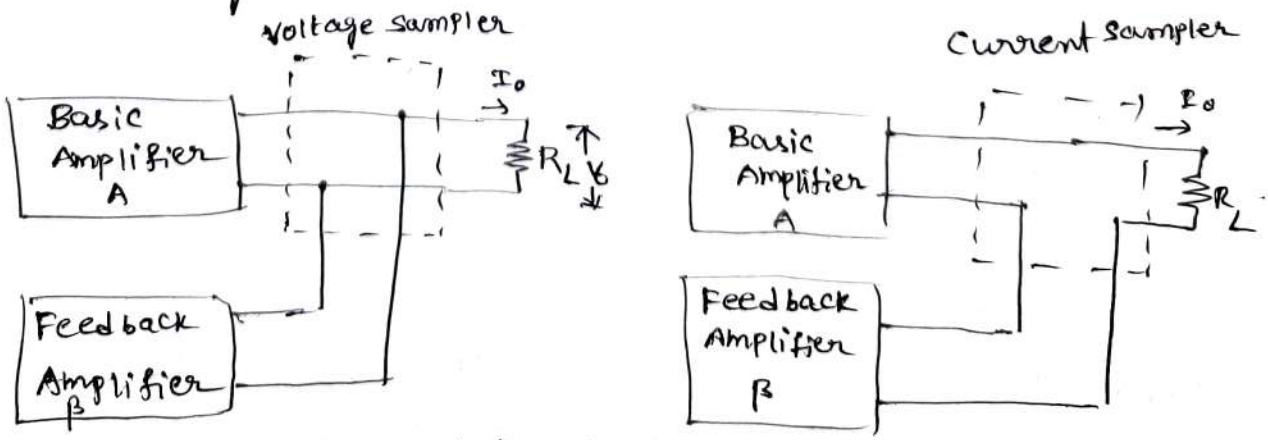


Fig:- Feedback Connections at the o/p of a basic amplifier, sampler o/p.

Mixer (or) comparator network is used for combining the feedback signal with the input signal. There are two types of mixer networks series mixer and shunt mixer as shown in below.

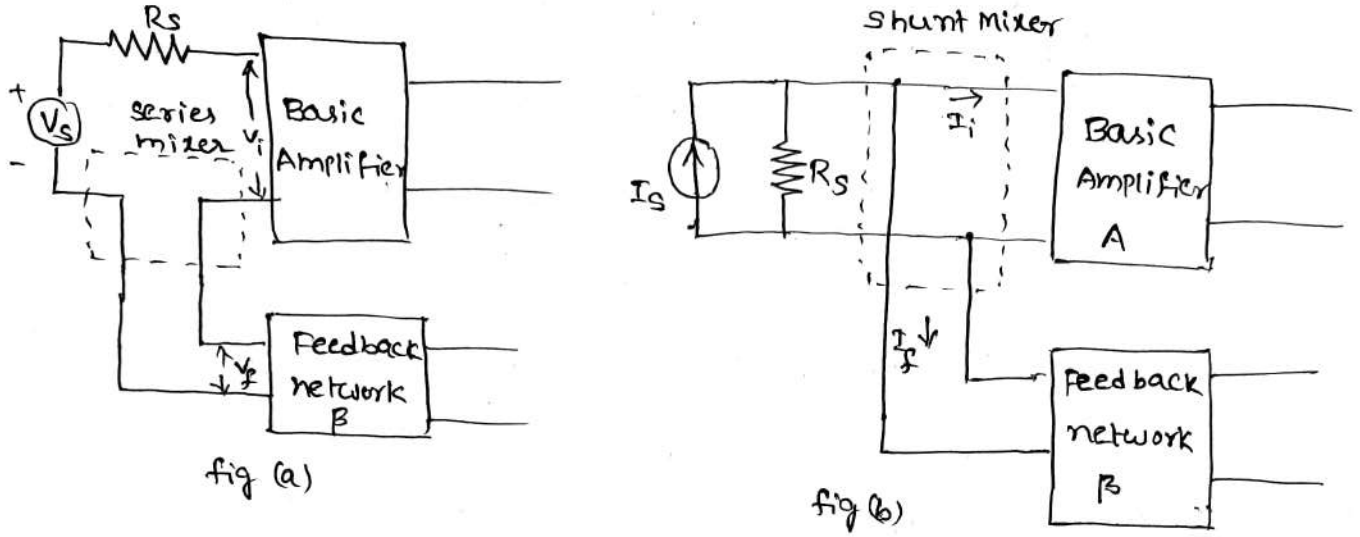


fig: Feedback connections at the input of the basic amplifier
fig(a) using series mixing fig(b) using shunt mixing

Transfer ratio (or) Gain:

The ratio of the output signal to the input signal of a basic amplifier is called as transfer ratio denoted as 'A'.

The transfer ratio V/V_i is the voltage gain denoted by A_V. Similarly the transfer ratio $\frac{I}{I_i}$ is the current gain denoted by A_I.

The transfer ratio $\frac{I}{V_i}$ is the trans conductance denoted by G_m. and the transfer ratio $\frac{V}{I_i}$ is the transresistance R_M.

Generally each of these four A_V, A_I, G_M and R_M are referred as the transfer gain of the basic amplifier without feedback and we use the symbol A to represent any one of these quantities.

The symbol A_f is defined as the ratio of the output signal to the input signal of the amplifier and is called as transfer gain of the amplifier with feedback. Hence A_f is used to represent any one of the four ratios $\frac{V_o}{V_s} = A_{Vf}$, $\frac{I_o}{I_s} = A_{If}$, $\frac{I_o}{V_s} = G_{mf}$, $\frac{V_o}{I_s} = R_{mf}$

Schematic representation (or) the general structure of a feedback amplifier:

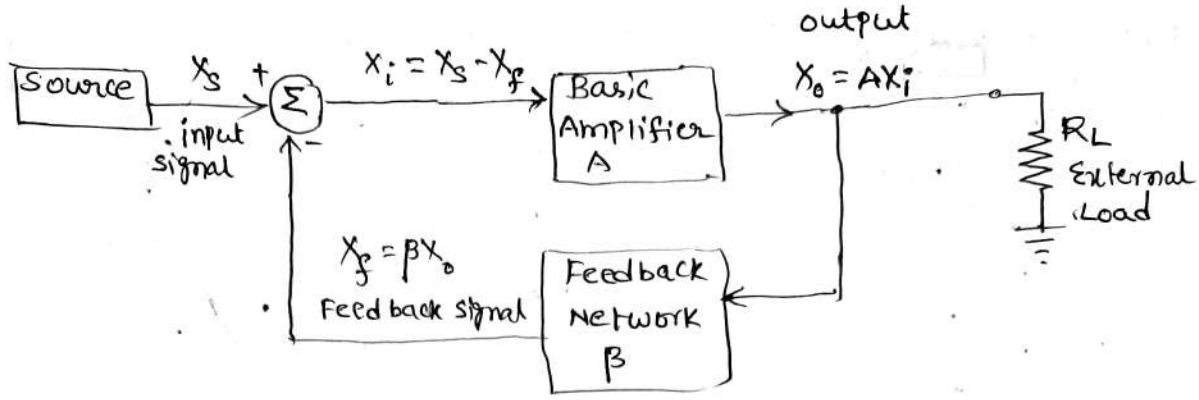


fig: Schematic representation of a single loop feed back amplifier.

The above figure shows the schematic representation of a feedback amplifier. Here X represents either voltage or current signals. when the feedback signal(X_f) and input signal (X_s) are out of phase that feedback is called negative feedback and if the feed back signal (X_f) and input signal (X_s) are in phase, that feedback is called as positive feedback.

Negative feed back is also called as degenerative feedback where as positive feed back is also called as regenerative feedback.

Positive feed back:

Positive feed back is also known as regenerative feedback. If the feedback signal (X_f) is in phase with the input signal X_s then that feed back is called as positive feedback. In this case, the positive feedback causes the input of the basic amplifier(X_i) to be increased, which causes the output (X_o) to increase.

The gain of amplifier with positive feed back is

$$A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i - X_f}$$

$$\Rightarrow A_f = \frac{1}{\left(\frac{X_i}{X_o}\right) - \left(\frac{X_f}{X_o}\right)} = \frac{1}{\left(\frac{1}{A}\right) - \beta} = \frac{A}{1 - A\beta}$$

$$\therefore A_f = \frac{A}{1 - A\beta}$$

Here $|A_f| > |A|$. The product of open loop gain and the feed back factor (β), is called as loop gain i.e loop gain = $A\beta$

If $|A\beta| = 1$ then $A_f = \infty$. Hence the gain of the amplifier with positive feedback is infinite and the amplifier gives an ac signal without ac input signal. Drawbacks of positive feedback is the positive feedback increases the instability of an amplifier, reduces the bandwidth and increases the distortion and noise.

The positive feedback is used in oscillators.

Negative feedback:

If the feedback signal (X_f) is out of phase with the input signal (X_s) then that feedback is called as negative feedback.

The negative feedback causes the input of the basic amplifier (X_i) to be decreased causing the output (X_o) to be decreased.

Negative feedback is also called as degenerat feedback.

The gain of the amplifier with negative feedback is

$$A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

$$\Rightarrow A_f = \frac{1}{\frac{X_i}{X_o} + \frac{X_f}{X_o}} = \frac{1}{\frac{1}{A} + \beta} = \frac{A}{1 + A\beta}$$

$$\therefore A_f = \frac{A}{1 + A\beta}$$

Here $|A_f|$ is less than $|A|$. If $|A\beta| >> 1$ then $A_f = \frac{1}{\beta}$ where β is feedback ratio. Then the gain A_f depends completely on feedback network.

If the feedback network contains only passive elements, the gain of the amplifier with negative feedback will be stable.

Advantages of negative feedback: (characteristics of negative feedback)

The stabilization of the operating point of a transistor amplifier is accomplished by using negative feedback with respect to the changes in dc supply voltage and the operating point is kept constant in the case of change in temperature or a change in h_{fe}

(or) β of a transistor.

Negative feedback is also used to improve the performance of an amplifier i.e frequency response is improved with negative feedback.

Negative feedback always helps to increase the bandwidth, decrease distortion and noise, modify the input and output resistances as desired.

All the above advantages are derived at an expense of reduction in voltage gain. But the amplifier with negative feedback provides a stabilised voltage gain.

Classification of feedback amplifiers (or) Feedback topologies:

Based on the type of sampling at output side and the type of mixing to the input side, feedback amplifiers are classified into four topologies. They are

1) Voltage series feedback (or) series shunt feedback
2) Current series feedback (or) series series feedback
3) Current shunt feedback (or) shunt series feedback
4) Voltage shunt feedback (or) shunt shunt feedback

The feedback amplifier topologies are given below.

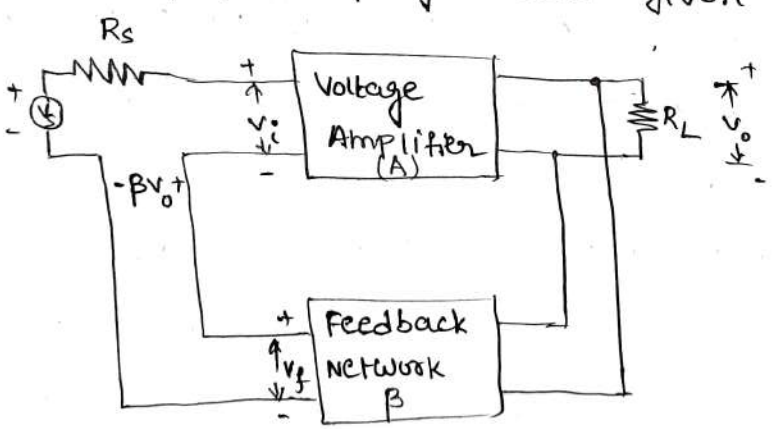


fig: Voltage series feedback Topology

(or) Voltage amplifier with Voltage series feedback

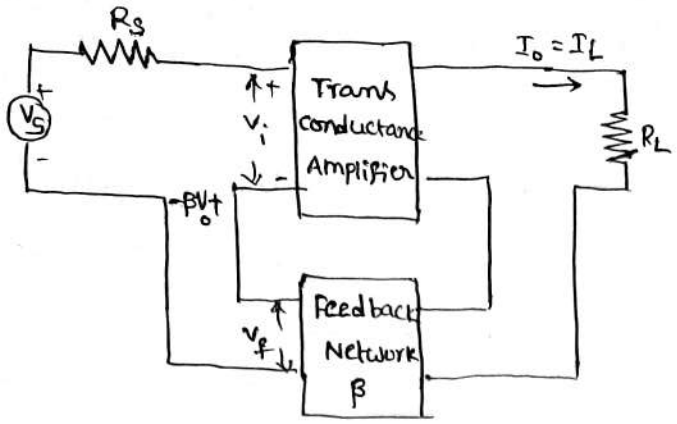


fig: Current series feedback (or) Transconductance amplifier with current series feed back.

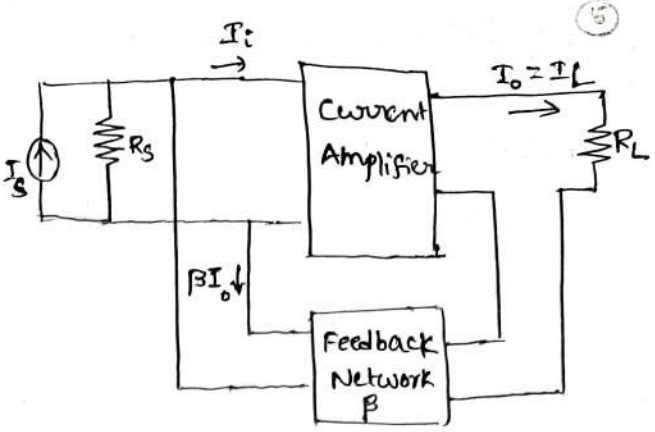


fig: current shunt feedback (or) current amplifier with current shunt - feedback

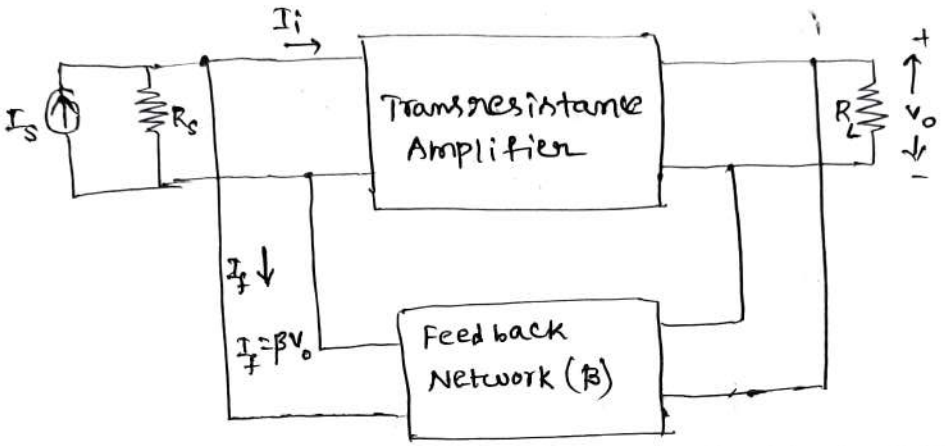


fig: Transresistance amplifier with feed back network i.e Voltage shunt feed back

Let the input signal as X_s, the output signal X_o, the feedback signal X_f and the input of the basic amplifier is X_i. These signals and the corresponding ratios A and β are listed below.

Signal (or) ratio	Voltage series feed back	Current series feed back	Current shunt feedback	Voltage shunt feed back
X_o	Voltage	Current	Current	Voltage
X_s, X_f and X_i	Voltage	Voltage	Current	Current
A	A_V	G_M	A_I	R_M
β	$\frac{V_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$	$\frac{I_f}{V_o}$

Characteristics of negative feed back amplifiers

1) Stability of gain (or) Desensitization :

The gain of the amplifiers is not constant in general as it depends on the factors such as temperature, ageing of the components and temperature dependent parameters. This lack of stability can be reduced by introducing negative feed back.

we know that the expression for gain with feedback

$$A_f = \frac{A}{1+A\beta} \longrightarrow (1)$$

differentiating A_f with respect to A.

$$\frac{dA_f}{dA} = \frac{(1+A\beta)\cdot(1) - A\cdot(\beta)}{(1+A\beta)^2}$$

$$\frac{dA_f}{dA} = \frac{1}{(1+A\beta)^2}$$

multiplying both sides with $\frac{1}{A_f}$ we get

$$\frac{dA_f}{dA}\cdot\frac{1}{A_f} = \frac{1}{(1+A\beta)^2}\cdot\frac{1}{A_f}$$

$$\frac{dA_f}{dA}\cdot\frac{1}{A_f} = \frac{1}{(1+A\beta)^2}\cdot\frac{1}{\frac{A}{(1+A\beta)}}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A}\cdot\frac{1}{(1+A\beta)}$$

$$\Rightarrow \left(\frac{dA_f}{A_f}\right)\Big/\left(\frac{dA}{A}\right) = \frac{1}{1+A\beta}$$

$$\therefore S = \frac{1}{1+A\beta} \longrightarrow (2)$$

The fractional change in amplification with feedback is divided by the fractional change in amplification with out feedback is called as sensitivity of the transfer gain denoted by S

The reciprocal of sensitivity is known as desensitivity denoted by D. i.e $D = \frac{1}{S} = \frac{1}{(1/1+A\beta)} = 1+A\beta$ → (3)

From equation (1) and (2) $A_f = \frac{A}{D}$

In equation (1) if $\beta A >> 1$ then $A_f = \frac{A}{1+\beta A} \simeq \frac{A}{\beta A} \simeq \frac{1}{\beta}$

Thus the gain A_f is made to depend entirely on feedback network. If the feed back network contains only passive elements the improvement in stability is achieved.

Then the voltagain $A_{vf} \simeq 1/\beta$ for voltage series feed back, Transconductance $G_{mf} \simeq \frac{1}{\beta}$ for current series feed back, the current gain $A_{If} \simeq \frac{1}{\beta}$ for a current shunt feed back and the trans resistance $R_{mf} \simeq \frac{1}{\beta}$ for a voltage shunt feed back is achieved.

2) Extension of bandwidth :

we know that the gain of the amplifier with negative feed back is given as $A_f = \frac{A}{1+A\beta}$ → (1)

Then we can write $A_{fmid} = \frac{A_{mid}}{1+A_{mid}\beta}$ → (2)

$A_{flow} = \frac{A_{low}}{1+A_{low}\beta}$ → (3)

$A_{fhigh} = \frac{A_{high}}{1+A_{high}\beta}$ → (4)

The effect of negative feedback on lower cut-off and upper-cut off frequencies of the amplifier is analysed here.

Lower cut-off frequency : (f_{Lf})

we know that the relation between the gain at lower-cut off frequency and the gain at mid band frequency of an amplifier is given as $A_{low} = (A_{mid}) / \left[1 - j\left(\frac{f_L}{f}\right)\right]$ → (5)

Substitute equation (5) in equation (3) we get

$$A_{f\,low} = \frac{(A_{mid})/(1 - j\frac{f_L}{f})}{1 + \left[A_{mid}/(1 - j\frac{f_L}{f})\right]\cdot\beta}$$

$$= \frac{A_{mid}}{1 - j\frac{f_L}{f} + A_{mid}\,\beta}$$

$$\therefore = \frac{A_{mid}}{(1 + A_{mid}\beta) - j\frac{f_L}{f}}$$

Dividing the numerator and the denominator with $\frac{1}{1 + A_{mid}\beta}$ we get

$$A_{f\,low} = \frac{\frac{A_{mid}}{(1 + A_{mid}\cdot\beta)}}{1 - j\left(\frac{f_L}{1 + A_{mid}\,\beta}\right)\frac{1}{f}}$$

$$A_{f\,low} = \frac{A_{fmid}}{1 - j\left(\frac{f_{Lf}}{f}\right)} \qquad \left(\text{since } A_{fmid} = \frac{A_{mid}}{1 + A_{mid}\,\beta}, \text{ let } f_{Lf} = \frac{f_L}{1 + A_{mid}\,\beta}\right)$$

where $f_{Lf} = \frac{f_L}{1 + A_{mid}\beta}$ is the lower cut-off frequency with feed back.

From this equation of f_{Lf} it is clear that the lower cutoff frequency of an amplifier with feed back (f_{Lf}) is lesser than that of the lower cut off frequency of an amplifier without feed-back (f_L) by a factor $(1 + A_{mid}\beta)$. Thus by introducing negative feedback, low frequency response of an amplifier is improved.

Higher Cut-off frequency (f_{Hf}):

We know that $A_{high} = \frac{A_{mid}}{1 + j\left(\frac{f}{f_H}\right)}$ ⟶ (6)

Substituting equation (6) in equation (4) we get

$$A_{f\,high} = \left[\frac{A_{mid}}{1 + j\left(\frac{f}{f_H}\right)}\right] \Big/ \left[1 + \left(\frac{A_{mid}}{1 + j\left(\frac{f}{f_H}\right)}\right)\cdot\beta\right]$$

$$\Rightarrow A_{f\,high} = \frac{A_{mid}}{1 + j\frac{f}{f_H} + A_{mid}\beta}$$

$$\Rightarrow A_{f\,high} = \frac{A_{mid}}{(1 + A_{mid}\beta) + j\frac{f}{f_H}}$$

Dividing the numerator and denominator of RHS with $1 + A_{mid}\beta$ we get

$$A_{f\,high} = \frac{\frac{A_{mid}}{1 + A_{mid}\beta}}{1 + j\frac{f}{f_H(1 + A_{mid}\beta)}} = \frac{A_{f\,mid}}{1 + j\frac{f}{f_{Hf}}}$$

where $A_{f\,mid} = \frac{A_{mid}}{1 + A_{mid}\beta}$ and $f_{Hf} = f_H(1 + A_{mid}\beta)$

f_{Hf} is the higher cut off frequency of an amplifier with feedback.

From the equation of f_{Hf} it is clear that upper cut off frequency of an amplifier with feedback (f_{Hf}) is greater than the upper cut off frequency of an amplifier without feedback (f_H) by a factor $1 + A_{mid}\beta$. Therefore by introducing negative feedback high frequency response of the amplifier is improved.

The bandwidth of an amplifier without feedback is given as $BW = f_H - f_L$.

The bandwidth of an amplifier with feedback is

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{mid}\beta)f_H - \frac{f_L}{(1 + A_{mid}\beta)}$$ or

it can also be written as $BW_f = BW(1 + A_{mid}\beta)$

It is very clear that $f_{Hf} - f_{Lf} > f_H - f_L$. So bandwidth of the amplifier with feedback is greater than the bandwidth of amplifier without feedback.

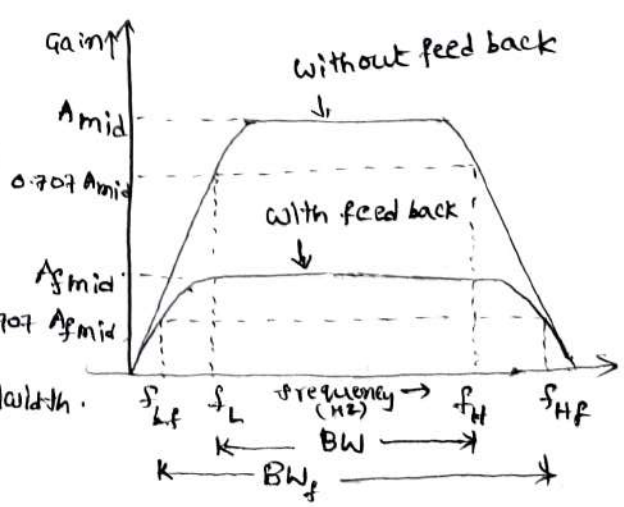


fig: Effect of negative - feedback on gain and bandwidth.

Note: As the voltage gain of the feedback amplifier reduces by a factor $1+A\beta$ and it's bandwidth increases by $1+A\beta$, the product of gain bandwidth product remains same for with feedback and for without feedback. $A_f \times BW_f = \left(\frac{A}{1+A\beta}\right) \times BW(1+A\beta)$

$$\therefore \boxed{A_f \times BW_f = A \times BW}$$

3) Frequency distortion: (or) Phase distortion reduction

If the feedback network doesnot contain reactive elements, the gain of the feedback amplifier is not a function of frequency. Under these circumstances the frequency distortion or Phase distortion can be reduced.

If feedback factor β is made up of reactive elements, the reactances of those elements will change with frequency, causing β to be changed. As a result feedback amplifier gain will also changes with frequency. So feedback network should be made up of passive elements.

4) Reduction in nonlinear distortion:

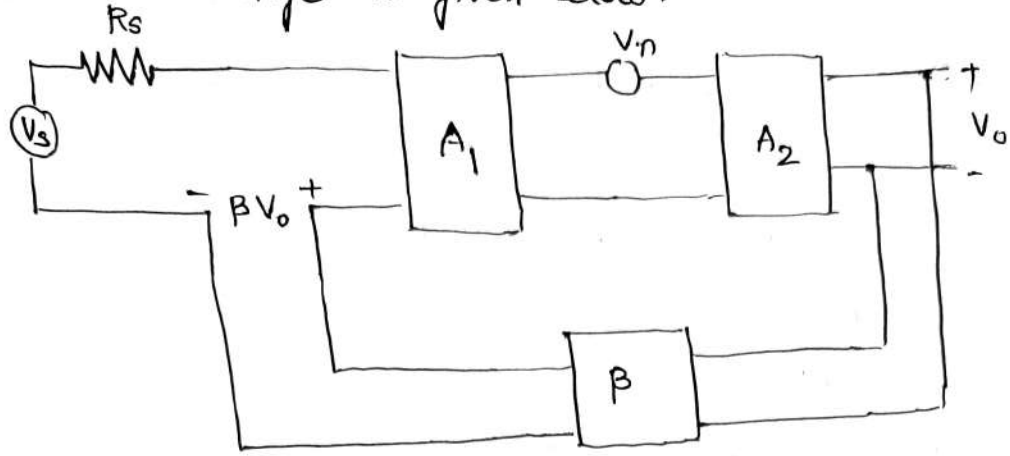
Consider a feed back amplifier with negative feed back, that has a basic amplifier with gain A and assume that the amplifier has the distortion 'D' without feedback and the distortion D_f with feed back. Then the distortion 'D' is reduced by a factor $1+A\beta$ and the distortion with feedback is given by $D_f = \frac{D}{1+A\beta}$.

5) Reduction in noise:

The negative feedback for an amplifier reduces the noise by increasing the ratio of signal to noise. Consider the amplifier block that has noise signal 'V_n' and gain A_2. Assume the input signal is V_s and the noise V_n is introduced at the second stage of amplifier as shown in below. The signal to noise ratio is given by

$$\frac{S}{N} = \frac{V_s}{V_n}.$$

The first stage of the amplifier with gain A_1 does not suffer from noise. This two stage amplifier with negative feedback having noise at 2nd stage is given below.



The output voltage V_o is given by

$$V_o = \frac{V_s A_1 A_2}{1 + A_1 A_2 \beta} + \frac{V_n A_2}{1 + A_1 A_2 \beta}$$

Signal to noise ratio at the output $= \left(\frac{V_s A_1 A_2}{1 + A_1 A_2 \beta}\right) \Big/ \left(\frac{V_n A_2}{1 + A_1 A_2 \beta}\right)$

$$\therefore \frac{S}{N} = \frac{V_s}{V_n} A_1$$

$\therefore$ Signal to noise ratio increases by a factor A_1. This improvement in signal to noise ratio results in reduction in noise.

The effect of negative feedback on input resistance:

Consider the negative feedback in an amplifier.

i) When the output of this negative feedback is connected to the input in series with the input signal the input resistance is increased. Since the feedback signal voltage V_f is out of phase with input voltage V_s that causes the input current I_i to be decreased and hence the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback R_i. Hence the input resistance with feed back (R_{if}) for voltage series feedback and current series feedback is

$$R_{if} = R_i (1 + A\beta) = R_i D.$$

ii) When the negative feedback signal is fed back to the input in shunt

with the amplifier input signal, then the input resistance is decreased. Since feedback current I_f and input current I_s are in out of phase then $I_i = I_s - I_f$. i.e $I_s = I_i + I_f$. Then the source input current I_s is increased and the input resistance with feed back $R_{if} = \frac{V_i}{I_s}$ is smaller than the input resistance without feedback i.e $R_{if} < R_i$. Hence for Voltage shunt and current shunt feedback amplifiers $R_{if} = \frac{R_i}{1+A\beta} = \frac{R_i}{D}$

That means the series mixing at input tends to increase the input resistance and the shunt mixing tends to decrease the input resistance.

1) Input resistance for voltage series feed back amplifier: The following fig shows the voltage series feedback circuit with the input circuit and output circuit replaced by thevenin's model. In this circuit A_v represents the open circuit voltage gain taking R_s into account. We have considered R_s being the part of the amplifier for determing input resistance.

For the voltage series feedback amplifier input resistance with feedback $R_{if} = \frac{V_s}{I_i}$.

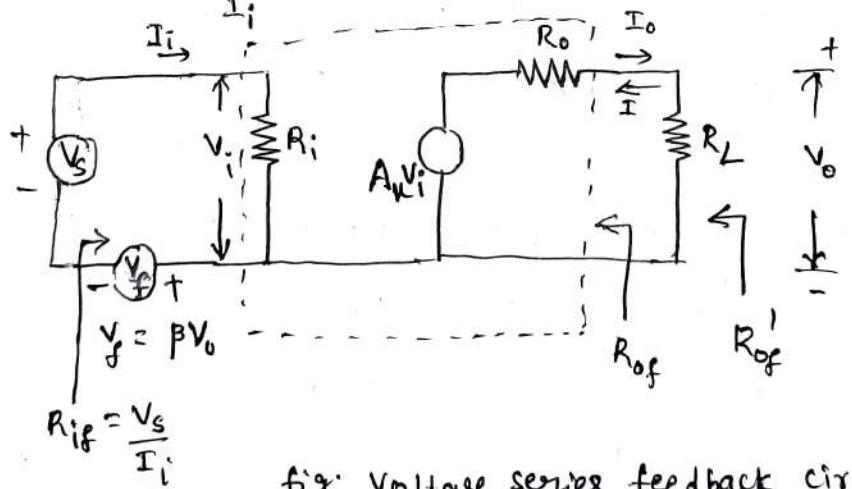


fig: Voltage series feedback circuit

Applying KVL to the input side $V_s = I_i R_i + V_f = I_i R_i + \beta V_o \rightarrow (1)$

out voltage $V_o = \frac{A_v V_i R_L}{R_o + R_L} = A_V V_i$ where $A_V = \frac{A_v R_L}{R_o + R_L} \rightarrow (2)$

From Equation ①, ② $V_s = I_i R_i + \beta V_o = I_i R_i + \beta A_V V_i$

$$\Rightarrow V_s = I_i R_i + \beta A_V I_i R_i$$

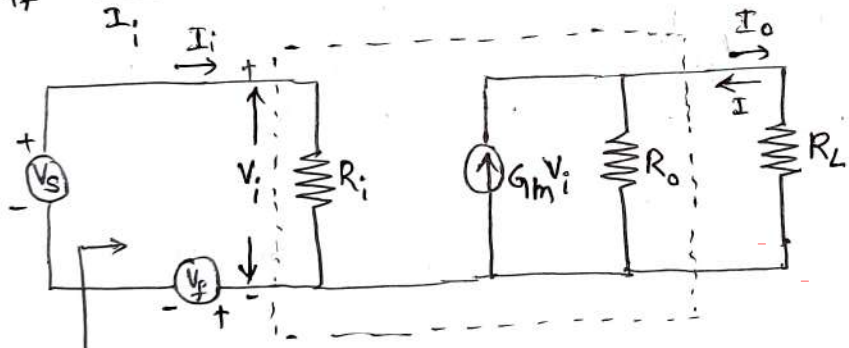
$$\Rightarrow V_s = I_i R_i (1 + \beta A_V)$$

$$\therefore \frac{V_s}{I_i} = R_{if} = R_i (1 + \beta A_V)$$

where A_u represents opencircuit voltage gain without feed back and A_V indicates the circuit voltage gain without feed back taking R_L into account. Therefore $A_u = \lim_{R_L \to \infty} A_V$

2) Input resistance for Current Series feedback amplifier:

Fig shows the current series feedback amplifier circuit with input circuit represented by thevenin's model and output circuit by Norton's equivalent circuit. Here input resistance with feedback is given by $R_{if} = \frac{V_s}{I_i}$.



$V_f = \beta I_o$

$R_{if} = \frac{V_s}{I_i}$

fig: current series feedback amplifier circuit

Applying KVL to the input side,

$$V_s = I_i R_i + V_f = I_i R_i + \beta I_o \longrightarrow ①$$

The output current is written as

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \longrightarrow ②$$

where $G_M = \frac{G_m R_o}{R_o + R_L}$

From equations ① and ② $V_s = I_i R_i + \beta I_o = I_i R_i + \beta G_M V_i$

$$\Rightarrow V_s = I_i R_i + \beta G_M I_i R_i$$

$$\Rightarrow V_S = I_i R_i (1+\beta G_M)$$

$$\Rightarrow \frac{V_s}{I_i} = R_i (1+\beta G_M)$$

$$\therefore \frac{V_S}{I_i} = R_{if} = R_i (1+\beta G_M)$$

where G_m represents short circuit transconductance without feedback and G_M represents transconductance without feed back taking R_L into account.

$$G_m = \lim_{R_L \to 0} G_M$$

3) Input resistance for current shunt feedback amplifier:

The fig' below shows the current shunt feedback amplifier circuit with input and output circuits replaced by norton's equivalent circuits. Here the input resistance with feedback is given by $R_{if} = \frac{V_i}{I_S}$.

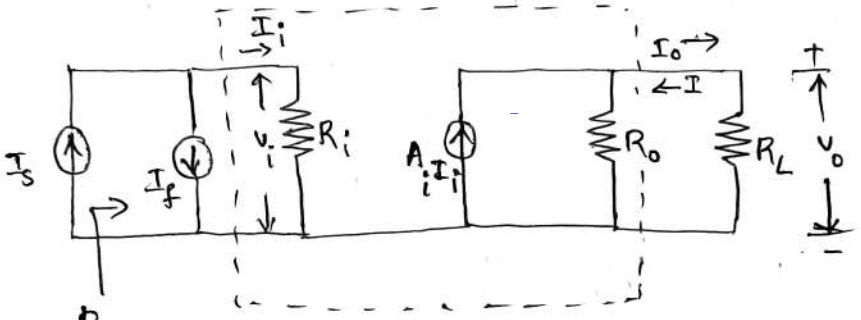


fig: Current shunt feedback amplifier circuit

Applying KCL at the input side $I_S = I_i + I_f = I_i + \beta I_o \longrightarrow (1)$

output current $I_o = \frac{A_i I_i R_o}{R_o + R_L} = A_I I_i \longrightarrow (2)$

where $A_I = \frac{A_i R_o}{R_o + R_L}$

From equations (1) and (2) $I_S = I_i + \beta A_I I_i = I_i (1+\beta A_I)$

$$\Rightarrow I_s = \frac{V_i}{R_i}(1+\beta A_I)$$

$$\therefore \frac{V_i}{I_S} = R_{if} = \frac{R_i}{1+\beta A_I}$$

where A_i represents the short circuit current gain without feedback and A_I represents the current gain without feedback taking R_L into account.

$$\therefore A_i = \lim_{R_L \to 0} A_I$$

4) Input resistance for Voltage Shunt feedback amplifier:

The following figure shows the voltage shunt feedback amplifier with input circuit is represented by Norton's equivalent circuit and the output circuit by thevenin's equivalent circuit. Here the input resistance with feedback is $R_{if} = \frac{V_i}{I_s}$

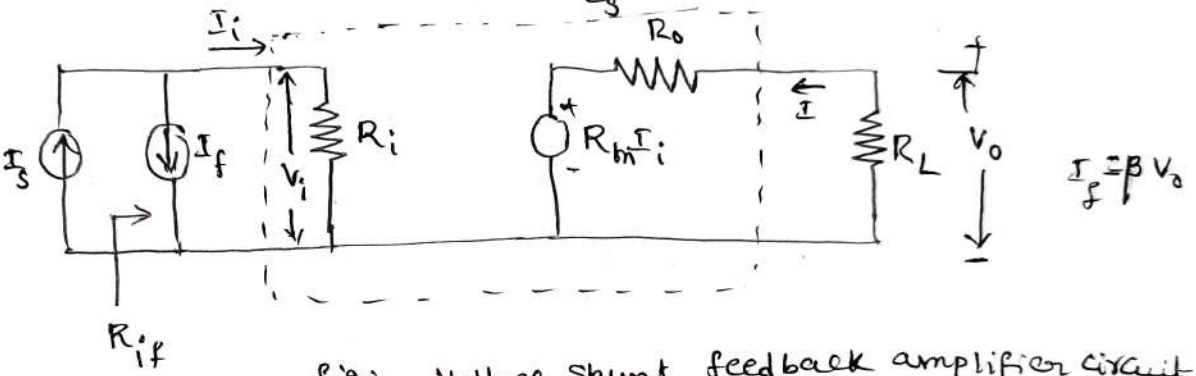


fig: Voltage shunt feedback amplifier circuit

Applying KCL at input circuit $I_s = I_i + I_f = I_i + \beta V_o \longrightarrow (1)$

The output voltage $V_o = \frac{R_m I_i R_L}{R_o + R_L} = R_M I_i \longrightarrow (2)$

where $R_M = \frac{R_m R_L}{R_o + R_L}$

From the equations (1) and (2) $I_s = I_i + \beta R_M I_i$

$$\Rightarrow I_s = I_i (1 + \beta R_M) = \frac{V_i}{R_i}(1 + \beta R_M)$$

$$\Rightarrow \frac{V_i}{I_s} = \frac{R_i}{1 + \beta R_M}$$

where R_m represents the open circuit transresistance without feedback and R_M represents the transresistance without feedback taking load R_L into account. Therefore $R_m = \lim_{R_L \to \infty} R_M$

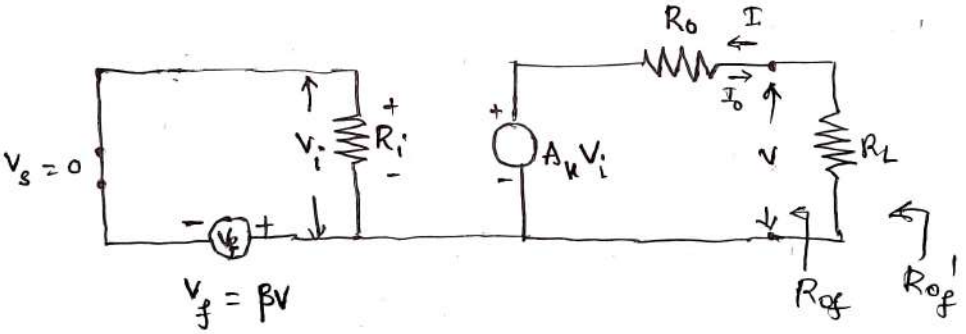
Effect of negative feedback on output resistance

The negative feedback which samples the output voltage irrespective of type of mixing at input side, decreases the output resistance. i.e voltage sampling causes the output resistance of the feedback amplifiers to decrease.

Similarly the negative feed back which samples the output current increases the output resistance irrespective of the type of mixing at input side. i.e current sampling increases the output resistance of the feedback amplifiers.

1) output resistance for a voltage series feedback amplifier:

In voltage series feedback amplifier the output resistance R_{of} is obtained by looking into the output terminals by disconnecting R_L (i.e $R_L = \infty$) and making source voltage V_s zero. (i.e $V_s = 0$)



Applying KVL to the output circuit

$$A_v V_i + I R_o = V \quad \longrightarrow (1)$$

We know that $V_s - V_f = V_i$

Since $V_s = 0$, $V_i = -V_f$.

$$V_i = -(\beta V) \quad \longrightarrow (2)$$

From equation (1) and (2)

$$A_v(-\beta V) + I R_o = V \qquad (\because V_f = \beta V \text{ with } V_s = 0)$$

$$V(1 + A_v\beta) = I R_o \Rightarrow \frac{V}{I} = \frac{R_o}{1 + A_v\beta}$$

$$\therefore \boxed{R_{of} = \frac{R_o}{1 + A_v\beta}}$$

Now $R'_{of} = R_{of} \| R_L$

$$= \left(\frac{R_o}{1+A_v\beta} \cdot R_L\right) \Big/ \left(\frac{R_o}{1+A_v\beta} + R_L\right)$$

$$\Rightarrow R'_{of} = \frac{R_o R_L}{R_o + R_L(1+A_v\beta)} = \frac{R_o R_L}{R_o + R_L + R_L A_v \beta}$$

Dividing numerator and denominator with $R_o + R_L$ we get

$$R'_{of} = \left(\frac{R_o R_L}{R_o + R_L}\right) \Big/ \left(1 + \frac{R_L A_v \beta}{R_o + R_L}\right)$$

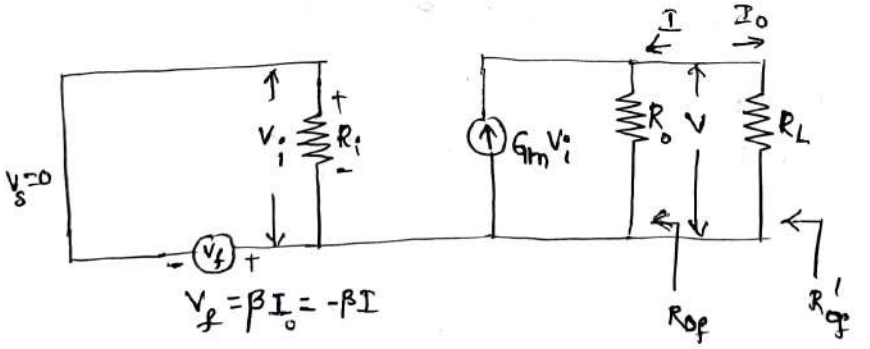
$$\boxed{R'_{of} = \frac{R'_o}{1 + A_V \beta}} \quad \left(\text{where } \frac{A_v R_L}{R_o + R_L} = A_V\right)$$

and $R'_o = \frac{R_o R_L}{R_o + R_L}$

where A_v is the open circuit voltage gain without feedback; and A_V is the voltage gain without feedback taking R_L into account.

2) output resistance for a current series feedback amplifier:

In this amplifier the output resistance is measured by looking into the output terminals disconnecting R_L (i.e $R_L = \infty$) and the external source voltage signal V_s is made zero.



Applying KCL to the output circuit $G_m V_i = \frac{V}{R_o} - I$

$$\Rightarrow I = \frac{V}{R_o} - G_m V_i \rightarrow (1)$$

we know that $V_s - V_f = V_i$

since $V_s = 0$, $-V_f = V_i$

$$\therefore V_i = -V_f = -(-\beta I) \rightarrow (2)$$

substituting equation (2) in equation (1) we get $I = \frac{V}{R_o} - G_m(\beta I)$

$$\Rightarrow I(1+G_m\beta) = \frac{V}{R_o}$$

$$\Rightarrow \frac{V}{I} = R_o(1+G_m\beta)$$

$$\therefore R_{of} = R_o(1+G_m\beta)$$

$$R_{of}' = R_{of} \| R_L = \frac{R_{of} R_L}{R_{of}+R_L} = \frac{R_o(1+\beta G_m) R_L}{R_o(1+\beta G_m)+R_L}$$

$$\Rightarrow R_{of}' = \frac{R_o R_L (1+\beta G_m)}{R_o + R_L + R_o \beta G_m}$$

Dividing numerator and denominator with $R_o + R_L$

$$R_{of}' = \frac{\left(\frac{R_o R_L}{R_o+R_L}\right)(1+\beta G_m)}{1+\frac{R_o \beta G_m}{R_o+R_L}} = \frac{R_o'(1+\beta G_m)}{1+\beta G_M}$$

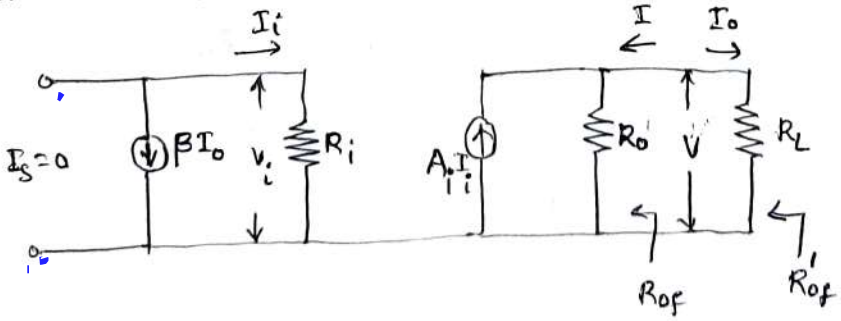
$$\therefore \boxed{R_{of}' = \frac{R_o'(1+\beta G_m)}{1+\beta G_M}} \quad \text{where } G_M = \frac{G_m R_o}{R_o+R_L}$$

Short circuit

where G_m is the transconductance without feedback and G_M is the transconductance without feedback taking R_L into account.

3) output resistance for a current shunt feedback amplifier:

In this amplifier the output resistance can be measured by looking into output terminals by disconnecting R_L and making the current source signal I_s zero.



Applying KCL at the output circuit we get

$$A_i I_i = \frac{V}{R_o} - I \quad \Rightarrow I = -A_i I_i + \frac{V}{R_o} \rightarrow (1)$$

we know that $I_s - I_f = I_i$

Since $I_s = 0$, $I_i = -I_f = -\beta I_o = \beta I$ $(\because I_o = -I)$

$$\therefore I_i = \beta I \quad \rightarrow (2)$$

Substituting equation (2) in equation (1) we get

$$I = -A_i \beta I + \frac{V}{R_o}$$

$$\Rightarrow \quad I(1 + A_i\beta) = \frac{V}{R_o}$$

$$\Rightarrow \quad \frac{V}{I} = R_o(1 + A_i\beta)$$

$$\therefore R_{of} = R_o(1 + A_i\beta)$$

$$R'_{of} = R_{of} \| R_L = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{R_o(1 + A_i\beta) R_L}{R_o(1 + A_i\beta) + R_L}$$

$$\Rightarrow R'_{of} = \frac{R_o R_L (1 + A_i\beta)}{R_o + R_L + R_o A_i \beta}$$

Divide the numerator and denominator by $R_o + R_L$

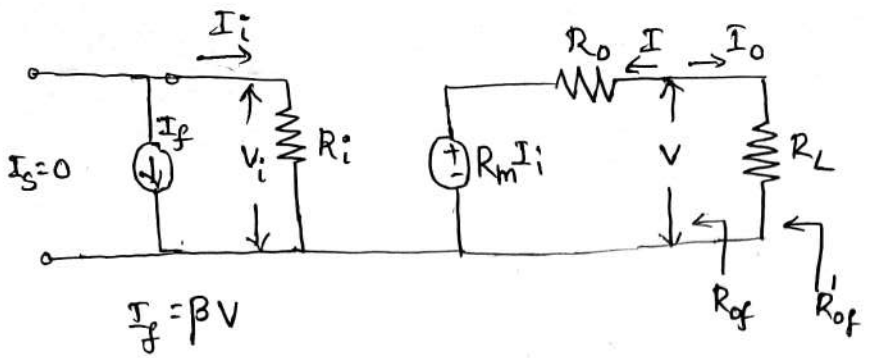
$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}(1 + A_i\beta)}{1 + \left(\frac{R_o}{R_o + R_L}\right) A_i \beta} = \frac{R'_o (1 + A_i\beta)}{1 + A_I \beta}$$

where $R'_o = R_o \| R_L$, $A_I = \frac{A_i R_o}{R_o + R_L}$

where A_i is the short circuit current gain without feedback and A_I is the current gain without feedback taking R_L into account

4) <u>output resistance of a voltage shunt feedback amplifier:</u>

Inthis amplifier the output resistance is measured by looking into output terminals by disconnecting R_L and making the current source signal I_s zero.



Applying KVL to the output side we get

$$V = R_m I_i + I R_o \longrightarrow (1)$$

We know that $I_S - I_f = I_i$.

since $I_S = 0$ $\quad I_i = -I_f = -\beta V \longrightarrow (2)$

substituting equation (2) in equation (1) we get

$$V = R_m(-\beta V) + I R_o$$

$$V(1+\beta R_m) = +I R_o$$

$$\therefore \frac{V}{I} = \frac{R_o}{1+\beta R_m}$$

$$\therefore R_{of} = \frac{R_o}{1+\beta R_m}$$

$$R'_{of} = R_{of} \| R_L = \frac{R_{of} R_L}{R_{of}+R_L} = \frac{\frac{R_o}{1+\beta R_m} R_L}{\frac{R_o}{1+\beta R_m} + R_L}$$

$$\Rightarrow R'_{of} = \frac{R_o R_L}{R_o + R_L(1+\beta R_m)} = \frac{R_o R_L}{R_o + R_L + R_L \beta R_m}$$

Dividing the numerator and denominator by $R_o + R_L$

$$R'_{of} = \frac{\left(\frac{R_o R_L}{R_o+R_L}\right)}{1 + \frac{R_L R_m}{R_o+R_L}.\beta} = \frac{R'_o}{1+R_M\beta}$$

where $R'_o = \frac{R_o R_L}{R_o+R_L}$ and $R_M = \frac{R_L R_m}{R_o+R_L}$

R_m is open circuit transresistance without feedback, R_M is the transresistance without feedback, taking R_L into account.

Expression for transfer gain of a negative feedback amplifier:

Let the input signal from source as X_s, the output signal X_o, the feed back signal X_f and the input of the basic amplifier as X_i, each of these represents either voltage or Current.

Then the difference between the applied input signal X_s and the feed back signal X_f is called as the difference signal (or) error (or) comparison signal denoted by X_i (or) X_d, given as

$$X_d = X_s - X_f = X_i \rightarrow (1) \text{ for negative feed back.}$$

The reverse transmission factor (or) feedback ratio of the feedback network, β is given as $\beta = \frac{X_f}{X_o} \longrightarrow (2)$

The transfer gain (or) transfer ratio of basic amplifier is A, and is given as $A = \frac{X_o}{X_i} \longrightarrow (3)$

considering the negative feedback, the transfer gain of the amplifier with negative feedback (A_f) is given as

$$A_f = \frac{X_o}{X_s} \longrightarrow (4)$$

$$= \frac{X_o}{X_i + X_f} \quad (\because \text{from equation (1) } X_s = X_i + X_f)$$

$$= \frac{1}{\frac{X_i}{X_o} + \frac{X_f}{X_o}}$$

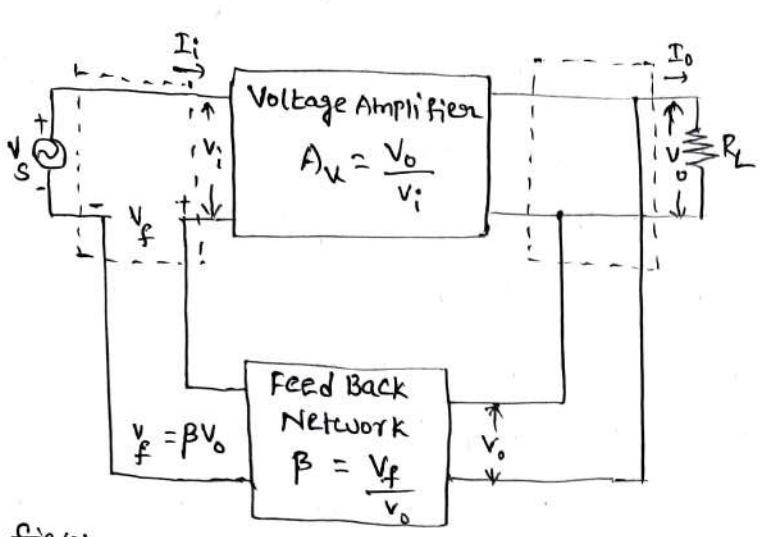
$$= \frac{1}{\frac{1}{A} + \beta} \quad (\because \text{from equations (2), (3)})$$

$$\therefore \boxed{A_f = \frac{A}{1 + A\beta}}$$

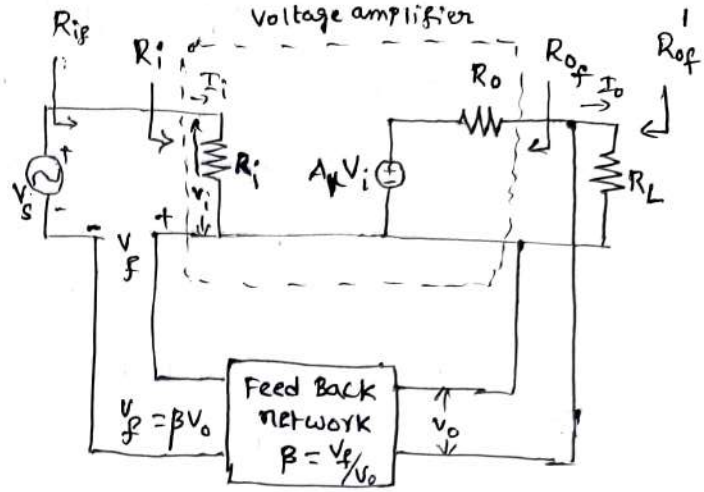
The expression for transfer gain of amplifier with negative feedback is denoted based on the type of basic amplifier.

The expression for transfergain of negative feedback amplifier for different basic amplifiers is derived below.

1) Transfer gain (or) Transfer ratio of a voltage series feed back amplifier:



fig(a) Voltage series feed back amplifier



fig(b): Equivalent circuit of Voltage series feedback amplifier.

* Figure (a) shows voltage series feedback amplifier, in which a part of the output voltage (V_f) is fed back in series with the input signal (V_s).

* The sampler used in voltage series feedback amplifier is voltage sampler. For voltage sampling the output voltage V_o is connected in shunt with the input of feed back network that has a feedback ratio of β.

* For combining the output of feedback network (V_f) with the input voltage (V_s), a series mixer is used i.e the output voltage of feedback network (V_f) is fed back in series with the input signal (V_s).

* The difference between V_s and V_f is applied as an input to the voltage amplifier, when the feed back connection is negative feedback.

$$\text{i.e} \quad V_i = V_s - V_f \longrightarrow (1)$$

Feedback ratio of the feedback network is β and is given as

$$\beta = \frac{V_f}{V_o} \longrightarrow (2)$$

The transfer gain of the voltage amplifier is A_v and is given as

$$A_v = \frac{V_o}{V_i} \longrightarrow (3)$$

The transfer gain of the voltage amplifier with feedback is given as

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{V_i + V_f} \quad (\because \text{from equation (1)}\ V_s = V_i + V_f)$$

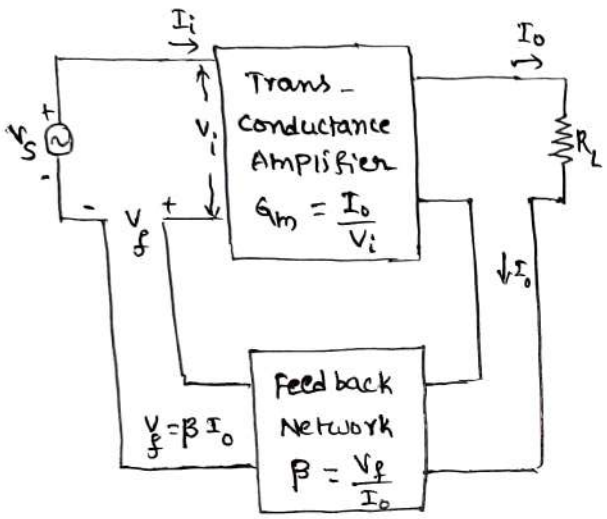
$$\Rightarrow \quad A_{Vf} = \frac{1}{\frac{V_i}{V_o} + \frac{V_f}{V_o}}$$

$$\Rightarrow \quad A_{Vf} = \frac{1}{\frac{1}{A_V} + \beta} \qquad (\because \text{from equations } ②, ③)$$

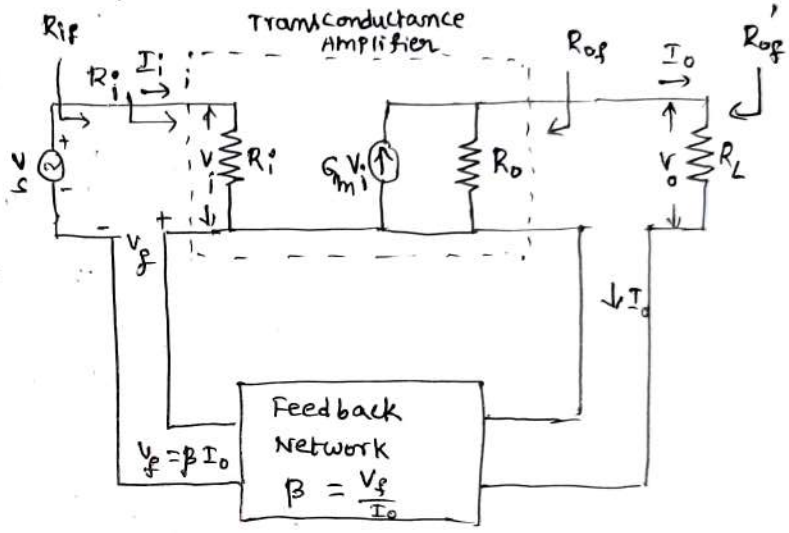
$$\therefore \boxed{A_{Vf} = \frac{A_V}{1 + A_V \beta}}$$

This equation says that the voltage gain with feedback is equal to the voltage amplifier gain reduced by a factor $1 + A_V\beta$.

2) Transfer gain (or) Transfer ratio of a current series feedback amplifier:



fig(a): Current series feedback Amplifier



fig(b): Equivalent Circuit of Current - Series feed back amplifier

* Figure (a) shows the current series feedback amplifier in which the value of the output current I_o is proportional to the developed voltage V_i.

* Here current sampler is used in a current series feedback amplifier. For current sampling the output current I_o is connected in series with the input of feedback network.

* For combining the output of feedback network (V_f) and the input voltage (V_s), a series mixer is used. i.e the output voltage (V_f) of the feedback network is fed back in series with the input voltage (V_s).

* The difference between V_s and V_f is applied as the input to

the transconductance amplifier, when feedback connection is negative feedback ie $V_i = V_s - V_f \longrightarrow (1)$

Feedback ratio of the feedback network is $\beta = \frac{V_f}{I_o} \rightarrow (2)$

The transfer gain of the transconductance amplifier is G_m and is given as $G_m = \frac{I_o}{V_i} \longrightarrow (3)$

The transfer gain of the trans conductance amplifier with feedback is G_{mf} and is given as $G_{mf} = \frac{I_o}{V_s} = \frac{I_o}{V_i + V_f}$ ($\because$ from eq(1) $V_s = V_i + V_f$)

$$\Rightarrow G_{mf} = \frac{1}{\frac{V_i}{I_o} + \frac{V_f}{I_o}}$$

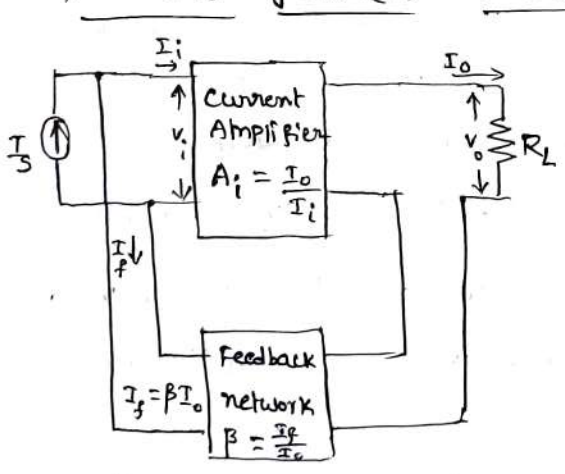
$$\Rightarrow G_{mf} = \frac{1}{\frac{1}{\frac{I_o}{V_i}} + \frac{V_f}{I_o}}$$

$$\Rightarrow G_{mf} = \frac{1}{\frac{1}{G_m} + \beta}$$ ($\because$ From equations ②, ③)

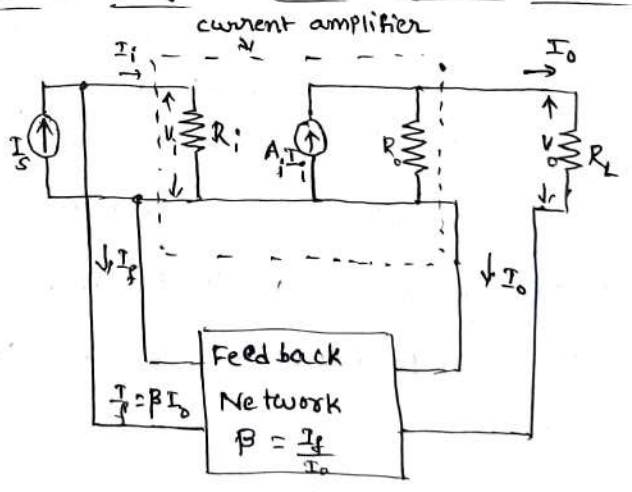
$$\therefore \boxed{G_{mf} = \frac{G_m}{1 + G_m \beta}}$$

This equation says that the transconductance with feedback is equal to transconductance without feedback reduced by a factor $1 + G_m \beta$.

3) Transfer gain (or) transfer ratio of a Current shunt feedback amplifier



fig(a): Current shunt - feed back amplifier



fig(b): equivalent circuit of a Current - shunt feedback amplifier.

* figure(a) shows the current shunt feedback amplifier block diagram
* In this amplifier, the current sampler is used. For current sampling the output current I_o is connected in series with the input of the feedback network.
* For combining the output of feedback network (I_f) and the input current I_s, a shunt mixer is used. i.e the output current I_f of the feedback network is fedback in shunt with the input current I_s.
* The difference between I_s and I_f is applied as the input to the current amplifier provided the feedback connection is negative feedback.

$$\text{i.e } I_i = I_s - I_f \longrightarrow (1)$$

Feed Back ratio of the feedback network is β given as

$$\beta = \frac{I_f}{I_o} \longrightarrow (2)$$

The transfer gain of current amplifier is A_i and is given as

$$A_i = \frac{I_o}{I_i} \longrightarrow (3)$$

The transfergain of current amplifier with negative feedback is given as

$$A_{if} = \frac{I_o}{I_s} = \frac{I_o}{I_i + I_f} \quad \left(\because \text{from equation (1)}\ I_s = I_i + I_f\right)$$

$$= \frac{1}{\left(\frac{I_i}{I_o}\right) + \left(\frac{I_f}{I_o}\right)}$$

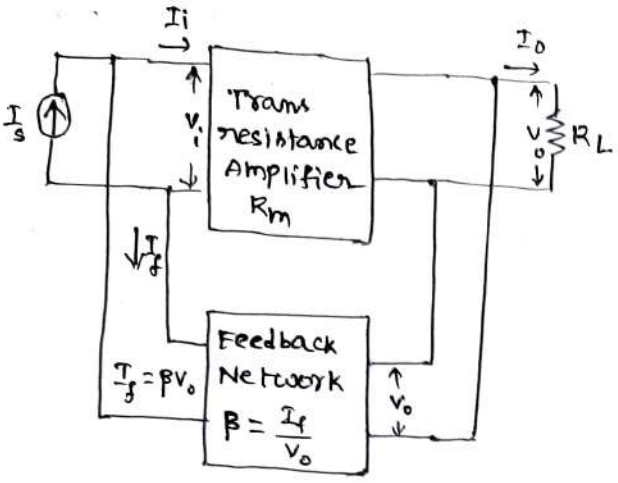
$$= \frac{1}{\frac{1}{\left(\frac{I_o}{I_i}\right)} + \frac{I_f}{I_o}}$$

$$= \frac{1}{\frac{1}{A_i} + \beta} \quad (\because \text{from equations (2), (3)})$$

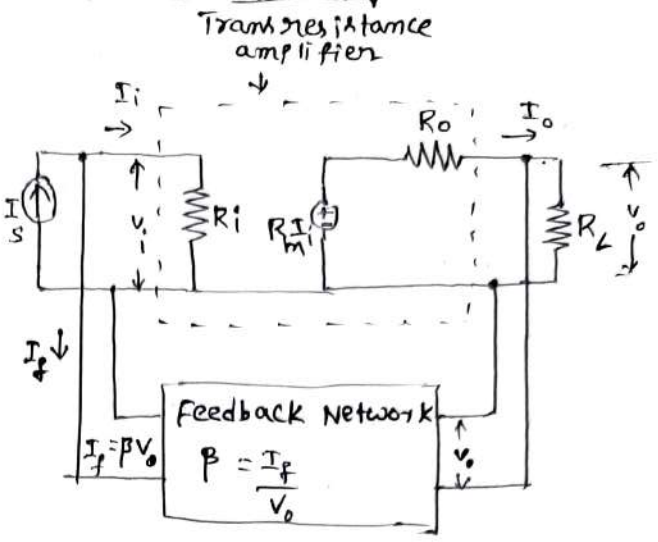
$$\therefore \boxed{A_{if} = \frac{A_i}{1 + A_i\beta}}$$

the above equation says that the current gain with negative feedback is equal to the Current gain without feedback reduced by a factor of $1 + A_i\beta$.

4) Transfer gain (or) transfer ratio of a voltage shunt feedback amplifier:



fig(a): Voltage shunt feedback Amplifier



fig(b): Equivalent circuit of a voltage - shunt feedback amplifier.

* figure (a) shows the voltage shunt feedback amplifier block diagram.
* In this amplifier the voltage sampler is used. For voltage sampling the output voltage (V_o) is connected in parallel with the input of the feedback network.
* For combining the output current (I_f) of the feedback network and the input current I_s, shunt mixing is used. i.e the output current (I_f) of the feedback network is fedback in parallel to the Input current (I_s).
* The difference between I_s and I_f is applied as the input to the transresistance amplifier provided the feedback is negative feedback.

$$\text{ie} \quad I_i = I_s - I_f \longrightarrow (1)$$

Feedback ratio of the feedback network is β and is given as

$$\beta = \frac{I_f}{V_o} \longrightarrow (2)$$

The transfer gain of the transresistance amplifier is R_m given as

$$R_m = \frac{V_o}{I_i} \longrightarrow (3)$$

The transfer gain of the transresistance amplifier with feedback is R_{mf} given as $R_{mf} = \frac{V_o}{I_s} = \frac{V_o}{I_i + I_f}$ ($\because$ from equation ① $I_s = I_i + I_f$)

$$\Rightarrow R_{mf} = \frac{1}{\frac{I_i}{V_o} + \frac{I_f}{V_o}}$$

$$= \frac{1}{\frac{1}{R_m} + \beta} \quad (\because \text{from equations ②, ③})$$

$$\therefore \boxed{R_{mf} = \frac{R_m}{1 + R_m\beta}}$$

The above equation says, the transresistance with negative feedback is equal to the transresistance without feedback reduced by a factor of $1 + R_m\beta$.

Method of analysis of a feedback amplifier:

For analysing the feedback amplifier it is necessary to go through the following steps.

Step 1: Identify the topology (type of feedback)

(a) To identify the type of sampling:

i) By shorting the output node (ie making $V_o = 0$), if the feedback signal becomes zero, then it is called voltage sampling

ii) By opening the output loop (ie making $I_o = 0$), if the feedback signal becomes zero, then it is called current sampling

(b) To identify the type of mixing:

i) If the feedback signal is subtracted from the externally applied signal as a voltage in the input loop it is called series mixing.

ii) If the feedback signal is subtracted from the externally applied signal as a current in the input loop, it is called shunt mixing.

Step 2: To find the input circuit

i) For voltage sampling, the output voltage is made zero by shorting the output node.

ii) for current sampling, the output current is made zero by opening the output loop.

Step3: To find the output circuit

i) For series mixing, the input current is made zero by opening the input loop.

ii) For shunt mixing, the input voltage is made zero by shorting the input node.

From step2 and step3 ensure that the feedback is reduced to zero, without altering the loading on the basic amplifier.

Step4: Replace each active device by proper model. for example the hybrid-π model for a transistor at high frequencies, or the h-parameter model at low frequencies.

Step5: Find A, i.e the open loop gain of the amplifier (gain without feedback).

Step6: Indicate X_f (i.e whether V_f (or) I_f) and X_o (i.e whether V_o (or) I_o) on the circuit and evaluate $\beta = X_f/X_o$.

Step7: From A and β find D, A_f, R_{if}, R_{of} and R_{of}'.

Comparison among the characteristics of feedback amplifiers:

Topology / Characteristics	Voltage series	Current series	Current shunt	Voltage shunt
1) Feed back signal (X_f)	Voltage (V_f)	Voltage (V_f)	Current (I_f)	Current (I_f)
2) Sampled signal (X_o)	Voltage (V_o)	Current (I_o)	Current (I_o)	Voltage (V_o)
3) To find the input circuit	Set $V_o = 0$	Set $I_o = 0$	Set $I_o = 0$	Set $V_o = 0$
4) To find the output circuit	Set $I_i = 0$	Set $I_i = 0$	Set $V_i = 0$	Set $V_i = 0$
5) Signal source	Thevenin	Thevenin	Norton	Norton
6) $\beta = \frac{X_f}{X_o}$	V_f/V_o	V_f/I_o	I_f/I_o	I_f/V_o
7) $A = \frac{X_o}{X_i}$	$A_V = V_o/V_i$	$G_M = I_o/V_i$	$A_I = \frac{I_o}{I_i}$	$R_M = \frac{V_o}{I_i}$
8) Desensitivity $D = 1+A\beta$	$1 + A_V\beta$	$1 + G_M\beta$	$1 + A_I\beta$	$1 + R_M\beta$
9) $A_f = A/(1+A\beta)$	$A_{Vf} = A_V/(1+A_V\beta)$	$G_{Mf} = G_M/(1+G_M\beta)$	$A_{If} = A_I/(1+A_I\beta)$	$R_{Mf} = R_M/(1+R_M\beta)$
10) R_{if}	$R_i(1+A_V\beta)$	$R_i(1+G_M\beta)$	$R_i/(1+A_I\beta)$	$R_i/(1+R_M\beta)$
11) R_{of}	$R_o/(1+A_V\beta)$	$R_o(1+G_M\beta)$	$R_o(1+A_i\beta)$	$R_o/(1+R_M\beta)$
12) R_{of}'	$R_o'/(1+A_V\beta)$	$R_o'(1+G_M\beta)/(1+G_M\beta)$	$R_o'(1+A_i\beta)/(1+A_I\beta)$	$R_o'/(1+R_M\beta)$

Problems

1) The distortion in amplifier is found to be 3%, when the feedback ratio of negative feedback amplifier is 0.04. when the feedback is removed, the distortion becomes 15%. Find the open loop gain & closed loop gain

Sol) Given negative feed back amplifier having feedback ratio $\beta = 0.04$

Distortion in amplifier with negative feedback is $D_f = 3\%$.

i.e $D_f = 0.03$

Distortion in amplifier when feed back is removed $D = 15\% = 0.15$

we know that $D_f = \frac{D}{1+A\beta} \Rightarrow 0.03 = \frac{0.15}{1+A(0.04)}$

$\Rightarrow 0.03 + A(0.0012) = 0.15$

$\therefore$ open loop gain $(A) = 100$

Closed loop gain $A_f = \frac{A}{1+A\beta}$ for negative feed back

$= \frac{100}{1+(100)(0.04)}$

$\therefore A_f = 20$

$\therefore$ open loop gain $A = 100$, closed loop gain $A_f = 20$.

2) An amplifier has midband voltage gain 500 with lower and upper cutoff frequencies as 100Hz and 100KHz respectively. If 5% feedback is applied find lower and upper cut off frequencies with feed back.

sol) Given $A_{Vmid} = 500$, $f_L = 100Hz$, $f_H = 100KHz$

feedback factor $\beta = 5\% = 0.05$

$f_{Lf} = ?$ $f_{Hf} = ?$

we know that f_{Lf} for negative feed back is given as

$f_{Lf} = \frac{f_L}{1+A_{mid}\beta} = \frac{100}{1+(500)(0.05)} = 3.84615\ Hz$

f_{Hf} for negative feed back amplifier is

$f_{Hf} = f_H(1+A_{mid}\beta) = 100\times10^3\left(1+(500)(0.05)\right)$

$\therefore f_{Hf} = 2.6MHz$

$\therefore$ Lower cutoff frequency with feedback $f_{Lf} = 3.84615\ Hz$

Upper cutoff frequency with feed back $f_{Hf} = 2.6\ MHz$.

3) A voltage series negative feedback amplifier has a voltage gain without feedback of $A = 50$, input resistance $R_i = 2K\Omega$, output resistance $R_o = 15K\Omega$, feed back ratio of 0.01. Calculate the voltage gain, input resistance and output resistance of amplifier with feedback.

Sol) Given A negative feed back voltage series amplifier.

Voltage gain without feed back $A_V = 50$

Input resistance without feedback $R_i = 2K\Omega$

output resistance without feed back $R_o = 15K\Omega$

Feedback ratio $\beta = 0.01$

Voltage gain with feedback $A_{Vf} = \frac{A_V}{1 + A_V\beta} = \frac{50}{1 + (50)(0.01)} = 33.3333$

Input resistance with feed back $R_{if} = R_i(1 + A_V\beta)$

$= 2 \times 10^3 (1 + 50(0.01))$

$\therefore R_{if} = 3K\Omega$

output resistance with feedback $R_{of} = \frac{R_o}{1 + A_V\beta} = \frac{15 \times 10^3}{1 + (50(0.01))}$

$\therefore R_{of} = 10K\Omega$

4) An amplifier has a midband gain of 1500 and a bandwidth of 4MHZ. The midband gain reduces to 150 when a negative feedback is applied. Determine the value of feedback factor and the bandwidth.

Sol) Given $A_{mid} = 1500$, $BW = 4MHZ = 4 \times 10^6$ HZ

Mid band gain reduces to 150 when negative feed back is applied.

i.e $A_{fmid} = 150$, Let feed back factor $= \beta$

we know that $A_{fmid} = \frac{A_{mid}}{1 + A_{mid}\beta}$

$\Rightarrow \quad 150 = \frac{1500}{1 + (1500\beta)}$ 10

$\Rightarrow \quad 1 + 1500\beta = 10 \Rightarrow 1500\beta = 9$

$\therefore$ feedback factor $\beta = 0.006$

Bandwidth with negative feedback $BW_f = BW(1 + A_{mid}\beta)$

$= 4 \times 10^6 (1 + (1500 \times 0.006))$

$\therefore$ Bandwidth with negative feedback $(BW_f) = 40MHZ$

5) An amplifier with 2.5kΩ input resistance and 50kΩ output resistance has a voltage gain of 100. the amplifier is now modified to provide 5% negative feed back in series with the input. Calculate the voltage gain, input resistance & output resistance with feedback.

Sol) Given $A_V = 100$, $R_i = 2.5k\Omega$, $R_o = 50k\Omega$

Given Feedback factor $\beta = 0.05$ (∵ 5%) negative feedback.

Voltage gain with feed back $A_{Vf} = \frac{A_V}{1+A_V\beta} = \frac{100}{1+(100)(0.05)} = 16.6666$

According to the given data the amplifier here we have is voltage-series feed back amplifier, for which $R_{if} = R_i(1+A_V\beta)$ and

$$R_{of} = \frac{R_o}{1+A_V\beta}$$

Input resistance with feed back $R_{if} = R_i(1+A_V\beta)$

$= 2.50\times10^3 (1+(100)(0.05))$

$\therefore R_{if} = 15\ k\Omega$

output resistance with feed back $R_{of} = \frac{R_o}{1+A_V\beta} = \frac{50\times10^3}{1+(100)(0.05)}$

$\therefore R_{of} = 8.333\ k\Omega$

6) An amplifier has an open loop gain of 1000 and feedback ratio of 0.04. If the open loop gain changes by 10% due to temperature, find the percentage change in gain of the amplifier with feedback

Sol) Given open loop gain $A = 1000$

feed back ratio $\beta = 0.04$

Refer Problem No(13)
(wrong method)

Gain of amplifier with feed back $A_f = \frac{A}{1+A\beta} = \frac{1000}{1+(1000)(0.04)}$

$\Rightarrow A_f = 24.39024$

The open loop gain changes by 10% due to temperature variation.

∴ New open loop gain $A_1 = 1000 + 10\%$ of $1000 = 1100$.

Gain of amplifier with feed back $A_{1f} = \frac{A_1}{1+A_1\beta} = \frac{1100}{1+(100)(0.04)} = 24.444444$

% change in gain of the amplifier with feed back $= \frac{24.44444 - 24.39024}{24.39024} \times 100$

∴ % change in gain of amplifier with feedback = 0.2222%

⑦ The voltage gain of an amplifier without feedback is 60dB. It decreases to 40dB with feed back. Calculate feed back factor.

Sol) Given voltage gain of an amplifier with out feedback = 60 dB

$$\text{i.e } 20 \log_{10} A_V = 60$$

$$\log_{10} (A_V) = 3$$

$$A_v = 1000.$$

Voltage gain with feedback = 40 dB

$$\text{i.e } 20 \log_{10} A_{vf} = 40$$

$$\log_{10} A_{vf} = 2$$

$$A_{vf} = 100.$$

Feedback factor $\beta = ?$

we know that $A_{vf} = \frac{A_v}{1 + A_v \beta} \Rightarrow 100 = \frac{1000}{1 + (1000\beta)}$ (10)

$$\Rightarrow 1 + 1000\beta = 10$$

$\therefore$ feedback factor $(\beta) = 0.009$ Ans

⑧ An amplifier with negative feedback has a gain of 50. It is found that without feedback, an input signal of 0.1V is required to produce a given output. Where as with feedback the input signal must be 0.8V for the same output. Calculate the voltage gain and feedback ratio.

Sol) Given $A_{vf} = 50$,

$V_i = 0.1V$,

$V_o = ?$

with feedback the i/p signal must be equal to 0.8V.

$$\text{i.e } V_s = V_i + V_f = 0.8V$$

$$\Rightarrow V_s = 0.1 + V_f = 0.8V$$

$$V_f = 0.7V.$$

we know that $A_{vf} = \frac{V_o}{V_s} = 50$

$$\Rightarrow \frac{V_o}{0.8} = 50 \Rightarrow V_o = 40V.$$

Voltage gain without feed back $A_V = \frac{V_o}{V_i} = \frac{40}{0.1} = 400$

Feedback factor $(\beta) = \frac{V_f}{V_o} = \frac{0.7}{40} = 0.0175$

9) A current shunt feedback amplifier has a current gain of 100, $Z_i = 2K\Omega$, $Z_o = 15K\Omega$, find A_{if}, Z_{if}, Z_{of}. $\beta = 0.05$

Sol) Given $A_i = 100$, $\beta = 0.05$, $Z_i = 2K\Omega$, $Z_o = 15K\Omega$

$$A_{if} = \frac{A_i}{1+A_i\beta} = \frac{100}{1+(100)(0.05)} = 16.6666$$

$$Z_{if} = \frac{Z_i}{1+A_i\beta} = \frac{2\times10^3}{1+(100)(0.05)} = 333.333\Omega$$

$$Z_{of} = Z_o(1+A_i\beta) = 15\times10^3(1+(100)(0.05)) = 90K\Omega$$

10) A current series feedback amplifier has $G_M = 500\mho$, $R_i = 3K\Omega$ $R_o = 30K\Omega$, $\beta = 0.01$. Find G_{Mf}, R_{if}, R_{of}.

Sol) Given $G_M = 500\mho$ $R_i = 3K\Omega$ and $R_o = 30K\Omega$. $\beta = 0.01$

$$G_{Mf} = \frac{G_M}{1+G_M\beta} = \frac{500}{1+((500)(0.01))} = 83.3333\mho$$

$$R_{if} = R_i(1+G_M\beta) = 3\times10^3(1+(500)(0.01)) = 18\ K\Omega$$

$$R_{of} = R_o(1+G_M\beta) = 30\times10^3(1+(500)(0.01)) = 180K\Omega$$

11) A voltage shunt feedback amplifier has $R_M = 300\Omega$, $R_i = 2K\Omega$ and $R_o = 20K\Omega$. $\beta = 0.05$. Find R_{Mf}, R_{if} and R_{of}

Sol) Given $R_M = 300\Omega$, $R_i = 2K\Omega$, $R_o = 20K\Omega$

$$R_{Mf} = \frac{R_M}{1+R_M\beta} = \frac{300}{1+(300)(0.05)} = 18.75\Omega$$

$$R_{if} = \frac{R_i}{1+R_M\beta} = \frac{2\times10^3}{1+(300)(0.05)} = 125\Omega$$

$$R_{of} = \frac{R_o}{1+R_M\beta} = \frac{20\times10^3}{1+(300)(0.05)} = 1.25K\Omega.$$

12) An amplifier has a midband gain of 125 and a bandwidth of 250KHZ. a) If 4 j. -ve feedback is applied find new bandwidth and new gain b) If Bandwidth is restricted to 1MHZ find β value

Sol) Given $A_{mid} = 125$, $BW = 250\,KHZ$,

a) $\beta = 4\% = 0.04$ with negative feedback.

New Bandwidth $BW_f = BW(1 + A_{mid}\beta) = 250\times10^3(1+(125\times0.04))$

$BW_f = 1.5\,MHZ$

New Gain with negative feedback $A_f = \frac{A}{1+A\beta} = \frac{125}{1+(125)(0.04)} = 20.8333$

b) BW_f' is given as $BW_f' = 1MHZ$, then $\beta' = ?$

$BW_f' = BW(1 + A_{mid}\beta')$

$1\times10^6 = 250\times10^3(1 + 125\beta')$

$\Rightarrow \beta' = 0.024 = 2.4\%$

13) An amplifier has an open loop gain of 1000, feedback ratio of 0.04. If the open loop gain changes by 10% due to temperature. Find the percentage change in the gain of amplifier with feedback.

Sol) Given open loop gain $(A) = 1000$,

feedback ratio $(\beta) = 0.04$.

Given the fractional change in open loop gain $= \frac{dA}{A} = 10\% = 0.1$

Fractional change (percentage change) in gain of the amplifier, with feedback $= \frac{dA_f}{A_f} = ?$

we know that the sensitivity $S = \frac{\left(\frac{dA_f}{A_f}\right)}{\left(\frac{dA}{A}\right)} = \frac{1}{1+A\beta}$

$\Rightarrow \frac{\left(\frac{dA_f}{A_f}\right)}{0.1} = \frac{1}{1+(1000)(0.04)}$

$\Rightarrow \frac{dA_f}{A_f} = \frac{0.1}{41} = 0.002439$

$\Rightarrow \frac{dA_f}{A_f} = 0.2439\%$

$\therefore$ Percentage change in the gain of the amplifier with feed back i.e $\frac{dA_f}{A_f} = 0.2439\%$

14) An amplifier has a voltage gain with feedback of 100. If the gain without feedback changes by 20% and the gain with feedback is restricted to 2%, determine the open loop gain and feedback factor.

Sol) Given the voltage gain with feedback $A_f = 100$.

Fractional change in the gain without feedback $= \frac{dA}{A} = 20\% = 0.2$

Fractional change in the gain with feedback $= \frac{dA_f}{A_f} = 2\% = 0.02$

we know that $\left(\frac{dA_f}{A_f}\right) \Big/ \left(\frac{dA}{A}\right) = \frac{1}{1+A\beta}$

$\Rightarrow \quad \frac{0.02}{0.2} = \frac{1}{1+A\beta}$

$\Rightarrow \quad 1 + A\beta = 10$

we know that $A_f = \frac{A}{1+A\beta} \qquad (\because A_f = 100)$

$\Rightarrow \quad 100 = \frac{A}{10} \qquad (\because 1+A\beta = 10)$

$\Rightarrow \quad A = 1000$

$1 + A\beta = 10 \quad \Rightarrow \quad 1 + (1000\beta) = 10$

$\therefore \beta = 0.009$

$\therefore$ Open loop gain(A) = 1000, feedback factor $\beta = 0.009$.

15) An amplifier has open loop gain of 4000 and a feedback ratio of 0.05. If the open loop gain changes by 15% due to temperature Find the percentage change in the gain of the amplifier with feedback.

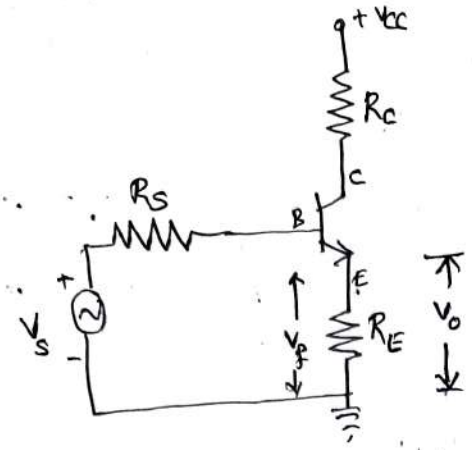
Sol) Given $A = 4000$, $\beta = 0.05$

$\frac{dA}{A} = 15\% = 0.15, \quad \frac{dA_f}{A_f} = ?$

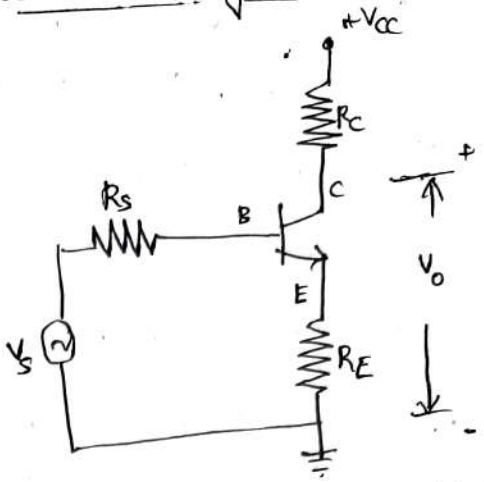
we know that $\frac{dA_f}{A_f} = \frac{(dA/A)}{1+A\beta} = \frac{0.15}{1+(4000)(0.05)}$

$\therefore \frac{dA_f}{A_f} = 0.07462\%$

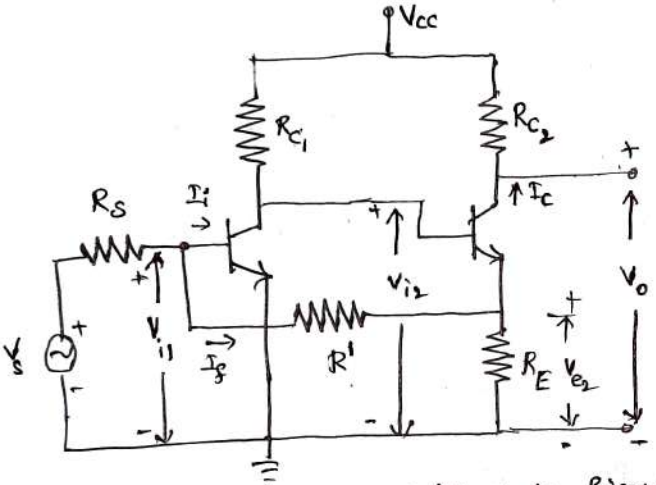
Practical circuits for different feedback topologies:



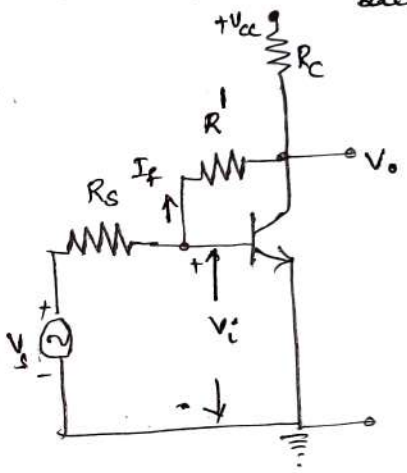
fig(a) BJT Emitter follower circuit (for voltage series feedback Amplifier)



fig(b): CE amplifier with unbypassed Emitter resistor (current series feedback amplifier)



fig(c): Second transistor emitter to first transistor base feedback pair (for Current Shunt feedback amplifier)



fig(d): Common Emitter with a resistor R' connected between input and output (for voltage Shunt feedback amplifier)

Explain the characteristics of negative feedback (or) Explain the effects of negative feedback on amplifier characteristics:

1) Stabilization of Gain:

The gain of the amplifier with negative feedback is

$$A_f = \frac{A}{1+A\beta} \rightarrow (1)$$

Differentiating the A_f with respect to A

$$\frac{dA_f}{dA} = \frac{(1+A\beta)(1) - A(\beta)}{(1+A\beta)^2} = \frac{1}{(1+A\beta)^2}$$

$$\Rightarrow \quad dA_f = \frac{dA}{(1+A\beta)^2}$$

2) Extension of bandwidth:

The difference between the upper cut off frequency and lower cut off frequency is called as the bandwidth of an amplifier given as Bandwidth $(BW) = f_H - f_L$.

The bandwidth of the amplifier with feedback increases by a factor of $(1+A\beta)$ i.e $BW_f = BW(1+A\beta)$. Because, due to negative feedback upper cut off frequency f_{Hf} is increased by a factor $(1+A\beta)$ and lower cut off frequency f_{Lf} is decreased by the same factor $(1+A\beta)$. i.e $f_{Hf} = f_H(1+A\beta)$, $f_{Lf} = \frac{f_L}{1+A\beta}$.

3) Frequency Distortion reduction (or) Phase distortion reduction:

If the feedback network does not contain reactive elements, the gain of the feedback amplifier is not a function of frequency. Under these circumstances the frequency distortion (or) phase-distortion can be reduced.

If feedback factor β is made up of reactive elements, the reactances of those elements will change with frequency, causing β to be changed. As a result feedback amplifier gain will also changes with frequency. so feedback network should be made up of passive elements.

4) Reduction in nonlinear distortion and noise:

The negative feedback introduced to an amplifier reduces both noise and non linear distortion by a factor $(1+A\beta)$. Thus noise and nonlinear distortion also reduced by the same factor as that of transfer gain.

5) Increase in input resistance:

An amplifier should have high input resistance. If the feedback signal is combined with the input source signal in series (i.e if the mixer used is a series mixer) the input resistance R_i increases with a factor $1+A\beta$. i.e $R_{if} = R_i(1+A\beta)$.

$$\Rightarrow \frac{dA_f}{A_f} = \frac{dA}{A_f(1+A\beta)^2}$$

$$\Rightarrow \frac{dA_f}{A_f} = \frac{dA}{\frac{A}{1+A\beta}(1+A\beta)^2}$$

$$\Rightarrow \left(\frac{dA_f}{A_f}\right) \Big/ \left(\frac{dA}{A}\right) = \frac{1}{1+A\beta}$$

$\therefore$ Sensitivity $S = \left(\frac{dA_f}{A_f}\right) \Big/ \left(\frac{dA}{A}\right) = \frac{1}{1+A\beta}$

Desensitivity $D = \frac{1}{S} = 1+A\beta$

The stability of the amplifier increases if the desensitivity is increased.

The gain of the amplifier is not constant as it depends on the factors such as temperature, aging of components, and temperature dependent parameters. This lack of stability can be reduced by introducing negative feedback.

The gain of amplifier with negative feedback is

$$A_f = \frac{A}{1+A\beta}$$

If $A\beta >> 1$ then $A_f = \frac{1}{\beta}$ and gain is dependent only on feedback network. Hence maintaining $A\beta >> 1$ and constructing feedback network only with stable passive elements a good stability is achieved.

Then for voltage series feedback $A_{Vf} = \frac{1}{\beta}$, voltage gain is stabilized

for Current series feedback $G_{Mf} = \frac{1}{\beta}$, transconductance is stabilized

For current shunt feedback $A_{If} = \frac{1}{\beta}$, Current gain is stabilized.

For voltage shunt feedback $R_{Mf} = \frac{1}{\beta}$, transresistance is stabilized

Thus the input resistance is increased with series mixer using negative feedback irrespective of the type of sampling.

6) Decrease in output resistance:

An amplifier with low output resistance is capable of delivering maximum power to the load without much loss. For such a low output resistance negative feedback is very helpful. The output resistance can be decreased by using a voltage sampler irrespective of the type of mixer; by a factor $(1+A\beta)$.

$$\text{i.e} \quad R_{of} = \frac{R_o}{1+A\beta} .$$

Effect of negative feedback on amplifier characteristics:

Characteristics	Type of feedback			
	Voltage series	Current series	Current shunt	Voltage shunt
Transfer gain	Decreases	Decreases	Decreases	Decreases
Bandwidth	Increases	Increases	Increases	Increases
Nonlinear Distortion	Decreases	Decreases	Decreases	Decreases
Noise	Decreases	Decreases	Decreases	Decreases
Input resistance	Increases	Increases	Decreases	Decreases
output resistance	Decreases	Increases	Increases	Decreases

UNIT - III
SINUSOIDAL OSCILLATORS

INTRODUCTION:

↦ Any circuit which is used to generate a periodic voltage without an ac input signal is called an oscillator. To generate the AC voltage the circuit is supplied with energy from a dc source.

↦ If the output voltage is a sine wave function of time, the oscillator is called as a sinusoidal oscillator (or) Harmonic oscillator.

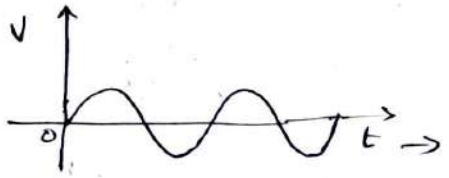
↦ There is an other category of oscillators which generate non-sinusoidal wave forms such as square, sawtooth, triangular or rectangular etc.

Classification of oscillators:

The oscillators can be classified in different ways.

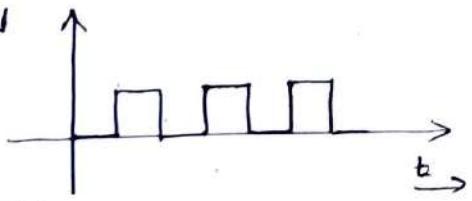
1) According to the wave forms generated
   a) sinusoidal oscillators
   b) Relaxation oscillators.

- sinusoidal oscillator generates voltage or current which is a sinewave function of time as shown in figure(a)

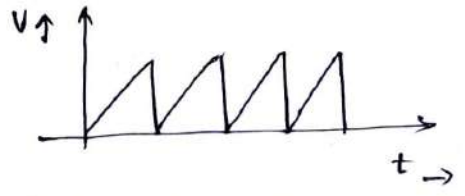


fig(a): Sinusoidal wave form

- A relaxation oscillator generates voltage or current which vary abruptly one or more times in a cycle of oscillation as shown in figure(b) and fig(c).



fig(b) Square wave form



fig(c): Sawtooth wave form.

2) According to the fundamental mechanisms involved
   a) Negative resistance oscillators
   b) Feedback oscillators

- In a negative resistance oscillator the negative resistance of the amplifying device is used to neutralize the positive resistance of the oscillator.

- Feedback oscillator is formed by using the positive feedback in a feedback amplifier such that it satisfies the Barkhausen criterion.

3) According to the frequency generated

a) Audio Frequency oscillator : 20Hz to 20KHz
b) Radio Frequency oscillator : 20KHz to 30MHz
c) Very High Frequency oscillator : 30MHz to 300MHz
d) Ultra high Frequency oscillator : 300MHz to 3GHz
e) Microwave Frequency oscillator : 3GHz and above.

4) According to the type of the circuit used, Sinusoidal oscillators are classified as

a) LC Tuned oscillator
b) RC Phase shift oscillator.

Concept of positive feedback :

If some portion of the output signal is fed back to the input of the amplifier in phase with the external signal from source, such feedback is known as positive feedback.

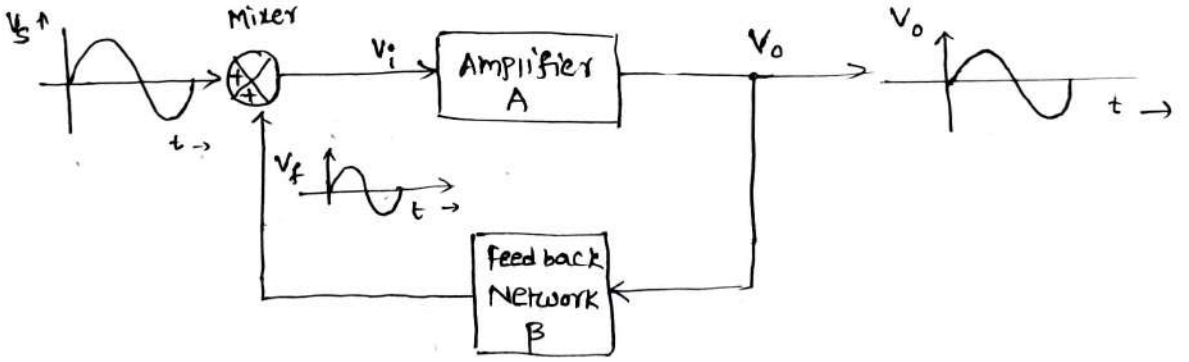


fig: Concept of positive feedback

Assume that a sinusoidal input signal V_s is applied to the circuit. The output of the amplifier as V_o. Some portion of the output signal is taken from the output of feedback network as V_f which is in phase with V_s. Hence V_f is added with V_s to give the input to the amplifier as V_i i.e $V_i = V_s + V_f$ ⟶ (1)

Let the gain of the amplifier without feed back as A

Then $A = \frac{V_o}{V_i}$ ⟶ (2)

The feedback factor of the feedback network 'β' is given as

$$\beta = \frac{V_f}{V_0} \longrightarrow (3)$$

The gain of the amplifier with feedback is A_f given as

$$A_f = \frac{V_0}{V_s} \longrightarrow (4)$$

$$= \frac{V_0}{V_i - V_f} \quad \left(\because \text{from eq } (1),\ V_s = V_i - V_f \right)$$

$$= \frac{1}{\left(\frac{V_i}{V_0}\right) - \left(\frac{V_f}{V_0}\right)}$$

$$= \frac{1}{\frac{1}{A} - \beta} \quad (\because \text{equation } (2) \text{ and } (3))$$

$$\therefore \boxed{A_f = \frac{A}{1 - A\beta}}$$

Conditions for oscillation (or) Barkhausen Criterion:

The oscillator circuit produces oscillations due to the random variation in the base current due to the noise component (or) a small variation in the DC supply. The noise components of extremely small electrical voltages are always present in the circuit environment, that causes small signal at the output of the amplifier, even in the absence of the external signal. Let the amplifier is tuned to a particular frequency f_0, hence the output signal produced due to noise will also be of frequency f_0. If a small fraction (β) of the output signal is fed back to the input, then this feedback signal will be amplified by the amplifier.

If the amplifier has a gain of more than $\frac{1}{\beta}$, then the output goes on increasing, but as the output increases, the gain of the amplifier decreases and at a particular value of output, the gain of the amplifier is reduced exactly equal to $\frac{1}{\beta}$. Then the output remains constant at frequency f_0. This frequency f_0 is called as frequency of oscillation.

The essential conditions for maintaining oscillations are

1) $|A\beta| = 1$ i.e the magnitude of loop gain must be unity.

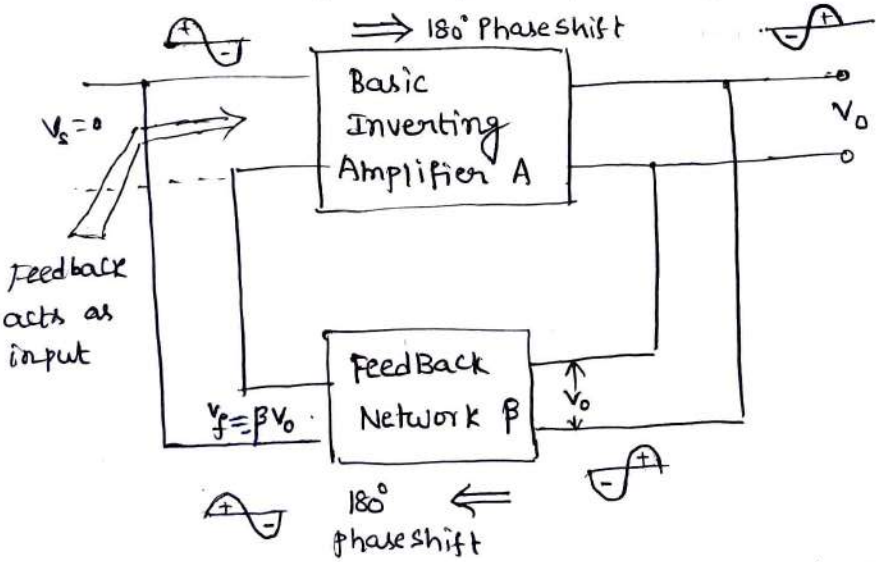
2) The total Phase shift around the closed loop is zero or 360°.

Consider an inverting basic amplifier with open loop gain A, which produces 180° Phase shift between it's input and output. And the feedback network has a feedback factor β. Assume $V_s = 0$.

An output is generated at the amplifier due to the variations in dc (or) due to noise from which a fraction of the output is fed back to the input of the amplifier through feedback network. This feed back signal acts as input V_i to the circuit now.

open loop gain $A = \frac{V_o}{V_i} \rightarrow (1)$

Feedback signal $V_f = -\beta V_o \rightarrow (2)$ '-' sign indicates 180° Phase shift



Since V_f is going as V_i here $V_f = V_i$

eq (1) $\Rightarrow V_o = AV_i = A \cdot V_f$

$\therefore V_o = A \cdot V_f \rightarrow (3)$

Substituting equation (3) in equation (2) we get

$$V_f = -\beta A V_f$$

$$\Rightarrow A\beta = -1$$

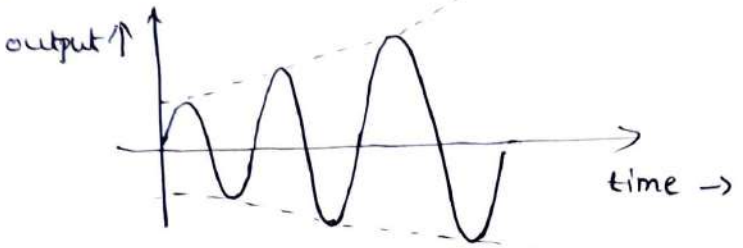
$$\Rightarrow A\beta = -1 + j0$$

$$\therefore |A\beta| = 1$$

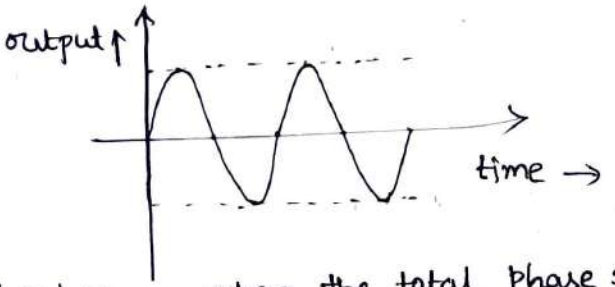
Here the basic inverting amplifier introduces 180° phase shift, in addition to which 180° phase shift should be provided by the feedback network to make the total phase shift around the closed loop as 360°.

Effect of magnitude of loop gain $|A\beta|$ on nature of oscillations:

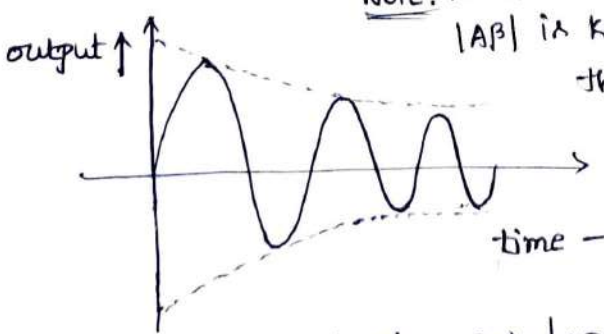
i) when $|A\beta| > 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| > 1$ then the output contains the oscillations of growing type. i.e the amplitude of oscillations goes on increasing.



ii) when $|A\beta| = 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| = 1$ then the output contains the oscillations with constant frequency and amplitude, these oscillations are called as sustained oscillations. (or) undamped oscillations.



iii) when $|A\beta| < 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| < 1$ then the oscillations are of decaying type i.e the amplitude decreases exponentially.



NOTE: To start oscillations without input $|A\beta|$ is kept higher than unity and then the circuit adjust itself to get $|A\beta| = 1$ to result sustained oscillations.

NOTE: The oscillations under $|A\beta| < 1$ (or) $|A\beta| > 1$ are called as under damped (or) over damped oscillations resp.

LC oscillators :

General form of an LC oscillator :

The general form of an LC oscillator requires any one of the active devices such as Transistor, FET, Vacuum tube, and op-amp may be used in the amplifier section.

Z_1, Z_2, and Z_3 are the reactive elements constituting the feedback tank circuit which determines the frequency of oscillation. Here Z_1 and Z_2 serve as an ac voltage divider for the output voltage and the feedback signal.

The voltage across Z_1 is the feedback signal.

The frequency of oscillation of an LC oscillator is

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

The general form of an LC oscillator and it's equivalent circuit are as shown in below, in which the output terminals are 2 and 3, and input terminals are 1 and 3.

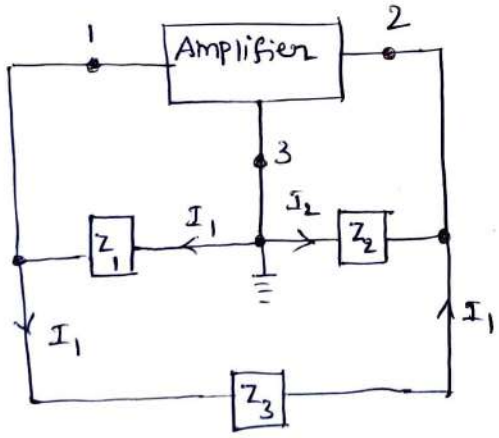


fig (a) General form of an LC oscillator

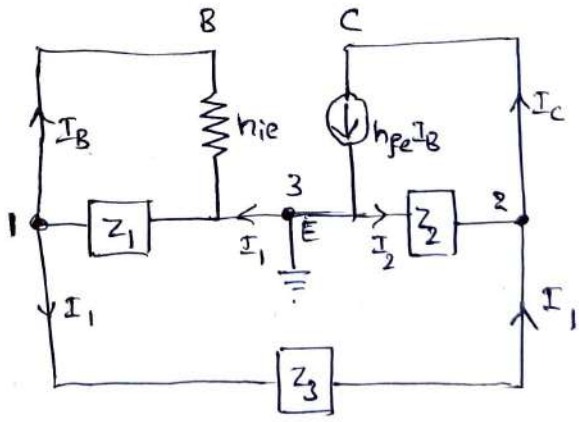


fig (b) : Equivalent Circuit of an LC oscillator

Load impedance : (Z_L)

Since Z_1 is in parallel with the resistance hie, their equivalent resistance Z' is given by

$$\frac{1}{Z'} = \frac{1}{Z_1} + \frac{1}{h_{ie}}$$

$$\therefore Z' = \frac{Z_1 h_{ie}}{Z_1 + h_{ie}} \longrightarrow (1)$$

Now the load impedance Z_L is the impedance between the terminals 2 and 3 (i.e output terminals) which is equal to Z_2 in parallel with $Z' + Z_3$.

$$\text{i.e} \quad \frac{1}{Z_L} = \frac{1}{Z_2} + \frac{1}{Z' + Z_3}$$

$$\Rightarrow \frac{1}{Z_L} = \frac{1}{Z_2} + \frac{1}{\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} + Z_3}$$

$$= \frac{1}{Z_2} + \frac{Z_1 + h_{ie}}{Z_1 h_{ie} + Z_1 Z_3 + Z_3 h_{ie}}$$

$$= \frac{1}{Z_2} + \frac{Z_1 + h_{ie}}{(Z_1 + Z_3) h_{ie} + Z_1 Z_3}$$

$$= \frac{h_{ie}(Z_1 + Z_3) + Z_1 Z_3 + Z_2 h_{ie} + Z_1 Z_2}{Z_2 \left[h_{ie}(Z_1 + Z_3) + Z_1 Z_3 \right]}$$

$$= \frac{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3}{Z_2 \left[h_{ie}(Z_1 + Z_3) + Z_1 Z_3 \right]}$$

$$\therefore Z_L = \frac{Z_2 \left[h_{ie}(Z_1 + Z_3) + Z_1 Z_3 \right]}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} \longrightarrow (2)$$

Voltage Gain without feed back (A_V)

$$\text{Voltage Gain } (A_V) = \frac{A_I Z_L}{Z_i} = -\frac{h_{fe} Z_L}{h_{ie}} \longrightarrow (3)$$

Feedback factor (β) :

The output voltage between the terminals 3 and 2 in terms of current I_1 is given by $V_0 = -I_1 (Z' + Z_3) = -I_1 \left(\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} + Z_3 \right)$

$$V_0 = -I_1 \left(\frac{h_{ie}(Z_1 + Z_3) + Z_1 Z_3}{Z_1 + h_{ie}} \right) \longrightarrow (4)$$

the voltage fed back to the terminals 3 and 1 is given by

$$V_f = -I_1 Z' = -I_1 \left(\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} \right) \longrightarrow (5)$$

The feed back ratio $\beta = \frac{V_f}{V_o} = -I_1 \left(\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} \right)$ ($\because$ from eq (4), (5))

$$-I_1 \left(\frac{h_{ie}(Z_1 + Z_3) + Z_1 Z_3}{Z_1 + h_{ie}} \right)$$

$$\Rightarrow \quad \beta = \frac{Z_1 h_{ie}}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \longrightarrow (6)$$

The equation for the oscillator

For producing oscillations $A_v \beta = 1$ is the condition

Substituting eq (3) and eq (6) in this equation we get

$$\frac{-h_{fe} Z_L}{h_{ie}} \left[\frac{Z_1 h_{ie}}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \right] = 1$$

$$\Rightarrow \quad \frac{h_{fe} Z_L Z_1}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} = -1 \quad , \text{ substituting } Z_L \text{ from equation (2)}$$

$$\Rightarrow \quad \frac{h_{fe} Z_1}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \left[\frac{Z_2 \left[h_{ie}(Z_1 + Z_3) + Z_1 Z_3 \right]}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} \right] = -1$$

$$\Rightarrow \quad \frac{h_{fe} Z_1 Z_2}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} = -1$$

$$\Rightarrow \quad h_{fe} Z_1 Z_2 = -\left[h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3 \right]$$

$$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1 + h_{fe}) + Z_1 Z_3 = 0 .$$

This is the general equation for the oscillator.

Hartley Oscillator:

In the Hartley oscillator Z_1 and Z_2 are inductors and Z_3 is a capacitor. The Hartley oscillator circuit is as shown in below.

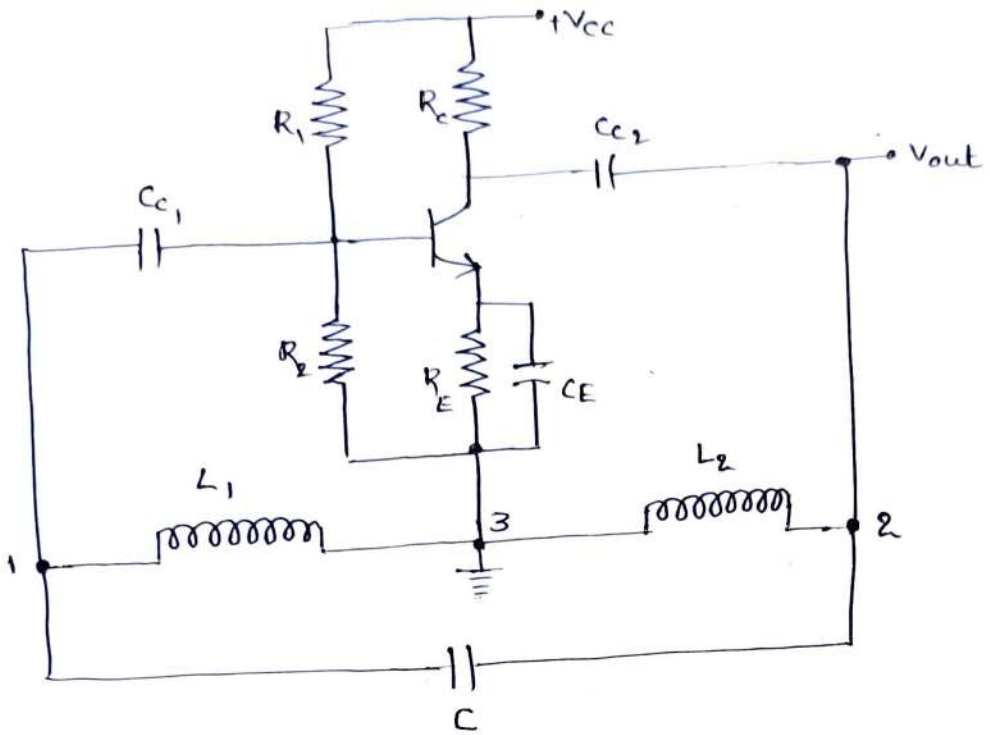


fig: Hartley oscillator

Here the resistors R_1, R_2 and R_E provides the required bias to the transistor. C_E is a bypass capacitor, C_{c_1} and C_{c_2} are the coupling capacitors. The feedback network consists of the inductors L_1 and L_2 and capacitor C determines the frequency of oscillation.

When the supply voltage $+V_{cc}$ is turned ON, a transient current is produced in the tank circuit. The current in the tank circuit develops AC voltages across L_1 and L_2. As the terminal 3 is grounded, it is at zero potential. If terminal 1 is at a positive potential with respect to terminal 3 at any instant, the terminal 2 will be at negative potential with respect to terminal 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180°. In the CE mode, the transistor produces 180° phase difference between input and output. Therefore the total phase shift is 360°. Thus at the frequency determined for the tank circuit, the necessary condition for sustained oscillations is satisfied.

If the feedback is adjusted such that the loop gain $A\beta = 1$, the circuit acts as an oscillator.

The frequency of oscillation is $f_o = \frac{1}{2\pi\sqrt{LC}}$

where $L = L_1 + L_2 + 2M$ and M is the mutual inductance value between L_1 and L_2 coils.

The condition for sustained oscillation is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}.$$

Analysis: In the Hartley oscillator, Z_1 and Z_2 are inductive reactances and Z_3 is the capacitive reactance. Suppose 'M' is the mutual inductance between the inductors, then

$$Z_1 = j\omega L_1 + j\omega M$$

$$Z_2 = j\omega L_2 + j\omega M$$

$$Z_3 = \frac{1}{j\omega C} = \frac{-j}{\omega C}$$

we know the general equation for the oscillator is

$$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1 + h_{fe}) + Z_1 Z_3 = 0$$

Substituting Z_1, Z_2 and Z_3 in this equation from above equations,

$$h_{ie}\left(j\omega L_1 + j\omega M + j\omega L_2 + j\omega M - \frac{j}{\omega C}\right) + (j\omega L_1 + j\omega M)(j\omega L_2 + j\omega M)(1 + h_{fe}) + (j\omega L_1 + j\omega M)\left(\frac{-j}{\omega C}\right) = 0$$

$$j\omega h_{ie}\left(L_1 + L_2 + 2M - \frac{1}{\omega^2 C}\right) - \omega^2 (L_1 + M)(L_2 + M)(1 + h_{fe}) + (L_1 + M)\frac{1}{C} = 0$$

$$j\omega h_{ie}\left(L_1 + L_2 + 2M - \frac{1}{\omega^2 C}\right) - \omega^2 (L_1 + M)\left[(L_2 + M)(1 + h_{fe}) - \frac{1}{\omega^2 C}\right] = 0 \quad \hookrightarrow (1)$$

The frequency of oscillation $f_o = \frac{\omega_o}{2\pi}$ is determined by equating the imaginary part of the above equation to zero by substituting $\omega = \omega_o$ i.e $\omega_o h_{ie}\left(L_1 + L_2 + 2M - \frac{1}{\omega_o^2 C}\right) = 0$

$$\Rightarrow \quad \frac{1}{\omega_0^2 C} = L_1 + L_2 + 2M$$

$$\Rightarrow \quad \omega_0^2 = \frac{1}{(L_1+L_2+2M)C}$$

$$\therefore \quad \omega_0 = \frac{1}{\sqrt{(L_1+L_2+2M)C}} \longrightarrow (2)$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}} \longrightarrow (3)$$

The condition for maintenance of oscillation is obtained by substituting eq (3) in eq (1) which makes the imaginary part to zero. Hence

$$(L_2+M)(1+h_{fe}) - \frac{1}{\omega_0^2 C} = 0$$

$$\Rightarrow \quad (L_2+M)(1+h_{fe}) - \frac{1}{C}(L_1+L_2+2M)C = 0$$

$$\Rightarrow \quad (L_2+M)(1+h_{fe}) = L_1+L_2+2M$$

$$L_2+M+(L_2+M)(h_{fe}) = L_1+L_2+2M$$

$$(L_2+M)h_{fe} = L_1+M \Rightarrow h_{fe} = \frac{L_1+M}{L_2+M}$$

$\therefore$ The condition for maintenance of oscillations is $\boxed{h_{fe} = \frac{L_1+M}{L_2+M}}$

COLPITTS OSCILLATOR:

In the Colpitt's oscillator Z_1 and Z_2 are capacitors and Z_3 is an inductor. The Colpitt's oscillator circuit is as shown in below fig.

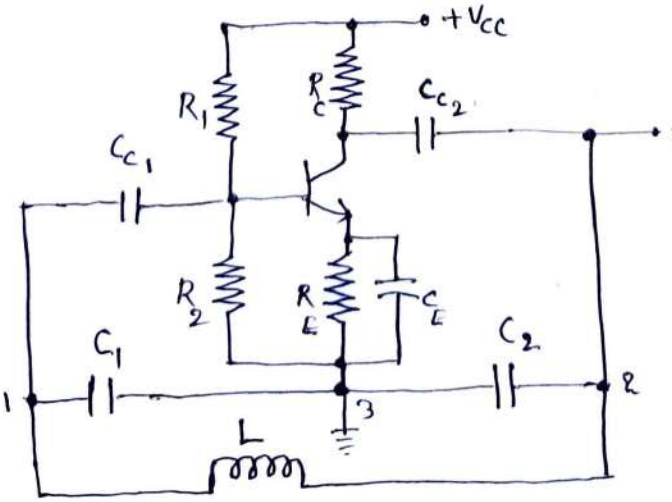


fig: COLPITTS OSCILLATOR

The resistors R_1, R_2 and R_E provide the necessary DC biasing to the transistor. C_E is the bypass capacitor, C_{C_1} and C_{C_2} are the coupling capacitors. The feedback network consists of C_1 and C_2 and an inductor L determines the frequency of oscillation. Here C_1 and C_2 are capacitors.

When the power supply voltage $+V_{CC}$ is switched ON, a transient current is produced in the tank circuit and consequently damped harmonic oscillations are setup in the circuit. The current in the tank circuit produces (or) develops AC voltages across C_1 and C_2. As terminal 3 is grounded, it will be at zero potential. Now if terminal 1 is at positive potential with respect to 3 at any instant, the terminal 2 will be at negative potential with respect to 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180°. In the common emitter configuration, the transistor provides a phase difference of 180° between the input and output. Therefore the total phase difference is 360°. Thus, at the frequency determined for the tank circuit, the necessary condition for sustained oscillations is satisfied. If the feedback is adjusted such that the loop gain $A\beta = 1$, the circuit acts as oscillator. The frequency of oscillation is

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

where $\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \Rightarrow C = \frac{C_1 C_2}{C_1 + C_2}$

It is widely used in commercial signal generators for frequencies between 1MHz to 500MHz. It is also used as a local oscillator in super heterodyne radio receiver.

Analysis: For Colpitts oscillator $Z_1 = \frac{1}{j\omega C_1}$, $Z_2 = \frac{1}{j\omega C_2}$, $Z_3 = j\omega L$

i.e $Z_1 = \frac{-j}{\omega C_1}$, $Z_2 = \frac{-j}{\omega C_2}$ and $Z_3 = j\omega L$

we know the general equation of an LC oscillator is

$$h_{ie}(z_1+z_2+z_3)+z_1z_2(1+h_{fe})+z_1z_3=0$$

substituting $z_3=+j\omega L$, $z_1=\frac{-j}{\omega C_1}$, $z_2=\frac{-j}{\omega C_2}$ in the above eq'

$$h_{ie}\left(\frac{-j}{\omega C_1}\frac{-j}{\omega C_2}+j\omega L\right)+\left(\frac{-j}{\omega C_1}\cdot\frac{-j}{\omega C_2}\right)(1+h_{fe})+\left(\frac{-j}{\omega C_1}\right)(j\omega L)=0$$

$$-jh_{ie}\left(\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right)-\frac{(1+h_{fe})}{\omega^2C_1C_2}+\frac{L}{C_1}=0$$

$$\Rightarrow\left[\frac{1+h_{fe}}{\omega^2C_1C_2}-\frac{L}{C_1}\right]+jh_{ie}\left(\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right)=0 \longrightarrow (1)$$

The frequency of oscillation $f_0=\frac{\omega_0}{2\pi}$ is determined by equating the imaginary part to zero, by substituting $\omega=\omega_0$.

i.e $$h_{ie}\left(\frac{1}{\omega_0C_1}+\frac{1}{\omega_0C_2}-\omega_0L\right)=0$$

$$\Rightarrow \omega_0L=\frac{1}{\omega_0C_1}+\frac{1}{\omega_0C_2}$$

$$\omega_0^2=\frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)$$

$$\omega_0=\sqrt{\frac{C_1+C_2}{LC_1C_2}} \longrightarrow (2)$$

$$f_0=\frac{\omega_0}{2\pi}=\frac{1}{2\pi}\sqrt{\frac{C_1+C_2}{LC_1C_2}} \longrightarrow (3)$$

The condition for maintenance of oscillation is obtained by substituting equation (3) in equation (1) which makes the imaginary part to zero.

Hence $$\frac{1+h_{fe}}{\omega_0^2C_1C_2}-\frac{L}{C_1}=0$$

$$\Rightarrow \frac{1+h_{fe}}{\omega_0^2C_1C_2}=\frac{L}{C_1}$$

$$\Rightarrow \frac{1+h_{fe}}{\left(\frac{C_1+C_2}{LC_1C_2}\right)\cdot C_1C_2}=\frac{L}{C_1} \qquad \left(\because \text{from eq (2)}\ \ \omega_0^2=\frac{C_1+C_2}{LC_1C_2}\right)$$

$$\Rightarrow 1+h_{fe} = \left(\frac{L}{C_1}\right)\left(\frac{C_1+C_2}{L}\right)$$

$$\Rightarrow 1+h_{fe} = \frac{C_1+C_2}{C_1}$$

$$\Rightarrow 1+h_{fe} = 1+\frac{C_2}{C_1}$$

$$\therefore \boxed{h_{fe} = \frac{C_2}{C_1}}$$

Problems: In the Hartley oscillator $L_2 = 0.4\,mH$ and $C = 0.004\,\mu F$ If the frequency of oscillator is 120kHz, find the value of L_1. Neglect the mutual inductance.

Sol) Given $L_2 = 0.4\,mH = 0.4\times10^{-3}\,H$, $C = 0.004\,\mu F = 4\times10^{-9}\,F$

$f_0 = 120\,kHz$, $L_1 = ?$

We know that the frequency of Hartley oscillator is given by

$$f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}$$

Neglecting mutual inductance

$$f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

$$\Rightarrow f_0^2 = \frac{1}{4\pi^2(L+L_2)C}$$

$$\Rightarrow (L_1+L_2)C = \frac{1}{4\pi^2 f_0^2}$$

$$\Rightarrow L_1C+L_2C = \frac{1}{4\pi^2 f_0^2}$$

$$\Rightarrow L_1C = \frac{1}{4\pi^2 f_0^2} - L_2C$$

$$\Rightarrow L_1 = \frac{1}{4\pi^2 f_0^2 C} - L_2$$

$$\Rightarrow L_1 = \frac{1}{4\pi^2(120\times10^3)^2(4\times10^{-9})} - (0.4\times10^{-3})$$

$$\Rightarrow L_1 = 0.03976\,mH$$

(2) A Hartley oscillator has two inductances as 2mH and 20μH while the frequency is to be changed from 950kHz to 2050KHz Calculate the range over which the capacitor is to be varied.

Sol) Given Hartley oscillator has $L_1 = 2mH = 2\times10^{-3}H$

$L_2 = 20\mu H = 20\times10^{-6}H$, $f_1 = 950KHz = 950\times10^3 Hz$

$f_2 = 2050KHz = 2050\times10^3 Hz$.

we know that the frequency of oscillation for hartley oscillator is $f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$

$\Rightarrow C = \frac{1}{4\pi^2 f_0^2 (L_1+L_2)}$

when $f_0 = 950\,KHz$, $C = \frac{1}{4\pi^2(950\times10^3)^2(2\times10^{-3}+20\times10^{-6})}$

$= 13.89\,PF$

when $f_0 = 2050\,KHz$, $C = \frac{1}{4\pi^2(2050\times10^3)^2(2\times10^{-3}+20\times10^{-6})}$

$C = 2.98\,PF$

Therefore the range of capacitance is from 2.98PF to 13.89PF.

3) A colpitts oscillator has $C_1 = 0.2PF$ $C_2 = 0.02PF$. If the frequency of oscillation is 10KHz, find the value of the inductor L?

Sol) Given $C_1 = 0.2PF$, $C_2 = 0.02PF$

$f_0 = 10KHz$

$L = ?$

we know that the frequency of oscillation for a colpitts oscillator is given by $f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1C_2}{C_1+C_2}\right)}} \Rightarrow f_0^2 = \frac{1}{4\pi^2\left(L\frac{C_1C_2}{C_1+C_2}\right)}$

$$\Rightarrow L = \frac{C_1 + C_2}{4\pi^2 f_0^2 C_1 C_2}$$

$$= \frac{(0.2\times10^{-12}) + (0.02\times10^{-12})}{4\pi^2 \times (10\times10^{3})^2 \times 0.2\times10^{-12} \times 0.02\times10^{-12}}$$

$$L = 13931\ H$$

4) In a colpitts oscillator the values of the inductors and capacitors are $L = 40mH$, $C_1 = 100pF$ $C_2 = 500pF$ i) find the frequency of oscillations ii) Find the value of h_{fe} for maintaining sustained oscillations

Sol) Given $L = 40mH$

$C_1 = 100pF$

$C_2 = 500pF$

For a colpitts oscillator the frequency of oscillations is

$$f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

$$= \frac{1}{2\pi\sqrt{40\times10^{-3} \times \frac{100\times10^{-12}\times500\times10^{-12}}{(100+500)\times10^{-12}}}}$$

$$\therefore f_0 = 87.172\ KHz$$

ii) The value of h_{fe} for maintaing sustained oscillations in a colpitts oscillator is given by $h_{fe} = \frac{C_2}{C_1}$

$$h_{fe} = \frac{500\times10^{-12}}{100\times10^{-12}}$$

$$\therefore h_{fe} = 5$$

CLAPP OSCILLATOR:

To achieve the frequency stability, colpitts oscillator is slightly modified in practice. This modified colpitts oscillator is called clapp oscillator. In clapp oscillator Z_1 and Z_2 are capacitors and Z_3 is the series combination of an inductor L and a capacitor C_3 as shown in figure below.

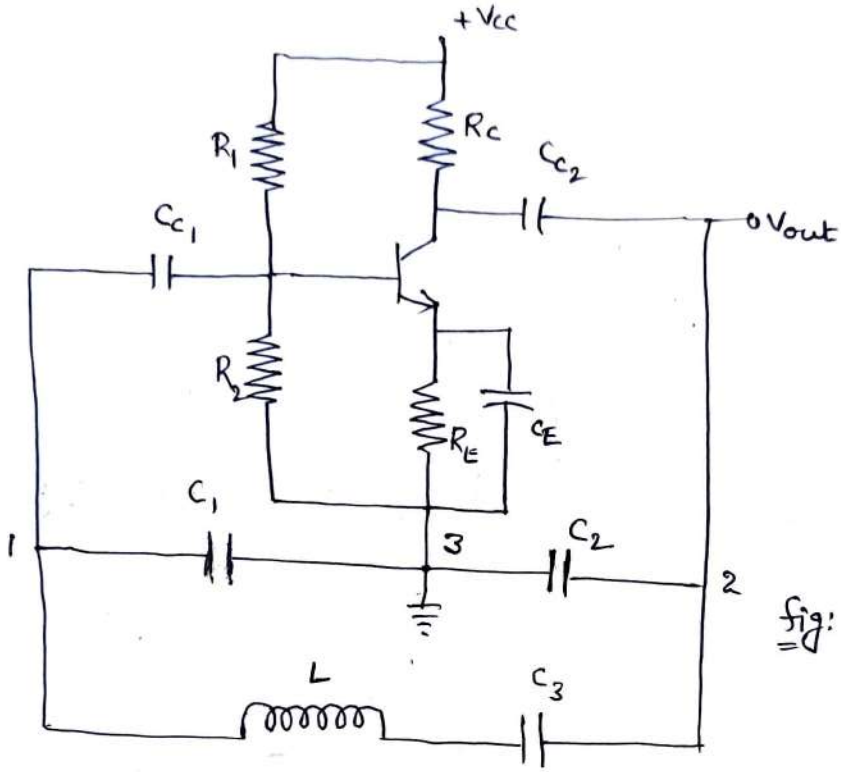


fig: clapp oscillator

The frequency of oscillation for a clapp oscillator is given as

$$f_0 = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

where $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$. The value of C_3 is very much smaller than the value of C_1 and C_2. So neglecting $\frac{1}{C_1}$ and $\frac{1}{C_2}$ we get

$$\frac{1}{C_{eq}} \simeq \frac{1}{C_3}$$

$$\text{ie } C_{eq} = C_3$$

$$\therefore f_0 = \frac{1}{2\pi\sqrt{L C_3}}$$

The Analysis of a clapp oscillator is as shown in below.

Analysis:

In a Clapp oscillator Z_1 and Z_2 are the capacitive reactances, Z_3 is a series combination of an inductive reactance and a capacitive reactance.

$$\text{i.e.} \quad Z_1 = \frac{1}{j\omega C_1} = -\frac{j}{\omega C_1}$$

$$Z_2 = \frac{1}{j\omega C_2} = -\frac{j}{\omega C_2}$$

$$Z_3 = j\omega L + \frac{1}{j\omega C_3} = j\omega L - \frac{j}{\omega C_3}$$

We know the general equation for an LC oscillator is

$$h_{ie}(Z_1 + Z_2 + Z_3) + (1 + h_{fe}) Z_1 Z_2 + Z_1 Z_3 = 0$$

Substituting Z_1, Z_2, Z_3 in the above equation

$$h_{ie}\left(-\frac{j}{\omega C_1} + \frac{-j}{\omega C_2} + j\omega L + \frac{-j}{\omega C_3}\right) + (1 + h_{fe})\left(\frac{-j}{\omega C_1}\right)\left(\frac{-j}{\omega C_2}\right) + \left(\frac{-j}{\omega C_1}\right) \cdot \left(j\omega L - \frac{j}{\omega C_3}\right) = 0$$

$$\Rightarrow \quad -j h_{ie}\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} + \frac{1}{\omega C_3} - \omega L\right) - \frac{(1 + h_{fe})}{\omega^2 C_1 C_2} + \frac{1}{\omega C_1}\left(\omega L - \frac{1}{\omega C_3}\right) = 0$$

$$\Rightarrow \quad -j h_{ie}\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} + \frac{1}{\omega C_3} - \omega L\right) - \frac{1}{\omega C_1}\left[\frac{(1 + h_{fe})}{\omega C_2} - \omega L + \frac{1}{\omega C_3}\right] = 0$$

The frequency of oscillation $f_0 = \frac{\omega_0}{2\pi}$ can be determined by equating the imaginary part to zero.

$$-h_{ie}\left(\frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2} + \frac{1}{\omega_0 C_3} - \omega_0 L\right) = 0$$

$$\Rightarrow \quad \frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2} + \frac{1}{\omega_0 C_3} - \omega_0 L = 0$$

$$\Rightarrow \quad \frac{1}{\omega_0}\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right) = \omega_0 L$$

$$\Rightarrow \quad \omega_0^2 = \frac{1}{L C_{eq}} \quad \text{where} \quad \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} = \frac{1}{C_{eq}}$$

$$\Rightarrow \omega_0 = \frac{1}{\sqrt{L C_{eq}}}$$

$$\Rightarrow f_0 = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

where $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$

As C_3 is very much smaller than C_1 and C_2. we can neglect $\frac{1}{C_1}$ and $\frac{1}{C_2}$.

$$\therefore \frac{1}{C_{eq}} \simeq \frac{1}{C_3}$$

$$\Rightarrow C_{eq} = C_3$$

$\therefore$ the frequency of oscillation for clapp oscillator is

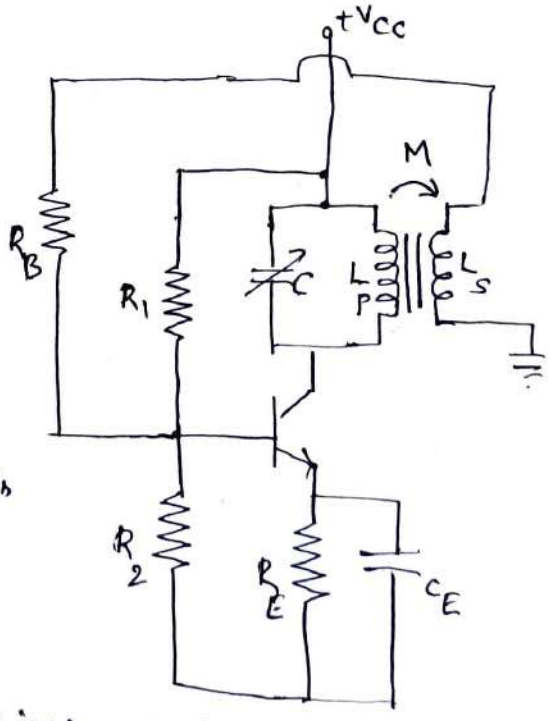
$$\boxed{f_0 = \frac{1}{2\pi\sqrt{LC_3}}}$$

Advantages:

1) The frequency is stable and accurate
2) The stray capacitances have no effect as C_3 decides the frequency.
3) keeping C_3 variable, the frequency can be varied in the desired range.

Tuned collector oscillator:

A tuned collector oscillator circuit is as shown in figure. There is a tuned LC circuit in the collector branch, which is connected to power supply $+V_{CC}$. Resistors R_1, R_2 and R_E are used to establish the proper biasing conditions as in a common emitter amplifier.



The capacitor C_E is a bypass emitter capacitor. The resistor R_B is used to control the amount of feedback to the value just needed for sustained oscillation.

When the power supply is switched on, the capacitor C starts charging. When it is fully charged, it starts to discharge through L_p. The energy stored in capacitor 'C' is in the form of electrostatic energy which gets converted to electromagnetic energy and gets stored in L_p. Once the capacitor discharges completely, L_p starts charging capacitor again. So the capacitor starts charging again and this cycle continues.

The coil L_s gets charged through the electromagnetic induction and feeds this to the transistor. The transistor amplifies the signal and is taken as the output at collector. A part of the output is fed back to the base through the LC circuit present at collector with positive feedback.

Here, the common Emitter amplifier introduces 180° phase shift and the transformer introduces an additional 180° phase shift hence a total 360° phase shift is obtained which satisfies the desired condition for sustained oscillations.

The frequency of oscillation $f_0 = \frac{1}{2\pi\sqrt{L_p C}}$

Drawbacks of LC oscillators:

1) Frequency instability
2) Waveform is poor
3) It cannot be used for deriving low frequencies.
4) Inductors are bulky and inexpensive.

Frequency Stability of oscillator:

↱ The frequency of oscillations should remain constant. But practically the frequency of oscillations will get changed due to various reasons.

↱ The analysis of the dependence of the oscillating frequency on various factors like temperature, internal capacitance etc is called as "frequency stability analysis."

↱ The measure of ability of an oscillator to maintain the desired frequency as precisely as possible for as long time as possible is called as the "frequency stability".

↱ The transistor parameters are temperature sensitive. Hence as temperature changes, the oscillating frequency also changes and no longer remains stable. So the circuit cannot provide stable frequency.

Factors that affect the frequency stability:

1) The operating point of the active devices such as BJT and FET must be in the active region. Due to the change in temperature the parameters of the active devices like BJT, FET may get changed that may lead to the change in frequency of oscillation.

2) The circuit components that are temperature dependent may affect the frequency of oscillation.

3) The changes in the DC supply voltage applied in the circuit may shift the oscillator's frequency of oscillation.

4) The changes in the atmospheric conditions and aging of the components may affect the frequency of oscillation.

5) The internal capacitances of the transistor may affect the oscillator's frequency of oscillation.

6) The changes in the output load / output resistance that may cause a change in the Q-factor of the tank circuit, thereby causing a change in the frequency oscillation.

The variation of frequency with respect to temperature variation is given by $S_{\omega,T} = \frac{\Delta\omega/\omega_0}{\Delta T/T_0}$ (ppmc Parts per million - per °C)

where ω_0 = The desired frequency of oscillation

T_0 = operating temperature

The frequency stability is debined as $S_\omega = \frac{d\theta}{d\omega}$

where θ is the phase shift which introduced due to the variation in the desired frequency (f_0).

The circuit should have $\frac{d\theta}{d\omega}$ as large as possible to have more frequency stability.

Amplitude Stability:

The ability of an oscillator to maintain a constant amplitude in the output waveform for as long time as possible is called as the amplitude stability of the oscillator.

The amplitude against the variations due to aging of the Components can be stabilized by replacing the resistors in bridge by sensistors which are temperature dependent resistors.

All the oscillators donot require positive feedback for their operation. If the positive resistance of the LC tank circuit is cancelled by introducing the right amount of -ve resistance across the tank circuit.

There are several devices that exhibit negative resistance such as dynatron, transitron, thermistor, UJT and tunnel diode, with in a particular region in their V-I characteristics. Such devices are operated under that negative resistance region and they are placed in the tank circuit to cancel the positive resistance of the tank circuit.

The negative resistance should be numerically less than the dynamic resistance of the tuned circuit.

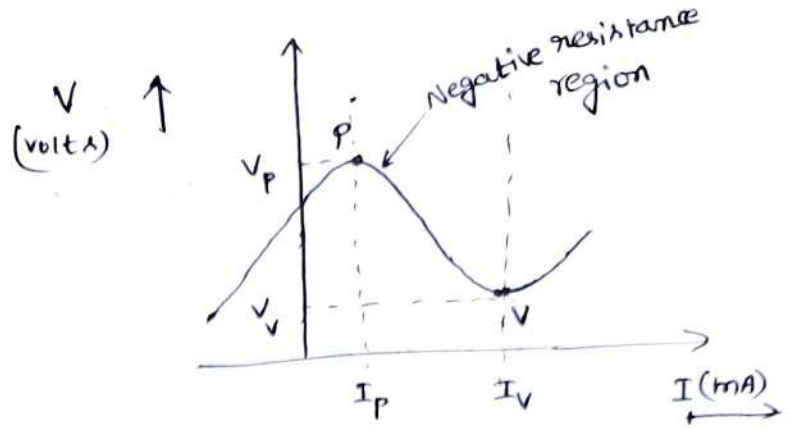


fig: V-I characteristics of negative resistance device

Crystal oscillators:

The following figure shows a crystal controlled oscillator. Here a colpitts oscillator is taken in which the inductor is replaced by a crystal. The crystal should be a piezo electric crystal usually quartz is used as a resonant circuit.

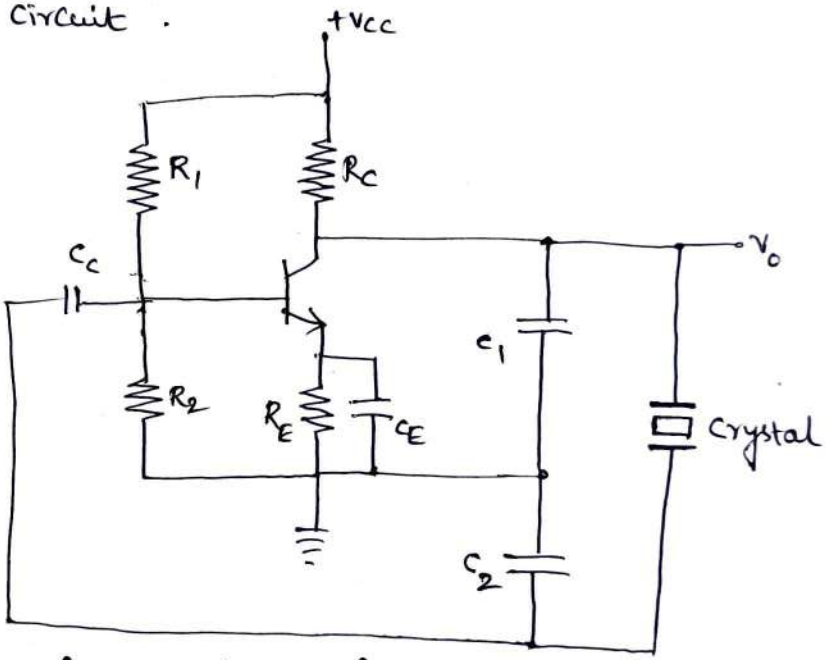


figure: crystal Controlled oscillator.

Principle of operation:

A crystal is a thin slice of piezo electric material such as quartz, tourmaline and rochelle salt which exhibit a property called piezo - electric effect.

Piezo electric effect means under the influence of the mechanical pressure on one face of the crystal, an ac voltage is developed across the opposite faces of the crystal. Conversely if the a.c - voltage is applied across two opposite faces, it causes a mechanical vibration in the crystal.

Quartz Crystal Construction:

Generally the crystal is a ground wafer of quartz or tourmaline stone placed between two metal plates. The crystal is placed after cutting crude crystal wafer into slices.

There are two methods of cutting the crystal. Based on the method of cutting the resonant frequency of the crystal and it's temperature coefficient is decided.

When the crystal wafer is cut in such a way that it's flat surfaces are perpendicular to it's electrical axis (X-axis), it is called as an X-Cut Crystal.

When the crystal wafer is cut in such a way that it's flat surfaces are perpendicular to it's mechanical axis (Y-axis), it is called as a Y-Cut Crystal.

If an AC voltage is applied, the crystal is set into vibration. The frequency of vibration is equal to the resonant frequency of the crystal. Usually the resonant frequency of the crystal is determined by the structural characteristics of the crystal. If the frequency of the applied AC voltage is equal to the natural resonant frequency of the crystal the vibration will be obtained with maximum amplitude.

In general the frequency of the vibration is given by

$$f = \frac{p}{2l}\sqrt{\frac{Y}{\rho}}$$

where $p = 1, 2, 3 \cdots$, Y is the young modulus,

ρ = density of the material

l = length of the material.

The crystal is suitably cut to get the vibrations with the required frequency and is mounted between two metal plates as shown in figure (a). The equivalent circuit of the crystal is

as shown in figure (b).

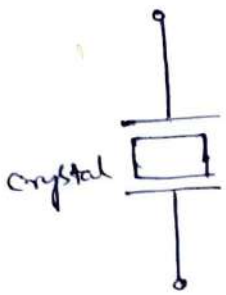
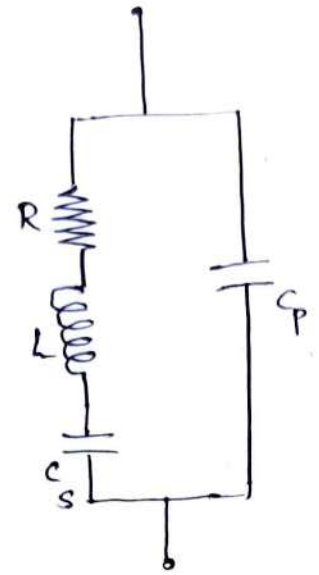


fig (a) Symbol of a Piezo electric crystal



fig(b) Equivalent circuit of a crystal

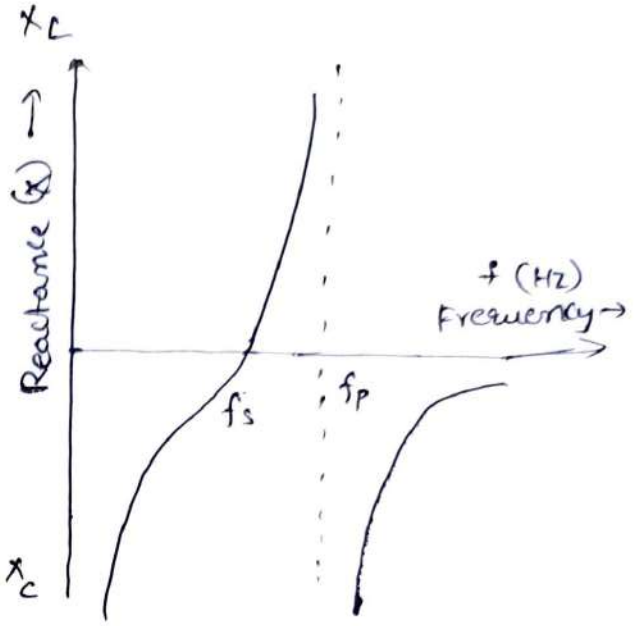


fig: reactance function with respect to frequency when R=0.

The reactance of the crystal is given by the formula

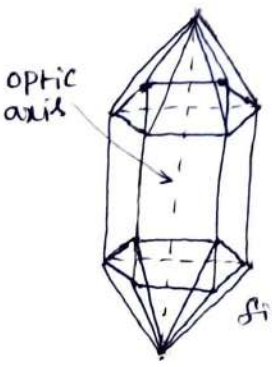
$$jX = \frac{1}{j\omega C_p} \cdot \left(\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2} \right) \text{ (neglecting R).}$$

Here ω_s = series resonant frequency $= \frac{1}{\sqrt{LC_s}}$

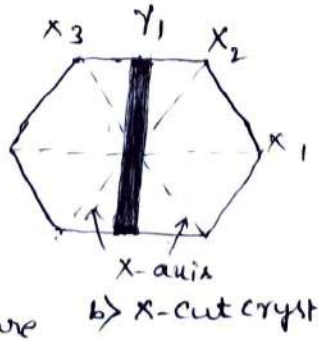
ω_p = parallel resonant frequency $= \frac{1}{\sqrt{L\left(\frac{C_s C_p}{C_s + C_p}\right)}}$

If C_p is very much larger than C_s then the parallel resonant frequency will be approximately equal to series resonant frequency.

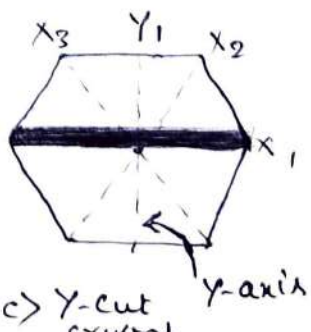
The structure of the Quartz crystal and the crystal wafer cutting, using X-cut and Y-cut are as shown in below.



fig(a): Quartz Crystal Structure



b) X-cut crystal



c) Y-cut crystal

series resonant frequency is the frequency at which reactance of the inductance L is equal to the reactance of the capacitance C_s. In this case the impedance of the equivalent circuit is equal to resistance 'R'.

The Parallel resonant frequency is the frequency at which the reactance of the RLC branch is equal to the reactance of the capacitor C_p.

Advantages of Crystal oscillator:

1) Crystal oscillator offers very high frequency stability.
2) Crystal oscillator circuits are less expensive
3) Quartz crystal has small size and light weight, which is preferred in crystal oscillator.
4) Crystals also have very high quality factor (Q).
5) It also provides good temperature stability.

Disadvantages of Crystal oscillator:

1) Crystals are very delicate and fragile, so they should be handled carefully.
2) The increase in the frequency, decreases the thickness of the crystal. This inturn reduces the mechanical strength of the crystal.
3) Crystal oscillators have fixed frequency of oscillation. Therefore, for every frequency of oscillation, the entire circuit must be redesigned.
4) The crystal oscillators are used only in low power circuits.

Problem

A crystal has L = 2H, C = 0.01PF and R = 2KΩ. It has a mounting capacitance of 2PF. Calculate it's series and parallel resonant frequencies.

Sol) Given $L = 2H$, $C = C_s = 0.01PF$, $R = 2K\Omega$

Mounting capacitance $C_p = 2PF$

series resonant frequency $f_s = \frac{1}{2\pi\sqrt{LC_s}} = \frac{1}{2\pi\sqrt{2 \times 0.01 \times 10^{-12}}} = 1.12MHz$

Parallel resonant frequency $f_p = \frac{1}{2\pi\sqrt{\frac{L C_s C_p}{C_s + C_p}}}$

$$\Rightarrow f_p = \frac{1}{2\pi\sqrt{\frac{2 \times 0.01 \times 10^{-12} \times 2 \times 10^{-12}}{(0.01 + 2)\, 10^{-12}}}}$$

$$\therefore f_p = 1.13\,MHz$$

Note: In the above problem $f_s \simeq f_p$ as the values of C_s and C_p are such that $C_p >> C_s$.

2) A crystal has $L = 0.5H$, $C_s = 0.06PF$, $C_p = 1PF$, $R = 5K\Omega$. Find the series and parallel resonant frequency and Q-factor of the crystal at series resonance and parallel resonance.

Sol) Given $L = 0.5H$, $C_s = 0.06PF$, $C_p = 1PF$, $R = 5K\Omega$

series resonant frequency $f_s = \frac{1}{2\pi\sqrt{LC_s}}$

$$= \frac{1}{2\pi\sqrt{(0.5)(0.06 \times 10^{-12})}}$$

$$\therefore f_s = 918.9\,KHz$$

Q-factor at series resonance is $Q_s = \frac{\omega_s L}{R}$

$$\Rightarrow Q_s = \frac{2\pi f_s L}{R} = \frac{2\pi \times 918.9 \times 10^3 \times 0.5}{5 \times 10^3}$$

$$\Rightarrow Q_s = 577$$

Parallel resonant frequency $f_p = \frac{1}{2\pi\sqrt{\frac{L C_s C_p}{C_s + C_p}}}$

$$\Rightarrow f_p = \frac{1}{2\pi\sqrt{(0.5)\left(\frac{0.06 \times 10^{-12} \times 1 \times 10^{-12}}{(0.06 + 1) \times 10^{-12}}\right)}}$$

$$\Rightarrow f_p = 946\,KHz$$

Q-factor at parallel resonance is $Q_p = \frac{\omega_p L}{R} = \frac{2\pi f_p L}{R}$

$$\Rightarrow Q_p = \frac{2\pi \times (946 \times 10^3) \times 0.5}{5 \times 10^3} = 594$$

Pierce Crystal oscillator:

The transistor pierce crystal oscillator is as shown in below figure.

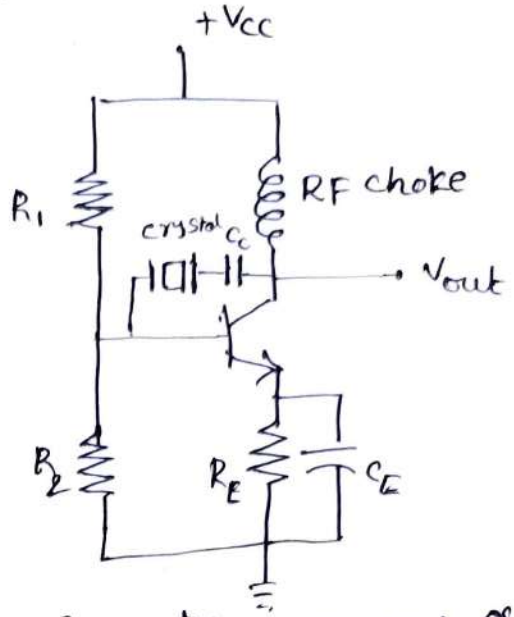


fig: Pierce crystal oscillator

Here the crystal is connected in the feed back path from collector to base.

The resistors R_1, R_2 and R_E are used to establish proper biasing in the circuit.

The RF choke used in the circuit, is for isolation of ac and dc.

C_c is the coupling capacitance. C_E is the emitter bypass capacitor which is used to prevent the amplification losses.

The coupling capacitor C_c blocks the dc voltage between the collector and base and it has a negligible impedance at the frequency of the oscillator.

The frequency of oscillation set by the series resonant frequency of the crystal is given by

$$f_o = \frac{1}{2\pi\sqrt{LC_s}}$$

The main advantage of the pierce crystal oscillator is it's simplicity.

It is the most frequently used crystal oscillator.

→ A tuned collector oscillator in a radio receiver has a fixed inductance of 60μH and has to be tunable over the frequency band of 400 KHz to 1200KHz. find the range of capacitor to be used.

sol> Given $L_p = 60\mu H$, $f_{min} = 400KHz$, $f_{max} = 1200KHz$

Frequency of oscillation for tuned collector oscillator is

$$f_o = \frac{1}{2\pi\sqrt{L_p C}}$$. At $f = f_{min}$, capacitance $C = C_{max}$

$$\Rightarrow C_{max} = \frac{1}{4\pi^2 f_{min}^2 L_p} = \frac{1}{4\pi^2 (400\times10^3)^2 (60\times10^{-6})} = 2641\,PF$$

At $f = f_{max}$ capacitance $C = C_{min}$

$$\therefore C_{min} = \frac{1}{4\pi^2 f_{max}^2 \cdot L_p} = \frac{1}{4\pi^2 (1200\times10^3)^2 \cdot (60\times10^{-6})}$$

$$\Rightarrow C_{min} = 293PF$$

∴ The range of the capacitor is 293 PF – 2641 PF.

→ Design a hartley oscillator that generates the frequency of oscillation at 1 MHz.

sol> In a hartley oscillator the tank circuit contains two inductors L_1 and L_2 and a capacitor 'C' which decides the frequency of oscillation $f_o = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}$ → ①

Let the mutual inductance $M = 0$.

Let us assume $C = 500pF$

given frequency of oscillation $f_o = 1MHz = 1\times10^6 Hz$

Substituting $M=0$ in equation ① we get

$$f_o = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

$$\Rightarrow f_o^2 = \frac{1}{4\pi^2 (L_1+L_2) C}$$

$$\Rightarrow L_1+L_2 = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{4\pi^2 (1\times10^6)^2 \times 500\times10^{-12}}$$

$$\Rightarrow L_1+L_2 = 5.066\times10^{-5} = 50.66\,\mu F \simeq 50\,\mu F$$

Let $L_1 = 32\,\mu F$ and $L_2 = 18\,\mu F$ such that the sum of L_1 and L_2 is $50\,\mu F$.

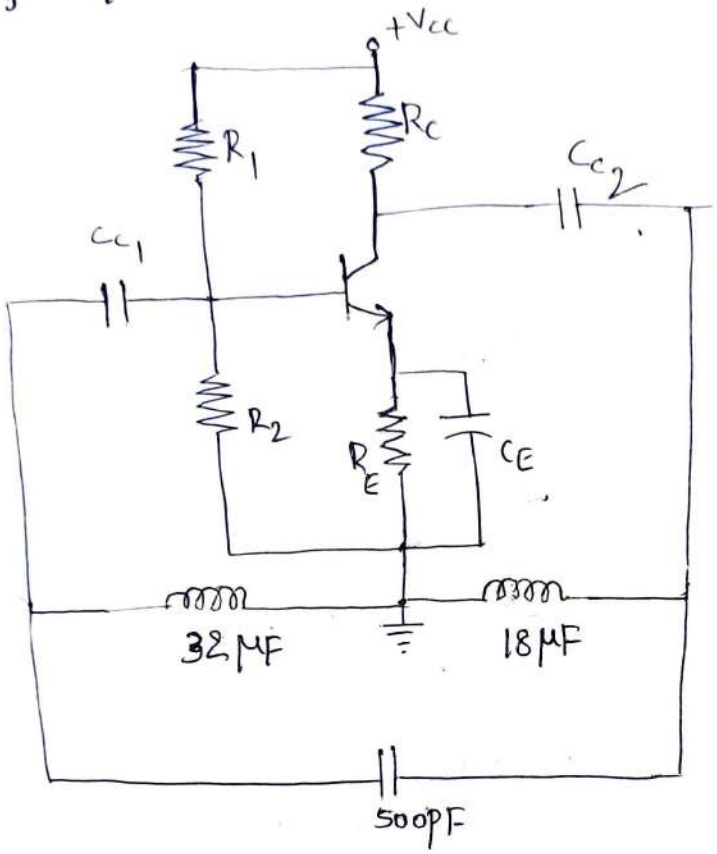


fig: Hartley oscillator

H.W Design a colpitt's oscillator that generates a signal with frequency of oscillation at 1MHz.

→ Find the value of h_{fe} to satisfy the condition for frequency of a signal (f_o) with sustained oscillations for a hartley oscillator having $L_1 = 10\,\mu F$, $L_2 = 2\,\mu F$ and $C = 5\,pF$. Assume $M = 0$.

Sol) To get sustained oscillation in hartley oscillator the condition for $h_{fe} = \frac{L_1}{L_2} = \frac{10\times10^{-6}}{2\times10^{-6}} = 5$

RC Oscillators :

All the LC oscillators are very useful to generate the signals with high frequencies. But the low frequency signals are generated with higher values of inductance and capacitances. This leads the circuit to be bulky and infact the circuit becomes expensive. The signals of low frequencies are easily generated with RC - oscillators.

RC oscillators are mainly of two types.

i) RC Phase shift oscillator ii) Wien bridge oscillator.

i) RC phase shift oscillator using cascade Connection of Highpass filter:

In this oscillator the required phase shift of 180° in the feedback loop from output to input is obtained by using R and C components instead of tank circuit.

The following figure shows the circuit of RC Phase shift oscillator using cascade connection of high pass filter.

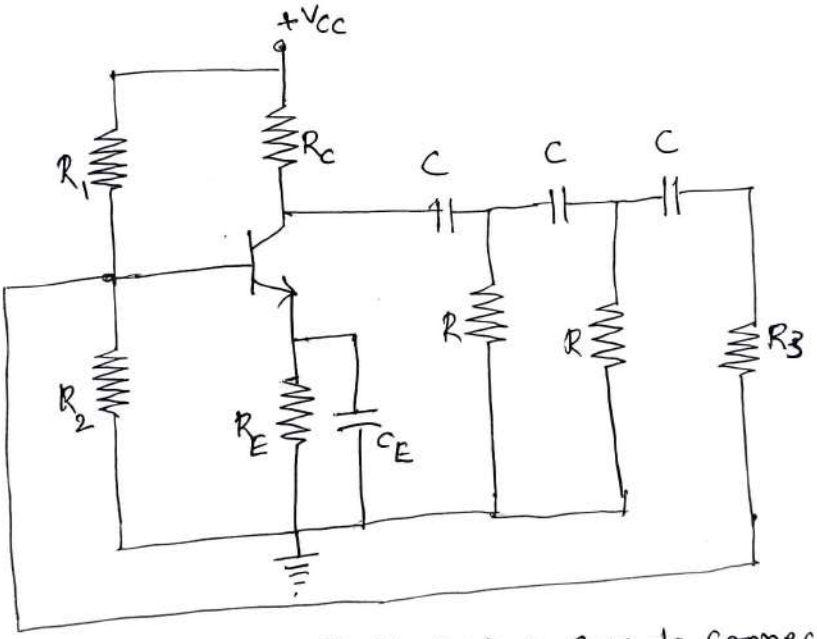


fig a) RC Phaseshift oscillator using cascade connection of High pass filter.

Here a common Emitter amplifier is followed by three sections of RC phase shift network. The output of the last section is connected as the input to the base of the transistor.

In order to make the three RC sections identical, R_3 is selected such that $R_3 + R_i = R$, where R_i is the input impedance of circuit.

Since the BJT is connected in CE configuration the input impedance R_i is equal to h_{ie}. That means $R_3 + h_{ie} = R$, neglecting R_1 & R_2.

The phase shift of each RC section is given by

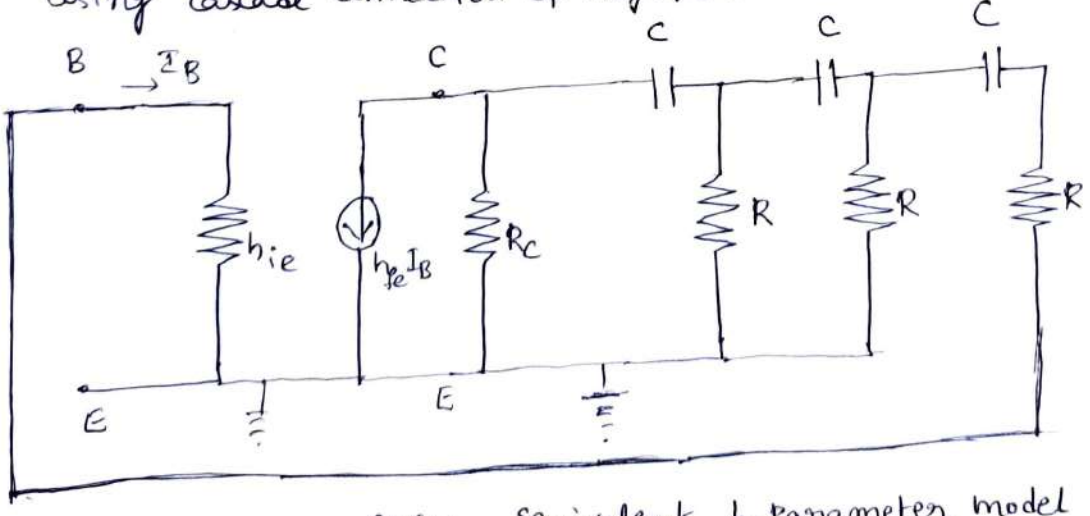
$$\phi = \tan^{-1}\left(\frac{1}{\omega CR}\right)$$

If R and C values are chosen such that for a given frequency f_r, the phase shift of each RC section is 60°. Thus the RC ladder network produces a total phase shift of 180°, between it's input and output voltages for the given frequency. The transistor of CE configuration provides a phase shift of 180°. Therefore a total phase shift of 360° is obtained, that satisfies the condition for sustained oscillations ie satisfying Barkhausen criterion. For RC phase shift oscillator the frequency of oscillation is given by $f_o = \frac{1}{2\pi RC\sqrt{6+4K}}$ where $K = \frac{R_c}{R}$.

At this frequency, it is found that the feedback factor β is $|\beta| = \frac{1}{29}$.

To get $|A\beta|$ not less than unity the transistor amplifier gain $|A|$ must be greater than or equal to 29.

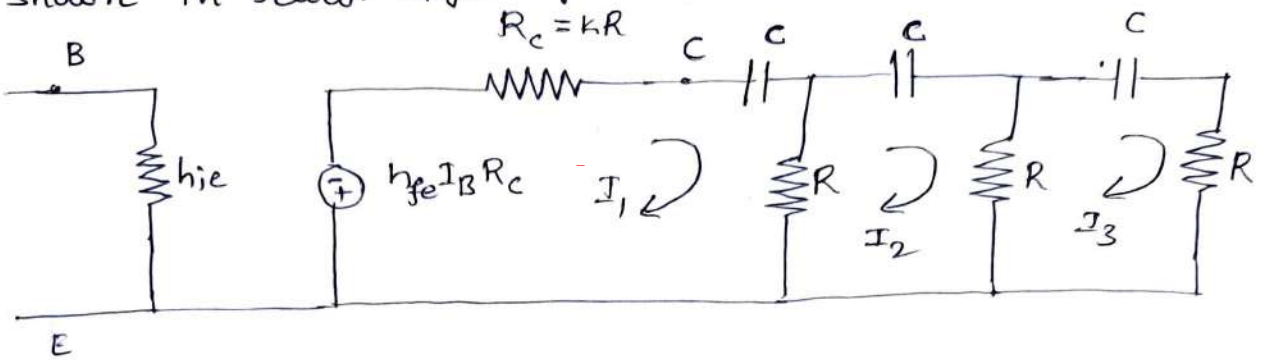
The equivalent h-parameter model for the RC phase shift oscillator using cascade connection of high pass filter is as shown in below.



fig(b) Equivalent h-parameter model

Analysis:

The h-parameter equivalent model for RC phase shift oscillator using cascade connection of highpass filter is modified as shown in below. Neglecting R_1 and R_2 input impedance $R_i \simeq h_{ie}$.



Here we have replaced $R_3 + h_{ie}$ with R and the current source $h_{fe} I_B$ is replaced by it's equivalent voltage source. Assume the ratio of the resistance R_c to R as k. i.e $k = \frac{R_c}{R}$

Applying KVL for loop1 we get

$$I_1 R_C + I_1 \frac{1}{j\omega C} + I_1 R - I_2 R = -h_{fe} I_B R_C$$

Replacing R_c with kR and $j\omega$ by s we get

$$I_1 kR + I_1 \frac{1}{s \cdot C} + I_1 R - I_2 R = -h_{fe} I_B kR$$

$$\Rightarrow \quad I_1 \left[(k+1)R + \frac{1}{sC} \right] - I_2 R = -h_{fe} I_B kR \longrightarrow (1)$$

Applying KVL for loop2 we get

$$I_2 \frac{1}{j\omega C} + I_2 R - I_3 R + I_2 R - I_1 R = 0$$

Replace $j\omega$ by s

$$I_2 \frac{1}{sC} + 2I_2 R - I_3 R - I_1 R = 0$$

$$\Rightarrow \quad -I_1 R + I_2 \left(2R + \frac{1}{sC} \right) - I_3 R = 0 \longrightarrow (2)$$

Apply KVL for loop3 we get

$$I_3 \left(\frac{1}{j\omega C} \right) + I_3 R + I_3 R - I_2 R = 0$$

Replace 'jw by s,

$$\frac{I_3}{sC} + 2I_3R - I_2R = 0$$

$$\Rightarrow \quad -I_2R + I_3\left(2R + \frac{1}{sC}\right) = 0 \longrightarrow (3)$$

using Cramer's rule to solve for I_3

$$D = \begin{vmatrix} (k+1)R + \frac{1}{sC} & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{vmatrix}$$

$$\Rightarrow \quad D = \left[(k+1)R + \frac{1}{sC}\right] \cdot \left[\left(2R + \frac{1}{sC}\right)^2 - R^2\right] - (-R)\left[(-R)\left(2R + \frac{1}{sC}\right) - 0\right] + 0\,(R^2)$$

$$D = \left[(k+1)R + \frac{1}{sC}\right]\left(2R + \frac{1}{sC}\right)^2 - \left[(k+1)R + \frac{1}{sC}\right] \cdot R^2 - R^2\left(2R + \frac{1}{sC}\right) \longrightarrow (4)$$

The first term in the above equation is

$$\left[(k+1)R + \frac{1}{sC}\right]\left(2R + \frac{1}{sC}\right)^2 = \left[\frac{(k+1)RSC + 1}{sC}\right]\left(\frac{2RSC + 1}{s^2C^2}\right)^2$$

$$= \frac{(kRSC + RSC + 1)(4R^2s^2C^2 + 4RSC + 1)}{s^3C^3}$$

$$= \frac{4kR^3s^3C^3 + 4kR^2s^2C^2 + kRSC + 4R^3s^3C^3 + 4R^2s^2C^2 + RSC + 4R^2s^2C^2 + 4RSC + 1}{s^3C^3}$$

$$= \frac{R^3s^3C^3(4k+4) + R^2s^2C^2(4k+8) + RSC(k+5) + 1}{s^3C^3}$$

The second and third terms in equation (4) are combinely written as

$$-\left[(k+1)R + \frac{1}{sC}\right]R^2 - R^2\left(2R + \frac{1}{sC}\right) = -\frac{[(k+1)RSC + 1]R^2}{sC} - \frac{R^2(2RSC+1)}{sC}$$

$$= -\frac{kR^3SC - R^3SC - R^2 - 2R^3SC - R^2}{SC}$$

$$= -\frac{kR^3SC - 3R^3SC - 2R^2}{SC}$$

$$= -\frac{(kR^3SC + 3R^3SC + 2R^2)}{SC}$$

Combining the first term equivalent and second & third term equivalent of equation (4) we get

$$D = \frac{R^3S^3C^3(4k+4) + R^2S^2C^2(4k+8) + RSC(k+5) + 1}{S^3C^3} - \frac{(kR^3SC + 3R^3SC + 2R^2)}{SC}$$

$$\Rightarrow D = \frac{R^3S^3C^3(4k+4) + R^2S^2C^2(4k+8) + RSC(k+5) + 1 - S^2C^2(kR^3SC + 3R^3SC + 2R^2)}{S^3C^3}$$

$$= \frac{R^3S^3C^3(4k+4) + R^2S^2C^2(4k+8) + RSC(k+5) + 1 - kR^3S^3C^3 - 3R^3S^3C^3 - 2R^2S^2C^2}{S^3C^3}$$

$$D = \frac{R^3S^3C^3(3k+1) + R^2S^2C^2(4k+6) + RSC(k+5) + 1}{S^3C^3} \longrightarrow (5)$$

Now

$$D_3 = \begin{vmatrix} (k+1)R + \frac{1}{SC} & -R & -h_{fe}I_B kR \\ -R & 2R + \frac{1}{SC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= 0 - 0 + (-h_{fe}I_B kR)\cdot(R^2 - 0)$$

$$D_3 = -kR^3 h_{fe} I_B \longrightarrow (6)$$

$$\therefore I_3 = \frac{D_3}{D} = \frac{-kR^3 h_{fe} I_B S^3C^3}{R^3S^3C^3(3k+1) + R^2S^2C^2(4k+6) + RSC(k+5) + 1} \longrightarrow (7)$$

($\because$ from equation (5) and (6))

I_3 = output current of the feedback circuit

I_B = Input current of the amplifier

$I_C = h_{fe} I_B$ = Input current of the feedback circuit

Amplifier gain $A = \frac{\text{output of the amplifier}}{\text{Input to the amplifier}} = \frac{I_3}{I_B} = h_{fe}$

Loop gain $A\beta = \frac{I_3}{I_B} \cdot \frac{I_3}{I_C} = h_{fe} \cdot \frac{I_3}{h_{fe} I_B} = \frac{I_3}{I_B}$ ⟶ (8)

$\left(\because \beta = \text{feed back factor} = \frac{\text{output of feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{I_C} \right)$

From equation (7) and (8)

$$A\beta = \frac{I_3}{I_B} = \frac{-KR^3 h_{fe} s^3 c^3}{R^3 s^3 c^3 (3K+1) + R^2 s^2 c^2 (4K+6) + RSC(K+5) + 1} \quad \rightarrow (9)$$

Substituting $s = j\omega$, $s^2 = j^2\omega^2 = -\omega^2$, $s^3 = j^3\omega^3 = -j\omega^3$ in the above equation we get

$$A\beta = \frac{+ j\omega^3 K R^3 h_{fe} c^3}{-j\omega^3 R^3 c^3 (3K+1) - \omega^2 R^2 c^2 (4K+6) + j\omega RC (K+5) + 1}$$

$$= \frac{K h_{fe}}{\frac{-j\omega^3 R^3 c^3 (3K+1)}{j\omega^3 R^3 c^3} - \frac{\omega^2 R^2 c^2 (4K+6)}{j\omega^3 R^3 c^3} + \frac{j\omega RC (K+5)}{j\omega^3 R^3 c^3} + \frac{1}{j\omega^3 R^3 c^3}}$$

$$= \frac{K h_{fe}}{-(3K+1) + j\frac{(4K+6)}{\omega RC} + \frac{K+1}{\omega^2 R^2 c^2} - \frac{j}{\omega^3 R^3 c^3}}$$

$$A\beta = \frac{K h_{fe}}{-(3K+1) + j(4K+6)\alpha + (K+5)\alpha^2 - j\alpha^3} \quad \left(\text{where } \alpha = \frac{1}{\omega RC} \right)$$

$$\Rightarrow A\beta = \frac{K h_{fe}}{\left[K\alpha^2 + 5\alpha^2 - 3K - 1\right] + j\left(-\alpha^3 + 4K\alpha + 6\alpha\right)} \quad \rightarrow (10)$$

As per Barkhausen criterion to get sustained oscillations $\angle A\beta = 0^\circ$ (or) 360°. To get $\angle A\beta = 0^\circ$, the imaginary part of the denominator should be 0.

$$\therefore \quad -\alpha^3 + 4k\alpha + 6\alpha = 0$$

$$\Rightarrow \quad \alpha(-\alpha^2 + 4k + 6) = 0$$

$$\Rightarrow \quad -\alpha^2 + 4k + 6 = 0$$

$$\Rightarrow \quad \alpha = \sqrt{4k+6}$$

Replacing $\alpha = \frac{1}{\omega_0 RC}$

$$\frac{1}{\omega_0 RC} = \sqrt{4k+6}$$

$$\omega_0 = \frac{1}{RC\sqrt{4k+6}}$$

$$\therefore \boxed{f_0 = \frac{1}{2\pi RC\sqrt{4k+6}}}$$

This is the frequency at which $\angle A\beta = 0^\circ$. At the same frequency $|A\beta| = 1$, substituting $\alpha = \sqrt{4k+6}$ in equation (10) we get

$$A\beta = \frac{k h_{fe}}{k(4k+6) + 5(4k+6) - 3k - 1}$$

$$= \frac{k h_{fe}}{4k^2 + 6k + 20k + 30 - 3k - 1}$$

$$= \frac{k h_{fe}}{4k^2 + 23k + 29}$$

Now $|A\beta| = 1$

$$\Rightarrow \left| \frac{k h_{fe}}{4k^2 + 23k + 29} \right| = 1 \quad \Rightarrow k h_{fe} = 4k^2 + 23k + 29$$

$$\Rightarrow \boxed{h_{fe} = 4k + 23 + \frac{29}{k}}$$

Minimum value of h_{fe} for the oscillations (or) minimum gain for sustained oscillations:

we know that $h_{fe} = 4K + 23 + \frac{29}{K}$ → (11)

To get minimum value of h_{fe} we have to find $\frac{dh_{fe}}{dk}$ and equate it to zero, in order to get the value of k.

$$\frac{dh_{fe}}{dk} = 4 + 0 + \left(\frac{29}{k^2}\right) = 0$$

$$\Rightarrow \quad 4 - \frac{29}{k^2} = 0$$

$$\Rightarrow \quad k^2 = \frac{29}{4}$$

$$\Rightarrow \quad k = 2.6925$$

$\therefore$ $K = 2.6925$ for minimum h_{fe}

substituting this in equation (11) we get

$$h_{fe_{min}} = 4(2.6925) + 23 + \frac{29}{2.6925}$$

$$\therefore \quad h_{fe_{min}} = 44.54$$

Therefore the minimum gain for sustained oscillations in an RC-Phase shift oscillator is $h_{fe\,min} = 44.54$.

Problem Find the capacitor C and h_{fe} for the transistor to provide the frequency of 10KHz of a transistorized Phase shift oscillator. Assume $R_1 = 25k\Omega$, $R_2 = 57k\Omega$, $R_c = 20k\Omega$, $R = 7.1k\Omega$, and $h_{ie} = 1.8k\Omega$.

Sol) Given $f_o = 10KHz$, $R_1 = 25k\Omega$, $R_2 = 57k\Omega$, $h_{ie} = 1.8k\Omega$, $R = 7.1k\Omega$

Input impedance $Z_i = h_{ie} = 1.8k\Omega$

$$Z_i' = Z_i \,||\, R_1 \,||\, R_2 = 1.8k\Omega \,||\, 25k\Omega \,||\, 57k\Omega = 1.631k\Omega$$

$$R_3 + Z_i' = R \Rightarrow R_3 = R - Z_i' = 7.1k\Omega - 1.631k\Omega = 5.469k\Omega$$

$$k = \frac{R_c}{R} = \frac{20\times10^3}{7.1\times10^3} = 2.8169$$

$$\therefore f = \frac{1}{2\pi RC\sqrt{6+4k}} \Rightarrow 10\times10^3 = \frac{1}{2\pi \times 7.1\times10^3 \times C\sqrt{6+4(2.8169)}}$$

$$\Rightarrow \quad C = \frac{1}{2\pi \times 7.1\times10^{3} \times 10\times10^{3}\sqrt{6+11.2676}}$$

$$\therefore \quad C = 539.44\,PF$$

we know that $h_{fe} \geq 4K + 23 + \frac{29}{K}$

$$\Rightarrow h_{fe} \geq 4(2.8169) + 23 + \frac{29}{2.8169}$$

$$\therefore h_{fe} \geq 44.5626$$

Advantages and disadvantages of RC Phase shift oscillator:

1) The circuit is simple to design.

2) It can produce the output over audio frequency range.

3) It produces sinusoidal output waveform.

The drawbacks of RC phase shift oscillator are

1) To change the frequency of oscillation in an RC phase shift oscillator, all the three capacitors or resistors should be changed simultaneously.

2) It is difficult to control the amplitude of the output signal, without affecting the frequency of oscillation.

3) Frequency stability is poor.

Problem: Find the capacitor C and h_{fe} for the transistor to provide a transistor to provide the frequency of oscillation of 10KHz of a transistorized oscillator designed with RC phase shift. Assume $R_1 = 25k\Omega$ $R_2 = 60K\Omega$, $R_c = 40K\Omega$, $R = 7.1K\Omega$ and $h_{ie} = 1.8K\Omega$.

Sol) Given $f_o = 10KHz$, $R_1 = 25K\Omega$, $R_2 = 60K\Omega$, $R_c = 40K\Omega$, $R = 7.1K\Omega$ and $h_{ie} = 1.8K\Omega$

Frequency of oscillation $f_o = \frac{1}{2\pi RC\sqrt{6+4K}}$

$$\Rightarrow C = \frac{1}{2\pi f_o R\sqrt{6+4K}} = \frac{1}{2\pi f_o R\sqrt{6+4\frac{R_c}{R}}}$$

$$\Rightarrow C = \frac{1}{2\pi\times10\times10^{3}\times7.1\times10^{3}\sqrt{6+4\left(\frac{40}{7.1\times10^{3}}\right)}}$$

$$C = 0.41nF$$

we know that $h_{fe} \geq 4K + 23 + \frac{29}{K}$

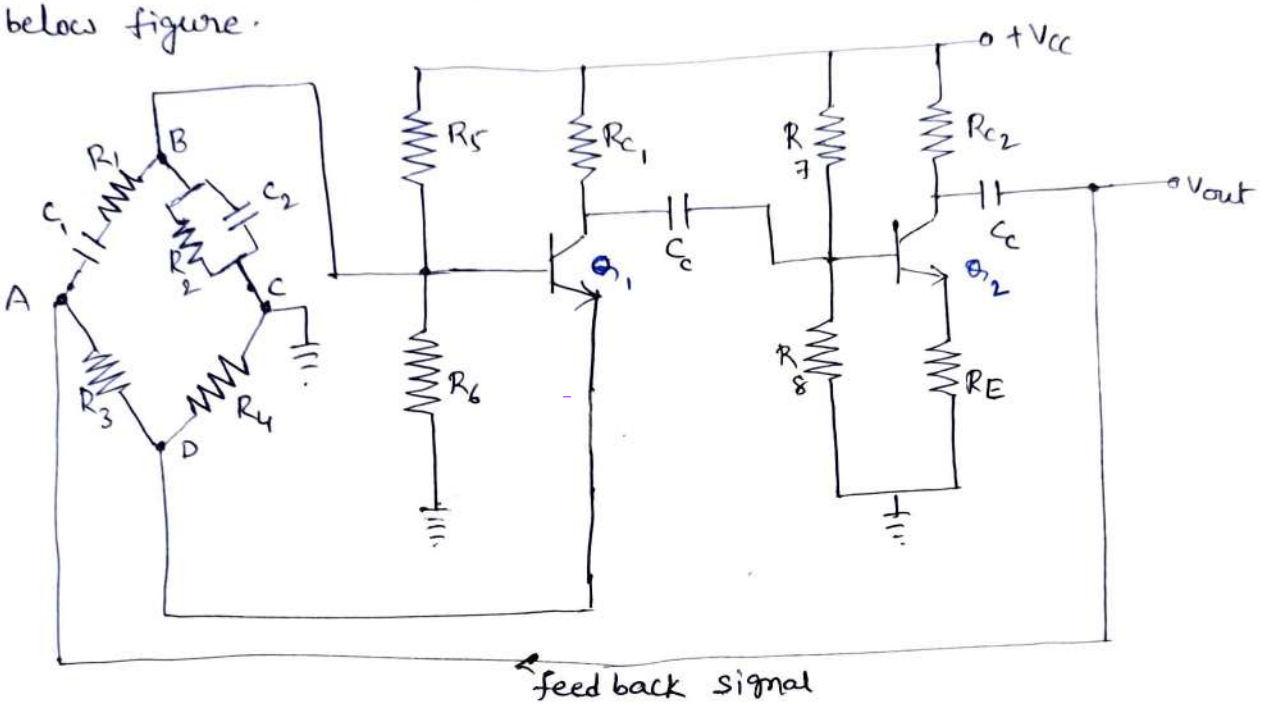
$$\Rightarrow h_{fe} \geq 4\left(\frac{R_c}{R}\right) + 23 + \frac{29}{(R_c/R)}$$

$$\Rightarrow h_{fe} \geq 4\left(\frac{40\times10^3}{7.1\times10^3}\right) + 23 + \frac{29\times7.1\times10^3}{40\times10^3}$$

$$\therefore h_{fe} \geq 50.67$$

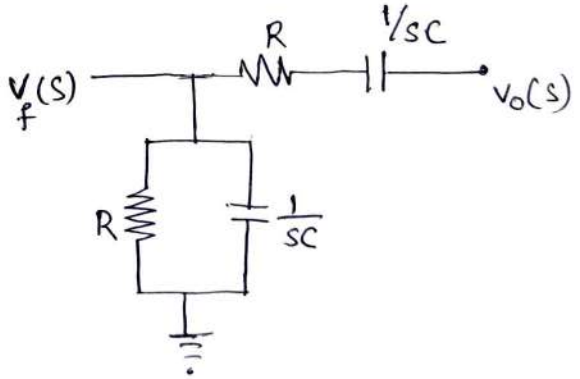
Wien-Bridge oscillator:

The circuit diagram for a wien-bridge oscillator is as shown in below figure.



fig(a): Wien-Bridge oscillator circuit

A wien-bridge oscillator circuit contains a two stage RC coupled amplifier which provides a phase shift of 360° (or) 0°.



fig(b): Equivalent Circuit

A balanced bridge is used as a feedback network in which there is no necessity for any additional phase shift.

The feedback network consists of a lead-lag network R_1-C_1 and R_2-C_2 and a potential divider R_3-R_4. The lead-lag network provides a positive feedback to the input of the first stage transistor Q_1 i.e base

of the transistor Q_1 and the voltage divider provides a negative feedback to the emitter of Q_1.

The frequency of oscillations is determined by the series element R_1, C_1 and parallel elements R_2, C_2 of the bridge and it is given as $f_0 = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then $f_0 = \frac{1}{2\pi\sqrt{R^2C^2}}$

$$\therefore f_0 = \frac{1}{2\pi RC}$$

The bridge is said to be balanced if $\frac{R_3}{R_4} = \frac{R_1 + \frac{1}{j\omega C_1}}{R_2 \| \frac{1}{j\omega C_2}} = \frac{R_1 - \frac{j}{\omega C_1}}{R_2 \| \frac{-j}{\omega C_2}}$

$$\Rightarrow \frac{R_3}{R_4} = \frac{R_1 - \frac{j}{\omega C_1}}{\left(\frac{-jR_2}{\omega C_2}\right) \Big/ R_2 - \frac{j}{\omega C_2}}$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2}\left(R_1 - \frac{j}{\omega C_1}\right)\left(R_2 - \frac{j}{\omega C_2}\right)$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2}\left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} - \frac{jR_2}{\omega C_1} - j\frac{R_1}{\omega C_2}\right]$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2}\left[\left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2}\right] - \frac{j}{\omega}\left[\frac{R_2}{C_1} + \frac{R_1}{C_2}\right]\right]$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2}\left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2}\right] + \frac{C_2}{R_2}\left[\frac{R_2}{C_1} + \frac{R_1}{C_2}\right]$$

Comparing imaginary parts on both sides we get

$$\frac{\omega C_2}{R_2}\left(R_1 R_2 - \frac{1}{\omega^2 C_1 C_2}\right) = 0 \Rightarrow R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} = 0$$

$$\Rightarrow \omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\Rightarrow \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\therefore f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (\because \omega = 2\pi f_0)$$

If $R_1 = R_2 = R$, $C_1 = C_2 = C$ then

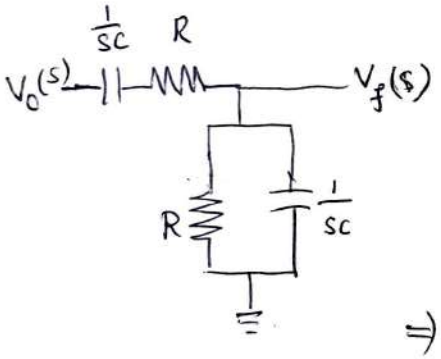
$$f_0 = \frac{1}{2\pi RC}$$

The ratio of R_3 and R_4 should be greater than 2 to provide a sufficient gain for the circuit to provide the desired frequency of oscillation.

Gain of the BJT amplifier used in Wien bridge oscillator

Assume $R_1 = R_2 = R$ and $C_1 = C_2 = C$. Then feed back circuit is as shown in figure (b).

From figure(b) $V_f(s) = V_0(s) \cdot \dfrac{\left(R \parallel \frac{1}{sC}\right)}{\left(R \parallel \frac{1}{sC}\right) + R + \frac{1}{sC}}$



$$\Rightarrow \frac{V_f(s)}{V_0(s)} = \frac{\frac{R \cdot \frac{1}{sC}}{R + \frac{1}{sC}}}{\frac{R \cdot \frac{1}{sC}}{R + \frac{1}{sC}} + R + \frac{1}{sC}}$$

$$\Rightarrow \frac{V_f(s)}{V_0(s)} = \frac{\frac{R}{RSC+1}}{\frac{R}{RSC+1} + R + \frac{1}{sC}} = \frac{\frac{R}{RSC+1}}{\frac{RSC + R^2S^2C^2 + RSC + RSC + 1}{(RSC+1)sC}}$$

$$\therefore \beta = \frac{V_f(s)}{V_0(s)} = \frac{RSC}{R^2S^2C^2 + 3RSC + 1}$$

We know that $A\beta = 1 \Rightarrow A = \frac{1}{\beta} = \frac{R^2S^2C^2 + 3RSC + 1}{RSC}$

$$\Rightarrow A = RSC + 3 + \frac{1}{RSC}$$

Substituting $S = j\omega = \frac{j}{RC}$

$$\Rightarrow A = R\left(\frac{j}{RC}\right)C + 3 + \frac{1}{R\left(\frac{j}{RC}\right)C}$$

$$A = j + 3 + \frac{1}{j} \Rightarrow \boxed{A = 3}$$

Therefore the gain of the BJT amplifier is atleast equal to 3 for oscillations to be occured in a wienbridge oscillator.

i.e $\boxed{A \geq 3}$

Problem: In a wien bridge oscillator if the value of R is 100KΩ, frequency of oscillation is 10KHz find the value of capacitor C.

Sol) For wien bridge oscillator the frequency of oscillation is

$$f_0 = \frac{1}{2\pi RC} \Rightarrow C = \frac{1}{2\pi R f_0} = \frac{1}{2\pi (100\times10^3)(10\times10^3)}$$

$$\therefore \quad C = 159PF.$$

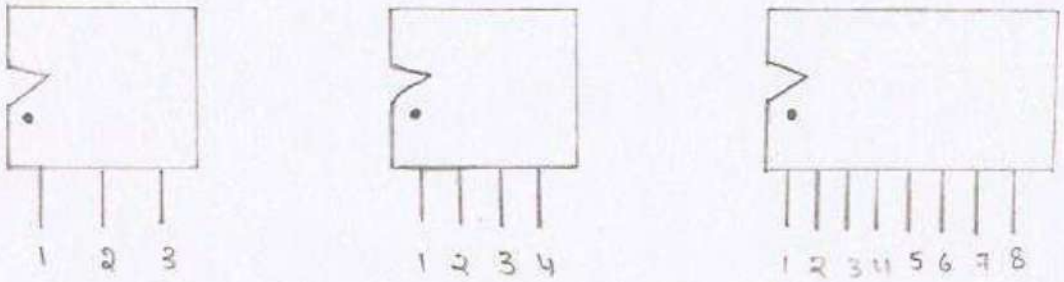
Introduction :-

Integrated Circuits (IC) play a very important part in Electronics.

Most of the IC's specially made for a specific task and contains upto thousands of Transistors, Diodes & Resistors.

Special purpose IC's such as Audio amplifiers, FM radios, logic blocks, regulators and even a whole micro computer in the form of a micro controller can be fitted inside a tiny package.

Some of simple integrated circuits are shown in below figures.



Depending on the way of manufacturing integrated circuits can be divided into two groups.

1. Hybrid
2. Monolithic

Hybrid :

Hybrid contains more than one layer.

Monolithic :

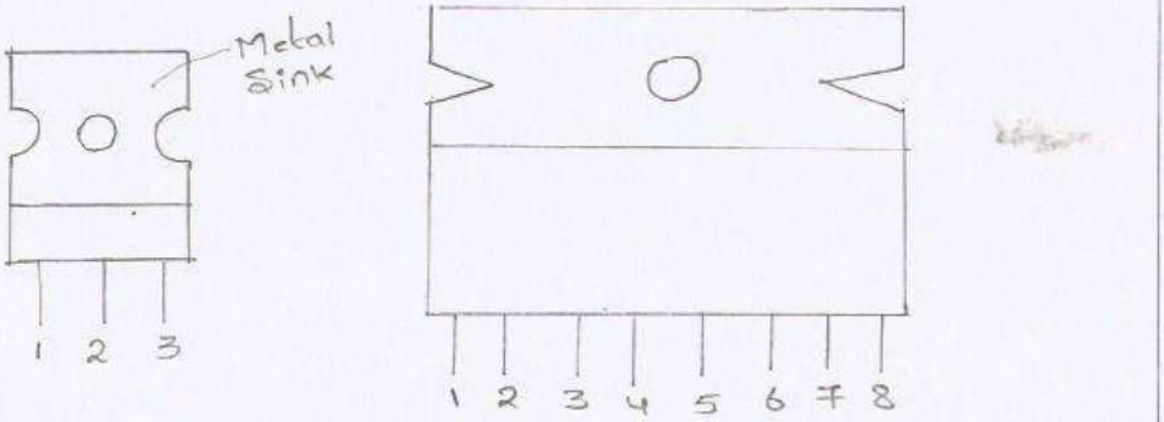
It contains only one layer.

Most of the integrated circuits are in DIL (Dual

in line) package. This means that there are two rows of pins.

The device is view from the top and the pins are numbered in an anticlockwise direction.

High power IC's can generate more heat and they have metal tag that can be connected to a heat sink to dissipate the heat.



IC's can be divided into two further groups.

1. Analog
2. Digital

Analog IC's :

Analog IC's is refered to as a output voltage of a linear circuit is continous and follows changes any input.

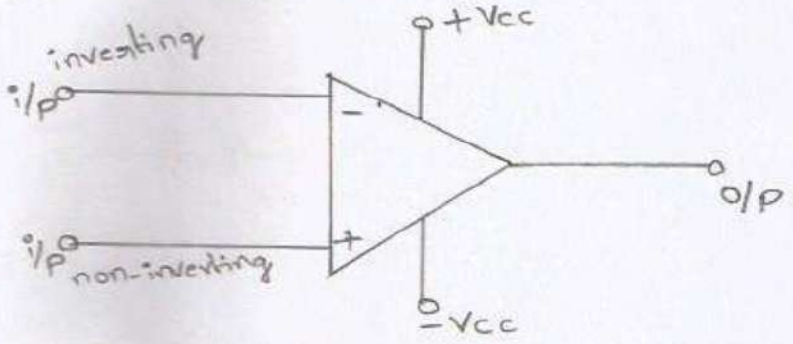
Ex : Audio Amplifier

When signal from a microphone is connected to the input, the output will vary in the same way as the voltage from microphone.

Digital IC's :

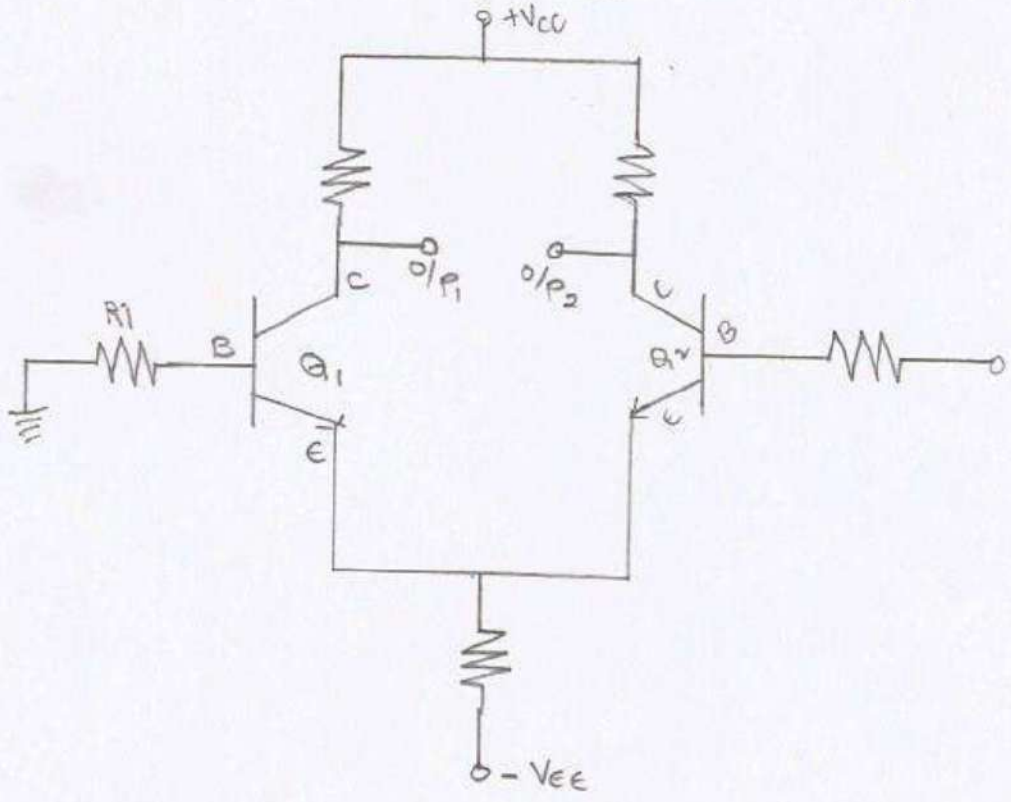
It is refered to as a output voltage is not continous. It is either low or high. and it changed from one state to other very quickly.

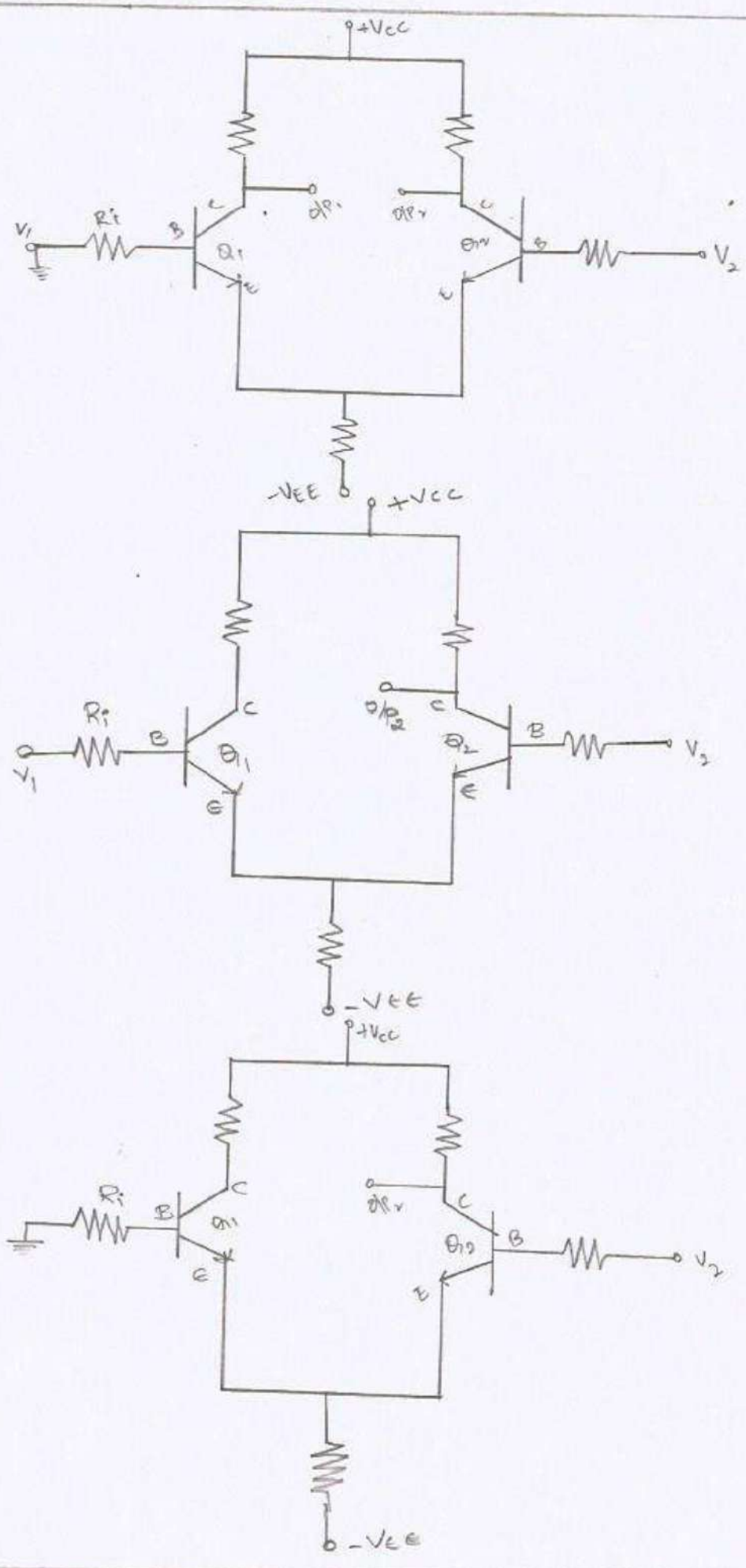
The symbol of an IC is commonly used as a amplifier (or) operational amplifier.



Differential amplifier is an device which is used to amplifies the difference of two input signals. It has 4 configurations.

1. Dual i/p, balanced o/p Differential Amplifier
2. Dual i/p, unbalanced o/p Differential Amplifier
3. Single i/p, balanced o/p Differential Amplifier
4. Single i/p, unbalanced o/p Differential Amplifier




+Vcc
V1
Ri
B
C
Q1
o/p1
o/p2
Q2
V2
E
-VEE
+Vcc
Ri
V1
B
C
Q1
o/p2
Q2
B
V2
E
-VEE
+Vcc
Ri
B
C
Q1
o/p2
Q2
B
V2
E
-Vee

* Basic Information of Op-Amp :-

Op-Amp is a operational Amplifier. Op-Amp is an integrated circuit that operates as a voltage amplifier. An Op-amp has a differential input. The symbol for an op-amp along with its various terminals is shown in below fig.

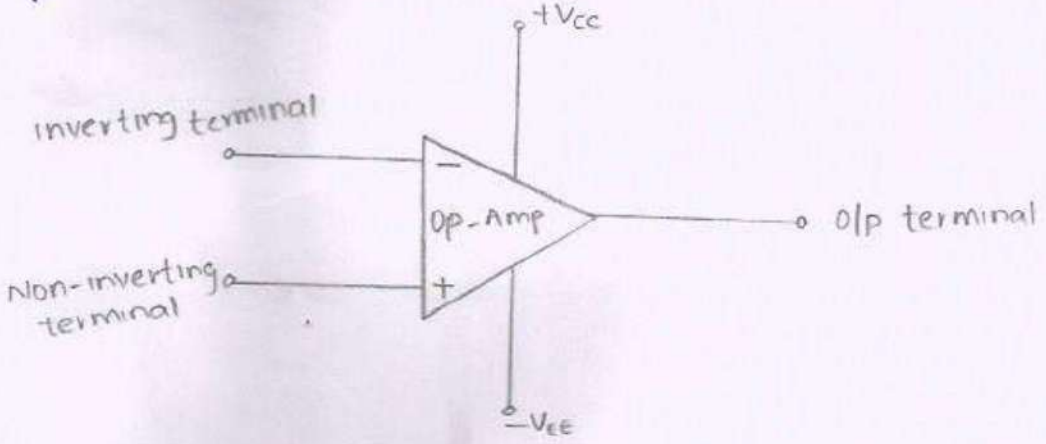


fig :- Symbol of an Op-Amp

The op-amp is indicated by a triangle with points in the direction of the signal flow.

→ Op-amp has 2 inputs of opposite polarities and it has single o/p and has 2 power supplies.

→ These amplifiers are called Operation Amplifiers because they were initially designed as an effective device for performing arithmetic operations (+, −, ×, %) in an analog circuit.

→ Almost all the op-amp have atleast 5 terminals

a. The positive supply voltage terminal $+V_{cc}$

b. Negative supply voltage terminal $-V_{EE}$

c. Output terminal

d. Inverting input terminal (−)

e. Non-inverting input terminal (+).

→ The i/p at inverting terminal is positive voltages the o/p is -Ve voltage and vice versa.

→ While the i/p at non-inverting terminal results is the same polarity output signal at the o/p terminal. This is shown in below fig:

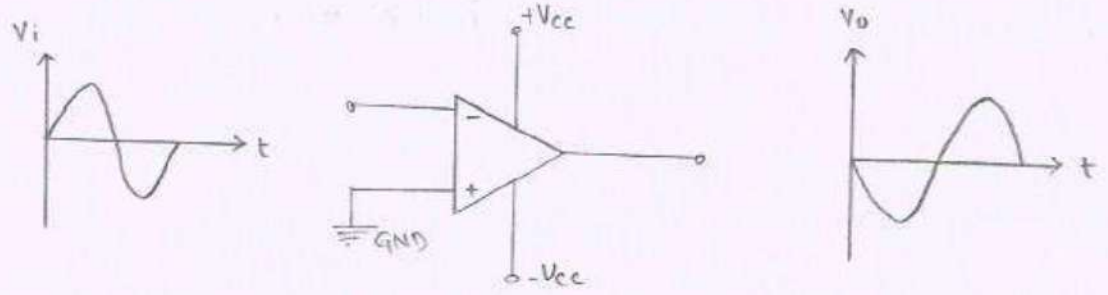


fig: input is applied to the inverting terminal

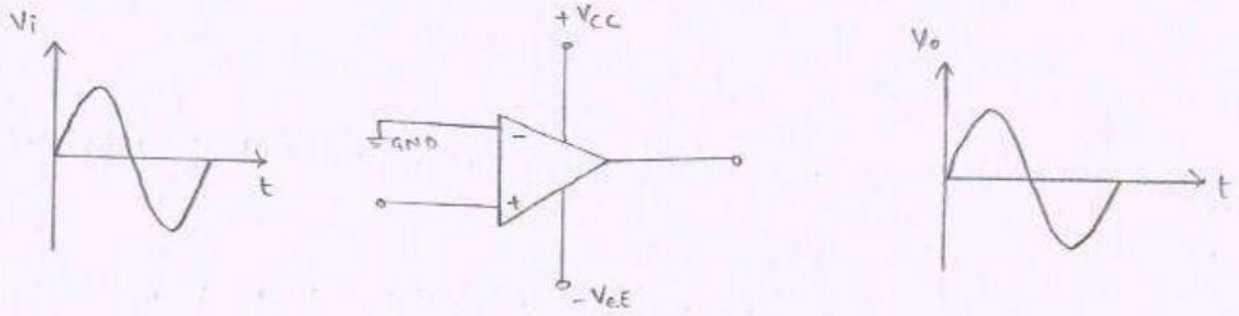


fig: input is applied to the Non-inverting terminal

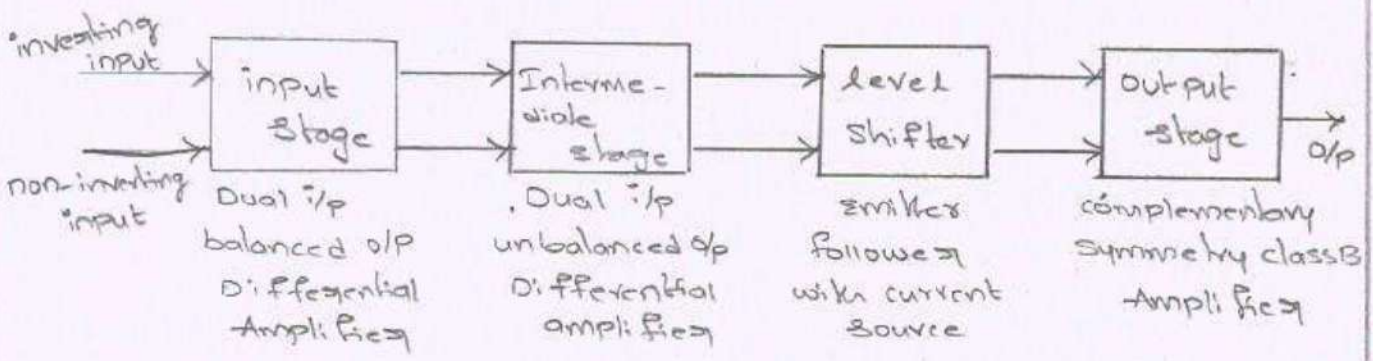
→ The Op-amp works on dual power supply.

→ The dual power supply is generally balanced i.e., the voltage of the +ve supply +Vcc and -Ve supply -VEE are in same magnitude. The typically used power supply voltages are ±15V.

→ But if the 2 voltage magnitudes are not equal in a dual supply it is called as unbalanced power supply.

→ But almost we use the balanced dual power supply for Op-amp in practically.

* Block Diagram of Op-Amp :-



The fig. shows the block diagram of Op-amp. It consists of 4 cascaded blocks.

a. Input stage
b. Intermediate stage
c. Level shifter
d. Output stage

1. Input stage :-

The ~~output~~ input stage requires high i/p impedence to avoid loading on the sources. It requires 2 i/p terminals & also it requires low o/p impedence.

→ All such requirements are achieved by using dual i/p balanced o/p differential amplifier at the i/p stage.

→ This stage provides most of the voltage gain of the amplifier & also establishes the i/p resistance of the amplifier.

2. Intermediate Stage :-

The o/p of the i/p stage drives the next stage which is an intermediate stage. This is another differential amplifier with dual i/p unbalanced o/p i.e., single ended o/p.

→ The overall gain of requirement of the op-amp is very high.

→ In most of the amplifier an intermediate stage is a dual i/p unbalanced o/p differential amplifier. This stage increases voltage gain of the amplifier.

3. Level shifting stage :-

The level shifting stage is used after the intermediate stage to shift the dc level at the o/p of the intermediate stage downward to zero volts wrt ground.

→ Here coupling capacitors are not used to couple the amplifiers in the intermediate state. Dc biasing voltage level propagates through the amplifier. Due to this a significant dc level appears at the o/p along with ac o/p.

→ Due to this effect o/p gets distorted & limits the maximum o/p voltage. This is shown in below fig.

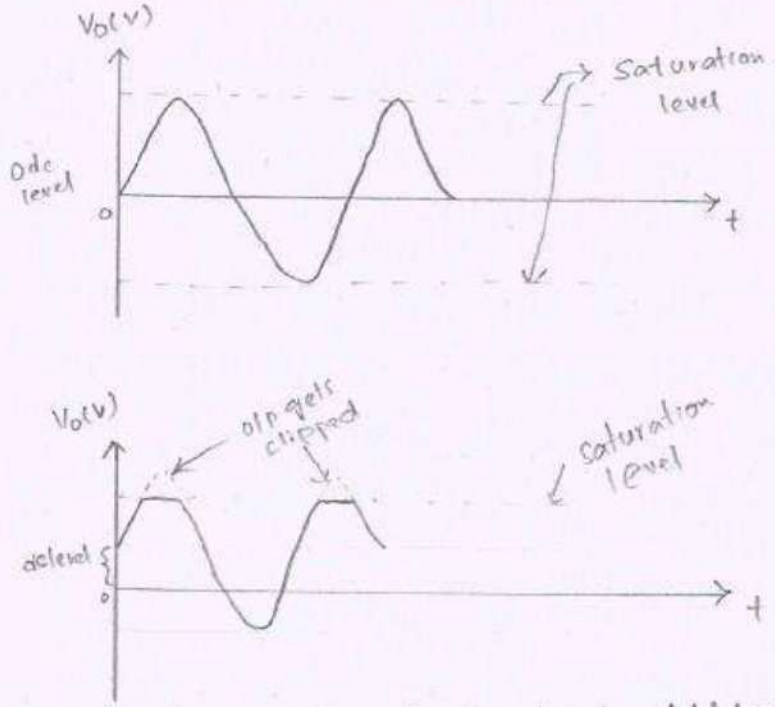


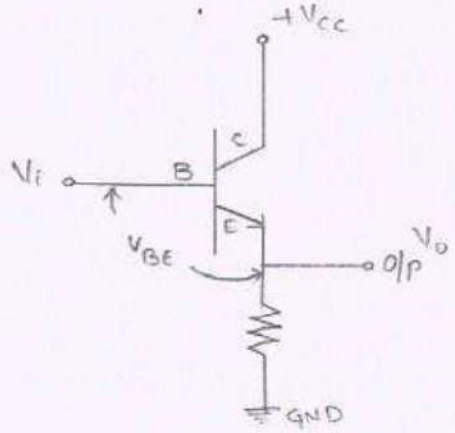
fig: Distorted o/p due to Additional level.

→ So the main purpose of the level shifting stage is to shift the o/p '0' point dc level towards the ground with

minimum change in the ac signal.

→ This also satisfies that the o/p should have equal voltage level of 0V for '0' i/p signal.

Eg :- 1. How to vary o/p vtg by giving i/p



Applying KVL to the i/p side

$$V_i - V_{GS} - V_o = 0$$

$$\boxed{V_o = V_i - V_{GS}}$$

By varying i/p vtg, the o/p is decreasing.

Proof :- Let us assume that

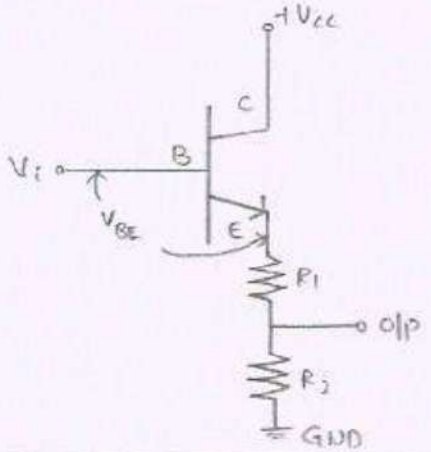
$$V_i = 5V \;,\; V_{GS} = V_{BE} = 0.7\,V$$

$$V_o = V_i - V_{GS}$$

$$= 5 - 0.7$$

$$\boxed{V_o = 4.3\,V}$$

Eg : 2



Applying KVL to the circuit

$$V_i - V_{BE} - I(R_1 + R_2)$$

$$I(R_1 + R_2) = V_i - V_{BE}$$

$$I = \frac{V_i - V_{BE}}{R_1 + R_2}$$

$$\frac{V_o}{R_2} = \frac{V_i - V_{BE}}{R_1 + R_2}$$

$$V_o = \frac{V_i - V_{BE}}{R_1 + R_2} \times R_2$$

proof :- Let us assume

$$V_{o'} = \frac{5 - 0.7}{10 + 4} \times 4$$

$$= \frac{4.3 \times 4}{14}$$

$$= \frac{17.2}{14}$$

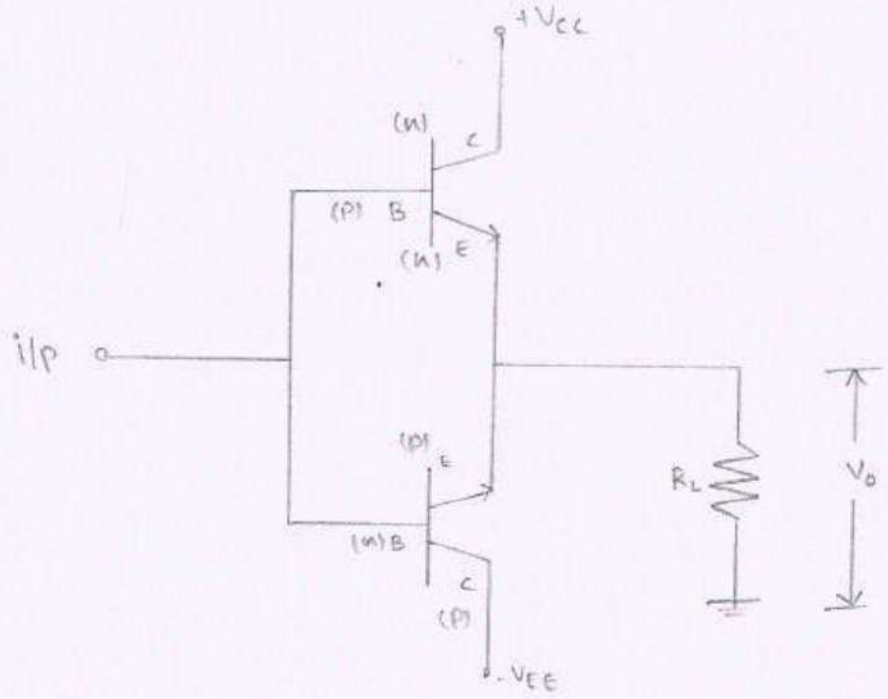
$$V_o = 1.22 \quad V_o \downarrow$$

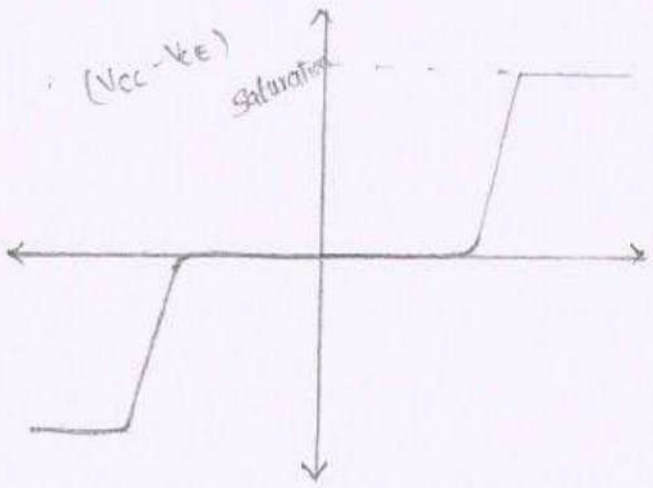
4. Output Stage :-

The last stage is a complimentary class B pushpull amplifier. The basic requirements of an o/p stage are low o/p impedence.

1. large o/p voltage
2. large o/p current
3. low o/p impedence
4. low power dissipation
5. Short circuit protection.

A pushpull amplifier satisfies the above requirements & hence commonly used in the o/p stage of an Op-amp.





*Packages and Pinouts :-

The Op-amp is fabricated on a very small silicon chip and is package in a suitable case.

The Op-amp is generally available in 2 packages.

1. Metal can
2. DIP (Dual in line package)

→ Metal can's are available with 8, 10 or 12 pins.

→ DIP packages are having 8 (or) 14 pins.

→ DIP package is most widely used.

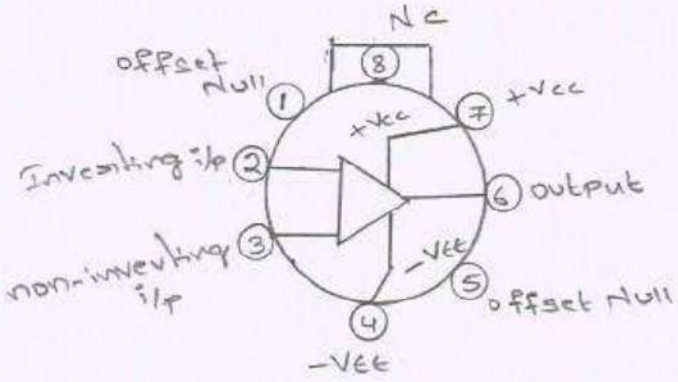


fig: Metal Can Package

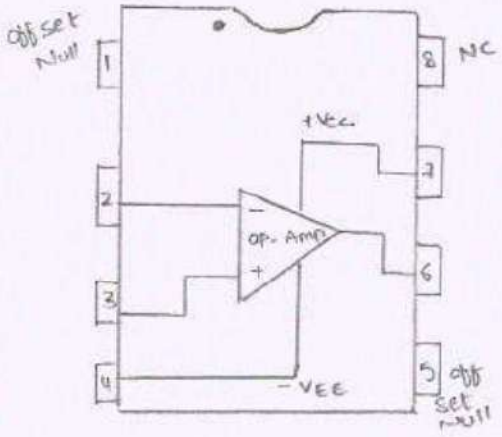


fig: 8-pin DIP package

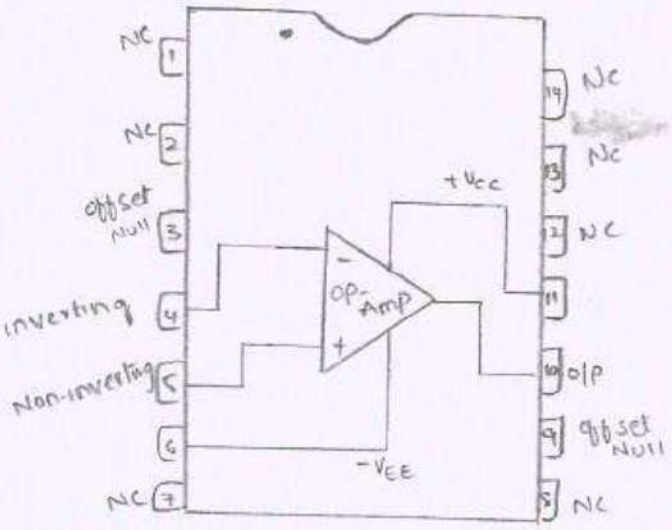
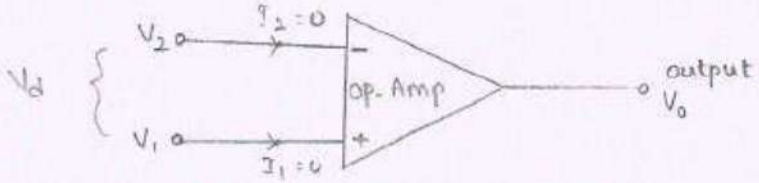


fig: 14-pin DIP package

* Ideal Op-Amp :-



The above fig. shows an ideal op-amp. It has two i/p signals V_1 & V_2 applied to non-inverting and inverting terminals respectively.

The op-amp amplifies the difference b/w the voltages applied at the non-inverting i/p & inverting i/p.

→ V_1 is the voltage applied at the non-inverting terminal and V_2 is the voltage applied at the inverting terminal. The difference between the 2 voltages ($V_1 - V_2$) can be acts as an input to the op-amp. It is denoted by V_d.

$$V_d = V_1 - V_2$$

→ If the gain of the op-amp is 'A', then

$$A = \frac{V_{out}}{V_d}$$

$$V_{out} = A \times V_d$$

→ The above expression says that the o/p voltage is directly proportional to the algebric difference b/w the 2 i/p voltages.

→ Hence the op-amp amplifies the difference b/w the 2 i/p voltages.

→ A ideal op-amp draws no current at the i/p terminals i.e., $I_1 = I_2 = 0$. Hence its i/p impedence is infinity ($Z_i = \infty$). This means that any source can drive it & there is no loading effect on the drivers stage.

→ The gain of an ideal op-amp is infinity, hence the differential i/p $V_d = V_1 - V_2$ is essentially zero for the finding o/p voltage V_{out}.

→ The o/p voltage V_{out} is independent of current drawn from the o/p terminals thus its o/p impedence is zero.

→ Hence output can drive an infinite of other circuits.

* Characteristics of an Ideal Op-Amp :-

1. Infinite input Resistance :

It is denoted by R_i and it is infinite for an ideal op-amp. This ensures that no current can flow into an ideal op-amp.

2. Infinite Voltage Gain :

It is denoted by A_{OL} (or) A. It is infinite for an ideal op-amp.

3. Zero o/p impedence :

It is denoted by R_o. It is infinite for an ideal op-amp.

4. Zero offset Voltage :

The presence of the small o/p voltage $V_1 = V_2 = 0$ is called as an offset voltage. It is zero for an ideal op-amp.

5. Infinite Band width :

The band width of an ideal op-amp is infinite. This means that the operating frequency range is from 0 to ∞. This ensures that the gain of the op-amp remains constant over the frequency range from dc to infinite frequency. Therefore an op-amp can amplify dc as well as ac signals.

6. Infinite CMRR :

It is defined as the ratio of differential gain and common mode gain. It is infinite for an ideal op-amp.

$$CMRR = \frac{A_D}{A_C}$$

7. Slew Rate :

It is defined as the maximum rate of change of o/p voltage with respect to time. It is infinite for an ideal op-amp.

It is denoted by 's'.

$$S = \frac{dV_o}{dt}$$

* Practical Op-Amp :-

The characteristics of an ideal op-amp can be approximated closely enough, for many practical op-amp characteristics are little bit different than the ideal op-amp characteristics.

1. Input Resistance :

It is denoted by R_i. It has large value in practical op-amp. The typical value of op-amp is $2M\Omega$.

2. Open loop Gain :

It is the voltage gain of an op-amp when no feedback is applied, practically it is large.

3. output Impedence :

It is denoted by R_o. It has very small value. The typical value of o/p resistance is few ohms i.e., 1Ω or 2Ω etc.

4. Band Width :

The band width of a practical op-amp is very small but if we apply -ve feedback it can be increased to a desired value.

* Virtual Ground :-

It is the situation in which the inverting input of an op-amp is at ground potential even though it is not connected directly to ground.

Assuming that the op-amp is ideal and it is producing some finite o/p. Then the open loop gain will be finite.

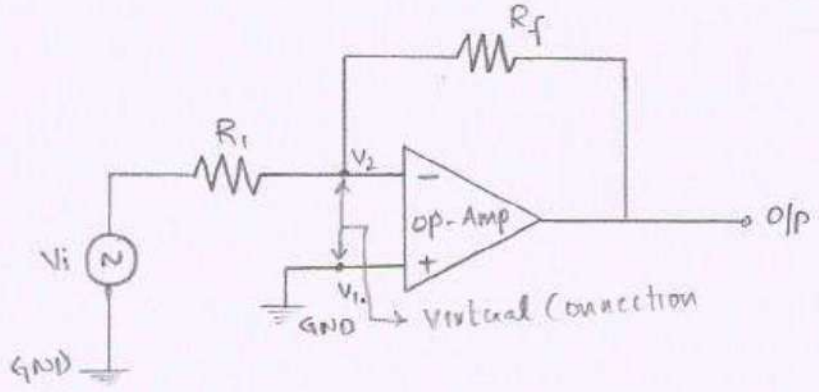


fig:- Practical Inverting Op-Amp.

For an op-amp, we know that

$$A = \frac{V_{out}}{V_d}$$

$$V_d = V_1 - V_2$$

$$A = \frac{V_{out}}{V_1 - V_2}$$

$$V_1 - V_2 = \frac{V_{out}}{A}$$

$$V_1 - V_2 = \frac{V_{out}}{\infty} = 0$$

$$V_1 - V_2 = 0$$

$$\boxed{V_1 = V_2}$$

→ From above eq" it is observes that the potential difference b/w 2 terminals is zero. We can say that virtual short circuit exists b/w the 2 i/p terminals.

→ Here, the word virtual is used to clear that actually we are not shorting the i/p terminals.

→ A virtual short circuit means that what ever voltage is at non-inverting terminal, it will automatically appear at the inverting terminal.

→ Here in fig. $V_1 = 0$, so we have $V_2 = 0$. Therefore potential at inverting terminal is zero and it is called virtual ground.

→ Virtual ground means that the terminal is not connected to the ground actually even then the voltage at the terminal is zero.

Temperature Ranges :-

There are 3 different temperature grades based on which the op-amp IC's are classified. These temperature ranges are;

1. Military Temperature Range : -55°c to +125°c (or) -55°c to +85°c.
2. Industrial Temperature Range : -20°c to +85°c (or) -40°c to +85°c.
3. Commerical Temperature Range : 0° to 70°c (or) 0°c to +75°c.

* DC characteristics :-

We have four different DC characteristics. They are;

1. input bias current.
2. input offset current.
3. input offset voltage.
4. Thermal Drift.

1. Input Bias Current :-

The average value of 2 currents flowing into the op-amp input terminals is called input bias currents. It is denoted by I_B. This is shown in below fig.

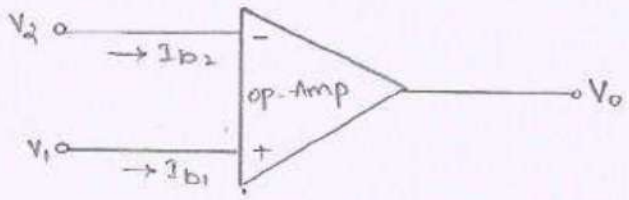


fig: input bias currents

Mathematically, it is expressed as

$$I_B = \frac{I_{b1} + I_{b2}}{2}$$

→ Ideally it should be zero, practically it should be $I_B = 200nA$.

→ Consider basic inverting amplifier as shown in fig. ②

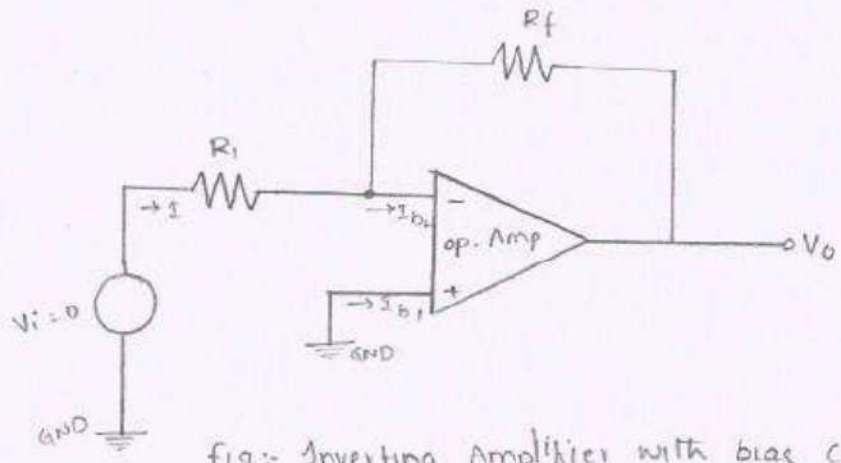


fig:- Inverting Amplifier with bias currents

→ If i/p voltage V_i is said to zero volts, the o/p voltage V_o should also be zero volt.

→ o/p voltage V_o is given that $V_o = I_b R_f$

for a op-amp have 1MΩ feedback resistor

$$V_o = 200\,nA \times 1M\Omega$$

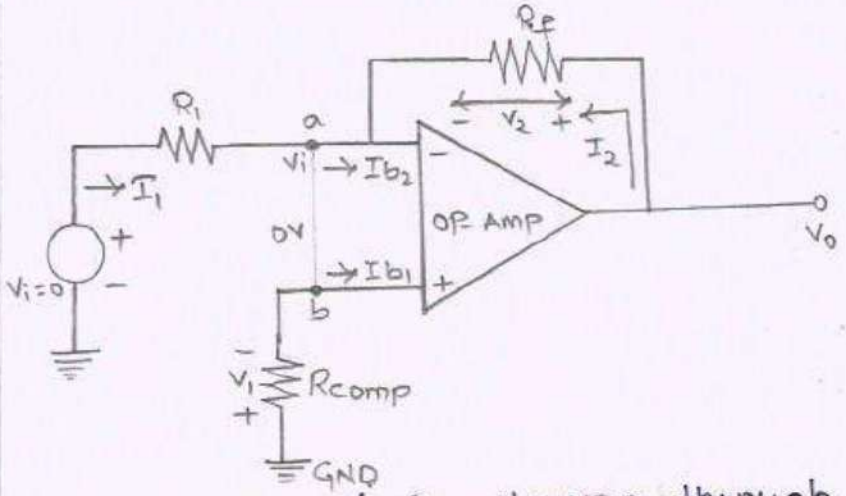
$$V_o = 200\,mV$$

→ The o/p is driven to 200mV with zero i/p because of the bias currents.

→ In applications where signal levels are measured in mV,

this is totally ac unacceptable.

→ This effect can be compensated by a compensation resistor [Rcomp] has been added between the non-inverting terminal and ground. It is shown in below fig.



→ Where current I_{b1} flowing through the compensating resistor [Rcomp] and V_1 voltage drop across it.

Applying KVL, we get

$$-V_1 + 0V + V_2 - V_0 = 0$$

$$V_0 = V_2 - V_1 \quad \rightarrow (1)$$

$$V_2 = V_1$$

→ By selecting proper value of Rcomp, V_2 can be cancelled with V_1 & o/p will be zero

→ The value of Rcomp is derived as

$$I_{b1} = \frac{V_1}{R_{comp}} \quad \rightarrow (2)$$

[droping vtg across Rcomp $V_1 = I_{b1} R_{comp}$]

→ The node 'a' is the voltage V_1 because the voltage at non-inverting terminal is V_1. so we get

$$I_1 = \frac{V_1}{R_1} \quad \rightarrow (3)$$

$$I_2 = \frac{V_2}{R_f}$$

from eq(1)

$V_1 = V_2$, so we get

$$I_2 = \frac{V_1}{R_f}$$

Applying KCL at node 'a' gives

$$I_{b2} = I_1 + I_2$$

$$= \frac{V_1}{R_1} + \frac{V_1}{R_f}$$

$$= V_1 \left[\frac{1}{R_1} + \frac{1}{R_f} \right]$$

$$= V_1 \left[\frac{R_f + R_1}{R_1 R_f} \right]$$

let us consider $I_{b1} = I_{b2}$

$$\Rightarrow \frac{V_1}{R_{comp}} = V_1 \left[\frac{R_1 + R_f}{R_1 R_f} \right]$$

$$\boxed{R_{comp} = \frac{R_1 R_f}{R_1 + R_f}} \qquad \left(\because R_{comp} = R_1 \| R_f \right)$$

i.e., to compensate for bias currents, the compensation resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting i/p terminal.

2. Input offset Current :

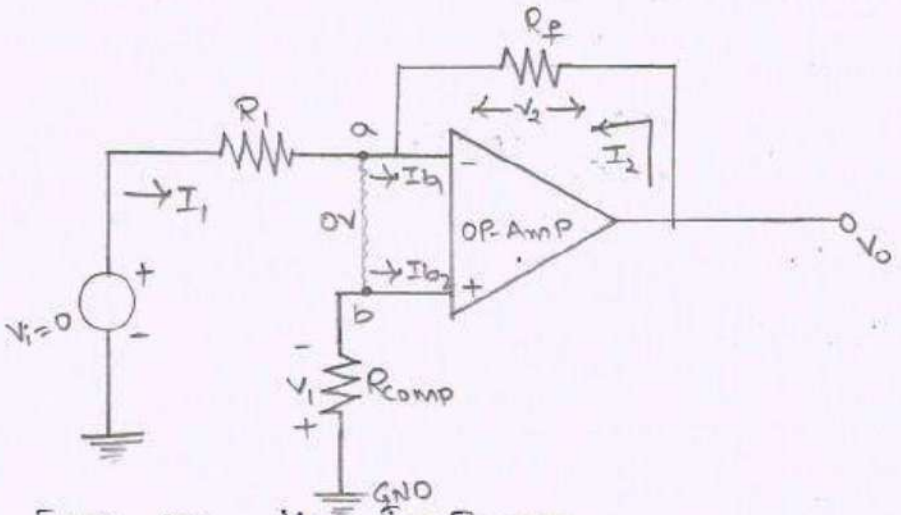
It is defined as the algebric difference between the currents flowing into the 2 i/p terminals of the op-amp. It is denoted by I_{ios}.

Mathematically it is given by

$$I_{ios} = I_{b1} - I_{b2}$$

Effect of i/p offset current on o/p voltage :

Let us consider the op-amp used in the closed loop configuration with R_{comp} as shown in below fig.



From fig. $V_1 = I_{b1} R_{comp}$

$$I_{b1} = \frac{V_1}{R_{comp}}$$

But $I_1 = \frac{V_1}{R_1}$

$$= \frac{I_{b1} R_{comp}}{R_1}$$

Now, $I_{b2} = I_1 + I_2$

$$I_2 = I_{b2} - I_1$$

So we get $I_2 = I_{b2} - \frac{I_{b1} R_{comp}}{R_1}$

We know that, $V_o = V_2 - V_1$

-from fig. $V_2 = I_2 R_f$

So, $V_o = I_2 R_f - I_{b1} R_{comp}$

$$= \left[I_{b2} - \frac{I_{b1} R_{comp}}{R_1} \right] R_f - I_{b1} R_{comp}$$

$$= \frac{\left[I_{b2} R_1 - I_{b1} R_{comp} \right] R_f}{R_1} - I_{b1} R_{comp}$$

$$= \frac{I_{b2} R_1 R_f - I_{b1} R_{comp} R_f - I_{b1} R_1 R_{comp}}{R_1}$$

$$= \frac{I_{b2} R_1 R_f - I_{b1} R_{comp} (R_1 + R_f)}{R_1}$$

$$= \frac{I_{b2} R_1 R_f - I_{b1} \left[\frac{R_1 R_f}{R_1 + R_f} \right] (R_1 + R_f)}{R_1}$$

$$= \frac{R_1 R_f (I_{b2} - I_{b1})}{R_1}$$

$$= R_f (I_{b2} - I_{b1})$$

$$\boxed{V_o = R_f I_{ios}}$$

→ The o/p voltage exists by the i/p offset current.

3. Input offset Voltage:

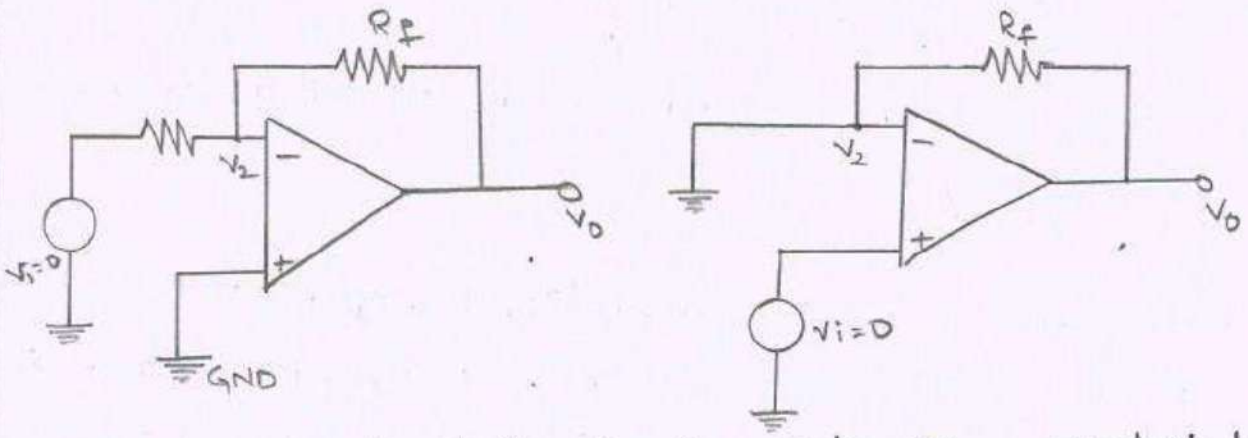
The differential voltage must be applied b/w the 2 i/p terminals of an op-amp, to make the o/p voltage zero is called as input offset voltage. It is denoted by V_{ios}.

→ Whenever both the i/p terminals of the op-amp are grounded ideally the o/p voltage should be zero. However, in this condition the practical op-amp shows a small non-zero o/p voltage. This is due to mis-matching present in the internal circuit of an op-amp. Such a voltage can cause error in the practical applications, for which op-amp is used.

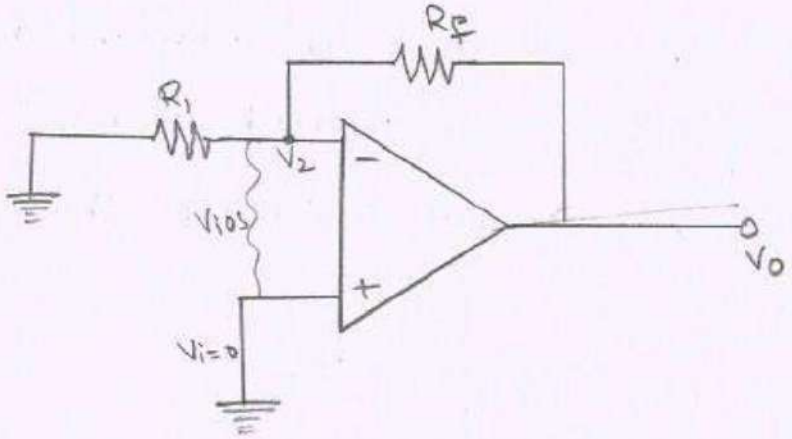
→ To make such a voltage to zero, it is necessary to apply small difference voltage b/w the 2 i/p terminals of an op-amp This voltage is called i/p offset voltage.

→ For an IC op-amp i/p offset voltage is 6mV.

→ Let us see the effect of V_{ios} on the o/p of non-inverting & inverting op-amp amplifiers shown in below figures.



→ The $V_i = 0$ for both the terminals, the equivalent becomes same as shown in below fig.



→ The voltage V_2 at the inverting i/p terminal is given by according to potential divider theorem.

$$V_2 = \frac{V_o R_1}{R_1 + R_f}$$

$$V_o = \frac{R_1 + R_f}{R_1} \times V_2$$

$$V_o = 1 + \frac{R_f}{R_1} \times V_2$$

Since $V_{ios} = V_i - V_2$

But $V_i = 0$

$$V_{ios} = V_2$$

we get,

$$V_o = \left[1 + \frac{R_f}{R_1}\right] \times V_{ios}$$

→ Thus the o/p voltage depends on the i/p offset voltage.

4. Thermal Drift :

Bias current, offset current (I_{ios}), off set voltage (V_{ios}) change with temperature. A circuit designed at 25°c may not remain so when temperature raises to 35°c. This is called drift.

→ Op-amp offset current drift is expressed nA/°c. and offset voltage drift is expressed in mV/°c.

→ There are very few circuit techniques that can be used to minimize the effect of drift.

1. Printed Circuit board layout (PCB)
2. Forced air cooling.

1. PCB Layout :

It can be used to keep op-amp away from source of heat.

2. Forced air Cooling :

It may be used to stablize the temperature.

Modes of Operation :

Op-Amp will performs the two modes operation.

1. Open loop mode of Operation
2. Closed loop mode of Operation.

1. Open Loop Mode of Operation :

It says that no feedback terminal in btw input and output but op-amp will performs the three basic operation in open loop mode of operation.

1. Inverting Amplifier
2. Non-inverting Amplifier
3. Differential Amplifier

(a) Inverting Amplifier :

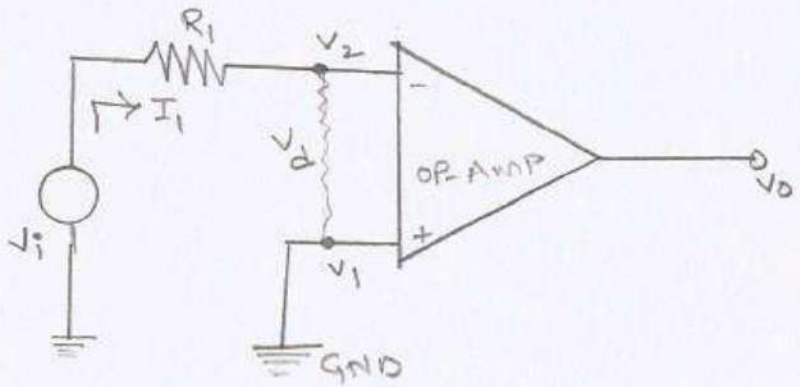


fig : Inverting Amplifier

→ In this the input is applied at inverting terminal and the non-inverting terminal is grounded.

→ In this the output is out of phase (180° phase shift) with the input.

→ we know that, open loop gain,

$$A = \frac{V_o}{V_d}$$

where, $V_d = V_1 - V_2$

So, $A = \frac{V_o}{V_1 - V_2}$

$V_o = A(V_1 - V_2)$

If source resistance R_i is very small, then it is neglected.

$\therefore V_2 = V_i$

$V_o = A(V_1 - V_i)$

from fig. $V_1 = 0$ (∵ it is connected to ground)

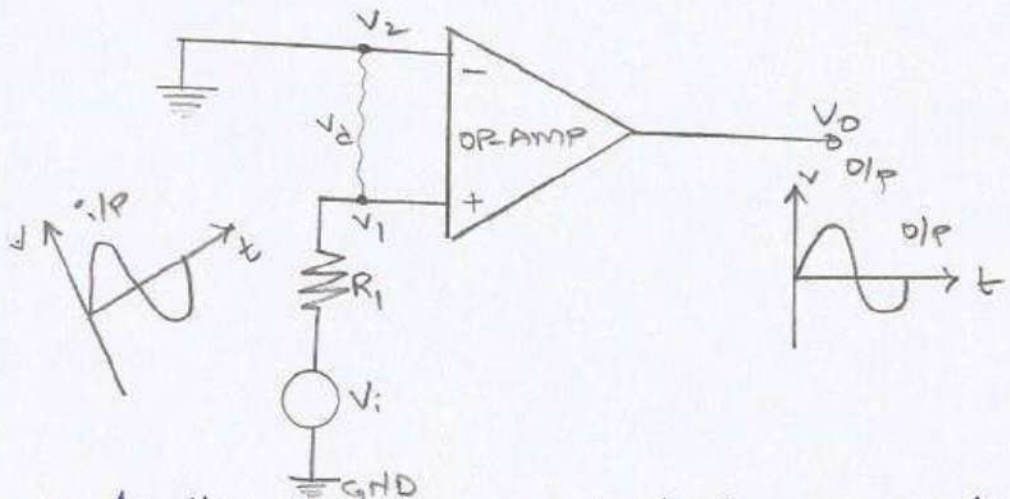
$V_o = A(0 - V_i)$

$$\boxed{V_o = -AV_i}$$

where, -ve sign indicates that phase shift provided in b/w input & output.

The above eqn says that the o/p voltage 'A' times larger (or) increased then the input.

(b) Non-inverting Amplifier:



→ In this the i/p is applied at non-inverting terminal and the inverting terminal is grounded.

→ In this the output is in phase (0° or 360°) with the i/p.

→ we know that open loop gain,

$$A = \frac{V_o}{V_d}.$$

where, $V_d = V_1 - V_2$

so, $$A = \frac{V_o}{V_1 - V_2}$$

$$V_o = A(V_1 - V_2)$$

→ If source resistance R_i is very small, then it is neglected.

$\therefore V_1 = V_i$

$$V_o = A(V_i - V_2)$$

from fig. $V_2 = 0$ (∵ it is grounded)

$$V_o = A(V_i - 0)$$

$$\boxed{V_o = AV_i}$$

where, +ve sign indicates that phase shift is zero provided in input and output.

(c) Differential Amplifier:

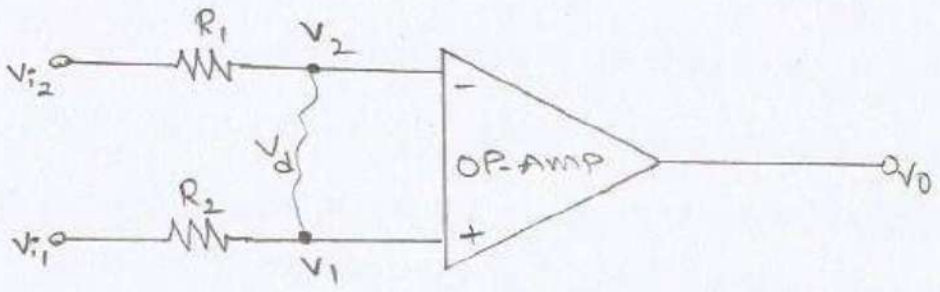


fig: Differential - Amplifier

→ In these inputs are applied at both the inverting and non-inverting terminals. Since the difference b/w two input signals is amplifies which is called Differential Amplifier.

→ We know that open loop gain,

$$A = \frac{V_o}{V_d}$$

where, $V_d = V_1 - V_2$

so, $A = V_o / V_d$

$$A = \frac{V_o}{V_1 - V_2}$$

$$V_o = A(V_1 - V_2)$$

→ If source resistance R_i is very small, then it is neglected.

$$V_{i_1} = V_1 \quad ; \quad V_{i_2} = V_2$$

so, $V_o = A(V_1 - V_2)$

$$\boxed{V_o = A(V_{i_1} - V_{i_2})}$$

2. Closed Loop Mode of Operation:

In this feedback exist, in b/w input & output. These feedback is a negative feedback.

→ Due to this negative feedback i/p resistance increases, output resistance decreases and noise is reduced. band width is increases and gain is decreases.

→ But op-amp will performs three basic operation in closed loop mode of operation.

1. Inverting Amplifier
2. Non-inverting Amplifier
3. Differential Amplifier.

(a) Inverting Amplifier :

In this inverting $^{i/p}$ is applied at the inverting terminal and non-inverting terminal is grounded.

→ In this o/p signal is out of phase with the input signal.

→ The o/p voltage V_o is fed back to the inverting input terminals through $R_f - R_1$ network.

Where, R_f = feedback resistor

→ The inverting amplifier circuit shown in below figure.

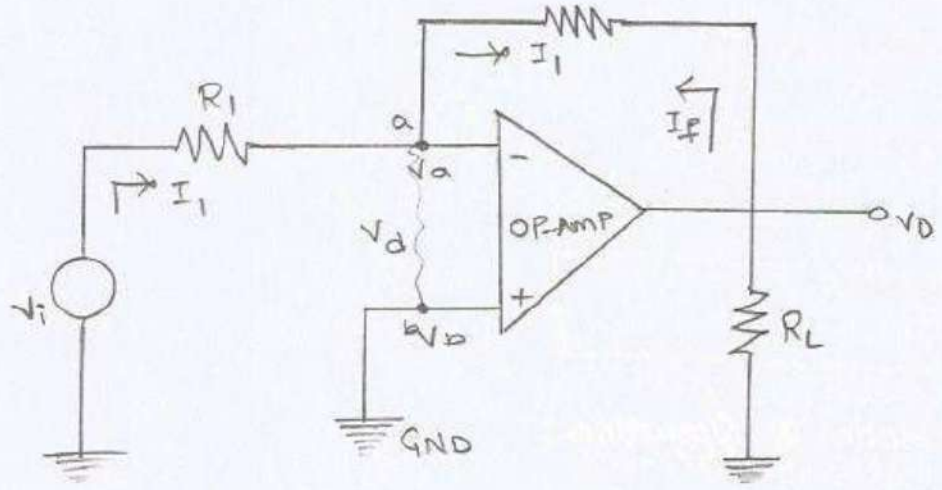


fig:

Analysis :

→ Let us assume an ideal op-amp $V_d = 0$. and node A is at ground potential (virtual ground potential) then and I_1 current flows through R_1 resistor.

So, $$I_1 = \frac{V_A}{R_1} \longrightarrow (1)$$

→ Since op-amp draws no current, all the current flowing with R_1 must flow through R_f resistors. The o/p voltage V_o is given by

$$V_o = -I_i R_f \rightarrow (2)$$

since on sub. eq(1) & (2), we get

$$V_o = -\frac{V_i}{R_1} \times R_f$$

$$\boxed{\frac{V_o}{V_i} = -\frac{R_f}{R_1}}$$

Hence the closed loop gain of the inverting amplifier is given by A_{CL}

$$A_{CL} = V_o/V_i$$

So, $$\boxed{A_{CL} = -\frac{R_f}{R_L}}$$

Method - II :

According to nodal eqn at node A,

$$I_1 = I$$

So, $$\frac{V_i - V_a}{R_1} = \frac{V_a - V_o}{R_f}$$

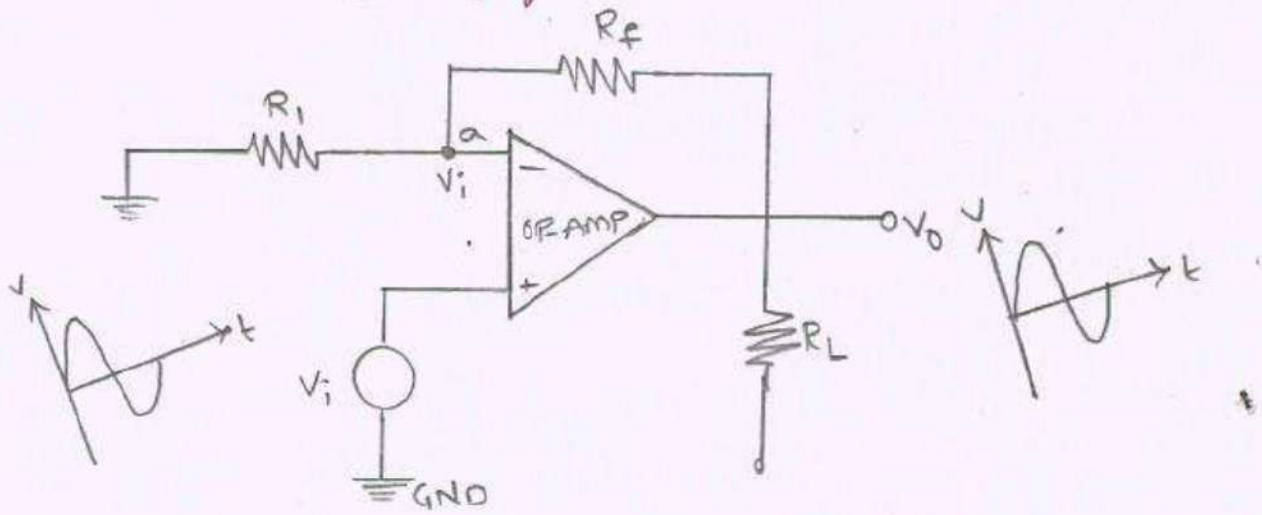
But $V_a = 0$; (because V_a is virtually grounded)

$$\frac{V_i}{R_1} = \frac{-V_o}{R_f}$$

$$\boxed{\frac{V_o}{V_i} = -\frac{R_f}{R_1}}$$

where, -ve sign indicates that the 180° phase shift provided in b/w input & output.

(b) Non-Inverting Amplifier :



→ If a signal is applied to the non-inverting input terminal then it is called as non-inverting amplifier.

→ If a signal is applied to the non-inverting terminal and feedback is connected from output to input as shown in above figure.

→ It may be noted that it is also a -ve feedback system as output is being fed back to the inverting input terminal.

→ As a differential voltage V_d at the input terminal of op-amp is zero, the voltage at node 'A' is V_i, same as the input voltage applied to non-inverting input terminal.

→ In circuit R_f and R_1 forms a potential divider. Hence, according to potential divider theorem,

$$V_i = \frac{R_1 V_o}{R_1 + R_f}$$

$$V_o = \frac{R_1 + R_f}{R_1} \times V_i$$

$$V_o = 1 + \frac{R_f}{R_1} \times V_i$$

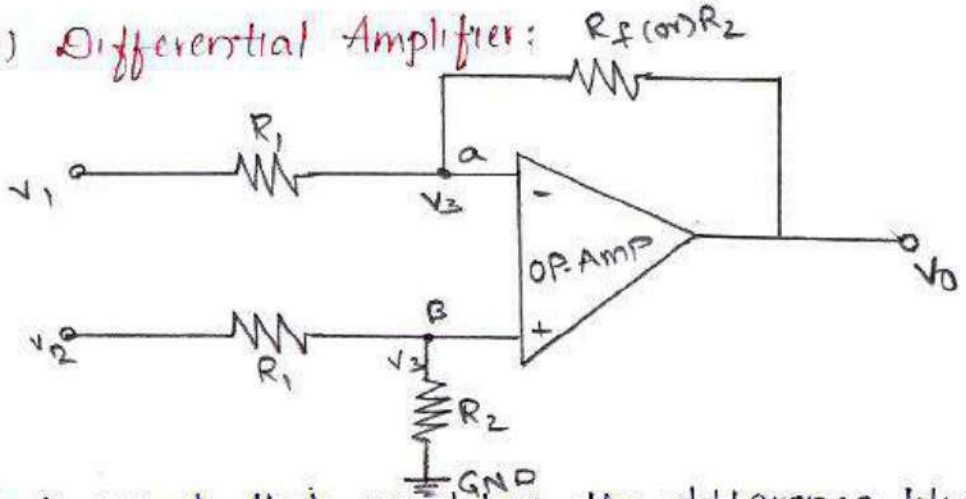
$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

We know that,

$$A_{CL} = \frac{V_o}{V_i}$$

$$\boxed{A_{CL} = 1 + \frac{R_f}{R_1}}$$

(e) Differential Amplifier:



→ A circuit that amplifies the difference b/w two input signals is called as difference amplifier (or) Differential amplifier.

→ The differential amplifier circuit is shown in above figure.

→ Since the differential voltage at the input terminal of the op-amp is zero.

→ Node A and Node B are at the same potential i.e., V_S.

→ The nodal eqn at node A is,

$$\frac{V_2 - V_3}{R_1} = \frac{V_S - V_o}{R_2}$$

$$\frac{V_3 - V_2}{R_1} + \frac{V_S - V_o}{R_2} = 0$$

$$V_S\left[\frac{1}{R_1} + \frac{1}{R_2}\right] - \frac{V_2}{R_1} - \frac{V_o}{R_2} = 0 \longrightarrow (1)$$

The nodal eqn at node B is

$$\frac{V_1 - V_3}{R_1} = \frac{V_3}{R_2}$$

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0$$

$$V_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right] - \frac{V_1}{R_1} = 0 \longrightarrow (2)$$

subtracting the above two equations, we get

$$V_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right] - \frac{V_2}{R_1} - \frac{V_0}{R_2} - V_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right] + \frac{V_1}{R_1} = 0$$

$$\frac{V_1}{R_1} - \frac{V_2}{R_1} - \frac{V_0}{R_2} = 0$$

$$1/R_1\left[V_1 - V_2\right] = V_0/R_2$$

$$\frac{V_0}{V_1 - V_2} = \frac{R_2}{R_1}$$

$$\boxed{V_0 = \frac{R_2}{R_1}(V_1 - V_2)}$$

Differential Mode Gain :

We know that,

$$V_0 = V A_d (V_1 - V_2)$$

$$V_0 = A_d \times V_d$$

where, A_d is the differential gain

→ The differential gain is the gain in which differential amplifier amplifies the difference b/w two input signals. Hence it is called as differential gain of the differential amplifier.

→ The difference b/w the two inputs $(V_1 - V_2)$ is generally is called as difference voltage that is represented by V_d.

So, $V_0 = A_d \times V_d$

$$A_d = \frac{V_o}{V_d}$$

→ The gain is represented by decibals and it is given by 20 log A_d.

Common Mode Gain:

→ The gain in which it amplifies the common mode signals (to same signals) to produce the output is called as Common mode gain of the differential amplifier. It is denoted by Ac.

→ If we apply two input voltages which are applied (or) equal in all the respects to the differential amplifier then ideally output voltage must be zero.

i.e., $V_o = V_1 - V_2$

If we know that, $V_1 = V_2$

we get, $\boxed{V_o = 0}$.

→ But the o/p voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs.

→ Such an average level of two input signals is called common mode signal, it is denoted as V_c.

i.e., $V_c = \frac{V_1 + V_2}{2}$

→ The o/p voltage is given by, when common input signal is consider.

$$\boxed{V_o = A_c \times V_c}.$$

→ Thus there exists some finite o/p. so the total o/p of any differential amplifier can be expressed as

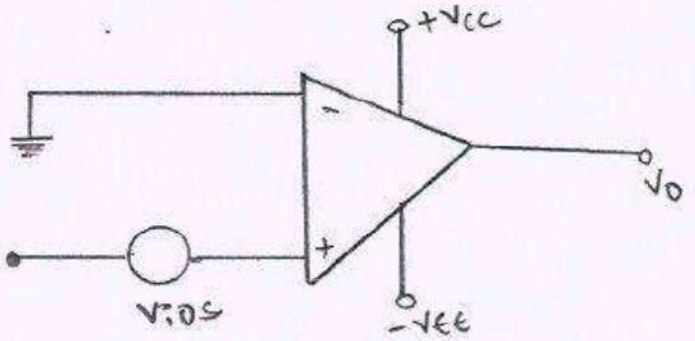
$$V_o = V_d A_d + A_c V_c$$

Note :

→ In op-amp differential mode gain is infinity and common mode gain is zero.

PSRR :

It is defined as the change in i/p offset voltage due to change in any one power supply, remaining power supply must be constant is called as "Power Supply Rejection Ratio". It is also called as power supply sensitivity (PSS).

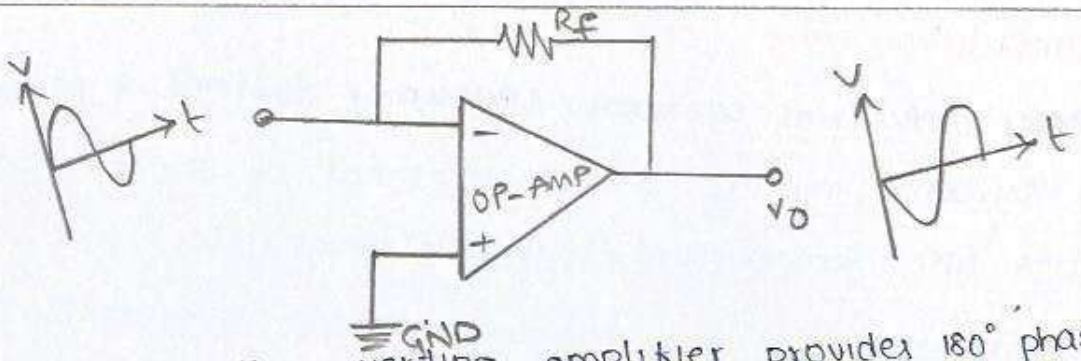


→ if V_{EE} = constant & due to certain change in V_{cc}, there is change in i/p offset voltage, then

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{cc}}\right|_{V_{EE} = \text{constant}}$$

→ if V_{cc} = constant & due to certain change in V_{EE}, there is change in i/p offset voltage, then

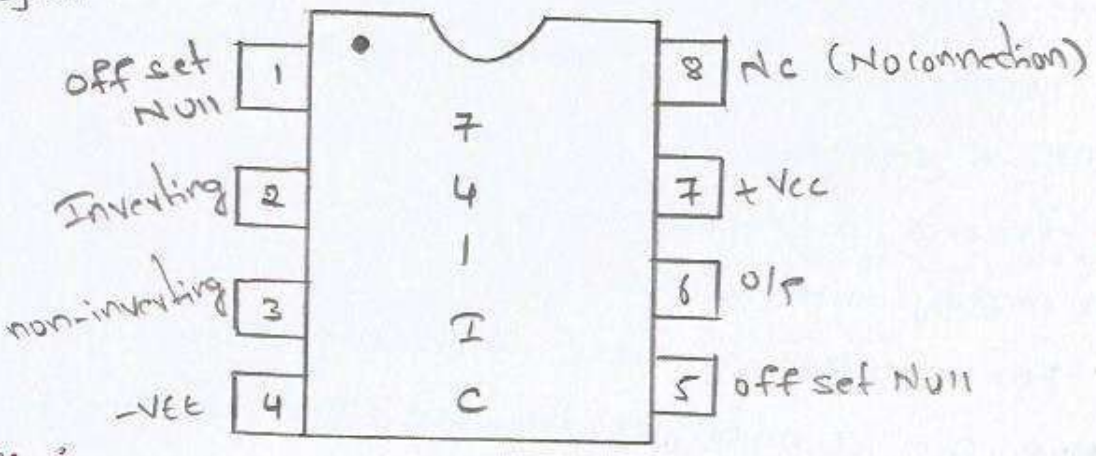
$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{EE}}\right|_{\Delta V_{cc} = \text{constant}}.$$



→ From fig. the inverting amplifier provides 180° phase shift blw o/p & i/p. so the op-amp can also be acts as inverter.

741 Op-amp and its features :

741 op-amp is a monolithic IC. It is available in 4 pin, 8 pin, 16 pin packages. Let us consider 8 pin package pin diagram.



Features :

1. No frequency compensation required.
2. short circuit protection provided.
3. offset voltage null capability.
4. Common mode & differential voltage range is large.
5. No latch-up.

UNIT IV
OP-AMPS APPLICATIONS

Basic Op-amp Applications

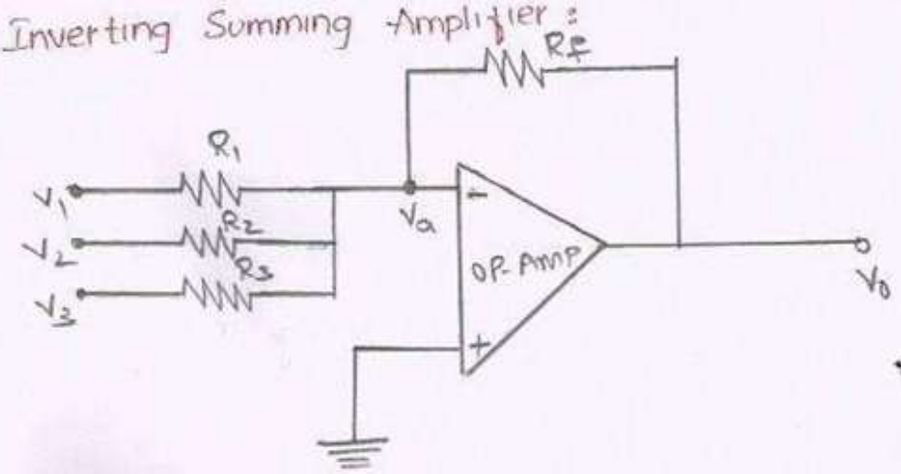
Summing Amplifier :

Op-amp may be used to design the circuit whose o/p is the sum of several i/p signals. such a circuit is called Summing Amplifier (or) summer.

→ The summing amplifier are classified into two types.

1. Inverting summing amplifier
2. Non-inverting summing amplifier.

1. Inverting Summing Amplifier :



→ A typical summing amplifier with 3 i/p voltages V_1, V_2, V_3 & three i/p resistors R_1, R_2, R_3 & one feedback resistor R_f shown in above fig.

→ The voltage at node 'a' is zero ($V_a = 0$) because the non-inverting terminal is grounded.

The nodal eqn at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = \frac{V_a - V_0}{R_f}$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_0}{R_f}$$

$$\frac{V_o}{R_f} = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

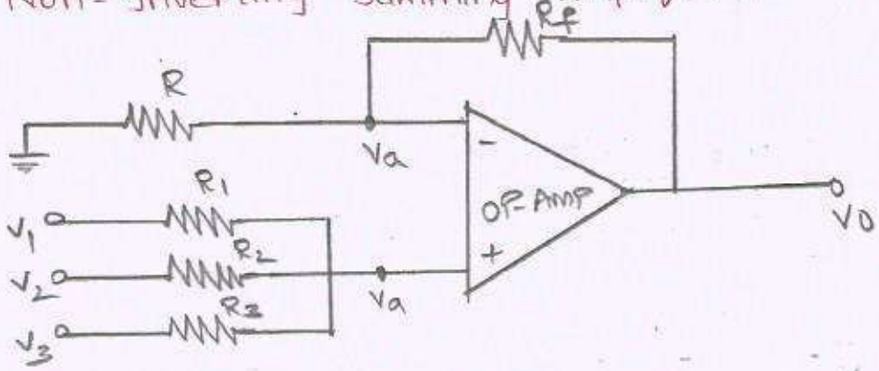
$$V_o = -\left[V_1 \frac{R_f}{R_1} + V_2 \frac{R_f}{R_2} + V_3 \frac{R_f}{R_3}\right]$$

Let $R_1 = R_2 = R_3 = R_f$

$$V_o = -\left[V_1 + V_2 + V_3\right]$$

where "-ve" sign indicates that phase difference b/w i/p & o/p. So it is called as inverting summing amplifier.

Q. Non-Inverting Summing Amplifier :



→ The non-inverting summing amplifier shown in above fig.

→ The i/p voltages V_1, V_2, V_3 is fed to the non-inverting terminal. The voltage at non-inverting i/p terminal is V_a.

→ The voltage at the inverting i/p terminal will also be V_a, because they are virtually grounded.

i.e., the voltage across the inverting terminal is same as that of the non-inverting terminal.

The nodal eq" at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$\frac{V_1}{R_1} - \frac{V_a}{R_1} + \frac{V_2}{R_2} - \frac{V_a}{R_2} + \frac{V_3}{R_3} - \frac{V_a}{R_3} = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = V_a\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right]$$

$$V_a = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_1 + 1/R_3}$$

w.k.t gain of non-inverting amplifier is

$$A = \frac{V_o}{V_d} = 1 + \frac{R_f}{R_1}$$

But Here $V_d = V_a$

$$V_o = \left[1 + \frac{R_f}{R}\right] V_a$$

sub. V_a in above eq^n

$$V_o = \left[1 + \frac{R_f}{R}\right]\left[\frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3}\right]$$

Let $R_1 = R_2 = R_3 = R = R_f/2$

$$V_o = \left[1 + \frac{R_f}{R_f/2}\right]\left[\frac{2V_1/R_f + 2V_2/R_f + 2V_3/R_f}{2/R_f + 2/R_f + 2/R_f}\right]$$

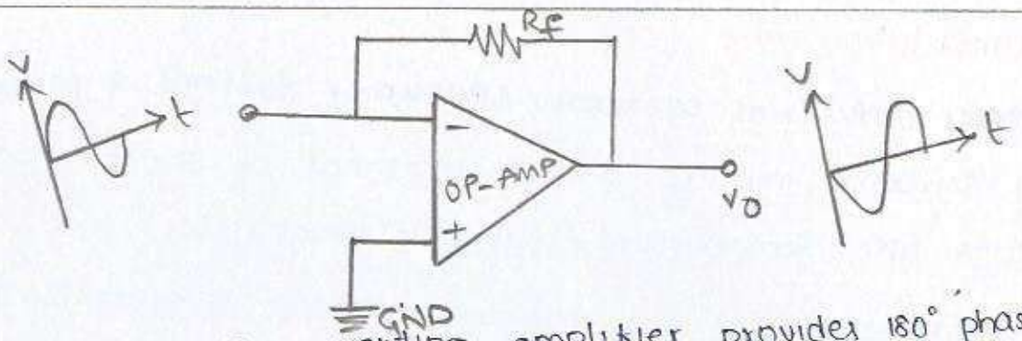
$$= 3 \times \frac{2(V_1 + V_2 + V_3)}{6}$$

$$\boxed{V_o = V_1 + V_2 + V_3}$$

→ Here the o/p voltage is in phase with sum of the i/p voltages. So it is called as non-inverting summing amplifier.

Invertor :

Invertor is defined as o/p is the compliment of i/p. For example, let us consider an inverting amplifier as shown in below fig.



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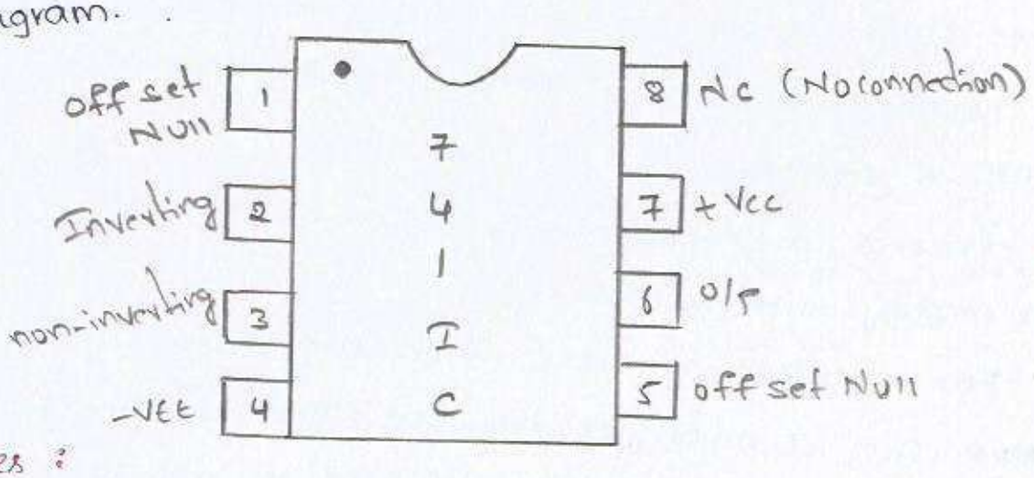


Features :

1. No frequency compensation required.
2. short circuit protection provided.
3. offset voltage null capability.
4. Common mode & differential voltage range is large.
5. No latch-up.

Instrumentation Amplifier :

Many industrial systems, consumer systems & process control systems require a measurement of the physical quantities like temperature, humidity, weight etc.

→ The measurement of the physical quantities is generally carried out with the help of a device called "Transducer."

→ A transducer is a device which converts one form of energy into another form of energy. Eg: Microphone.

→ But most of the transducer o/p are generally very low level signals. such low level signals are not sufficient to drive the next stage of the op-amp. Hence, before the next stage it is necessary to amplify the level of such signal, rejecting the noise & interference.

→ However, a general amplifier like CE amplifier is not suitable to amplify such signals.

→ For rejection of noise, such amplifiers must have high CMRR. But CE amplifier has low CMRR. So it is not useful. Therefore a special amplifier is used to amplify such signals.

→ A special amplifier which is used for such a low level amplification with high CMRR, high i/p impedence, low o/p impedence, low power consumption is known as instrumentation amplifier. It is also called as Data Amplifier.

→ The requirements of an good instrumentation amplifier is given by :

(a) High i/p impedence

(b) Low o/p impedence

(c) High CMRR

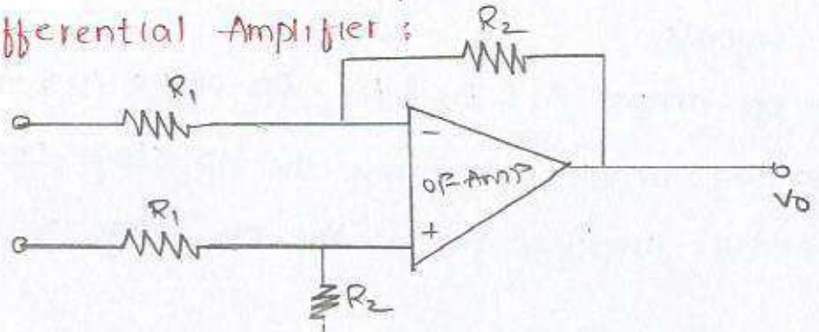
(d) Low power consumption

(e) Easier gain adjustment

(f) High slew rate.

(g) Gain is high (or) finite stable gain.

Differential Amplifier :



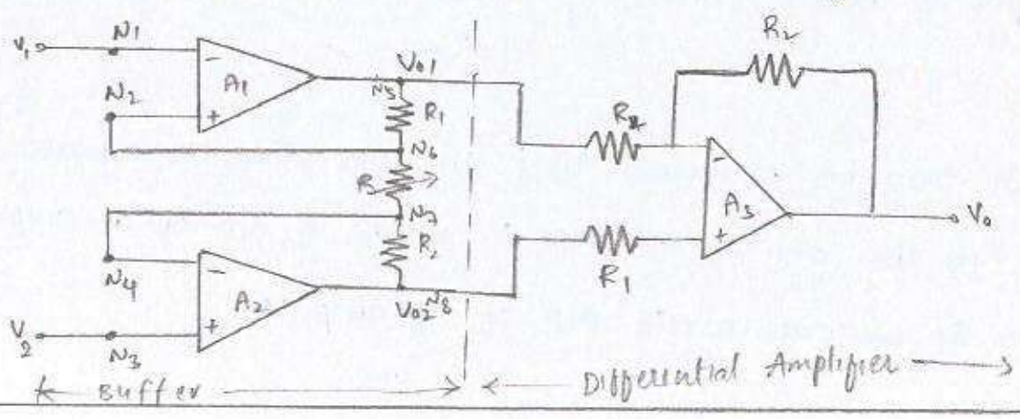
→ The instrumentation amplifier is a type of differential amplifier. Hence differential amplifier is shown in above fig.

From fig.

$$V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

→ The instrumentation amplifier is a type of D.A i.e, the D.A using op-amp can be used as instrumentation amplifier. But the main problem in using it as an instrumentation amplifier is its i/p impedence.

→ The i/p impedence of D.A is low while the I.A needs very high i/p impedence. To get very high i/p impedence, the D.A can be modified by using Buffer (or) voltage follower circuits at the i/p. It is shown in below fig.



→ The gain of the voltage follower circuit is unity. While its i/p impedence is very high. Hence the circuit provides same voltage gain as provided by the op-amp differential amplifier.

→ The above ckt provides high i/p impedence for accurate measurement of signals.

→ It consists of op-amps A_1 & A_2 & A_3. Op-amps A_1 & A_2 are the non-inverting amplifiers forms the i/p stage. Op-amp A_3 is the differential amplifier forms the o/p stage of the amplifier.

→ One variable resistor R, is inserted b/w the o/p's of A_1 & A_2 op-amp's with the help of this resistor gain can be varied.

→ Gain depends on the external resistances & hence can be adjusted accurately.

→ The i/p impedence depends on the i/p impedence of the non-inverting amplifier which is very high.

→ The o/p impedence is the o/p impedence of the op-amp A_3 which is very low.

→ The CMRR of the op-Amp A_3 is very high. Thus the circuit satisfies the all the requirements of a good instrumentation amplifier & hence commonly used in practical applications.

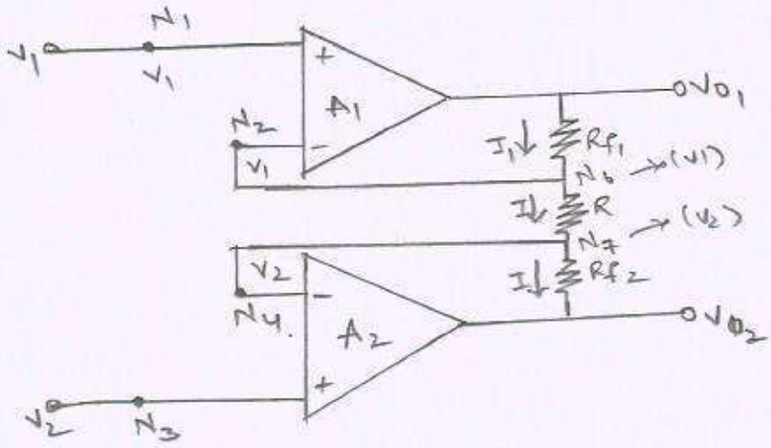
-Analysis :

It may be observed that the o/p stage is a basic D.A. Hence if the o/p of op-amp A_1 is V_{o1} & o/p of op-amp A_2 is V_{o2}. So we can write o/p of op-amp is

$$V_o = \frac{R_2}{R_1}(V_{o_2} - V_{o_1}) \quad \rightarrow (1)$$

→ Let us find out the expression for V_{o_2} & V_{o_1} in terms of $V_1, V_2, R_{f_1}, R_{f_2}, R$.

→ Let us consider the first stage of an I.A shown in fig.



→ The node N_1 voltage of op-amp A_1 is V_1. So that will be appeared at the node N_2 by virtual connection. so the voltage at node N_6 is V_1.

→ The node N_3 voltage of op-amp A_2 is V_2. So that will be appeared at the node N_4 by virtual connection. so the voltage at node N_7 is V_2.

→ The i/p current of op-amp A_1 & A_2 both are zero. Hence current I remains same through R_{f_1}, R, R_{f_2}.

→ Applying ohms law blw the nodes N_5 & N_8, we get

$$I = \frac{V_{o_1} - V_{o_2}}{R_{f_1} + R + R_{f_2}}$$

let, $R_{f_1} = R_{f_2} = R_f$

So $$I = \frac{V_{o_1} - V_{o_2}}{2R_f + R} \quad \rightarrow (2)$$

Now at the nodes N_6 & N_7

$$I = \frac{V_1 - V_2}{R} \longrightarrow (3)$$

Equate eq(2) & eq(3), we get

$$\frac{V_{01} - V_{02}}{2R_f + R} = \frac{V_1 - V_2}{R}$$

multiply '-' on b/s, we get

$$\frac{V_{02} - V_{01}}{2R_f + R} = \frac{V_2 - V_1}{R}$$

$$V_{02} - V_{01} = \frac{V_2 - V_1}{R} (2R_f + R)$$

$$= V_2 - V_1 \left(\frac{2R_f}{R} + \frac{R}{R} \right)$$

$$V_{02} - V_{01} = V_2 - V_1 \left(1 + \frac{2R_f}{R} \right) \longrightarrow (4)$$

Sub. eq(4) in eq(1), we get

$$V_0 = \frac{R_2}{R_1} \left(1 + \frac{2R_f}{R} \right) (V_2 - V_1)$$

This is the overall voltage gain of the I.A. where R is the variable resistor.

∴ The gain is depends on the R.

Applications :

1. Temperature controller
2. Light intensity meter
3. Analog weight scale
4. Measure the pressure, weight & humidity.

AC Amplifier :

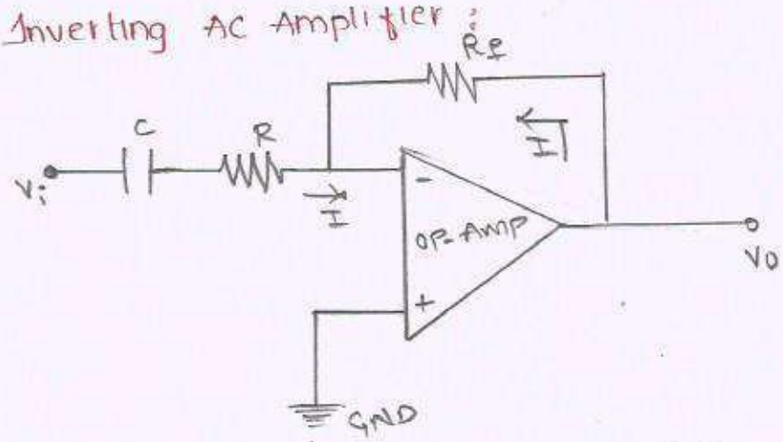
→ The op-amp can amplifies both the types of signals i.e., DC to AC. The op-amp responding to ac signal then it is called as AC amplifier.

→ If the ac i/p signal is super imposed with the dc signal, to restrict the amplification of such dc signals, the coupling capacitors must be used at the i/p of the ac amplifier.

→ There are 2 types of AC amplifiers.

1. Inverting AC amplifier
2. Non-inverting AC amplifier

1. Inverting AC Amplifier :



→ The above circuit shows the inverting ac amplifier because the AC i/p signal is fed to the inverting terminal.

→ The capacitor 'c' blocks the dc components and resistor 'R' sets the lower 3 dB frequency of the amplifier.

→ since node 'a' is at ground potential by the virtual connection. The o/p voltage V_o is given by

$$\boxed{V_o = -I R_f}$$

from fig. $I = \dfrac{V_i}{R + \frac{1}{j\omega c}}$

According to laplace transform

let $j\omega = s$

So, $$I = \frac{V_i}{R + \frac{1}{sC}} \rightarrow (2)$$

Sub. eq(2) in eq(1)

$$V_o = -\left[\frac{V_i}{R + 1/sC}\right] \times R_f \rightarrow (3)$$

W.K.T closed loop gain

$$A_{CL} = \frac{V_o}{V_i} \rightarrow (4)$$

Sub. eq(3) in eq(4)

$$A_{CL} = \frac{-\left(\frac{V_i}{R + 1/sC}\right) R_f}{V_i}$$

$$= -\frac{1}{R + 1/sC} \times R_f$$

$$= -\frac{R_f}{R}\left[\frac{1}{1 + \frac{1}{sCR}}\right]$$

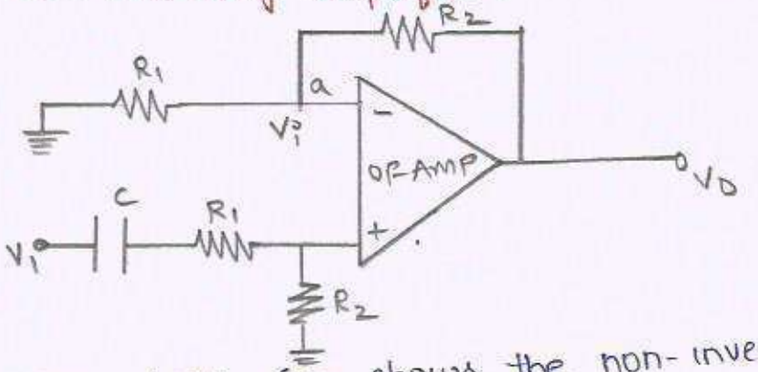
$$= -\frac{R_f}{R}\left[\frac{1}{1/s(s + 1/RC)}\right]$$

$$A_{CL} = -\frac{R_f}{R}\left[\frac{s}{s + 1/RC}\right]$$

The capacitor 'C' is short circuited for mid frequencies so the 2nd term in the above eq" becomes unity.

$$\therefore A_{CL} = -\frac{R_f}{R}$$

2. Non-inverting Amplifier :



The above fig. shows the non-inverting Ac amplifier because the i/p Ac signal is fed to the non-inverting terminal. The o/p voltage Vo is given by.

$$V_o = 1 + \frac{R_2}{R_1}$$

Voltage - Current Convertor :

→ In V-I convertor the o/p load current is proportional to the i/p voltage.

→ According to connection of load there are 2 types

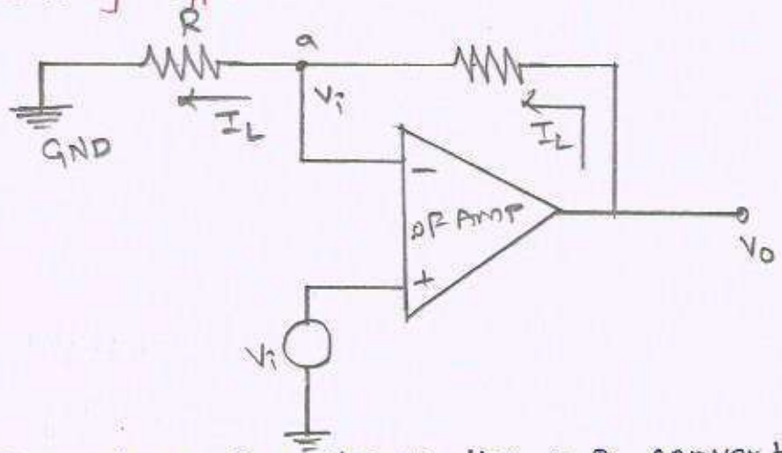
1. Floating type V-I convertor
2. Grounded type V-I convertor

→ In floating type V-I convertor, the load resistor R_L is not connected to the ground.

→ In grounded type V-I convertor, the load resistor R_L is directly connected to the ground.

→ This circuit is also called as voltage controlled current source (VCCS) because here the i/p voltage controls the o/p current (or) o/p current is controlled by the input voltage.

1. Floating Type V-I convertor :



→ The above fig. shows the V-I convertor. Here the load resistor R_L is not connected to the ground.

Since the voltage at node 'a' is $\boxed{V_i = I_L R}$

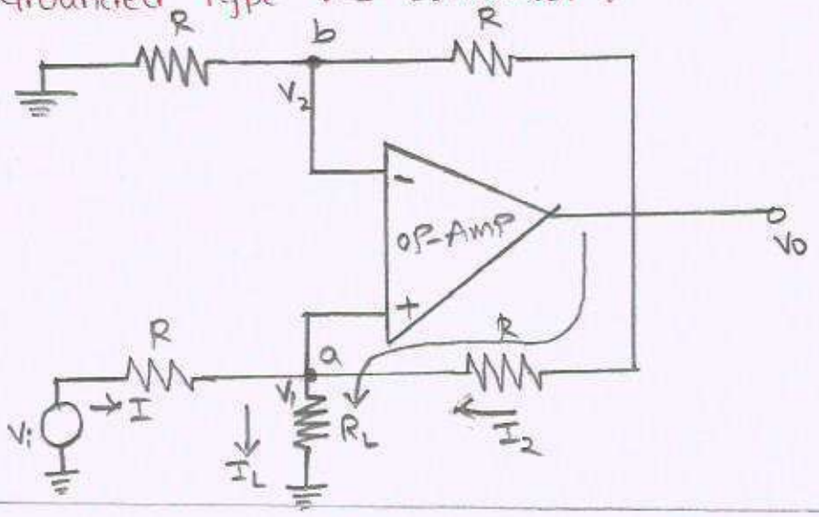
$$\therefore I_L = \frac{V_i}{R}$$

→ Thus the load current is directly proportional to the i/p voltage and it is given by

$$\boxed{I_L \propto V_i}$$

i.e., the i/p voltage Vi is converted into an o/p current I_L. Here we observed that the proportionally constant is generally $1/R$. Therefore this circuit is called Transconductance amplifier.

2. Grounded Type V-I convertor :



→ A V-I convertor with grounded load is shown in above fig.

→ Let V_1 be the voltage at node 'a'. applying KCL at node 'a' we get

$$\boxed{I_1 + I_2 = I_L} \longrightarrow (1)$$

From fig. $I_1 = \dfrac{V_i - V_1}{R_f} \longrightarrow (2)$

$$I_2 = \frac{V_o - V_1}{R} \longrightarrow (3)$$

Sub. eq(2) & eq(3) in eq(1)

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = I_L$$

$$V_i - V_1 + V_o - V_1 = I_L R$$

$$V_i - 2V_1 + V_o = I_L R$$

$$\boxed{V_1 = \frac{V_i + V_o - I_L R}{2}} \longrightarrow (4)$$

W.K.T, $A = \dfrac{V_o}{V_1} = 1 + \dfrac{R_f}{R}$

But here we have $R_f = R$

$$\frac{V_o}{V_1} = 1 + \frac{R}{R}$$

$$= 2$$

$$\boxed{V_o = 2V_1} \longrightarrow (5)$$

Sub. eq(4) in eq(5)

$$V_o = \frac{2(V_i + V_o - I_L R)}{2}$$

$$V_o = V_i + V_o - I_L R$$

$$V_i = I_L R$$

$$\therefore I_L = \frac{V_i}{R}$$

→ From the above expression, we can say that the load current I_L depends on the i/p voltage V_i.

$$\therefore I_L \propto V_i$$

Applications :

1. Low voltage to dc voltage convertor
2. Diode tester
3. Zener Diode tester.

Current - Voltage Convertor :

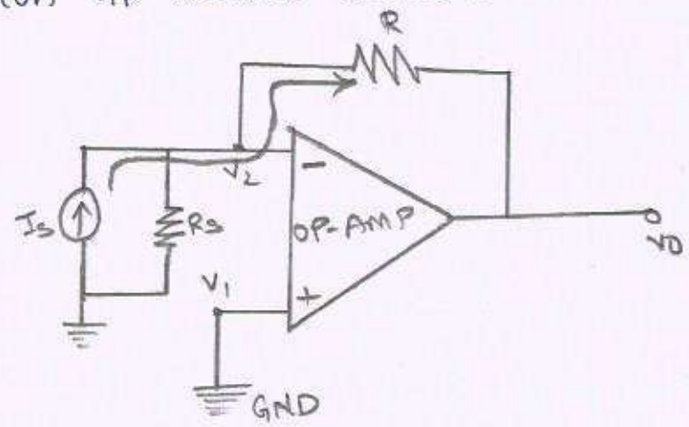
→ In I-V convertor the o/p voltage is directly proportional to the i/p current.

$$V_o \propto I_s$$

where, V_o = o/p voltage

I_s = i/p current

→ This circuit is also called as current controlled voltage source (CCVS) because the o/p voltage controlled by i/p current (or) i/p current controlls the o/p voltage.



→ The above fig. shows the current to voltage convertor because of virtual ground the voltage $V_2 = 0$.

Applying KCL at node 'a'.

$$I_S = \frac{V_2 - V_0}{R}$$

$$V_2 = 0$$

$$I_S = \frac{-V_0}{R}$$

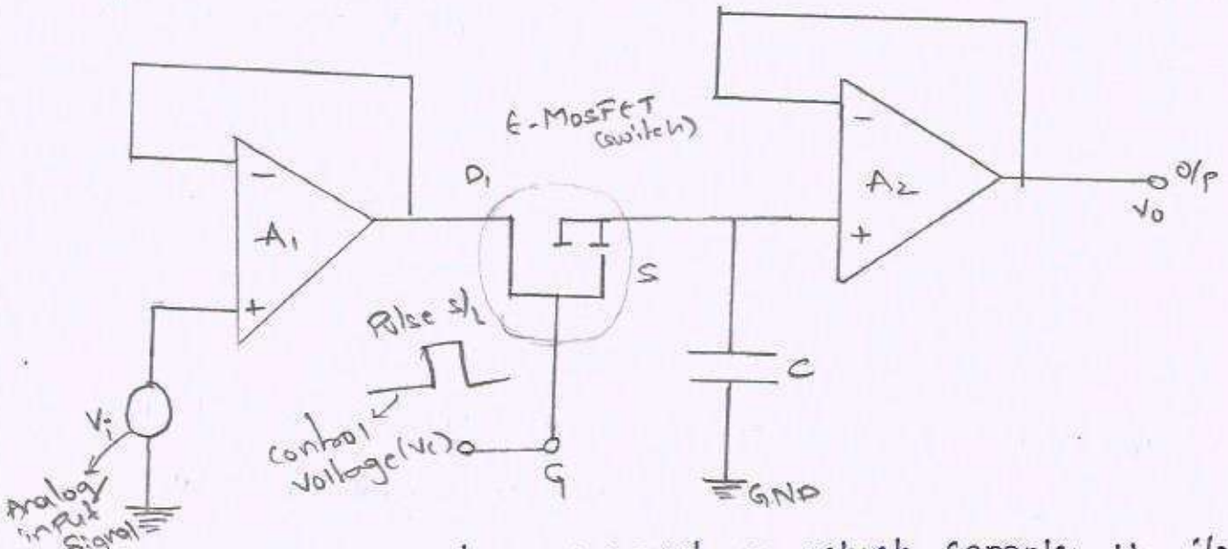
$$\boxed{V_0 = -I_S R}$$

→ Thus the o/p voltage is proportional to the i/p current so the circuit works as current to voltage convertor. It is also called as Trans resistance amplifier.

Applications :

1. Photo diode detectors
2. photo Fet detector.

Sample And Hold Circuits :



→ Sample hold circuit is a circuit in which samples the i/p signal and holds on to its last sampled value untill the o/p is sampled again.

→ This type of circuit is very useful in analog to digital convertors & digital communications etc.

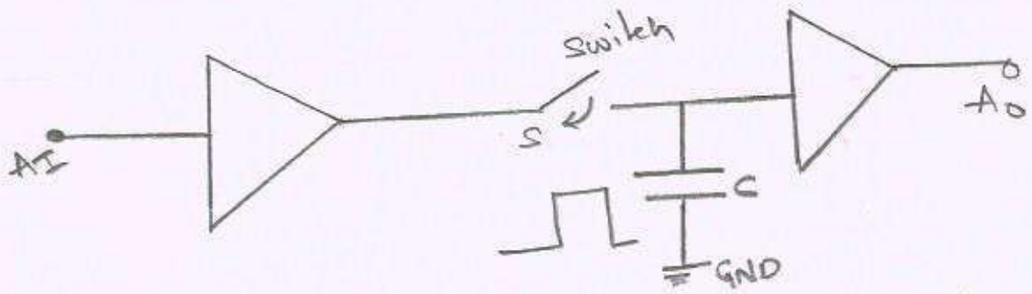
→ The above fig. E-MOSFET acts as switch & is controlled by the control voltage V_c & capacitor 'C' stores the charge.

→ The analog signal V_i to be sampled is applied at the non-inverting terminal of A_1 op-amp & the same vtg appeared at the drain terminal of E-MOSFET. When the control voltage V_c is applied to its gate, the +ve half cycle is going, the MOSFET is ON which acts as a closed switch & the capacitor 'C' charged by the i/p voltage V_i and the same voltage appears at the o/p of the op-amp.

→ when -ve half cycle is going the MOSFET is switched OFF & only discharge path for capacitor C through non-inverting i/p of the op-amp.

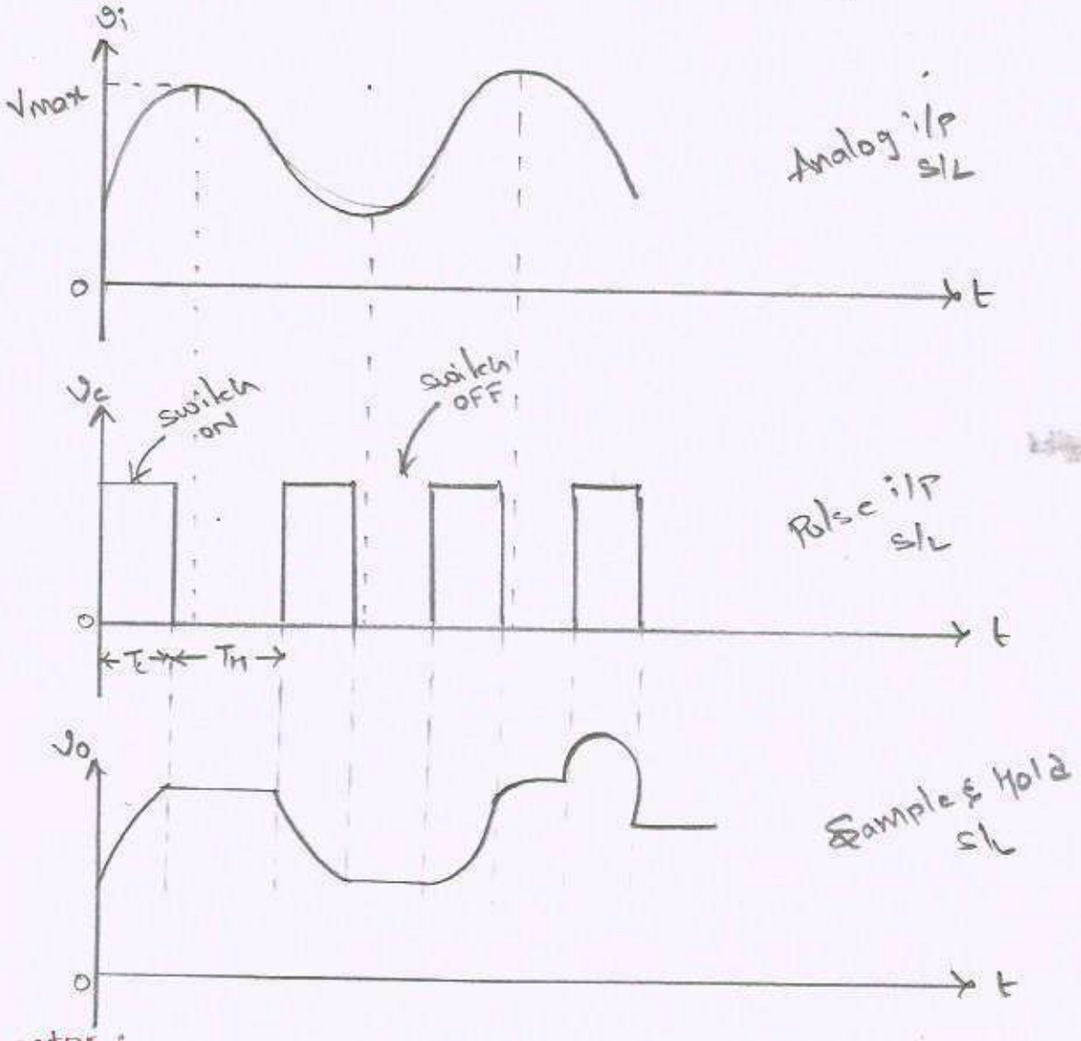
→ Since the i/p impedence of the op-amp is high, the voltage V_i is retained & it is appears at the o/p of the op-amp.

→ The i/p & o/p waveforms of the circuit shown in below fig.



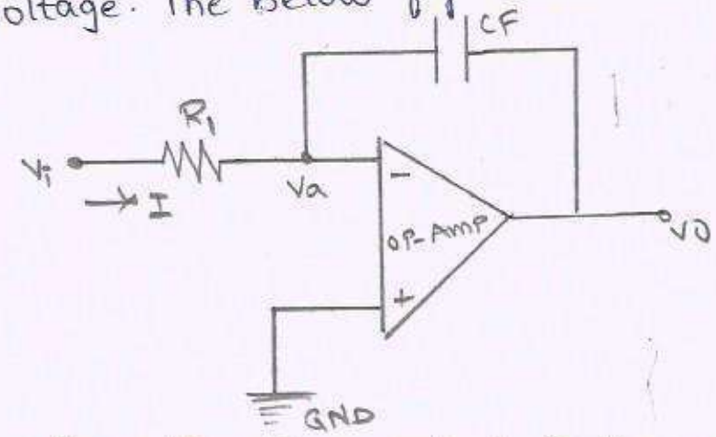
→ The time period of the signal during which the voltage across the capacitor (V_c) is equal to V_i is called sample period (T_s) (or) on time (or) charging time.

→ The time period of the signal during which the voltage across the capacitor V_c is held constant are called Hold period (T_H) (or) OFF time (or) Discharging time.



Integrator :

Integrator is a circuit in which o/p voltage is integral of i/p voltage. The below fig. shows the ideal integrator circuit.



→ The i/p voltage V_i is applied to the inverting i/p terminal through

R_1 resistor.

→ The capacitor current I is given by $I = C_F \frac{dv}{dt}$.

→ Since o/p current of Op-amp is zero, the entire current I flowing through R_1 & C_F.

Applying KCL at node 'a'

For i/p side $I = \frac{V_i - V_a}{R_1}$

where $V_a = 0$ V ; because virtual connection

$$\boxed{I = \frac{V_i}{R_1}} \rightarrow (1)$$

At o/p side ; $I = C_F \frac{d(V_a - V_o)}{dt}$

$$\boxed{I = -C_F \frac{dV_o}{dt}} \rightarrow (2)$$

equating eq(1) & eq(2)

$$\frac{V_i}{R_1} = -C_F \frac{dV_o}{dt}$$

$$dV_o = -\frac{V_i dt}{R_1 C_F}$$

integrating on b.s, we get

$$\int_0^t dV_o = -\frac{1}{R_1 C_F} \int_0^t V_i \, dt$$

$$V_o(t) - V_o(0) = \frac{-1}{R_1 C_F} \int_0^t V_i(t) \, dt$$

$$V_o(t) = \frac{-1}{R_1 C_F} \int_0^t V_i(t) \, dt + V_o(0)$$

where, $R_1 C_F = \tau$ = Time constant of integrator

$V_o(0)$ is the initial o/p voltage

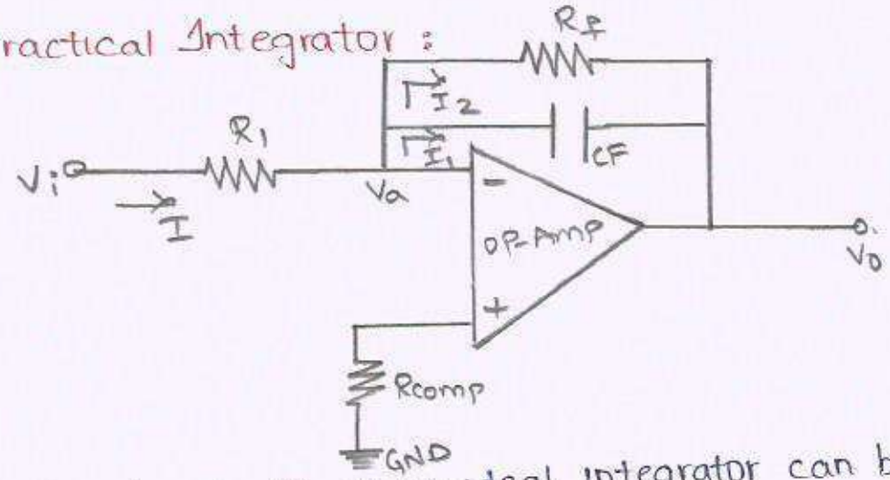
→ The above eqn shows that the o/p is $\frac{-1}{R_1 C_F}$ times the integral of i/p.

Drawbacks :

1. Without giving any i/p, we get some voltage at the o/p so we can treat that as error signal.
2. Capacitor gets charging & discharging due to bias currents & add its effects on o/p error voltage. After some time o/p of op-amp may achieve its saturation level.
3. Band width is very small for ideal integrator. Hence ideal integrator can be used for very small frequency range of i/p's only.

→ Because of all the above drawbacks the ideal integrator is not used in practically. Some additional components are used along with basic integrator circuit to reduce the effect of an error voltage in practically such an integrator is called as practical integrator circuit.

Practical Integrator :



→ The drawbacks of an ideal integrator can be minimised in the practical integrator circuit, which consists of resistance R_F in parallel with the capacitance C_F.

→ The practical integrator circuit shown in above fig.

→ The resistance Rcomp is used to over come the errors due to the bias currents.

→ The resistance R_f reduces the low frequency gain of the Op-amp.

→ The parallel combination of R_f & C_f behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason this circuit is also called as "Lossy integrator."

→ Since i/p current of op-amp is zero, from the concept of virtual ground $V_a = 0$.

Applying KCL at node 'a',

$$I = I_1 + I_2 \quad \rightarrow (1)$$

But $$I = \frac{V_i - V_a}{R_1}$$

$$I = \frac{V_i}{R_1} \quad \rightarrow (2)$$

$$I_1 = -C_F \frac{dV_o}{dt} \quad \rightarrow (3)$$

$$I_2 = \frac{-V_o}{R_f} \quad \rightarrow (4)$$

Sub. eq(2), (3) & (4) in eq(1)

$$\frac{V_i}{R_1} = -C_F \frac{dV_o}{dt} - \frac{V_o}{R_f}$$

Apply L.T on b.s, we get

$$\frac{V_i(s)}{R_1} = -sC_F V_o(s) - \frac{V_o(s)}{R_f}$$

$$\frac{V_i(s)}{R_1} = -V_o(s)\left[sC_F + \frac{1}{R_f}\right]$$

$$V_o(s) = \frac{-V_i(s)}{R_1\left[sC_F + 1/R_f\right]}$$

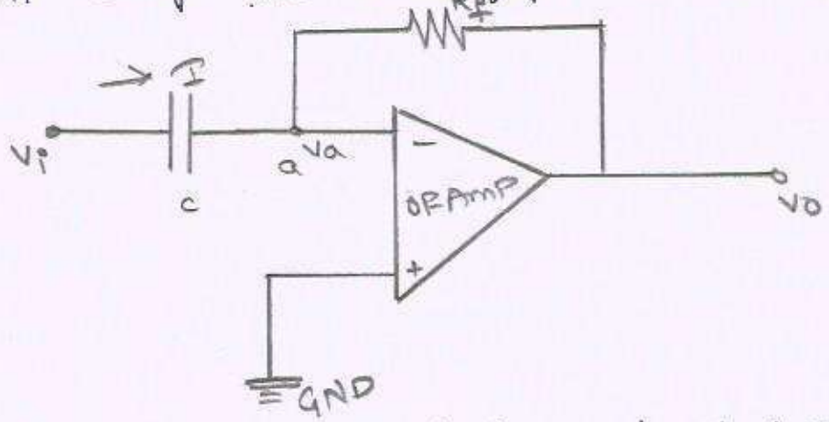
$$V_o(s) = \frac{-V_i(s)}{sCR_1 + R_1/R_f}$$

Applications :-

1. It is used in Analog computers
2. It is used in analog to digital convertors
3. It is used in solving differential equations
4. It is used in wave shapping circuits.

Differentiator :-

Differentiator is a circuit in which o/p voltage is differentiate of i/p voltage. The below fig. shows the ideal differentiator.



The node 'a' is at virtual ground potential i.e., $V_a = 0$.

→ The current I flowing through the capacitor is

$$I = C \frac{dv}{dt}$$

→ Apply KCL at node 'a'

$$I = C \frac{d(V_i - V_a)}{dt}$$

Due to virtual connection $V_a = 0$

$$I = C \frac{dV_i}{dt} \quad \rightarrow (1)$$

Similarly at the o/p side

$$I = \frac{V_a - V_o}{R_f}$$

$$I = \frac{-V_o}{R_f} \rightarrow (2)$$

Equating above 2 eqns

$$C \frac{dV_i}{dt} = \frac{-V_o}{R_f}$$

$$\boxed{V_o = -R_f C \frac{dV_i}{dt}}$$

where, $R_f \cdot C$ = Time constant.

→ Thus the o/p voltage V_o is constant ($-R_f \cdot C$) times the derivative of the i/p voltage.

Drawbacks :

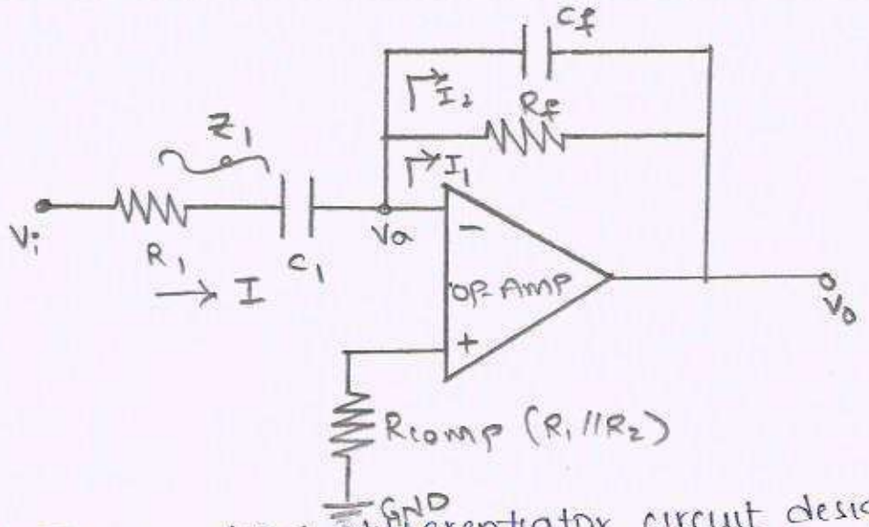
1. The gain of the differentiator increases at frequency increases. Thus at some high frequency the differentiator may become unstable & break into the oscillations.
2. The i/p impedence $X_{C_1} = \frac{1}{2\pi f C}$, if frequency increases impedence decreases. This makes the circuit very much sensitive to the noise.
3. This noise may completely overwrite the o/p of the differentiator.

Hence the differentiator circuit ~~satisfies~~ suffers from the stability & noise problem at high frequencies.

→ These problems can be overcome by adding additional components.

Practical Differentiator :

→ The differentiator circuit suffers from the stability & noise problems at high frequencies. These problems can be eliminated by practical differentiator.



→ The practical differentiator circuit designed by using resistance R_1 is in series with C_1 & capacitor C_f is in parallel with resistance R_f.

→ The resistance Rcomp is used for bias compensations.

Analysis :

→ The current I flowing through the R_1 & C_1 components. But the series combination of R_1 & C_1 is denoted by impedence Z_1.

$$\text{So, } I = \frac{V_i}{Z_1}$$

According to L.T

$$I = \frac{V_i(s)}{Z_1} \longrightarrow (1)$$

$$\text{W.K.T, } Z_1 = R_1 + \frac{1}{j\omega C_1}$$

$$= R_1 + \frac{1}{sC_1}$$

$$\boxed{Z_1 = \frac{R_1 sC_1 + 1}{sC_1}}$$

Sub. Z_1 in eq(1)

$$I = \frac{V_i(s)\, sC_1}{1 + R_1 sC_1}$$

Similarly $I_1 = \frac{-V_o}{R_f}$

$$I_1 = \frac{-V_o(s)}{R_f}$$

$$I_2 = -C_F \frac{dV_o}{dt}$$

$$I_2 = -sC_F V_o(s)$$

Apply KCL at node 'a'

$$I = I_1 + I_2$$

$$\frac{V_i(s)\, sC_1}{1 + R_1 sC_1} = \frac{-V_o(s)}{R_f} - sC_f V_o(s)$$

$$= \frac{-V_o(s)}{R_f} \cdot -V_o(s)\left[\frac{1}{R_f} + sC_f\right]$$

$$= -V_o(s)\left[\frac{1 + sC_f R_f}{R_f}\right]$$

$$V_o(s) = -\frac{V_i(s) sC_1 R_f}{(1 + sC_1 R_1)(1 + sC_f R_f)}$$

Let us assume $R_f C_f = R_1 C_1$

$$V_o(s) = -\frac{V_i(s)\, sC_1 R_f}{(1 + sC_f R_f)^2}$$

If $R_f C_1 > C_f R_f$, then the denominator can be neglected

$$\therefore V_o(s) = -V_i(s)\, sC_1 R_f$$

By applying inverse L.T to the above eqn, we get

$$\therefore V_o(t) = -R_f C_1 \frac{dV_i(t)}{dt}$$

Applications :

1. It is used in wave shaping circuits
2. It is used in convertors i.e., analog to digital.

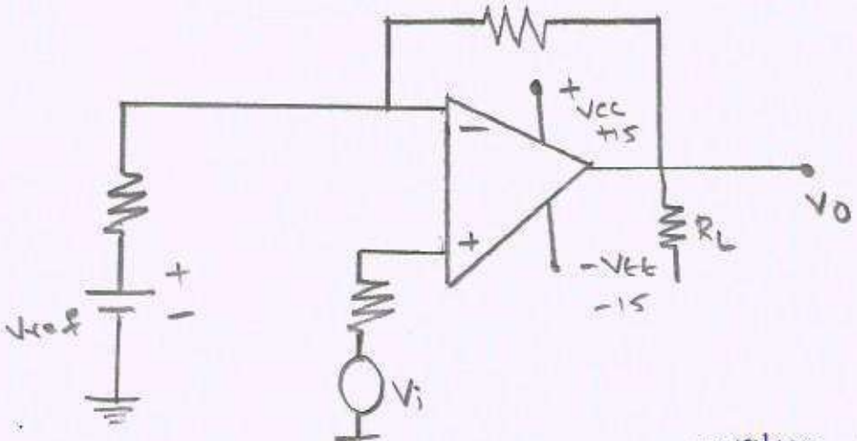
Comparator :

→ Comparator is a circuit in which compares the signal voltage at one i/p terminal of an op-amp with a known reference voltage at another i/p terminal of an op-amp.

→ Basically comparators are of 2 types.

1. Non-Inverting Comparator
2. Inverting Comparator.

1. Non-Inverting Comparator :



→ The above fig. shows the non-inverting comparator.

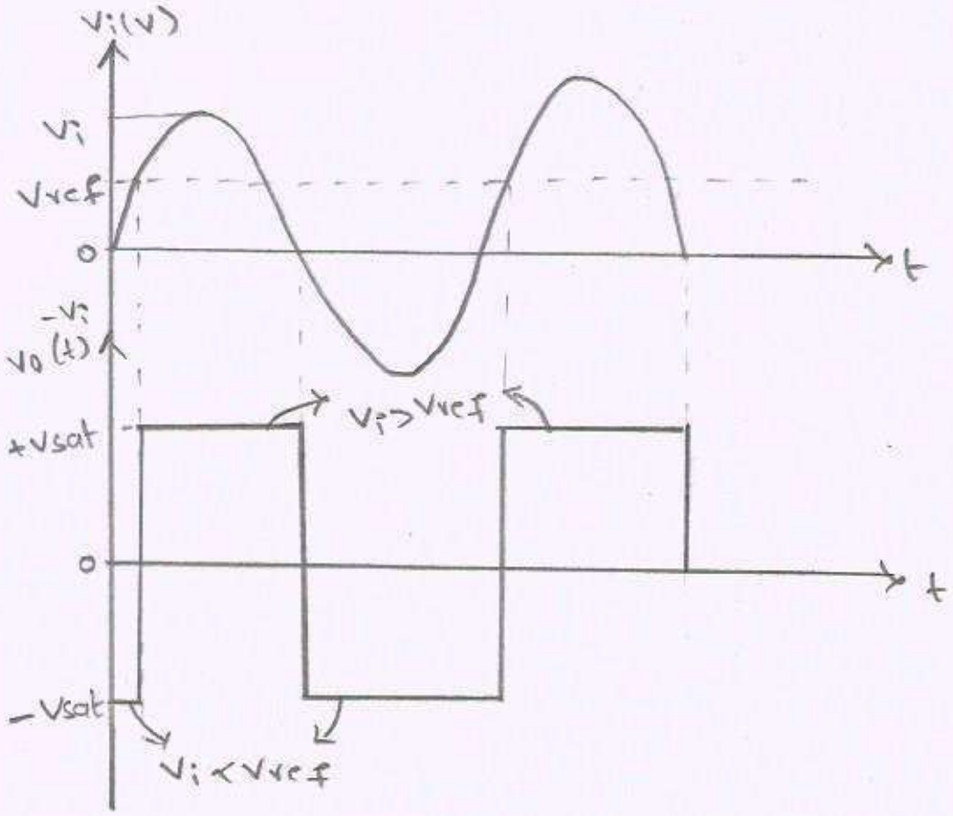
→ A fixed reference voltage V_{ref} is applied to the inverting i/p terminal & signal voltage V_i is applied to the non-inverting i/p terminal.

→ Because of this arrangement the circuit is called non-inverting comparator.

→ When $V_i < V_{ref}$, the o/p voltage V_o is at $-V_{sat}$ ($\cong -V_{EE}$) because the voltage at the inverting i/p terminal (-ve i/p terminal) is higher than that of non-inverting i/p terminal (+ve i/p terminal).

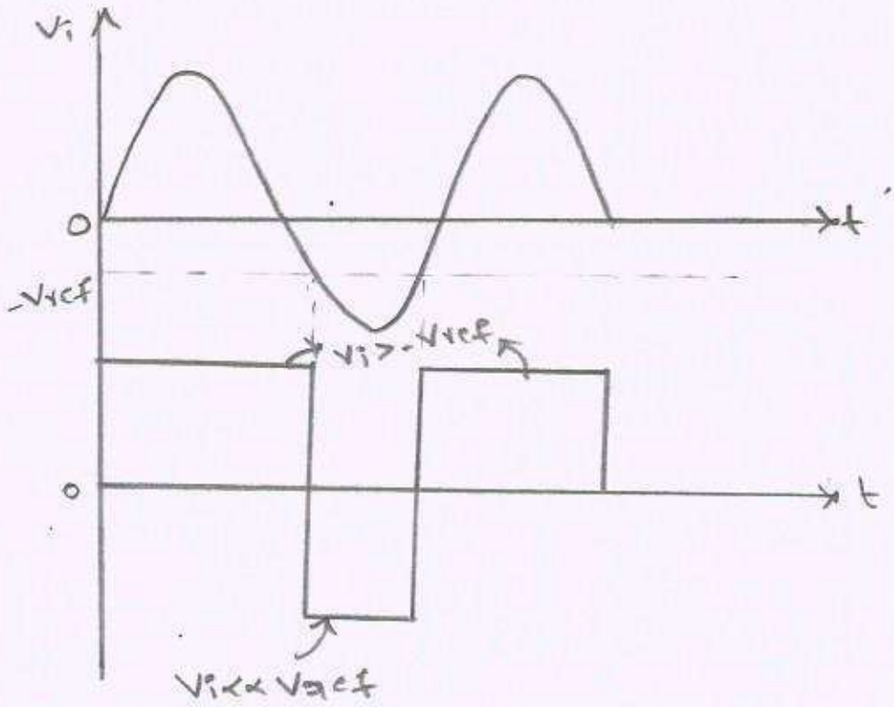
→ Similarly when $V_i > V_{ref}$, the +ve i/p voltage is greater than the -ve i/p voltage. so o/p voltage V_o goes to $+V_{sat}$ ($\cong +V_{cc}$).

→ Thus o/p voltage V_o changes from one saturation level to another saturation level whenever $V_i = V_{ref}$, the corresponding i/p & o/p waveforms for +ve reference vtg is shown in fig.

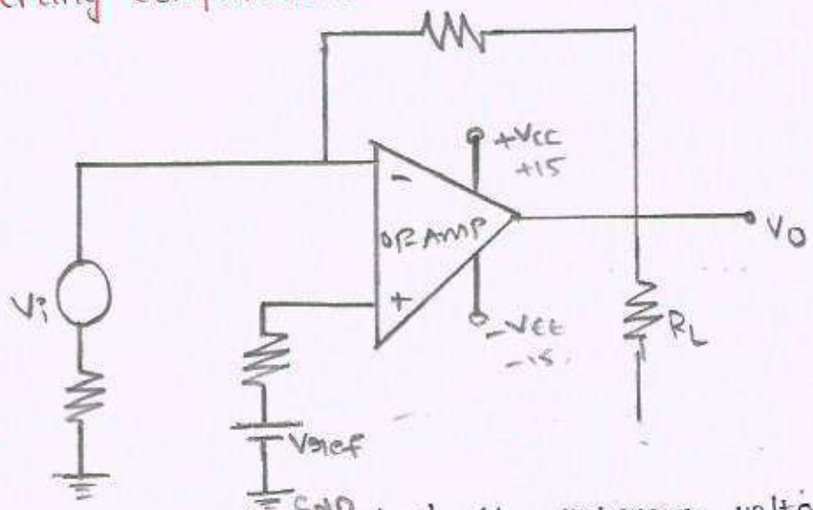


→ If the reference voltage V_{ref} is -ve with respect ground with the signal applied to the +ve terminal.

→ The corresponding waveforms are shown below.



Inverting Comparator :

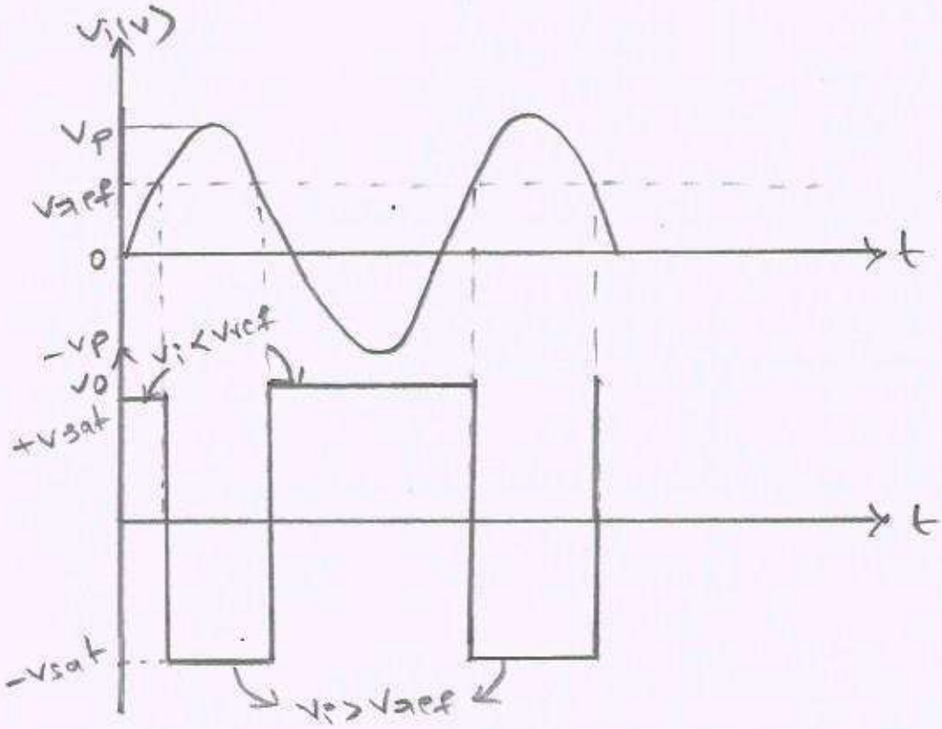


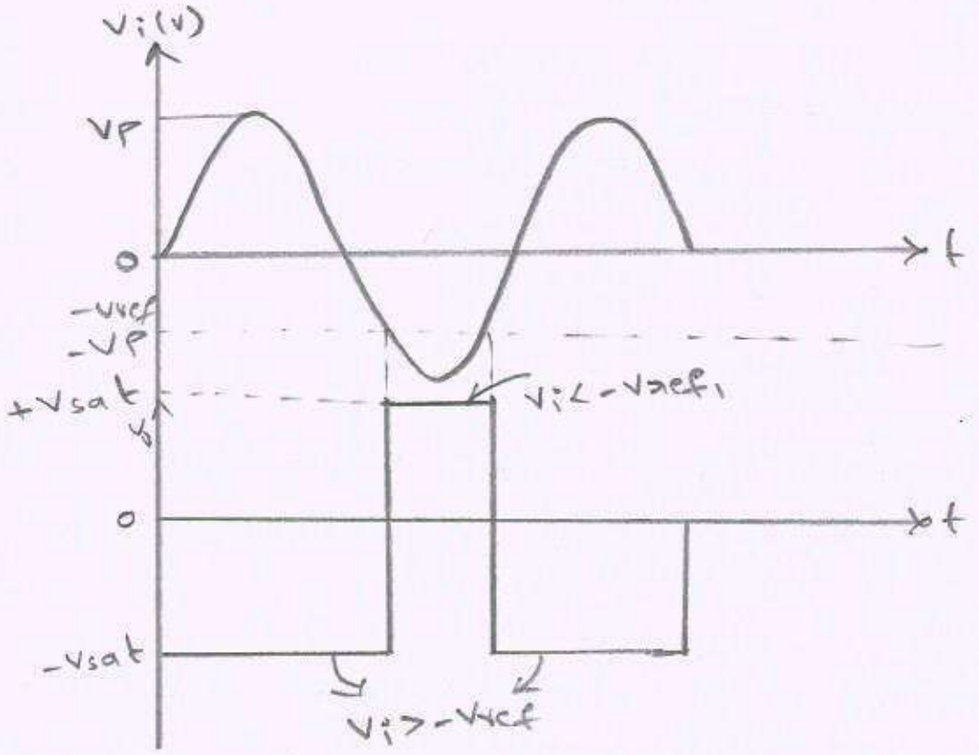
→ It is a circuit in which the reference voltage V_{ref} is applied to non-inverting terminal & signal voltage is applied to the inverting terminal.

→ When $V_i < V_{ref}$, the o/p voltage V_o is at $+V_{sat}$ $(+V_{CC})$, because the voltage at the inverting input is less than that the non-inverting i/p voltage.

→ Similarly when $V_i > V_{ref}$, the non-inverting i/p is less than the inverting i/p then V_o goes to $-V_{sat}$ $(-V_{EE})$.

→ The corresponding waveforms is shown in below fig.





Applications :

1. zero crossing detector
2. Schmitt trigger (regenerative comparator)

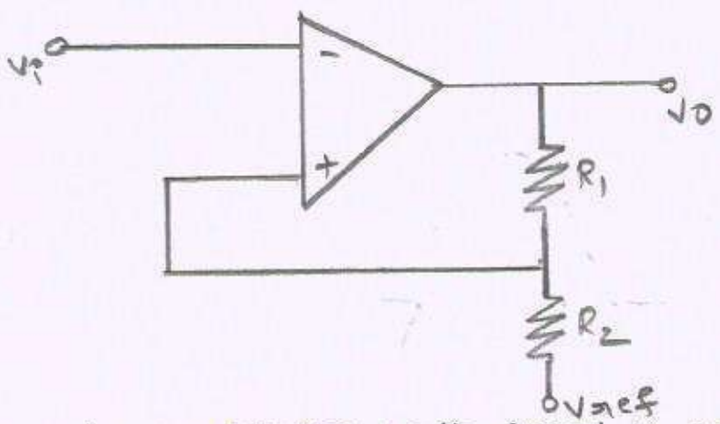
Schmitt Trigger :

→ In basic comparator circuit flb is not used & op-amp is used in open loop mode.

→ In open loop op-amp gain is large. At any cost where small noise voltages can cause triggering of the comparator. such unwanted noise cause the olp to jump blw high & low state.

→ The comparator circuit used to avoid such unwanted triggering (change) is called regenerative comparator (or) schmitt trigger which basically uses +ve flb.

→ A comparator circuit with +ve flb is known as schmitt trigger (or) regenerative comparator.



→ A +ve flb comparator with signal is applied at -ve ilp is shown in above fig.

→ The i/p voltage Vi triggers the olp voltage Vo every-time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) & lower threshold voltage (V_{LT})

→ The difference blw these voltages are called hysterisis voltage (V_H)

$$\therefore V_H = V_{UT} - V_{LT}$$

→ The threshold voltages are calculated as follows.

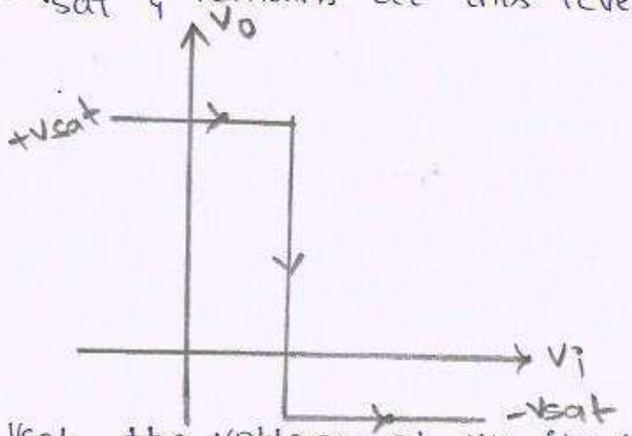
(a) Suppose o/p voltage $V_o = +V_{sat}$, the voltage at +ve i/p terminal can be obtained by using super position theorem.

$$V_{UT} = \frac{V_{ref} \cdot R_1}{R_1 + R_2} + \frac{V_{sat} R_2}{R_1 + R_2}$$

These voltage is called upper threshold voltage (V_{UT}).

(b) if $V_i < V_{UT}$, the o/p V_o remains constant at $+V_{sat}$.

(c) When V_i is just greater than V_{UT}, the o/p regeneratively switches to $-V_{sat}$ & remains at this level untill $V_i > V_{UT}$.



(d) For $V_o = -V_{sat}$, the voltage at +ve i/p terminal is

$$V_{LT} = \frac{V_{ref} \cdot R_1}{R_1 + R_2} - \frac{V_{sat} R_2}{R_1 + R_2}$$

This voltage is called lower threshold voltage.

(e) The i/p voltage is V_i must become lesser than V_{LT} in order to cause V_o to switch from $-V_{sat}$ to $+V_{sat}$.

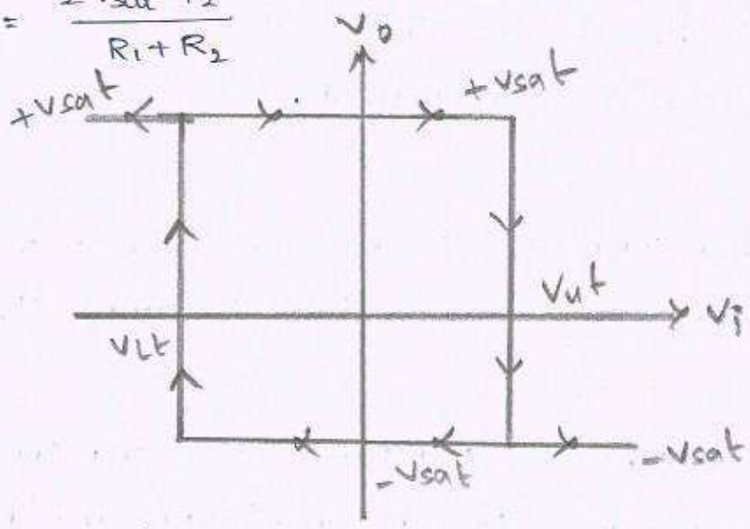
(f) A regenerative transistion takes place & o/p V_o returns from $-V_{sat}$ to $+V_{sat}$, shown in below fig.

(g) The difference b/w 2 threshold voltage called as hysteresis voltage V_H

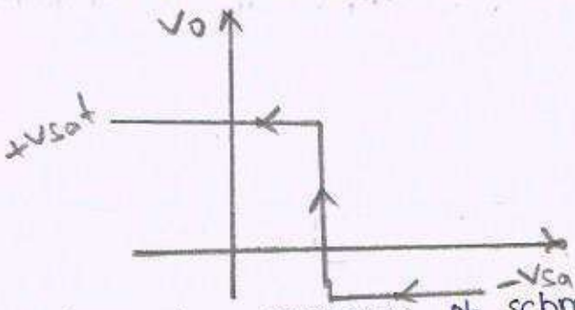
$$V_H = V_{UT} - V_{LT}.$$

$$= \frac{V_{ref} \cdot R_1}{R_1+R_2} + \frac{V_{sat} \cdot R_2}{R_1+R_2} - \frac{V_{ref} \cdot R_1}{R_1+R_2} + \frac{V_{sat} \cdot R_2}{R_1+R_2}$$

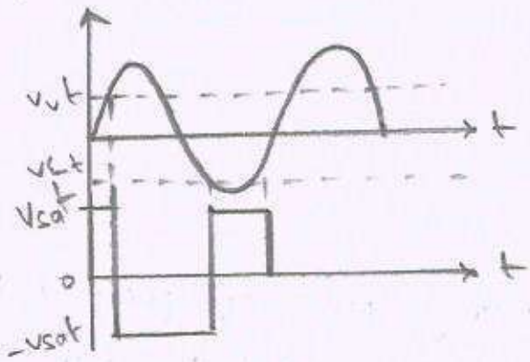
$$V_H = \frac{2\,V_{sat} \cdot R_2}{R_1+R_2}$$

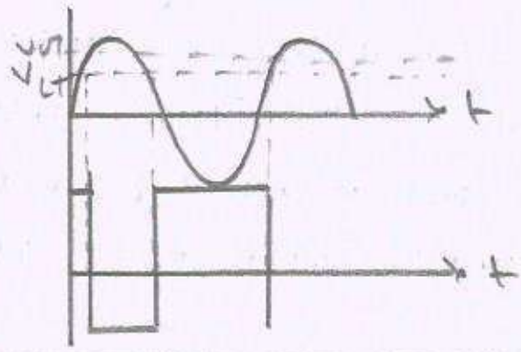


(b) The hysterisis curve is shown in below fig.



→ Corresponding i/p & o/p waveform, of schmitt trigger shown in fig.





Waveform Generators

A **waveform generator** is an electronic circuit, which generates a standard wave. There are two types of op-amp based waveform generators –

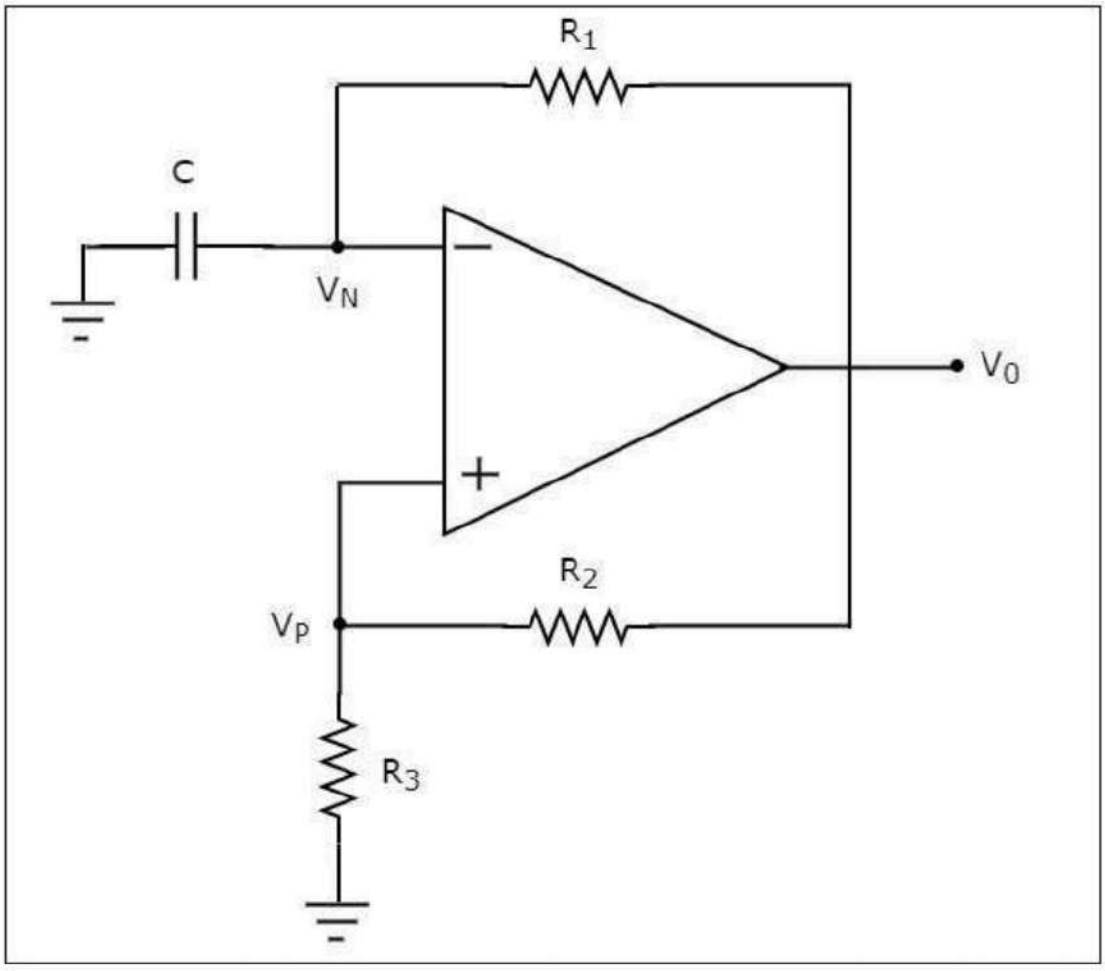
- Square wave generator
- Triangular wave generator

This chapter discusses each of these op-amp based waveform generators in detail.

Square Wave Generator

A **square wave generator** is an electronic circuit which generates square wave. This section discusses about op-amp based square wave generators.

The **circuit diagram** of a op-amp based square wave generator is shown in the following figure



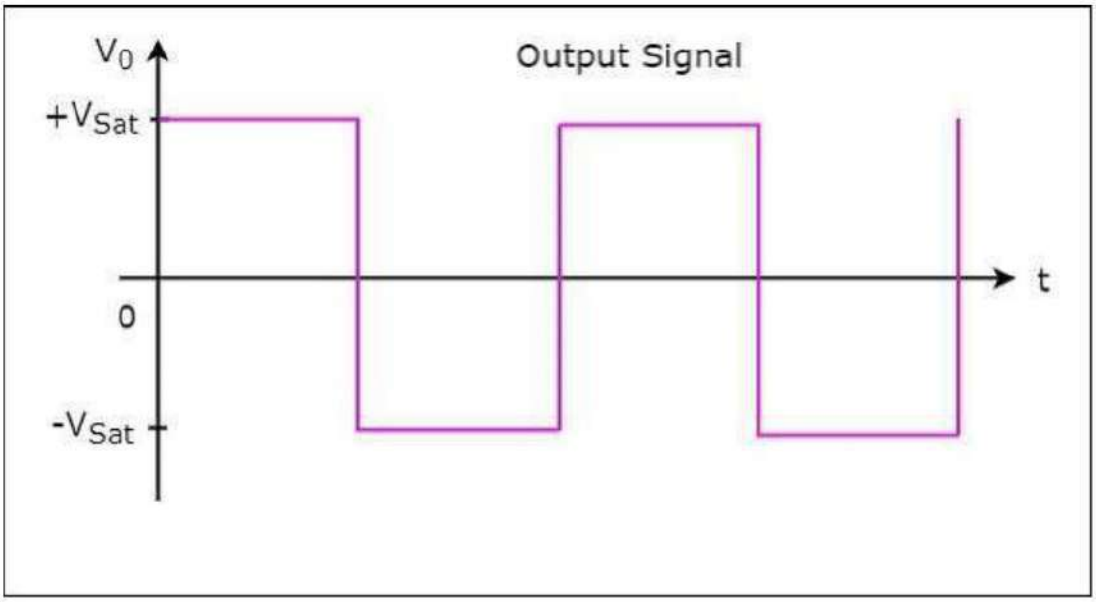
Observe that in the circuit diagram shown above, the resistor R_1 is connected between the inverting input terminal of the op-amp and its output of op-amp. So, the resistor R_1 is used in the **negative feedback**. Similarly, the resistor R_2 is connected between the noninverting input terminal of the op-amp and its output. So, the resistor R_2 is used in the **positive feedback** path.

A capacitor C is connected between the inverting input terminal of the op-amp and ground. So, the **voltage across capacitor C** will be the input voltage at this inverting terminal of op-amp. Similarly, a resistor R_3 is connected between the non-inverting input terminal of the op-amp and ground. So, the **voltage across resistor** R_3 will be the input voltage at this non-inverting terminal of the op-amp.

The **operation** of a square wave generator is explained below –

- Assume, there is **no charge** stored in the capacitor initially. Then, the voltage present at the inverting terminal of the op-amp is zero volts. But, there is some offset voltage at non-inverting terminal of op-amp. Due to this, the value present at the output of above circuit will be $+V_{sat}$.
- Now, the capacitor C starts **charging** through a resistor R_1. The value present at the output of the above circuit will change to $-V_{sat}$, when the voltage across the capacitor C reaches just greater than the voltage (positive value) across resistor R_3.
- The capacitor C starts **discharging** through a resistor R_1, when the output of above circuit is $-V_{sat}$. The value present at the output of above circuit will change to $+V_{sat}$,when the voltage across capacitor C reaches just less than (more negative) the voltage (negative value) across resistor R_3.

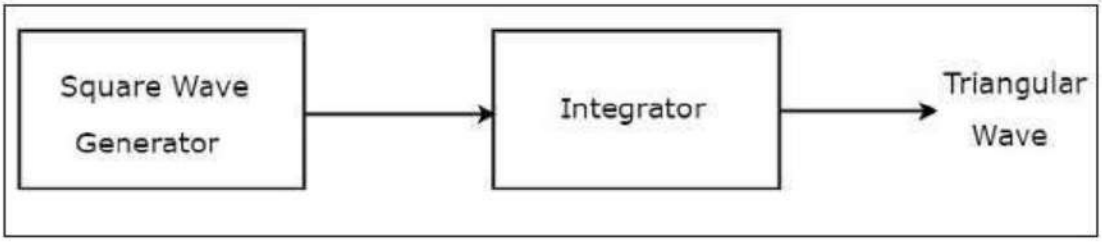
Thus, the circuit shown in the above diagram will produce a **square wave** at the output as shown in the following figure –



From the above figure we can observe that the output of square wave generator will have one of the two values: $+V_{sat}$ and $-V_{sat}$. So, the output remains at one value for some duration and then transitions to another value and remains there for some duration. In this way, it continues.

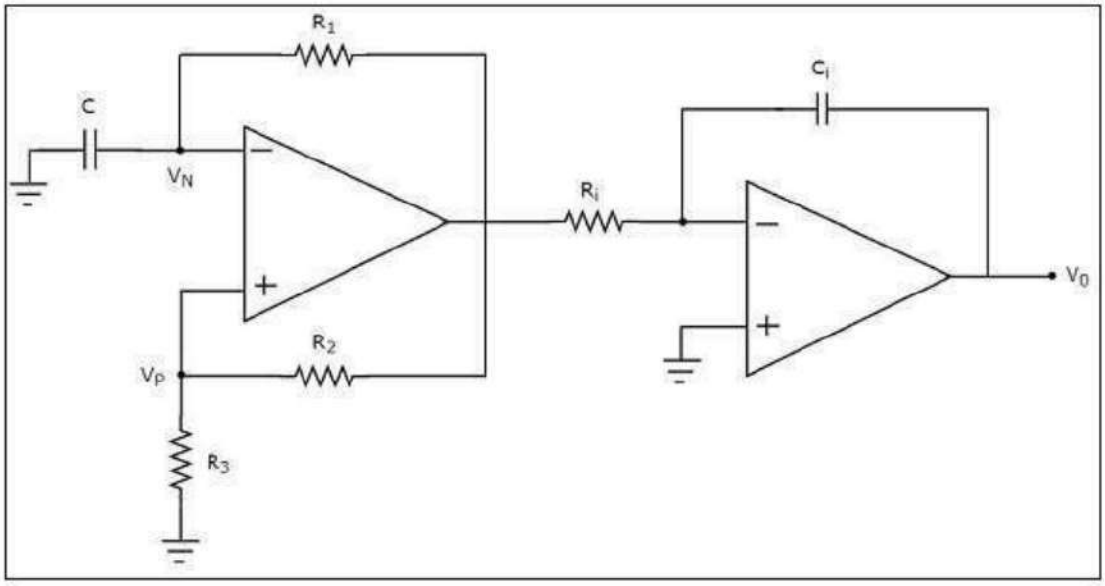
Triangular Wave Generator

A triangular wave generator is an electronic circuit, which generates a triangular wave. The **block diagram** of a triangular wave generator is shown in the following figure –



The block diagram of a triangular wave generator contains mainly two blocks: a square wave generator and an integrator. These two blocks are **cascaded**. That means, the output of square wave generator is applied as an input of integrator. Note that the integration of a square wave is nothing but a triangular wave.

The **circuit diagram** of an op-amp based triangular wave generator is shown in the following figure –



We have already seen the circuit diagrams of a square wave generator and an integrator. Observe that we got the above **circuit diagram** of an op-amp based triangular wave generator by replacing the blocks with the respective circuit diagrams in the block diagram of a triangular wave generator.

UNIT-V

TIMERS, PHASE LOCKED LOOP & D-A & A-D CONVERTORS

Introduction:

555 Timer:

→ 555 timer is a timing circuit that can produce accurate & high stable time delays (or) oscillations.

→ 555 timer is available in 8 pin DIP & 14 pin DIP packages.

→ It can be used with supply voltages range in b/w +5V to +18V.

→ The below fig. shows the pin diagram of 8 pin DIP package.

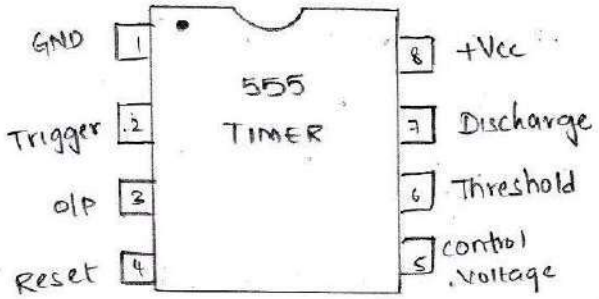


fig: 555 Timer

Features:

1. It can be used with supply voltages over a range in b/w +5V to +18V.
2. It is easy to use.
3. It can drive the load upto 200 mA.
4. It is compatable with TTL (Transistor transistor logic) & CMOS (complimentary metal oxide semiconductor).
5. It is used in various applications such as square wave generator, ramp & pulse wave generator, astable & monostable multivibrators.

Functional Diagram:

→ It consists of 2 comparators namely upper comparator & lower comparator that can drive set (S) & reset (R) terminals of a flip flop.

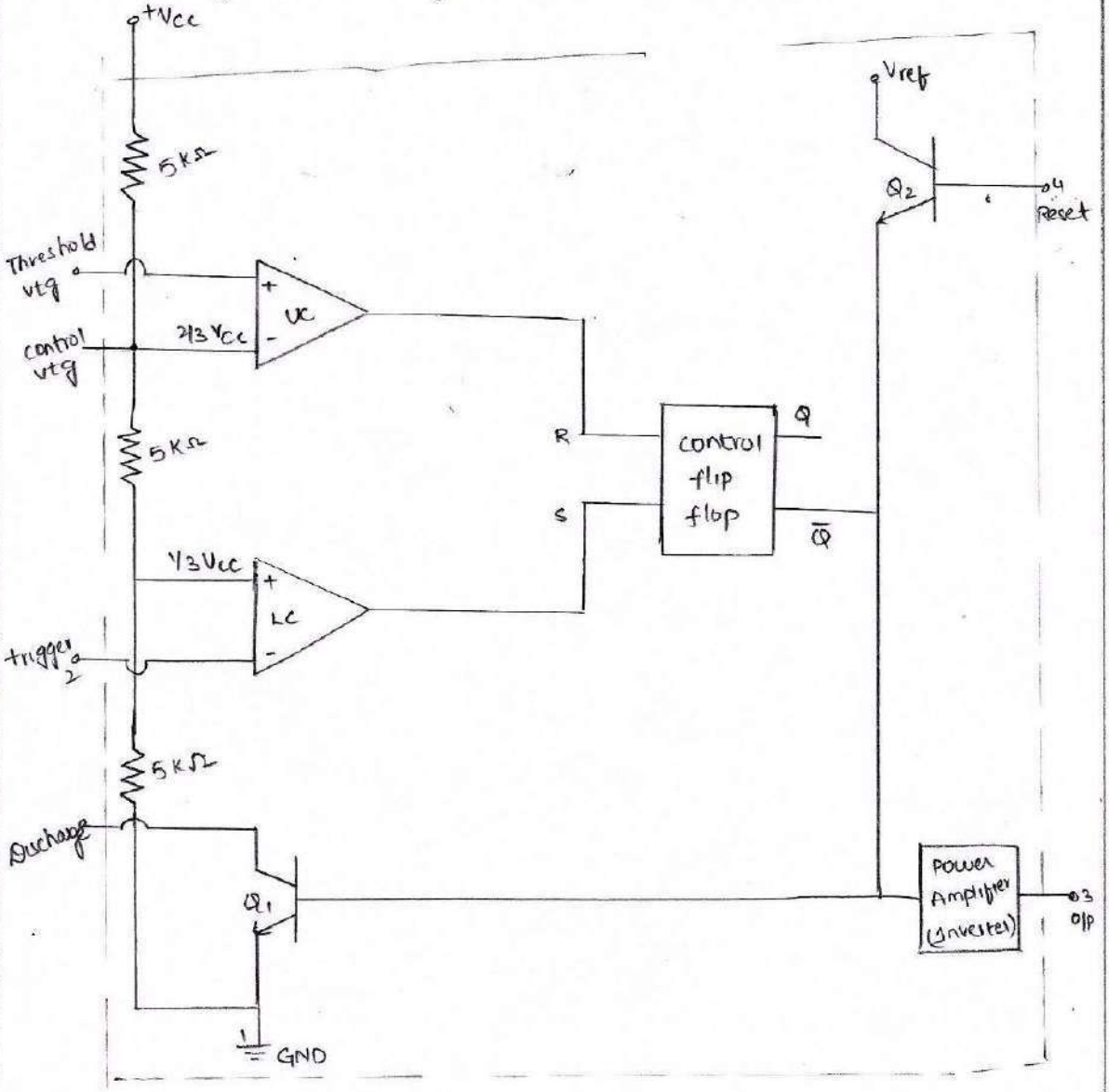
→ These flipflops can control the ON & OFF cycles of the discharge transistor Q_1.
→ It has 3, 5KΩ resistors which acts as potential divider, providing biasing voltages of 2/3 V_{cc} to the upper comparator & 1/3 V_{cc} to the lower comparator where V_{cc} = supply voltage.
→ These voltages are called as reference voltages. These are required to control the timing.
→ The timing can be controlled by externally applying voltage to the control voltage terminal.
→ If no such control voltage is required then the control voltage terminal can be bypassed by a capacitor to ground.
→ Typically the capacitor value is choosen of about 0.1μF.

Operation:

→ In the stand by state (stable state), the o/p $\bar{Q}$ of the control flipflop is high ($\bar{Q}=1$; $Q=0$). This makes o/p low because of power amplifier can be acts as a inverter.
→ A -ve triggering pulse passes through $\frac{V_{cc}}{3}$, the o/p of the lower comparator goes high & sets the flipflop ($Q=1$; $\bar{Q}=0$)
→ When the threshold voltage at pin 6 passes through 2/3 V_{cc} the o/p of upper comparator goes high & resets the flipflop ($Q=0$; $\bar{Q}=1$)
→ A separate reset terminal is produced to reset the flipflop externally.
→ Normally the reset terminal is not used, if we need it should be connected to +ve supply voltage V_{cc}.
→ The transistor Q_2 acts as buffer to isolate the reset i/p from the flipflop & the transistor Q_1.

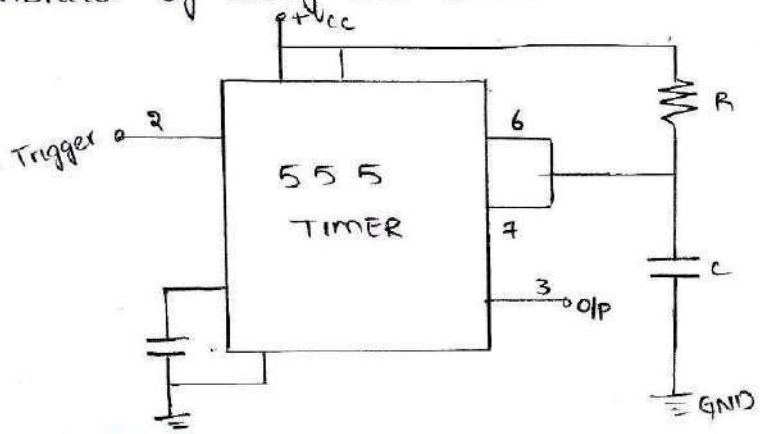
→ The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{cc}.

→ 1] $\bar{Q}$ is high, the transistor Q_1 is ON due to this it become s/c in b/w discharge pin to ground. Similarly $\bar{Q}$ is low, the transistor Q_1 is OFF & it becomes open circuit in b/w discharge pin to ground.

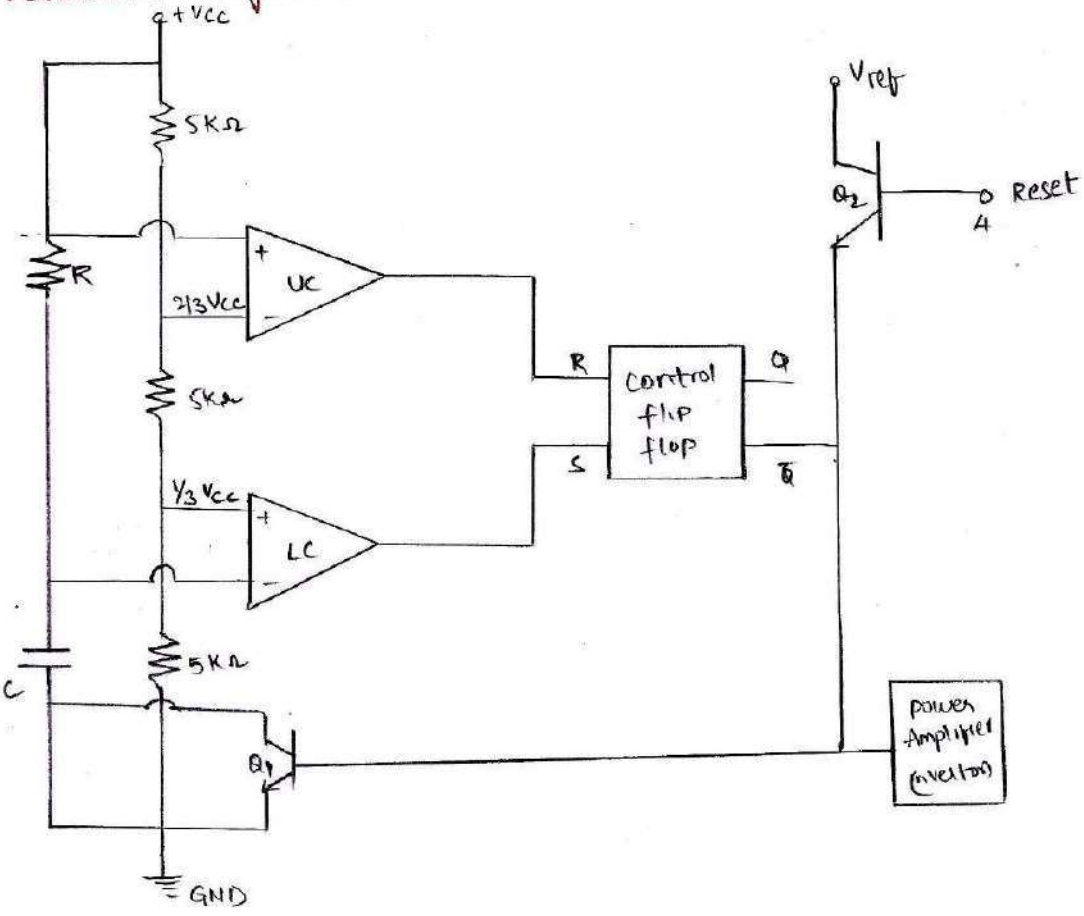


Monostable Multivibrator :-

Monostable multivibrator is a circuit which generates the non-sinusoidal signals. It has one stable state and one quasi stable state. The below fig. shows the monostable multivibrator by using 555 timer.

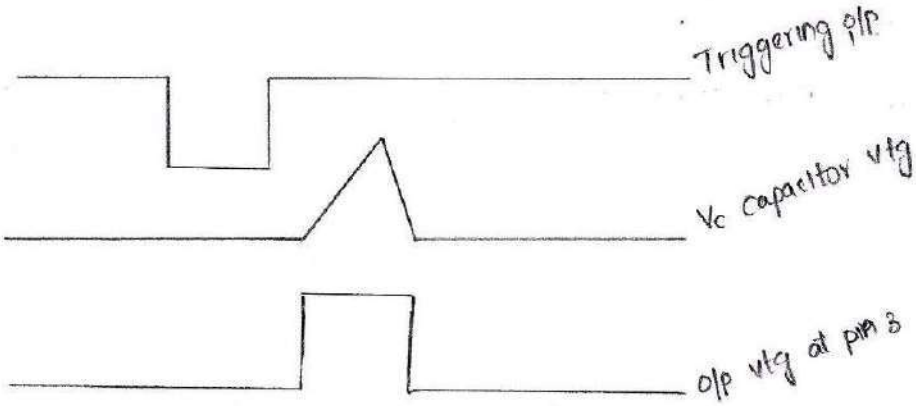


Functional Diagram :-



The above fig. shows the functional block diagram of monostable multivibrator.

1. In the stand by state [stable state] $Q = 0$; $\bar{Q} = 1$. So o/p is low. Under this condition transistor is ON i.e., it becomes short circuit through capacitor, 'C' to the ground.
2. Now the triggering passes through $V_{cc}/3$ at 2nd pin, due to this lower comparator o/p is high. So $Q = 1$, $\bar{Q} = 0$. This makes transistor Q_1 OFF & it becomes a open circuit across the capacitor. so o/p is high.
3. Now, the capacitor takes charging by V_{cc}.
4. After a time period T, the capacitor voltage is just greater than 2/3 V_{cc} and upper comparator o/p is high. so $Q = 0$; $\bar{Q} = 1$.
5. Under this condition, o/p is low & transistor Q_1 goes on there by discharging capacitor 'C' rapidly to ground.
6. The corresponding o/p waveforms of monostable multivibrator is shown in fig.



Analysis of Time Constant :

The capacitor voltage across the capacitor is given by

$$V_c = V_{cc}\left(1 - e^{-t/RC}\right) \rightarrow (1)$$

At $t = T$, the capacitor charges by $V_c = 2/3\, V_{cc}$ → (2)

Sub. eq(2) in eq(1)

$$2/3\, V_{cc} = V_{cc} - V_{cc}\, e^{-t/RC}$$

$$2/3\, V_{cc} + V_{cc}\, e^{-T/RC} = V_{cc}$$

$$e^{-T/RC} = \frac{V_{cc} - 2/3\, V_{cc}}{V_{cc}}$$

Apply log on b.s

$$\ln[a/b] = -\ln[b/a]$$

$$\ln\left[e^{-T/RC}\right] = \ln\left[\frac{V_{cc} - 2/3\, V_{cc}}{V_{cc}}\right]$$

$$+\frac{T}{RC} = +\ln\left[\frac{V_{cc}}{V_{cc} - 2/3\, V_{cc}}\right]$$

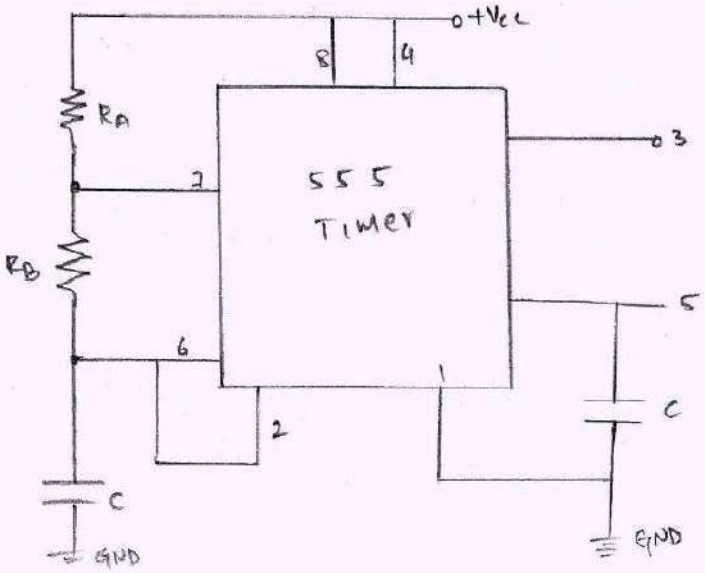
$$T = \ln RC(3)$$

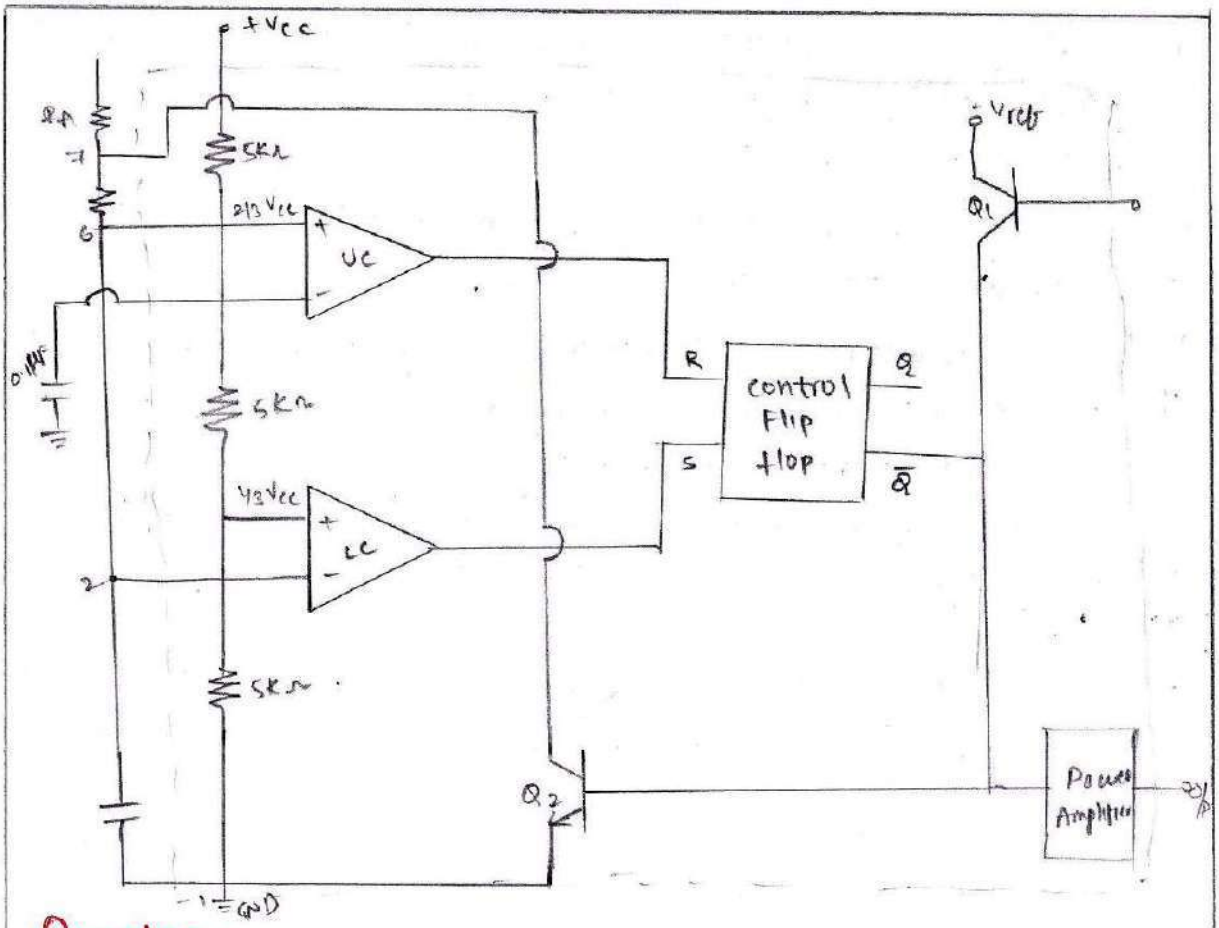
$$\therefore T = 1.1\, RC$$

Applications :

1. Pulse width generator
2. Water level control.

Asstable Multivibrator :





Operation :

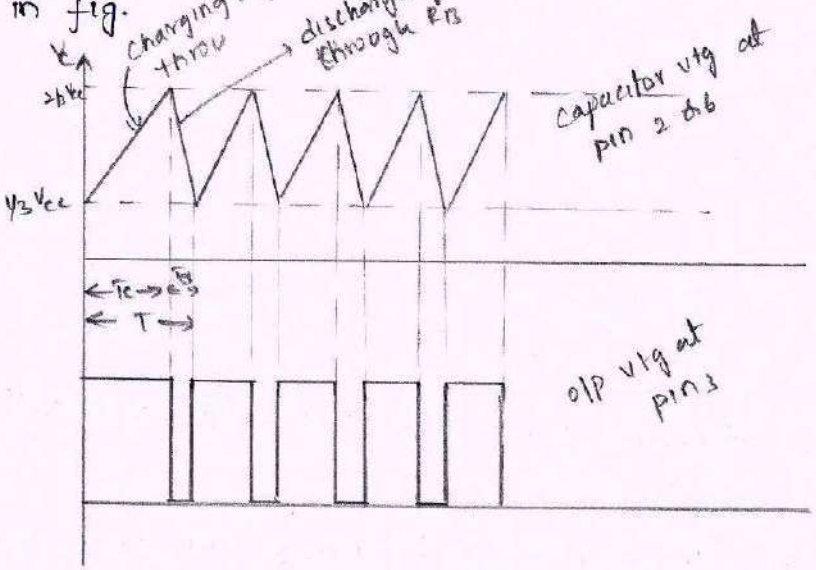
1. Asstable multivibrator has no stable states. It has 2 quasi stable states.
2. The astable multivibrator circuit by using 555 timer is shown in above fig.
3. Comparing with monostable multivibrator, the timing resistor is now split into 2 sections i.e., R_A & R_B.
4. The discharging transistor Q, is connected in blw R_A & R_B.
5. When supply voltage is connected, the external capacitor gets charging through R_A & R_B resistors.
6. When the charging voltage reaches the 1/3 Vcc voltage then lower comparator goes high. Due to this R=0; S=1; $\bar{Q}$=0; Q=1 and therefore o/p is high.

7. Similarly when Charging voltage reaches 2/3 V_{cc} then upper comparator o/p goes high. Due to this R = 1 ; S = 0 ; $\bar{Q}$ = 1 ; Q = 0 and the o/p becomes low.

8. When $\bar{Q}$ = 1 , the discharging transistor Q_2 is ON & it makes short circuited across the capacitor.

9. So the capacitor gets discharging through R_B resistor towards the ground. The capacitor discharging voltage reaches 1/3 V_{cc} & again lower comparator o/p goes high.

10. The corresponding waveforms of Astable multivibrator is shown in fig.



-Analysis of time constant :-

$$V_c = V_{cc}(1 - e^{-t/RC}) \rightarrow (1)$$

at $t = t_1$, $V_c = 1/3\, V_{cc}$

$$1/3\, V_{cc} = V_{cc} - V_{cc}\, e^{-t_1/RC}$$

$$V_{cc}\, e^{-t_1/RC} = V_{cc} - 1/3\, V_{cc}$$

$$e^{-t_1/RC} = \frac{V_{cc} - 1/3\, V_{cc}}{V_{cc}}$$

Taking log on b/s

$$-\frac{t_1}{RC} = \ln\left[\frac{V_{cc} - 1/3\,V_{cc}}{V_{cc}}\right]$$

$$-\frac{t_1}{RC} = -\ln\left[\frac{V_{cc}}{V_{cc} - 1/3\,V_{cc}}\right]$$

$$t_1 = RC \ln\left[\frac{1}{1-1/3}\right]$$

$$t_1 = RC \ln(1.5)$$

$$\therefore t_1 = 0.405\,RC$$

→ When the capacitor charges from $1/3\,V_{cc}$ to $2/3\,V_{cc}$.

at $t = t_2$; $V_{ce} = 2/3\,V_{cc}$

$$2/3\,V_{cc} = V_{cc} - V_{cc}\,e^{-t_2/RC}$$

$$V_{cc}\,e^{-t_2/RC} = V_{cc} - 2/3\,V_{cc}$$

$$e^{-t_2/RC} = \frac{V_{cc} - 2/3\,V_{cc}}{V_{cc}}$$

Taking log on b/s

$$-t_2/RC = \ln\left[\frac{V_{cc} - 2/3\,V_{cc}}{V_{cc}}\right]$$

$$t_2 = \ln RC\left[\frac{V_{cc}}{V_{cc} - 2/3\,V_{cc}}\right]$$

$$t_2 = RC \ln(3)$$

$$\therefore t_2 = 1.1\,RC$$

$$T_C = t_2 - t_1$$

$$= 1.1 - 0.405$$

$$= 0.695\,RC$$

$$\therefore T_C = 0.695\,(R_A + R_B)\,C$$

→ The capacitor takes discharging from 2/3 Vcc to 1/3 Vcc

$$1/3\ V_{cc} = 2/3\ V_{cc}\ e^{-t/RC}$$

$$e^{-t/RC} = \frac{1/3\ V_{cc}}{2/3\ V_{cc}}$$

$$e^{-t/RC} = 1/2$$

$$-t/RC = \ln(1/2)$$

$$t/RC = \ln(2)$$

$$t = RC\ln(2)$$

$$\therefore T_d = 0.69 R_B C$$

→ Total time constant $T = T_C + T_D$

$$= 0.69(R_A + R_B)C + 0.69 R_B C$$

$$= 0.69 R_A C + 0.69 R_B C + 0.69 R_B C$$

$$\therefore T = 0.69 (R_A + 2R_B) C$$

$$f = 1/T$$

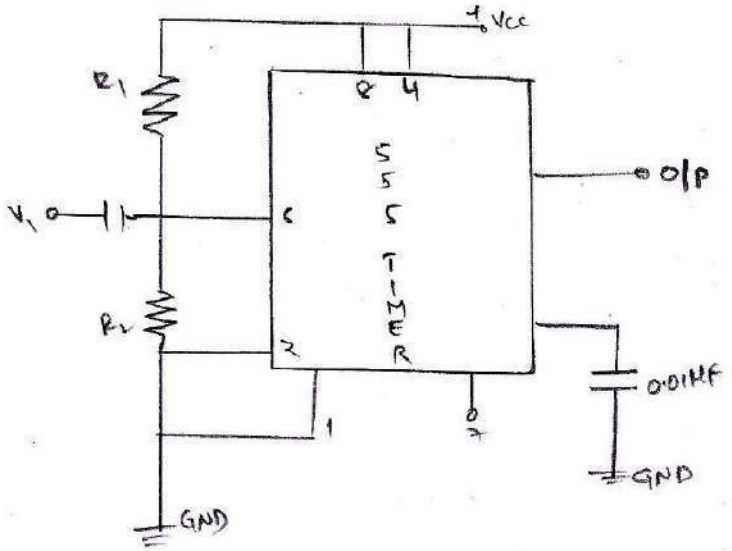
$$= \frac{1}{0.69(R_A + 2R_B)C}$$

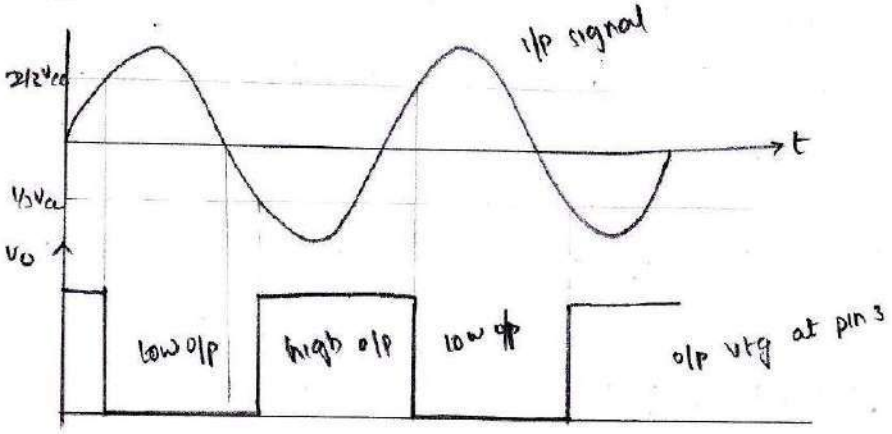
$$\therefore f = \frac{1.449}{(R_A + 2R_B)C}$$

Applications :-

1. Frequency shift key (FSK)
2. Pulse position modulator

Schmitt Trigger :-





→ Here 2 internal comparators are connected together an externally biased through R_1 & R_2 resistors.

→ Since upper comparators will be ON (or) o/p is high when the given i/p signal reaches the 2/3 Vcc.

→ Similarly lower comparator o/p is high when the given i/p signal reaches the 1/3 Vcc.

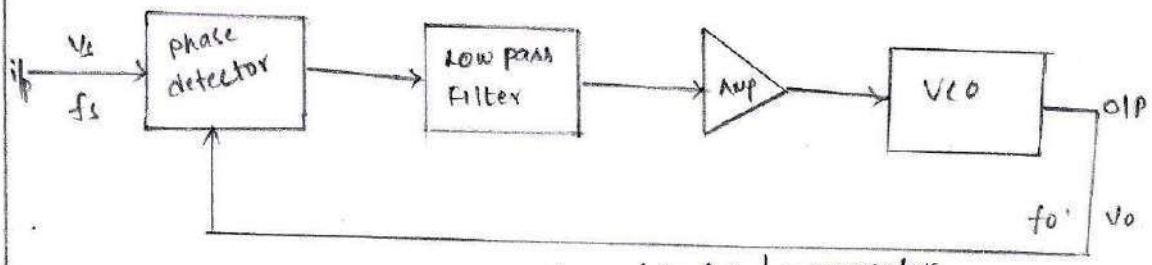
→ Due to this the o/p of the circuit is changing from one state to another state. i.e., When Uc is high, o/p is low when Lc is high, o/p is high ($R=0$; $S=1$; $\phi=1$; $\bar{\phi}=0$).

Phase Locked Loop :-

Introduction :

1. PLL is a phase locked loop. It is a closed loop circuit & its o/p frequency & o/p phase (ϕ) to be locked.
2. The PLL is an important building block of linear systems.
3. The PLL was used in 1930. At the time PLL has many features. So PLL circuits was very costly.
4. However, after the development of integrated technology, the cost of PLL has reduced.
5. Hence we observed that PLL has become one of the fundamental building block in electronic technology.
6. The PLL principle is used in FM demodulation, FSK demodulation, motor speed control, frequency multiplication & division etc.
7. The PLL is available in single package. The example of PLL is 565 IC.

Block Diagram of PLL :



It consists of 4 blocks ; 1. phase detector / comparator
2. Low pass filter
3. Amplifier
4. VCO (voltage controlled oscillator)

1. Phase Detector / comparator :

1. When i/p signal V_s at frequency f_s is applied to the phase detector & it compares the phase or frequency of incoming signal to that of the o/p of VCO.
2. The phase detector compares the 2 i/p signals & produce an voltage.
3. Phase detector basically acts as an multiplier, so it produces the sum $(f_s + f_o)$ & difference $(f_s - f_o)$ components at its o/p.

2. Low pass Filter :

The low pass filter used to remove high frequency signals ie, coming from phase detector. It passes only low frequency signals ie., the difference of two i/p signal $(f_s - f_o)$.

3. Amplifier :

The amplifier is used to amplifies the difference of frequency signal & the amplified signal is given to the voltage controlled oscillator.

4. Voltage Controlled Oscillator :

1. VCO is a frequency running multivibrator and operates at a set frequency f_o called free running frequency.
2. This frequency is determined by an external timing capacitor and an external resistor.
3. It can be shifted to either side by applying a dc control voltage V_c.
4. The frequency derivation is directly proportional to the dc current control voltage and it is called VCO.

5. The VCO frequency f_o is compared with the i/p frequency f_i by the phase detector and it is adjusted continuously until it is equal to the i/p frequency f_s.

$$f_o = f_s$$

6. The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference b/w f_s and f_o.

7. Once this action starts, we say that the signal is in the capture range.

8. The circuit is then said to be locked. Once locked, the o/p frequency f_o of VCO is identical (same) to f_s except for a finite phase ϕ. Thus, a PLL goes through 3 stages.

1. Free Running state :

In this state, there is no control on VCO o/p frequency f_o.

2. Lock Range :

In this state when f_o is exactly equal to f_i, the PLL is said to be phase locked. Once locked $f_o = f_i$ except for a finite ϕ.

3. Capture Range :

In this state, the comparison of f_o and f_i begins. The control voltage V_c starts adjusting f_o to bring it closer to f_i. The LPF controls the capture range.

Basic DAC Techniques :

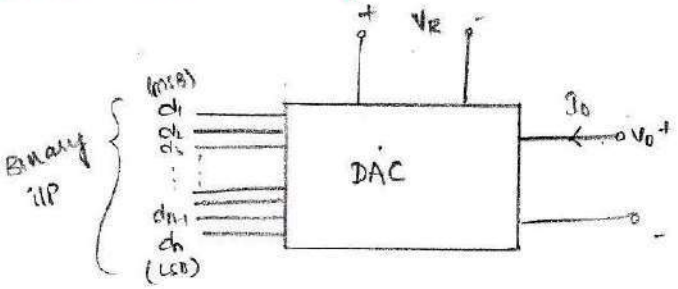


fig: Schematic of DAC

1. The i/p is an n-bit binary word D and is combined with a reference voltage V_R to give an analog o/p signal.
2. The o/p of a DAC can be either of a voltage (or) current.
3. For a voltage o/p DAC, the D/A converter is mathematically described as

$$V_0 = K V_{FS} \left(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n} \right)$$

where, V_0 = o/p voltage

V_{FS} = full scale o/p voltage

K = scaling factor = unity

$d_1 \cdots d_n$ = n bit binary fractional word with the decimal point located at the left

d_1 = MSB bit

d_n = LSB bit

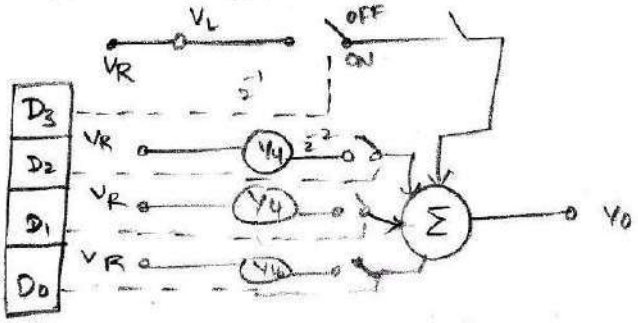


fig: Digital to Analog Conversion

→ Fig. shows explanation of DAC. Here V_R is fixed reference voltage.

→ The digital signal is contained in the register on the left.

→ Each flipflop in the register controls an analog switch as shown in the dotted lines.

$$V_0 = \left[D_3 2^{-1} + D_2 2^{-2} + D_1 2^{-3} + D_0 2^{-4} \right] V_R$$

If $D_3\ D_2\ D_1\ D_0 = 1001$

$$V_0 = 1\left[\frac{V_R}{2} + 0\,\frac{V_R}{4} + 0\,\frac{V_R}{8} + 1\,\frac{V_R}{16} \right]$$

$$\boxed{V_0 = \frac{9V_R}{16}}$$

→ There are 2 types D/A converters

1. Weighted - resistor D/A converter
2. R-2R ladder D/A converter.

1. Weighted - Resistor D/A converter :

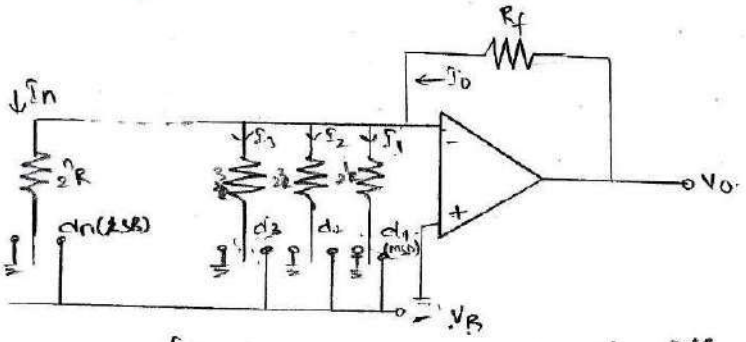


fig: A simple weighted Resistor DAC

→ One of the simplest CKt uses a summing amplifier with a binary weighted resistor N/w. It has n-electronic switches $d_1, d_2 \cdots d_n$ controlled by binary i/p word.

→ These switches are SPDT (single pole double throw) types switch

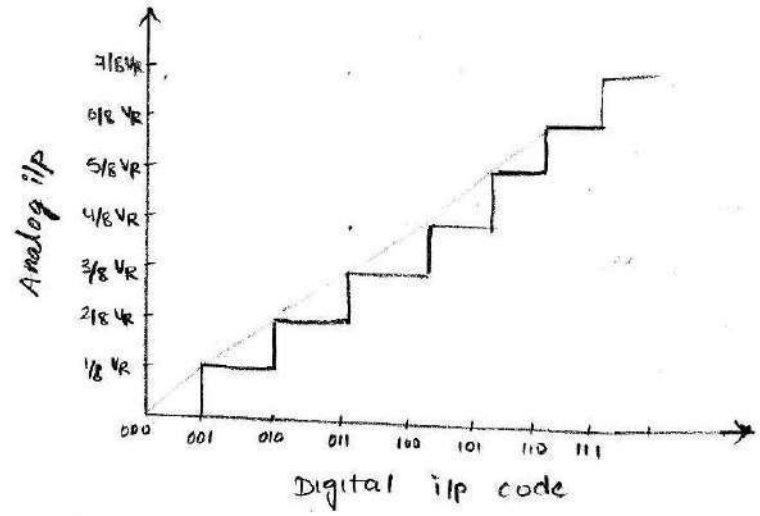


fig: Transfer char'n of a 3 bit DAC

Eg: If the binary i/p to a particular switch is 1, its connects the resistance to the reference voltage ($-V_R$).

→ The binary weighted resistor DAC uses an op-amp to sum of 'n' binary weighted currents derived from a reference voltage V_R via current scalling resistors $2R, 4R, 8R \ldots 2^nR$ as shown in the fig.

Working:

In fig. switch positions are controlled by the digital i/p's. When digital i/p logic 1, it connects the corresponding resistance to the reference voltage V_R otherwise it leaves resistor open.

∴ for ON switch $I = \frac{-V_R}{R}$

for OFF switch $I = 0$

Here op-amp is used as a summing amplifier. Due to high i/p impedence of op-amp, summing current will flow through R_f. Hence the total current through R_f can be given as.

$$I_0 = I_1 + I_2 + I_3 \cdots I_n$$

The o/p voltage is the voltage across R_f and it is given as

$$\text{so} \quad V_0 = -I_0 R_f$$

$$V_0 = -[I_1 + I_2 + I_3 + \cdots I_n] R_f$$

$$V_0 = \left[D_1 \frac{V_R}{2R} + D_2 \frac{V_R}{4R} + D_3 \frac{V_R}{8R} + \cdots D_n \frac{V_R}{2^n R} \right] V_f$$

$$= \frac{V_R}{R} R_f \left[D_1 2^{-1} + D_2 2^{-2} + \cdots D_n 2^{-n} \right]$$

When $R_f = R$

$$\therefore V_0 = V_R \left[D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} + \cdots D_n 2^{-n} \right]$$

→ The above eqn indicates that the analog o/p voltage is proportional to the i/p digital word.

Drawbacks :

1. Wide range of resistor values are required.

For 8 bit DAC, the resistor required are 2^1R, 2^2R, 2^3R ... and 2^8R. Therefore, the largest resistor is 128 times the smallest one.

This wide range of resistor values has restrics on both higher & lower ends.

. The finite resistance of the switches disturbs the binary weighted relationship among the various currents, particularly in the MSB positions, where the current setting resistances are smaller.

2. R-2R Ladder DAC :

→ In this type, reference voltage is applied to one of the switch positions and other switch position is connected to ground. It is shown in below figure.

→ Wide range of resistors are required in binary weighted resister type DAC. This can be avoided by using R-2R ladder type DAC where only 2 values of resistors are required.

→ The typical value of R ranges from 2.5 KΩ to 10 KΩ.

→ For simplicity let us consider a 3-bit DAC. where the switch position $D_1\ D_2\ D_3$ corresponds to the binary word 100.

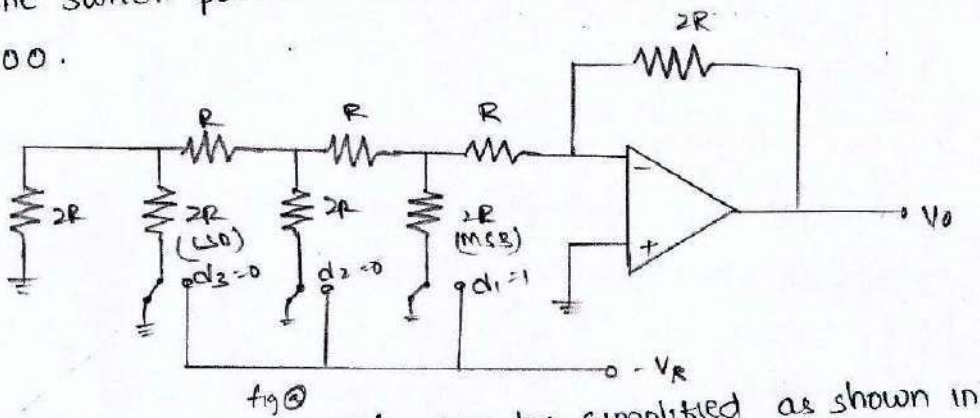


fig ⓐ

→ The equivalent circuit can be simplified as shown in below fig.

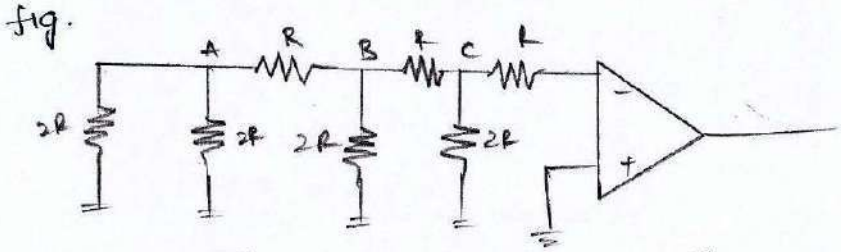
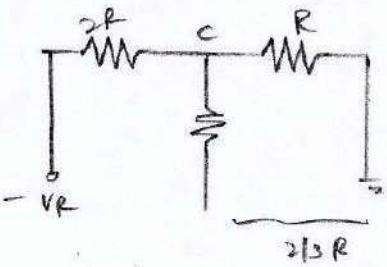


fig ⓑ Equivalent ckt of fig ⓐ



equivalent ckt of fig ⓑ

→ Then voltage at node c can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = \frac{-V_R}{4}$$

The o/p voltage is

$$V_o = -\frac{2R}{R}\left(\frac{-V_R}{4}\right)$$

$$= \frac{V_R}{2}$$

$$\boxed{V_o = \frac{V_{FS}}{2}}$$

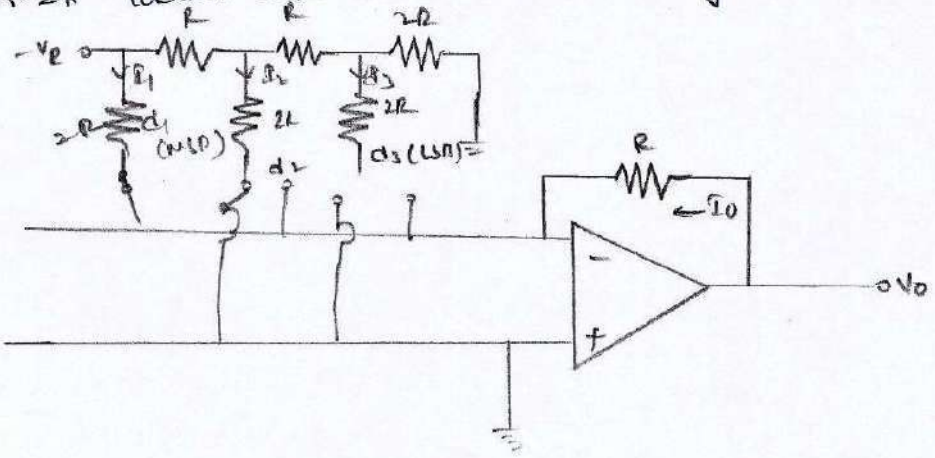
3. Inverted R-2R ladder :

→ In weighted resistor type DAC and R-2R ladder type DAC current flowing in the resistors changes as the i/p date changes.

→ more power dissipation causes heating.

→ this problem can be avoided completely in inverted R-2R ladder type DAC.

→ R-2R ladder D/A convertor uses only 2 resistors values.



→ Here each bit of binary word converts the corresponding switch either to ground (or) to the inverting i/p terminal of the op-amp which is at the virtual ground.

→ Since both the positions of switch are at ground potential, the current flowing through resistances is constant and it is independent of switch position.

→ These current can be given as

$$I_1 = \frac{V_R}{R}$$

$$I_2 = \frac{V_R/2}{2R}$$

$$= \frac{V_R}{4R}$$

$$I_2 = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R}$$

$$= \frac{V_R}{8R}$$

$$I_3 = \frac{I_1}{4}$$

We know that,

$$V_0 = -I_0 R_f$$

$$= -R_f (I_1 + I_2 + I_3)$$

$$V_0 = -R_f \left[D_1 \cdot \frac{V_R}{2R} + D_2 \frac{V_R}{4R} + D_3 \frac{V_R}{8R} \right]$$

$$= -\frac{V_R R_f}{R} \left[D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} \right]$$

If $R_f = R = V_0 = -V_R \left(D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} \right)$

Let us consider 3-bit i/p with binary 011.

Here the o/p voltage is given as

$$V_O = -V_R \left[0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}\right]$$

$$= -V_R \left[0 + \frac{1}{4} + \frac{1}{8}\right]$$

$$= -V_R \left[0.25 + 0.125\right]$$

$$= -V_R \left[0.375\right]$$

Let $V_R = 5\,V$

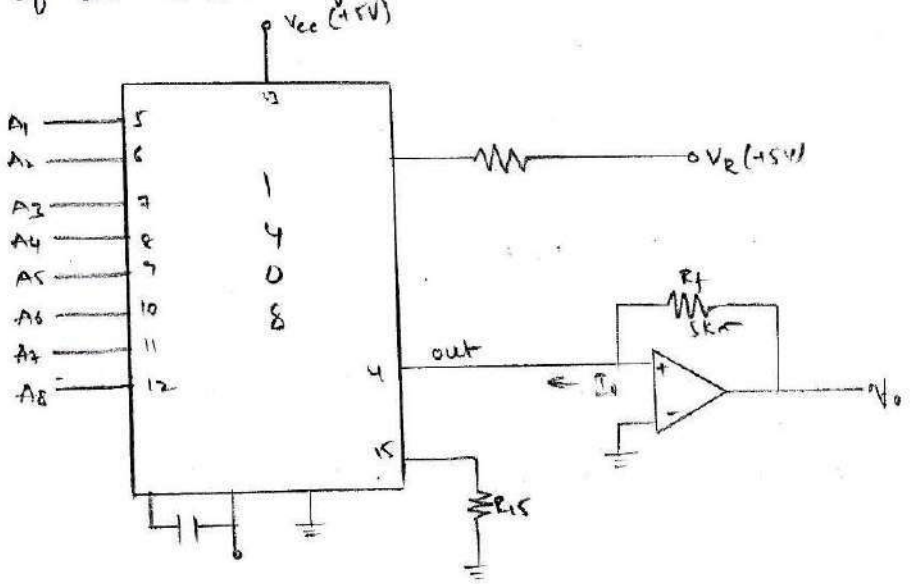
$$= -5 \times 0.375$$

$$\boxed{V_O = -1.875\ V}$$

IC 1408 DAC :

→ The 1408 is an 8-bit R-2R ladder type D/A Convertor compatible with TTL and CMOS logic.

→ It is designed to use where the o/p current is linear product of an 8-bit digital word.



→ The IC 1408 consists of a reference current amplifier, an R/2R ladder and 8-bit high speed current switch.

→ It has 8 i/p data lines as A1 (MSB) through A8 (LSB) which controls the positions of current switches.

→ It requires 2 mA reference current for full scale i/p & 2 power supplies $V_{CC} = +5\,V$ and $V_{EE} = -5\,V$.

→ The voltage V_R and resistor R_{14} determines the total reference current source.

i.e., Current $I = \frac{V_R}{R_{14}}$

$= \frac{5}{2.5K\Omega} = 2\,mA$.

→ R_{15} is generally equal to R_{14} to match the i/p impedence of the current amplifier.

→ The below fig. shows a typical 8-bit DAC 1408 compatible with TTL and CMOS logic.

→ If settling time is around 300 ns.

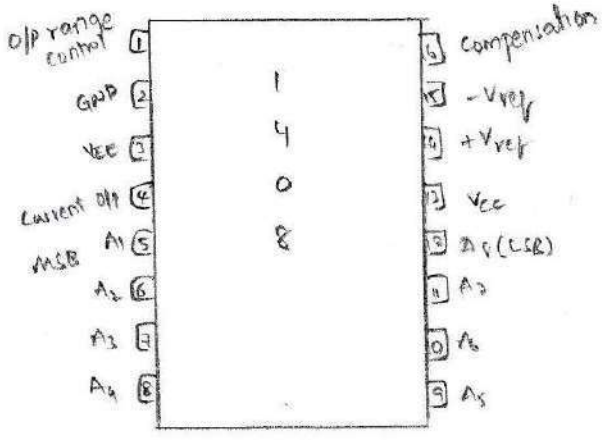


fig : pin diagram

→ It consist of 8 i/p data lines A_1 (MSB) to A_8 (LSB).

→ It needs 2mA reference current for full scale i/p.

→ The two power supplies $V_{CC} = 5V$ & $V_{EE} = -5V$.

→ The resistance R_{15} is equal to R_{14}. Hence match the i/p impedence of the reference source.

The o/p current I_o is given by

$$I_o = \frac{V_R}{R_{14}} \left[\sum_{i=1}^{n} A_i 2^{-i} \right]$$

$A_i = 0$ (or) 1

The total reference current is equal to

$$\frac{V_R}{R_{14}} = 5V / 2.5K\Omega = 2mA.$$

for full scale i/p

$$I_o = \frac{5}{2.5K} \left[\sum_{i=1}^{8} A_i \times 2^{-i} \right]$$

$$= 1.992\ mA$$

The o/p voltage V_o for full scale i/p is

$$V_o = 2mA \left[\frac{255}{256} \right] \times 5 \times 10^3$$

$$= 9.91\ V.$$

The o/p voltage eqn

$$V_o = \frac{V_R}{R_{14}} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \cdots + \frac{d_8}{256} \right]$$

→ for the bipolar range from -5V to 5V the 1408 DAC can calibrated by adding R_B blw V_R and o/p voltage pin4

as indicator in the following fig.

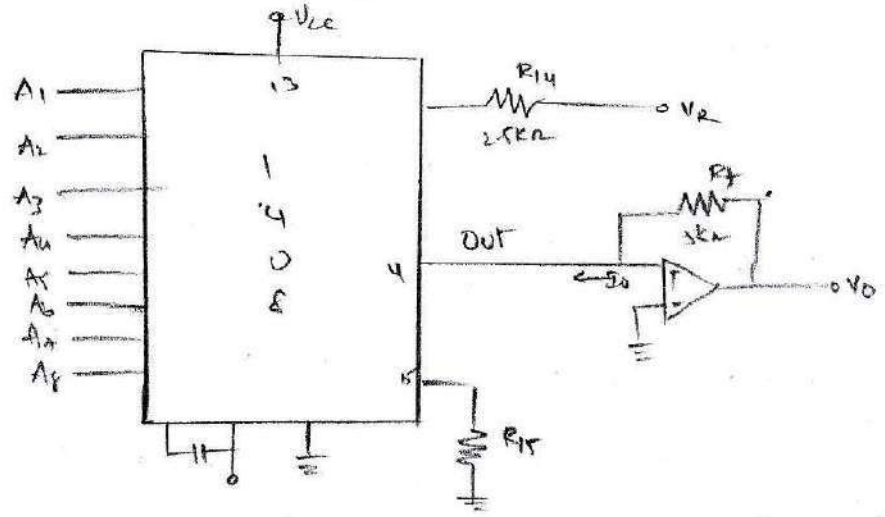
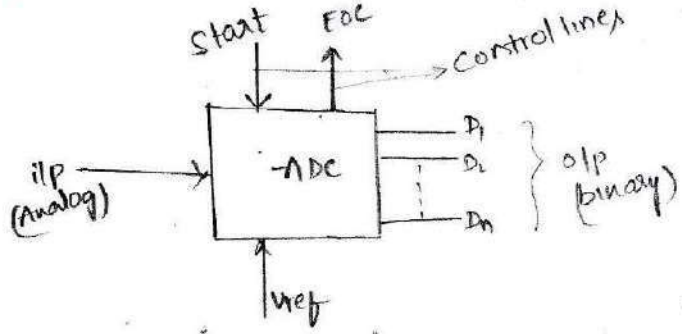


fig: 1408 D/A Converter Voltage o/p range in Unipolar Range

→ The resistor R_B gives 1mA current to the o/p. The o/p current for the bipolar operation I_o' is

$$I_o' = I_o - \left[\frac{V_R}{R_{14}}\right]\left[\sum_{i=1}^{8} d_i 2^{-i}\right] - \left(\frac{V_B}{R_B}\right)$$

Analog to Digital Convertors :



EOC = end of conversion

→ The ADC, is a circuit in which analog i/p combines with reference voltage to give the digital o/p. The schematic representation of ADC is shown in above fig.

→ ADC is a opposite version of DAC. ADC also uses the reference voltage to give an o/p.

The o/p eqn is

$$D = d_1 2^{-1} + d_2 2^{-2} + \cdots d_n 2^{-n}.$$

where d_1 = MSB ; d_n = LSB

→ ADC consists of 2 control lines i.e., start & EOC.

Start : It is a i/p control line to tell the ADC to start the conversion.

EOC : It is a o/p control line to announce when the conversion is completed.

→ Depending upon the type of application ADC are designed for micro processor.

→ ADC are classified into 2 types. 1. Direct type ADC
2. Integrating type ADC.

1. Direct type ADC :

It compares the given analog signal with the internally generated equivalent signal. There are classified into 3 types.

(a) Parallel Comparator type ADC
(b) Counter type ADC
(c) Successive Approximation type ADC.

2. Integrating Type ADC :

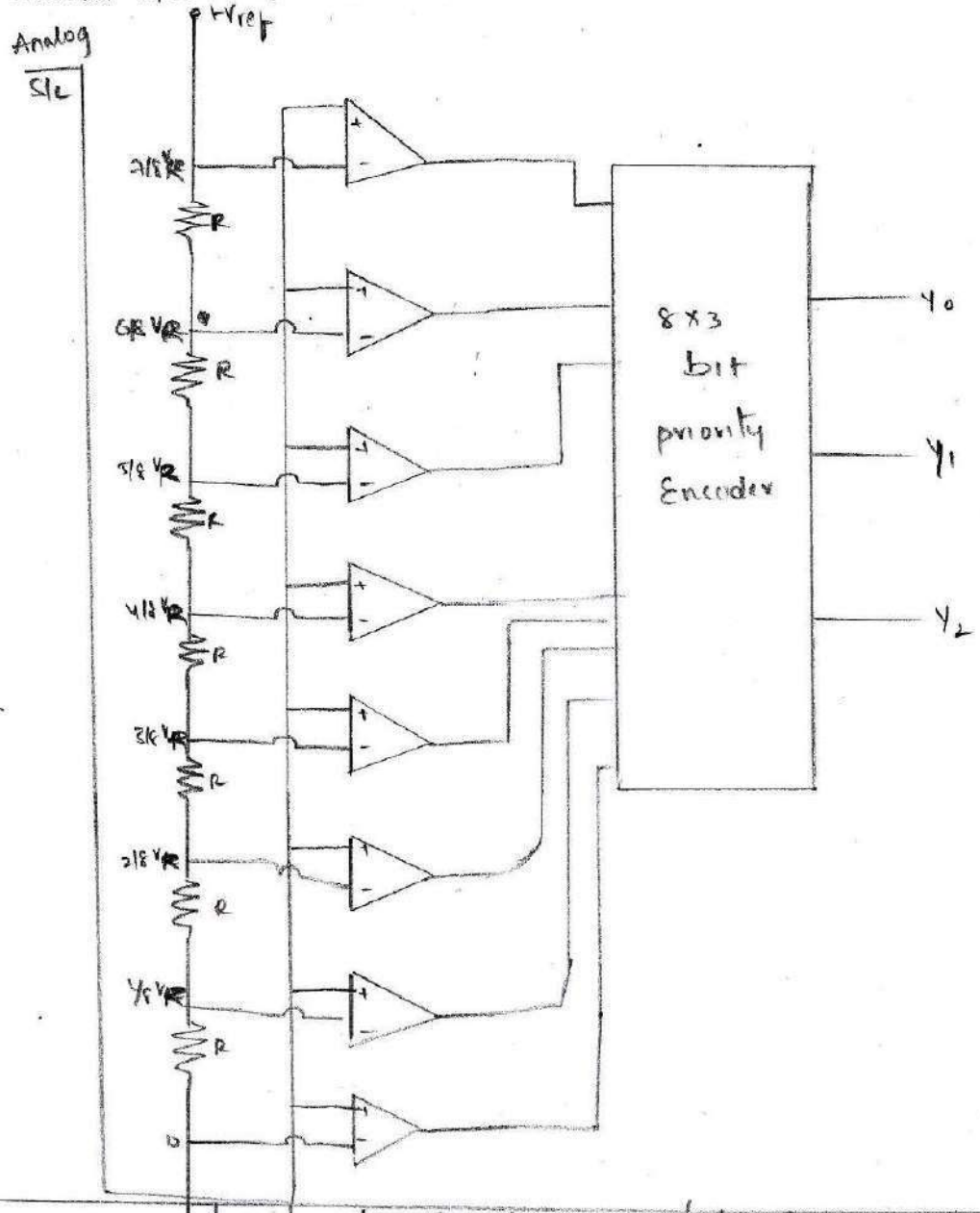
It performs conversion in indirect manner by first changing the analog i/p signal to a linear function of time & then to a digital bits. There are classified into 2 types.

(a) Dual Slope type ADC.
(b) Charge Balance type ADC.

(a) Parallel Comparator type ADC :

It is the simplest convertor at the same time it is fastest & most expensive technique.

→ The fig. shows the 3-bit A/D convertor. It consist of resistive divider n/w. Op-Amp comparators & priority encoder.



Va	I0	I1	I2	I3	I4	I5	I6	I7	Y0	Y1	Y2	Y
0 to 1/8 VR	1	0	0	0	0	0	0	0	0	0	0	
1/8 to 2/8 VR	1	1	0	0	0	0	0	0	0	0	1	

2/8 V_R to 3/8 V_R	1	1	1	0	0	0	0	0	1	0
3/8 to 4/8	1	1	1	1	0	0	0	0	1	1
4/8 to 5/8	1	1	1	1	1	0	0	1	0	0
5/8 to 6/8	1	1	1	1	1	1	0	1	0	1
6/8 to 7/8	1	1	1	1	1	1	1	1	1	0

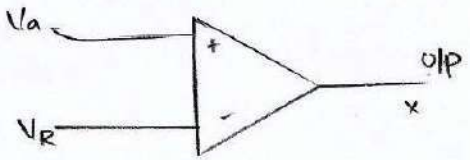
→ One i/p of each comparator is connected to the i/p signal Va & other i/p is connected to the reference signal V_R generated by the resistive divider nlw.

→ At each node of the resistive divider equal voltage is available.

→ Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided blw V_R & GND.

→ The purpose of the circuit is to compare the analog i/p Va with each of the node voltages. Corresponding truth table is shown in above fig.

→ The individual comparator truth table is shown in below fig.



i/p's	o/p
$V_a > V_R$	x = 1
$V_a < V_R$	x = 0
$V_a = V_R$	previous o/p

→ It is also called as Flash type A/D comparator.

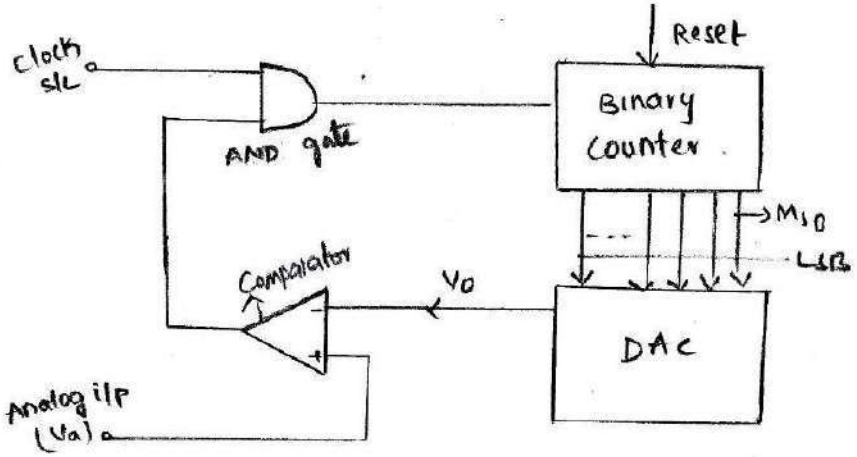
(b) Counter type ADC :

It is one type of analog to Digital convertor.

→ Here the o/p of DAC is continously compared with the i/p analog signal.

→ When the o/p of DAC is greater than analog i/p then only the o/p of comparator is high.

→ The block diagram of counter type ADC is shown in fig.
→ It consists of a binary counter, DAC, comparator & AND gate.



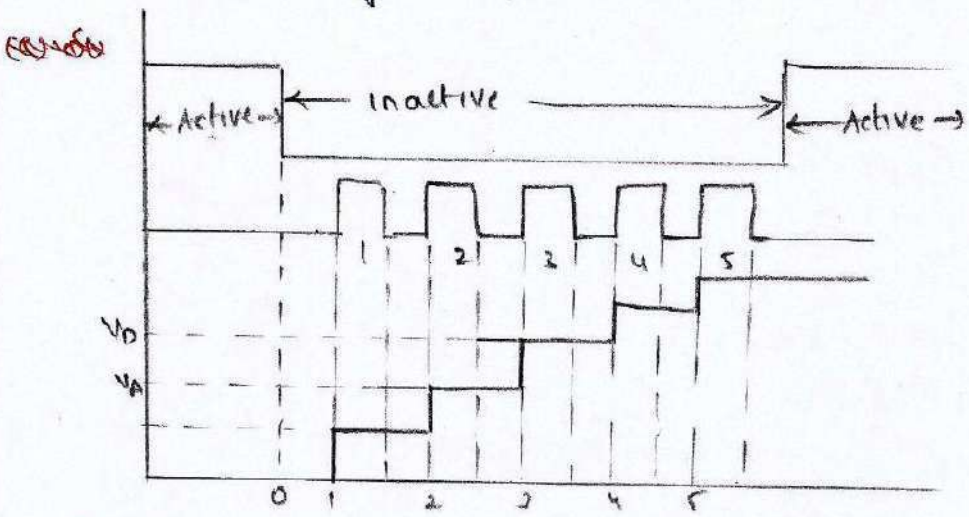
Working :

1. Initially the counter is reset i.e., its o/p is set to zero by applying a reset pulse.
2. The o/p of counter is given as digital i/p to DAC. Since i/p to DAC is zero. Its o/p is zero.
3. When the analog i/p is applied to comparator, it becomes greater than V_D.
4. Here V_A is applied to the non-inverting terminal of the comparator & V_D is applied to the inverting terminal of the comparator. When $V_A > V_D$, the comparator o/p goes high.
5. For an "AND" gate one i/p is clock pulse applied & another i/p is the o/p of the comparator.
6. When comparator o/p is high then the AND gate is able to allow the clock pulses & it is given to the binary counter.
7. The counter starts counting these clock pulses according to the clock pulses goes on increasing. This increases the o/p of the DAC.

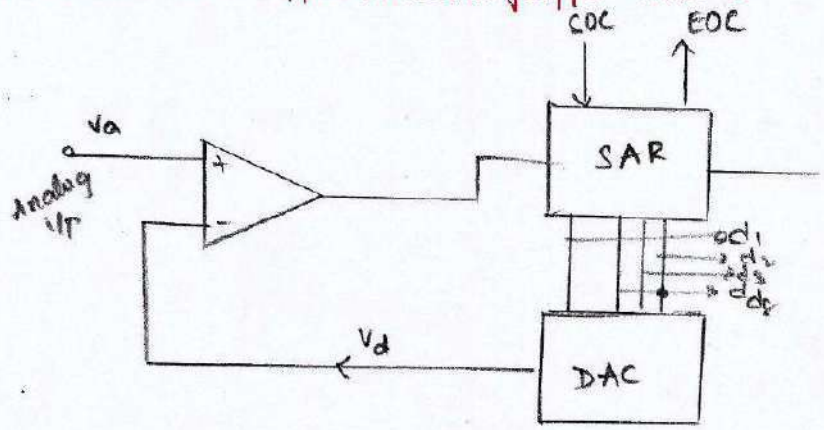
The above steps are repeated till $V_A < V_D$. when V_A is less than V_D the o/p of comparator goes low due to this "and" gate disables i.e., AND gate is not allow the clock pulses so the counting process of counter is stopped.

→ For next A/D conversion the i/p voltage V_A changes. The binary counter is cleared by applying second reset pulse.

→ The corresponding waveforms shown in below figure.



(c) Successive Approximating type ADC :



→ It is one of the most popular A/D convertor. The block diagram of successive approximation type ADC shown in above figure.

→ It consists of SAR (Successive Approximation register), SOC, EOC and DAC, comparator.

→ The successive approximation method uses ~~process~~ for to search binary bits, it completes the searching process for n-bit conversion in 'n' clock ~~pl~~ cycles.

→ The external clock signal is used to set the internal timing parameters.

→ The control signal SOC is used to start the conversion and EOC is used to end the conversion.

→ The analog i/p signal V_a is applied at one i/p of the comparator before slot the SOC the o/p should be zero.

→ After initializing the SOC, the SAR sets the four bit binary code as an input of DAC. i.e., its sets the MSB bit $d_1 = 1$, while all other bits to zeros. So that the trail code is 1000.

→ Now the o/p of DAC is compared with the analog i/p signal V_a.

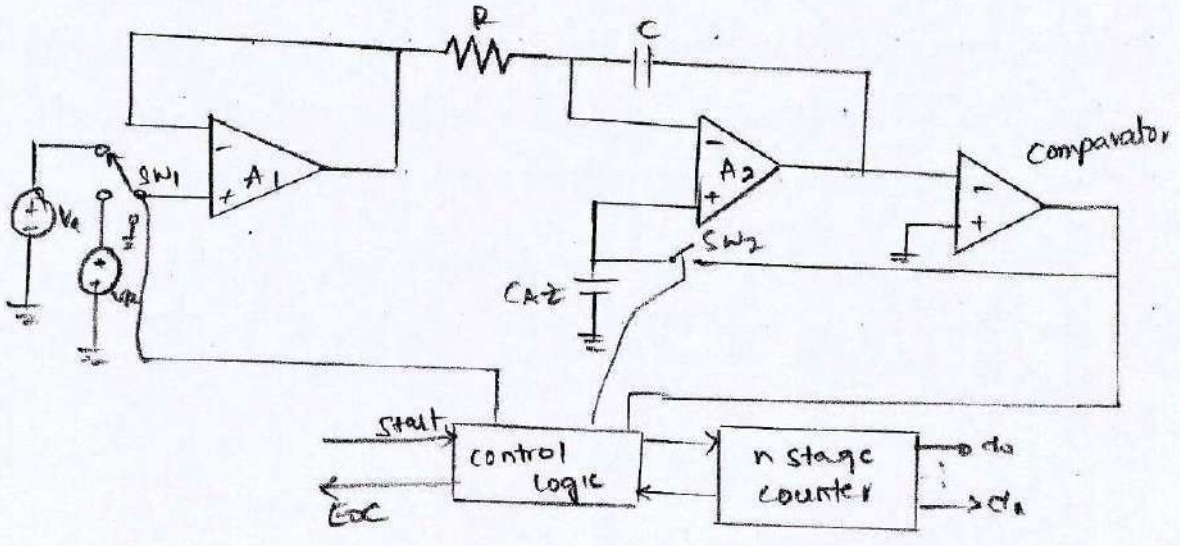
→ If $V_a > V_d$, the o/p of comparator is one then the MSB bit (or) SCR sets the MSB bit is left 1 and next LSB bit is made one and further tested.

→ However if $V_a < V_d$, the o/p of comparator is zero then SCR sets the MSB bit zero and next LSB bit is made one.

→ This process repeated for all subsequent bits, one at a time until all bit positions have been tested.

→ Whenever the DAC o/p crosses V_A, the comparator changes the state and this can be taken as the EOC control signal.

Dual Slope Type ADC :



→ The above figure shows the dual slope type ADC.

→ It consists of high input impedence buffer A_1, integrator A_2 and voltage comparator, control logic & n-stage counter.

→ The convertor first integrates the analog i/p signal V_a for a fixed duration of 2^n clock periods.

→ Then it integrates an reference voltage V_R of opposite polarity until the integrator o/p is zero.

→ The number of N ~~of~~ clock cycles required to return the integrated to zero is proportional to the value of Va average over the integration period.

→ Before the start signal switch sw_1 is connected to ground and switch sw_2 is closed.

→ So, any ~~effect~~ offset voltage present in the A_1 & A_2, it appears across the capacitor in C_{A2} till the threshold of the comparator is achieved. Thus the capacitor C_{A2} is provides the input offset voltage of all the 3 amplifiers.

→ Later when sw_2 opens C_{A2} acts as memory device to store the energy levels (or) voltage.

→ After START signal initiates ~~the~~ at $t = t_1$, the control logic open sw_2 switch and sw_1 switch connects to the V_A and enables the counter starting from zero.

→ Here n stage ripple counter is used so the counter resets to zero after counting 2^n clock cycles (or) pulses.

→ If the clock period is t_1, the integration takes place for a time $t_1 = 2^n T$ and the o/p is a ramp going downward shown in below figure.

→ The counter resets itself to zero at the end of the interval T and the switch Sw_1 is connected to the reference voltage $-V_R$.

→ Now, the o/p voltage V_o will have positive slope.

→ However when V_o becomes just zero at a time $t = t_3$ the control logic issues an end of conversion signal. So no further clock pulses enter the counter.

→ It can be shown that the reading of the counter at t_3 is proportional to the analog i/p voltage V_a.

$$T = t_2 - t_1$$

$$= 2^n \cdot \frac{\text{clock period}}{\text{clock pulses}}$$

$$t_3 - t_2 = n \frac{\text{clock cycles}}{\text{clock period}}$$

for an integrator

$$\frac{\Delta V_o}{\Delta t} = \frac{-1}{RC} V_t$$

$$\Delta V_o = -\frac{1}{RC} \Delta V_t$$

The voltages V_o will be equal to V_1 at the instant t_2 and it can be written as

$$V_1 = -\frac{1}{RC} V_a (t_2 - t_1)$$

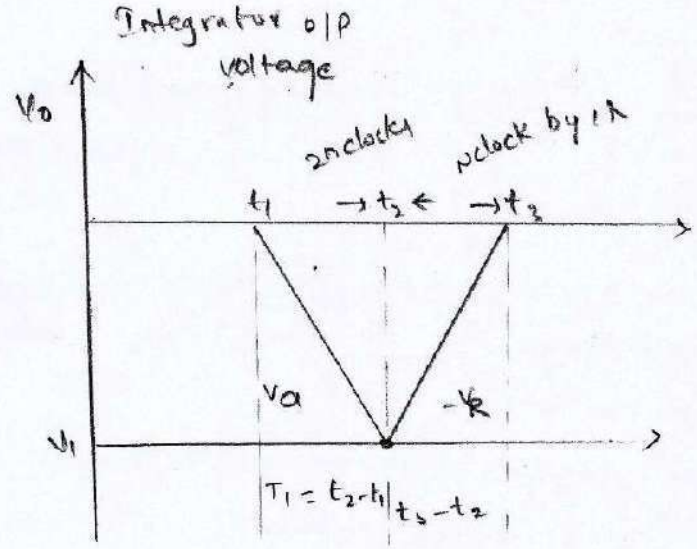
It can be also written as

$$V_1 = \frac{-1}{RC} V_R (t_3 - t_2)$$

$$V_a (t_2 - t_1) = -V_R (t_3 - t_2)$$

$$V_a (2^n) = -V_R (N)$$

$$V_a = \frac{-V_R (N)}{2^n}$$



Specifications of A/D and D/A convertor :

1. Resolution
2. Linearity
3. Accuracy
4. Settling time
5. Stability

Both A/D & D/A convertor are available with wide range of specifications.

→ The various important specifications of convertor generally specified by the manufacture are analysing.

Resolution :

The resolution of a convertor is the smallest change in voltage which may be produced at the o/p of the convertor.

Linearity :

Linearity specification of convertors. It is an important measure of accuracy and tells us how close the convertor o/p is to its ideal transfer characteristics.

Accuracy :

It is a maximum deviation b/w the ~~load~~ actual convertor (or) practical convertor o/p to the ideal convertor o/p.

settling Time :

It represents the time it takes for the o/p of settle with in a specified band of its final value following a code change at the input.

settling ranges from 100 ns to 10 ms depending upon word length and type of circuit used.

Stability :

Stability shows the performance of the convertor. The performance of convertor changes with temperature, age of components, power supply variations.