



ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES

(AUTONOMOUS)

UTUKUR (P), C. K. DINNE (V&M), KADAPA, YSR DIST.

Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu.

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ELECTRONIC DEVICES & CIRCUITS (23HPC0403)



LECTURE NOTES II-B.TECH & I-SEM

Prepared by

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**ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND
SCIENCES, KADAPA
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Web Site: <https://aitskadapa.ac.in>

II Year B.Tech. – I Semester

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(23HPC0403) ELECTRONIC DEVICES & CIRCUITS**Course Objectives:**

- Students will be able understand the basic principles of all semiconductor devices.
- Able to analyze diode circuits, various biasing and small signal equivalent circuits of amplifiers, compare the performance of BJTs and MOSFETs
- Able to design rectifier circuits and various amplifier circuits using BJTs and MOSFETs.

Course Outcomes: *After the completion of the course students will be able to*

- Understand principle of operation, characteristics and applications of semiconductor diodes, special diodes, BJTs, JFET and MOSFETs. (L2)
- Applying the basic principles solving the problems related to Semiconductor diodes, BJTs, and MOSFETs. (L3)
- Analyze diode circuits for different applications such as rectifiers, clippers and clampers also analyze biasing circuits of BJTs, and MOSFETs. (L4)
- Design of diode circuits and amplifiers using BJTs, and MOSFETs. (L4)
- Compare the performance of various semiconductor devices. (L4)

UNIT I

PN junction diode: Review, diode current equation, Diode resistance, Transition and Diffusion Capacitance, effect of temperature on PN junction diode, Quantitative analysis of Half-wave, Full-wave and Bridge Rectifiers with and without Filters, Ripple Factor and Regulation Characteristics, Illustrative problems.

Special Diodes: Construction, operation and VI characteristics of Tunnel Diode, Varactor Diode, LED, LCD, Photo Diode, SCR and UJT.

UNIT II

Review of Bipolar Junction Transistors, Characteristics, Transistor as an Amplifier and as a Switch, BJT Configurations, Limits of Operation.

Biasing and Stabilization: Operating Point, DC and AC Load Lines, Importance of Biasing, Fixed Bias, Collector to Base Bias, Self-Bias, Bias Stability, Thermal Runaway, Thermal Stability.

UNIT III

BJT Small Signal Operation and Models- the transconductance, input resistance at the base, input resistance at the emitter, Voltage gain, separating the Signal and the DC Quantities, The Hybrid π Model. Single Stage BJT Amplifiers - Common-Emitter (CE) amplifier without and with emitter resistance, Common-Base (CB) amplifier, Common- Collector (CC) amplifier or Emitter Follower, Problem solving.

UNIT IV

Junction Field Effect Transistor (FET): Construction, Principle of Operation, V-I Characteristics, Comparison of BJT and FET, FET as Voltage Variable Resistor. FET biasing.

MOS Field Effect Transistors: Introduction, Device Structure and Physical Operation, CMOS, V - I Characteristics, MOSFET Circuits at DC, MOSFET as an Amplifier and as a Switch. Biasing in MOS Amplifier circuits - biasing by fixing V_{GS} with and without source resistance, biasing using drain to gate feedback resistor, biasing using constant current source, body effect, Problem solving.

UNIT V

MOSFET Small Signal Operation Models– the dc bias, separating the DC analysis and the signal analysis, Small signal equivalent circuit models, the transconductance, the T equivalent circuit model, Single stage MOS Amplifiers – common source (CS) amplifier without and with source resistance, common gate (CG) amplifier, source follower, Problem Solving.

Textbooks:

1. Adel S. Sedra and Kenneth C. Smith, “Microelectronic Circuits – Theory and Applications”, 6th Edition, Oxford Press, 2013.
2. J. Milliman and C Halkias, “Integrated electronics”, 2nd Edition, Tata McGraw Hill, 1991.

References:

1. Donald A Neamen, “Electronic Circuits – analysis and design”, 3rd Edition, McGraw Hill (India), 2019.
2. Behzad Razavi, “Microelectronics”, Second edition, Wiley, 2013.
3. R.L. Boylestad and Louis Nashelsky, “Electronic Devices and Circuits,” 9th Edition, Pearson, 2006.
4. Jimmie J Cathey, “Electronic Devices and Circuits,” Schaum’s outlines series, 3rd edition, McGraw-Hill (India), 2010.

Introduction

Semiconductor Materials:-

Introduction:-

- * materials such as copper, aluminium etc are good "conductors", And wood, glass, mica etc. are "very bad conductors" are called "INSULATORS".
- * Another class of materials, whose conductivity & carry electricity, materials are called as "SEMICONDUCTORS".
- * Silicon [Si] & Germanium [Ge] are well known semiconductors.

Matter:-

Matter which occupies the space may be solid, liquid, gaseous.

⇒ According to the modern electron theory, matter is composed of three fundamental particles —

- * Neutron.
- * Proton.
- * Electron.

information about the these 3 particles.

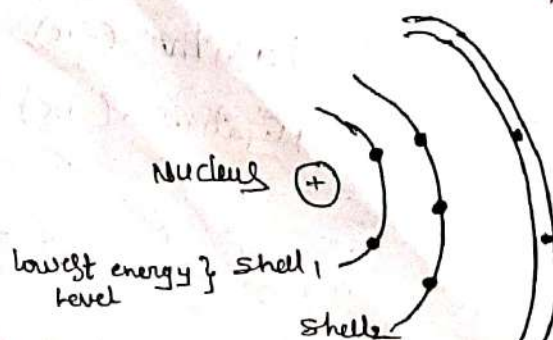
Particle	Nature of charge	Mass in kg
Neutron	No charge	1.675×10^{-27}
Proton	Positive (+ve)	1.672×10^{-27}
Electron	Negative (-ve)	9.107×10^{-31}



Structure of an ATOM:-

- All protons & neutrons are bound the center of an atom, called "NUCLEUS".
- Electrons are moving around the nucleus
- In a normal atom no. of protons equal to the no. of electrons. No. of protons in an atom is called as it's "atomic number".
- Electrons which are revolving around the nucleus, electrons are arranged in the different orbits at fixed distances from the nucleus [SUN].
- Each shell (orbit) contain a fixed NO. of electrons, A shell contain max no. of " $2n^2$ " electrons. n - shell number
- 1st - shell having 2 electrons
- 2nd - shell occupy max of 8 electrons.
- 3rd - shell " " " 18 " "
- remaining electrons are arranged in outer most shell (orbit).

Note:- The outermost shell is called the VALENCE SHELL and the electrons in this shell are called VALENCE electrons



* Concept of energy level

→ energy level increases from first shell to valence shell, as the distance from the nucleus increases.

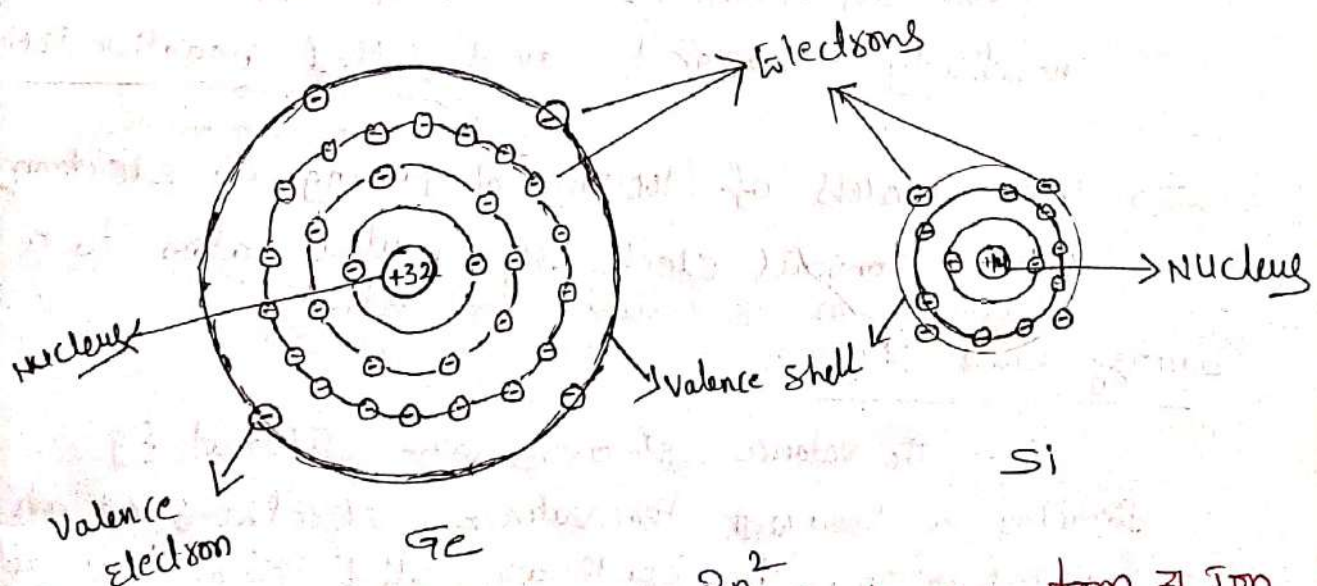
Note:- Each shell has Energy level associated with it.

→ An electron which is not attached to the nucleus and free to move when external energy applied is subjected to the force of attraction of the nucleus is called a free electron, such free electrons are basically responsible to the flow of current.

→ more no. of free electrons, better is the conductivity of the metal.

STRUCTURE OF semiconductor materials:-

→ The semiconductor materials such as Si, Ge have 4 electrons in their valence shell i.e. outermost orbit as shown in below fig.



→ Any electron that is not attached to an atom or ion or molecule but is free to move under the influence of an electric field.

→ Germanium has a nucleus with 32 protons & 32 electrons. There are 2 $\ominus$ in 1st orbit, & 8 $\ominus$ in 2nd orbit & 18 $\ominus$ in 3rd orbit. Remaining 4 $\ominus$ are in the outer or valence orbit.

→ Silicon has nucleus with 14 protons & 14 electrons

* 2 $\ominus$ are in 1st shell

* 8 $\ominus$ are in 2nd shell

Remaining 4 $\ominus$ are in outmost orbit (shell).

Note:- When there are four electrons in the outmost orbit, the semiconductor material is referred to as pure or intrinsic semiconductor.

Ionization:-

⇒ Atom as a whole loses its electrical neutral nature & becomes positively charged, that atom is called Positive ION.

⇒ Similarly, An electrically neutral atom gaining an additional electron then it becomes negatively charged and called negative ION.

⇒ This process of losing or gaining an electron, which converts electrically neutral atom to a charged ion is called Ionization.

Energy-band theory:-

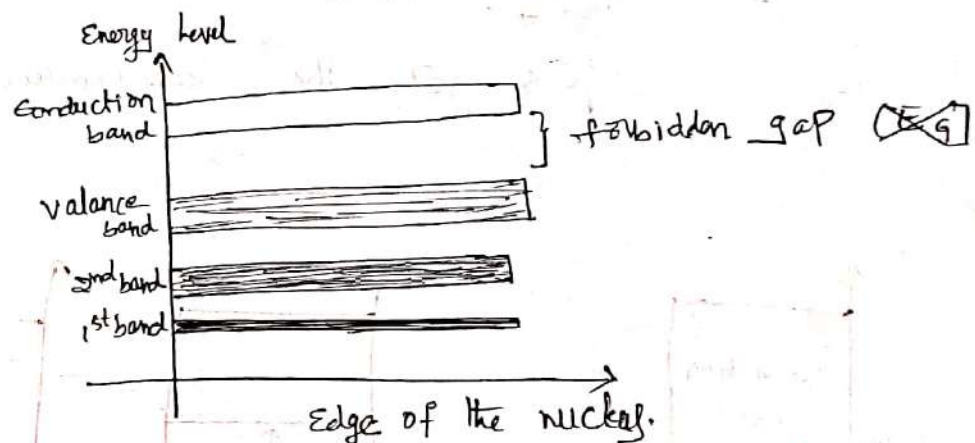
The valence electrons are shared by forming a band with the valence electrons of an adjacent atom, these bonds are called covalent bonds.

valance electrons possess highest energy level

Valence band:- The energy band formed due to merging of energy levels associated with the valence electrons i.e. electrons in the last shell, is called valance band

conduction band:- The energy band formed due to merging of energy levels associated with the free electrons is called conduction band.

forbidden gap:- The distance B/w valance band & conduction band is called forbidden band gap.



The energy associated with forbidden band is called energy gap (E_g) & measured in the unit Electron-volt (ev)

Materials:-

materials are classified in to 3 types

- conductors
- insulators
- semi conductors

* In the conductors, large no. of free electrons exist at room temperature so E_g does not exist

→ in ~~insu~~ conductors the valence & conduction bands are overlapped

* In insulators, the energy gap E_g is large of the order of 7 eV. → not conduct at any temp @ volt. Ex:- wood, glass.

* Semiconductors are materials, the energy gap is 1 eV. & the energy gap depends up on the temperature.

* At 27°C Si has E_g is 1.12 eV & Ge has E_g is 0.78 eV.

Ex:- for the Semiconductors is Si & Ge

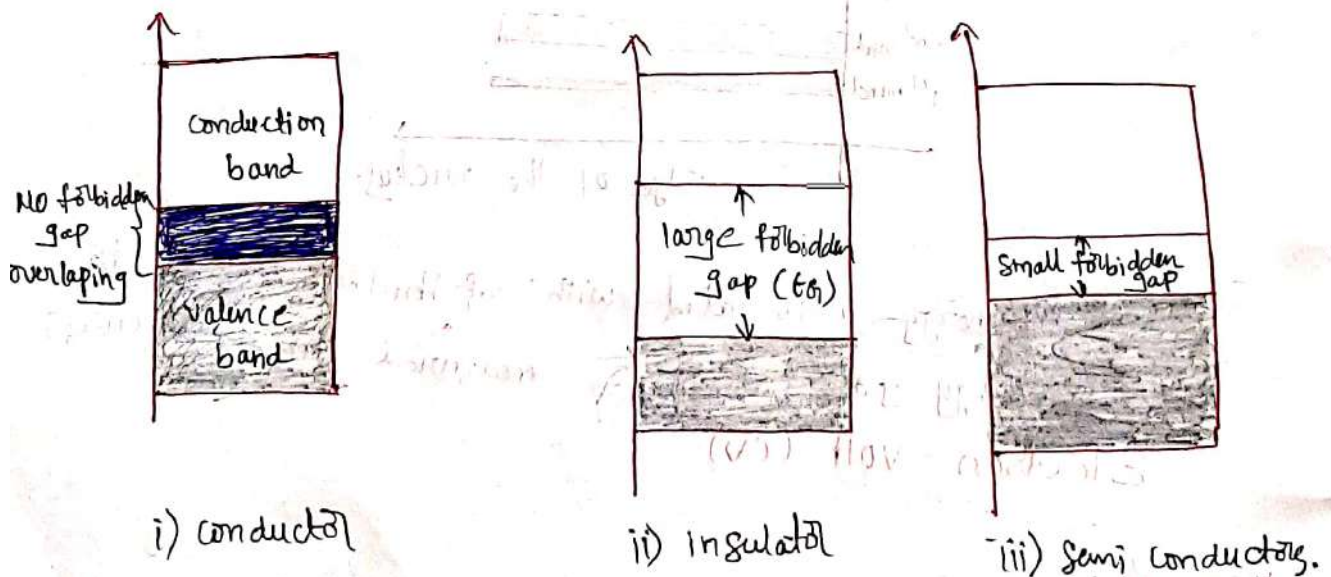


fig:- Energy band diagrams

Si is most widely used:-

- valence shell of Si is 3rd shell, while Ge is 4th shell
- valence electrons distance from nucleus of Ge is larger than Si.

* valence electrons of Ge are more loosely bound to the nucleus than those of Si.

* valence electrons are easily escaped from the atom in Ge.

Intrinsic Semiconductor:-

-> which semiconductor in its purest form is called an intrinsic semiconductor.

→ The impurity content in intrinsic semiconductor is very very small, of the order of one part in 100 million part of semiconductor, in impurity content.

Structure of Intrinsic Semiconductor:-

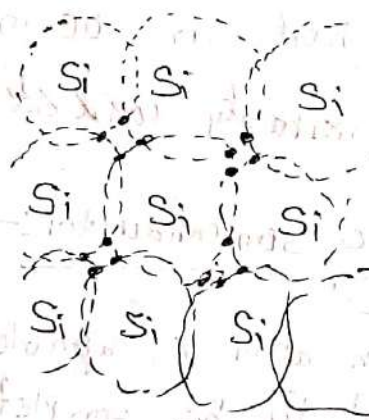
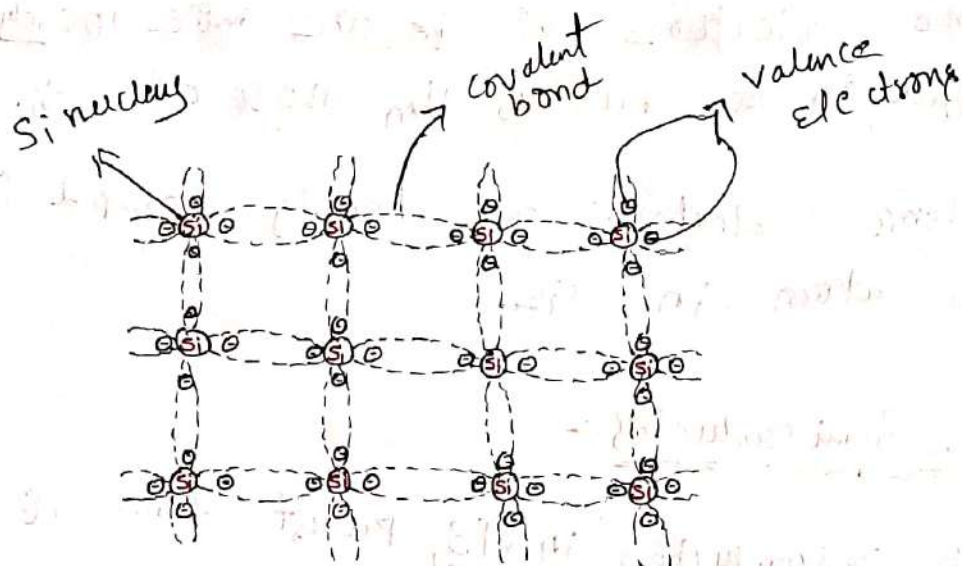
* An outermost shell of an atom is capable of holding 8 electrons, it is said to be completely filled & stable, if it contains 8 electrons.

* But the outermost shell of an intrinsic semiconductor like silicon has only 4 electrons.

* Each of these four electrons form a bond with another valence electron of neighbour atom.

- This is nothing but sharing of electrons.

- such bonds are called as "covalent bonds".

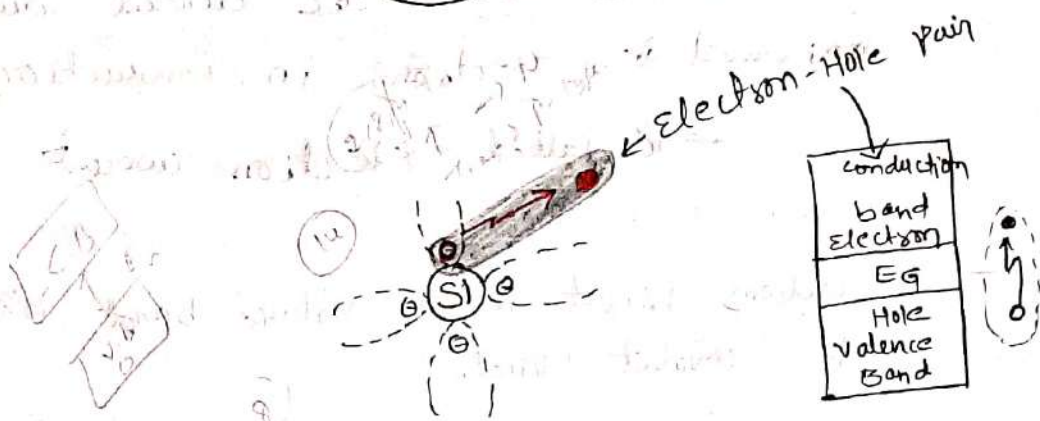
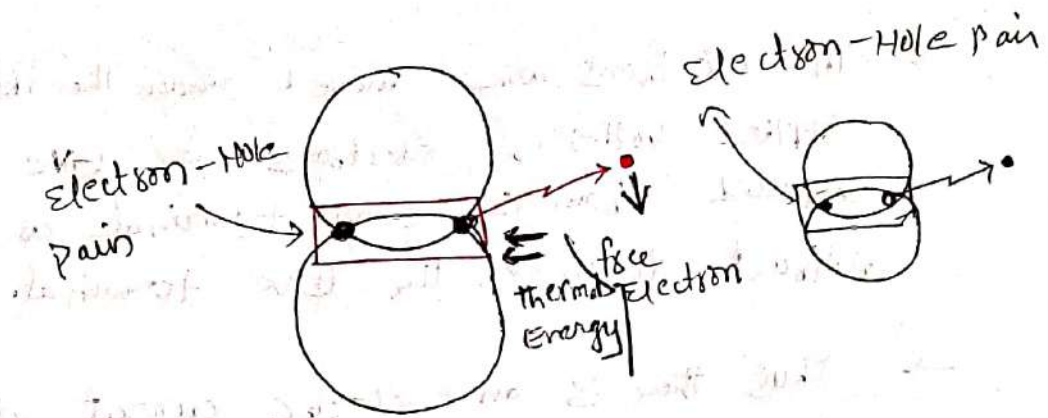


* Hence such an intrinsic semiconductor behaves as a perfect insulator at absolute zero temperature.

Electron-Hole Pair generation:-

→ at room temperature, the no. of valence electrons absorb the thermal energy, due to which they break the covalent bond & drift to the conduction band.

Such electrons become free to move in the crystal as shown in the fig.



* Valence electron drift from valence to conduction band breaking a covalent bond, a vacancy is created in the broken covalent band,

— such vacancy is called a "hole".

* So free electron & holes get generated in pairs in the form of electron-hole pair as shown in above fig.

→ An electron is -vely charged particle. Thus a hole getting created due to electron drift is said to be +vely charged.

⇒ Under the influence of applied voltage there is electron as well as hole motion in one particular direction, causing the flow of current.

→ The electrons are moved under the influence of Applied Voltage, electrons are ~~one~~ charged get repelled from the ~~one~~ terminal of Battery & Attract to ~~with~~ the $\oplus$ ve terminal.

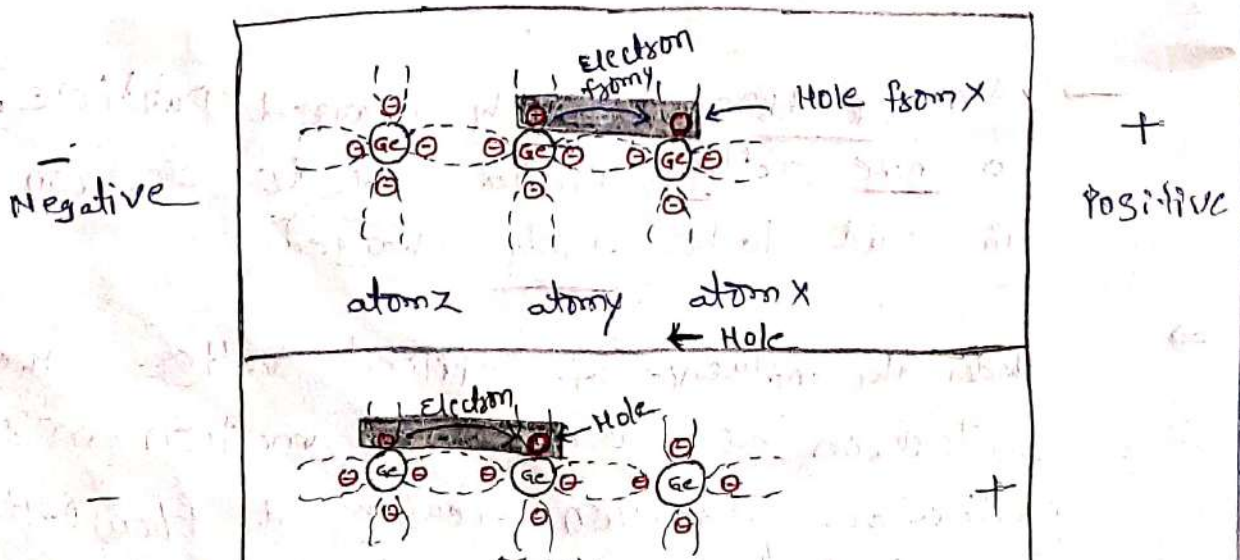
→ Thus there is an electric current due to the movement of electrons in conduction band.
- It's called electron current

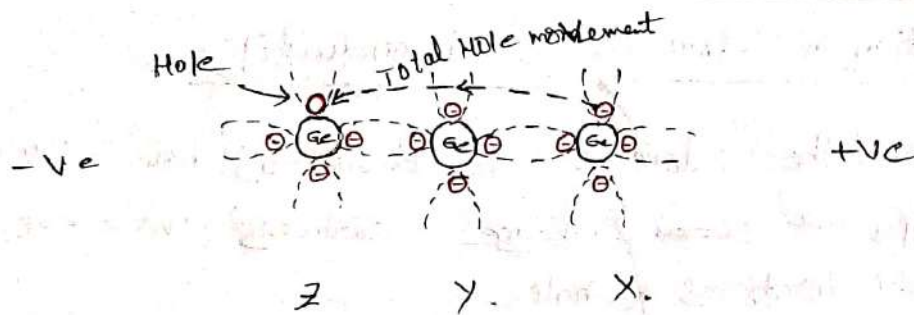
→ electrons present in the valence band, it's forming the covalent bonds.

→ Some holes are present in the valence band, due to escape of electrons from valence to conduction band.

→ when applied voltage to atom, at the electrons of covalent bond break it, & try to fill the holes present

→ The electron breaking the covalent bond jumps to the hole of neighbouring atom, leaving a hole behind, shown in fig 8.





* A movement of holes in valence band constitute the current which is called hole current.

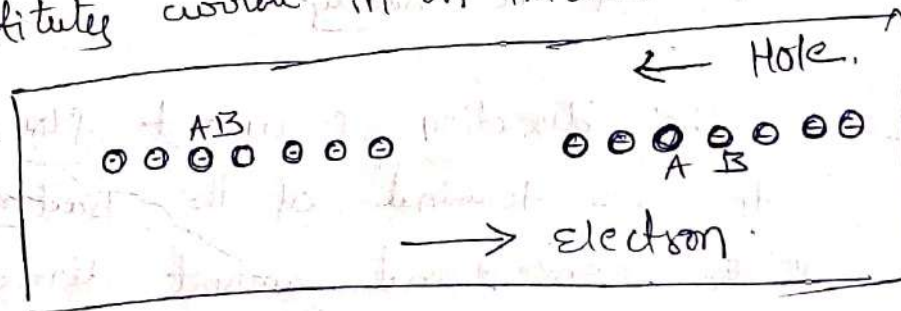
- The direction of motion of holes is the opposite direction to that of electrons.

→ current due to movement of free electrons in the conduction band is an "electron current".

→ current due to movement of holes in valence band is an "hole current".

NOTE :-

The electron as well as hole current together constitute current in an intrinsic semiconductor.

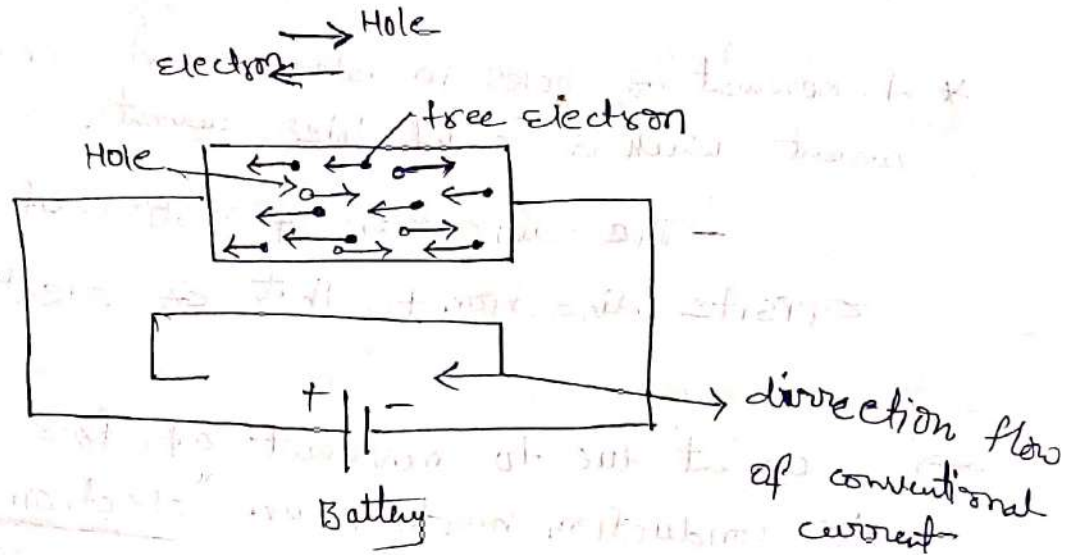


⇒ conduction of an electric current due to the ~~present~~ movement of electrons in the conduction band & holes in the valence band.

Total current = electron current + hole current.

conduction in intrinsic semi conductors:-

→ in the intrinsic semi conductors have two types of ~~semi~~ charge carriers, there are electrons & holes.



→ electrons are -vely charged, force towards the +ve terminal of the battery, while the hole are +vely charged, force towards -ve terminal of the battery.

Note:- The direction of current flows from +ve to -ve terminal of the battery is referred as the conventional current direction.

* intrinsic semi conductors are having the Low conductivity.

→ The movement of free electrons & holes continues for that result, it will form (2) produce a NEW hole-electron pair — is called RECOMBINATION

At any temperature, at any instant, the free electrons & holes are two type of charge carriers are present in equal numbers.

— This concentration is called as "intrinsic concentration."

i.e. $n = p = n_i$

n — no. of free electrons per unit volume

p — no. of holes per unit volume

n_i — Intrinsic concentration.

unit's of n_i is number per m^3 or number per cm^3

Conductivity of An INTRINSIC Semiconductor:-

→ in the Intrinsic semiconductor having two type of charge carriers.

→ one is -vely charged free electron

→ one is +vely charged hole.

→ These two particles move in opposite direction, they constitute current in the same direction.

→ A pure semiconductor the total current density is the sum of the current density due to free electron & due to holes.

$$J = J_n + J_p$$

$J_n = n n u q E$, $J_p = p \mu p q E$, then $J = J_n + J_p$
for the semiconductors:-

n = concentration of free electrons/ m^3

p = " " " holes/ m^3

μ_n - mobility of electrons in $m^2/V-s$

μ_p - mobility of holes in $m^2/V-s$

Then the current density is given by

$$J = (n \mu_n + p \mu_p) q E \quad A/m^2 \rightarrow (1)$$

q - charge one electron = $1.6 \times 10^{-19} C$

E - Electric field in V/m

W.K.T According to ohm's law

$$J = \sigma E \rightarrow (2)$$

σ - conductivity in $(\Omega-m)^{-1}$

from eq (1) & (2)

$$\sigma = (n \mu_n + p \mu_p) q \quad (\Omega-m)^{-1}$$

for intrinsic semiconductors $n = p = n_i$

$$\therefore \sigma_i = (n_i \mu_n + n_i \mu_p) q \quad (\Omega-m)^{-1}$$

$$\sigma_i = n_i (\mu_n + \mu_p) q \quad (\Omega-m)^{-1}$$

EXTRINSIC Semiconductor:-

→ To improve the intrinsic semiconductor conductivity
Adding other material to the intrinsic semiconductor.
- it is called as doping.

* The impurity added is called dopant

→ The Resulting doped semiconductor material is called
"Extrinsic Semiconductor".

→ After doing, it increases the conductivity of
basic semiconductor hence the extrinsic semiconductors
are used in practice for manufacturing of
various electronic devices such as
Diodes & Transistors.

Depending upon doping, it's classified in to 2
Types → n-type
→ p-type.

Types of impurities:-

→ The basic semiconductor having 4 electrons in
valence band - is called Tetravalent atom.

→ Added impurity material having 5 valence electrons
- is called Pentavalent Atom.

→ This impurity Added to an intrinsic semiconductor
- is called donor doping - Each impurity
Atom donates one free electron to an Intrinsic
materials.

Ex of impurity's are Arsenic, bismuth, Phosphorous etc.

— This creates An extrinsic Semiconductor with large no. of free electrons. called n-type ~~type~~ Semiconductor.

→ Another Added impurity material having only 3 electrons in valence band is called Trivalent Atom.

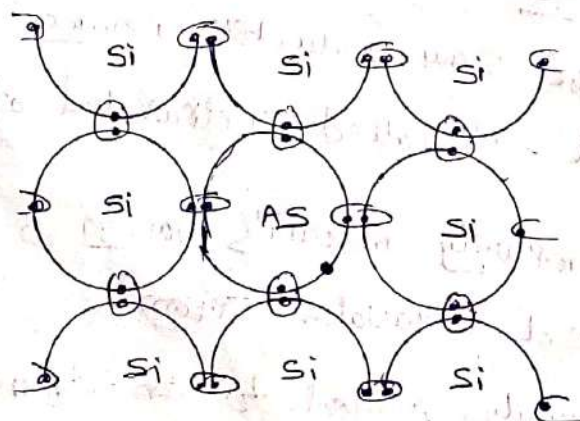
Such impurity is called "Acceptor impurity".

→ These impurity is Added to an intrinsic Semiconductor, it creates more holes & ready to accept An electron, hence the doping is called "acceptor doping".

Ex :- Gallium, Indium & Boron

These creates An extrinsic Semiconductor with large no. of holes is called P-type Semiconductor.

n-type Semiconductor:-



→ A small Amount of Pentavalent impurity is Added to a pure Semiconductor, it is called n-type Semiconductor.

N-type material

* Pentavalent impurity has 5 valence electrons, ex- ARSENIC, BISMUTH, PHOSPHOROUS & ANTIMONY. — is called "DONOR IMPURITY."

* n-type material formation by Adding (As) Arsenic in to Si. it has 5 valence electrons

→ The (As) arsenic Atom fits in the Si crystal in such a way that it's 4 v. electrons form covalent bonds with 4 adjacent Si atom.

— The 5th electron has no chance to forming a covalent bond. This spare electron enters the conduction band as a free electron.

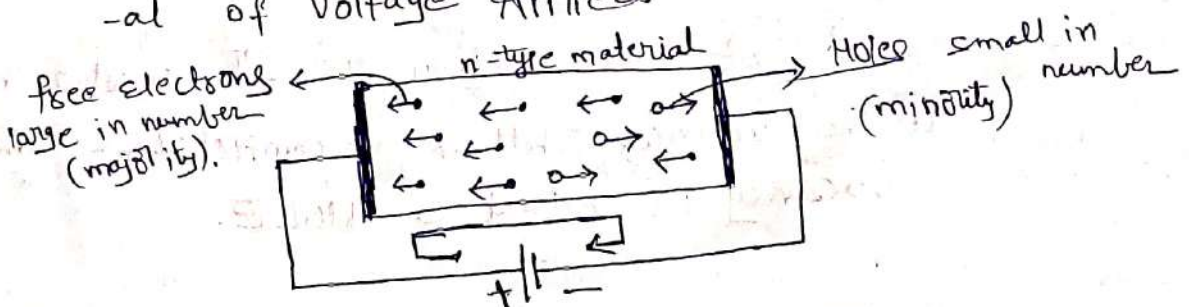
— The formation is shown in above fig.

* This means that each ARSENIC ATOM ADDED INTO SILICON ATOM GIVES ONE FREE ELECTRON

→ Since free electrons have negative charges, the material is known as n-type material.

Conduction in n-type Semiconductor:-

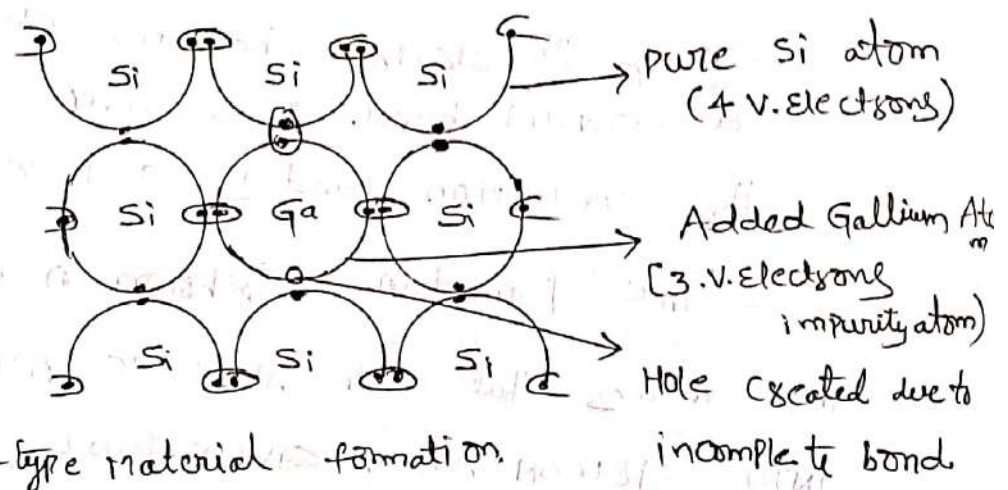
→ voltage is applied to the n-type Semiconductor, the free electrons (available due to added impurity), move in a direction of +ve terminal of voltage Applied.



→ Holes are less in number hence electron current is dominant over the hole current.

* Hence, in n-type semiconductor free electrons are called majority carriers while the holes which are small number are called minority carriers.

P-type Semiconductors:-



→ Small Amount of trivalent impurity is Added to a pure semiconductor - is called as P-type semiconductor.

* this impurity called as "ACCEPTOR IMPURITY".

→ The Ga has 3 v. electrons, Ga atom fits in the Si crystal in such a way that it has 3 v. electrons from 3 covalent bonds with adjacent Si atoms.

→ Short of one electron, the 4th covalent bond in the valence shell is incomplete - that vacancy is called a HOLE.

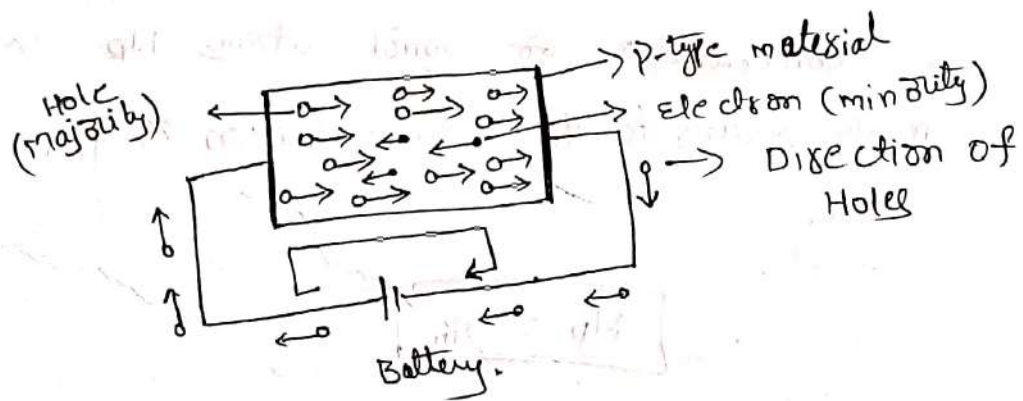
→ Such more Ga atoms are Added to Si crystal, Each gives one HOLE, these hole are treated as +vely charged, - it is called P-type material.

Conduction in P-type Semiconductor:-

* Apply the voltage to the P-type material. The Holes move in valence band and are mainly responsible for the conduction.

* So the current conduction in P-type material is predominantly due to the holes, free electrons are very less numbers.

— Hence Holes are majority carriers while electrons are minority carriers in P-type material.



Conductivity of Extrinsic Semiconductor:-

→ There are two type of materials n-type & p-type

conductivity of n-type material:-

in n-type material, the free electrons are majority carriers while holes are minority carriers.

Let n_n - concentration of free electrons in n-type

p_n - concentration of holes in n-type

N_D - concentration of donor atoms

* main letter n or p indicates concentration of type of charge carrier electron (n) hole - suffix indicates the type of material.

W.K.T conductivity in n-type

$$\sigma_n = (n_n \mu_n + p_n \mu_p) q$$

But $p_n \ll n_n$

$$\sigma_n = n_n \mu_n q$$

Concentration of donor atoms N_D is approximately equal to the concentration of free electrons n_n .

$$N_D \approx n_n$$

$$\sigma_n \approx N_D \mu_n q$$

conductivity of p-type material:-

for p-type material, holes majority & electrons are minority

n_p - concentration of free electrons in

p_p - " " " holes in p-type

N_A - " " " acceptor atoms

$$\sigma_p = (n_p \mu_n + p_p \mu_p) q$$

$$n_p \ll p_p$$

$$\sigma_p = (p_p \mu_p) q$$

concentration of acceptor N_A is equals to the concentration of holes in P-type p_p .

$$N_A \approx p_p$$

$$\sigma_p = (N_A \mu_p) q$$

low mass Action

P-N JUNCTION ~~DIODE~~:

* We have the two type of extrinsic semiconductors, n-type & p-type.

→ In n-type electrons are majority & holes are minority charge carriers, such p-type vice versa.

* These two type materials are combined chemically with a special fabrication technique to form a P-N JUNCTION - that electronic device called DIODE.

DRIFT CURRENT:

→ voltage is applied to a semiconductor, the free electrons try to move in a straight line towards the +ve terminal of the battery.

→ The electrons moved into +ve terminal ^{crash} collide with the atoms of semiconductor & connecting wires.

→ The electron strikes an atom in each time, it rebounds in a random direction.

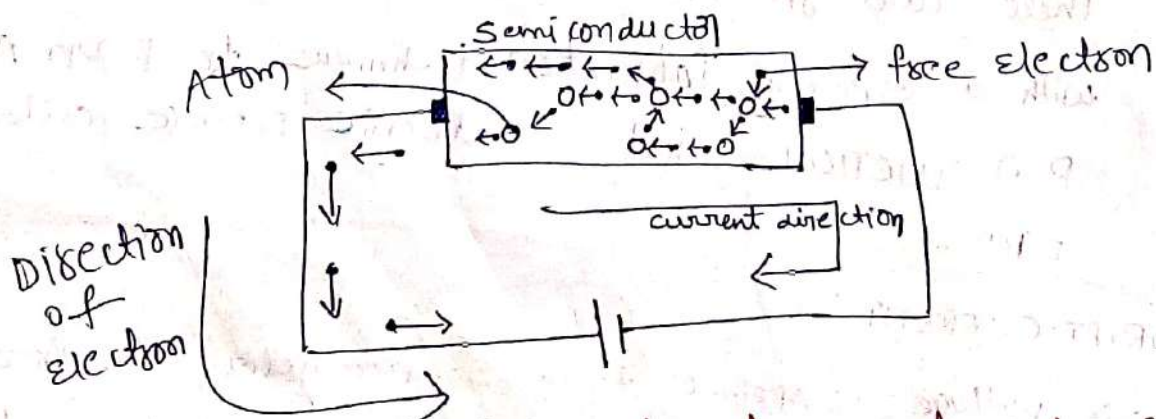
→ Still Applied voltage make the electrons drift to wards +ve terminal.

* This drift causes current to flow in a Semiconductor, under the influence of the Applied voltage.

* → This current produced due to drifting of free electrons is called Drift current.

→ The velocity with which electrons drift is called drift velocity.

* The drift current means the flow of current due to bouncing of electrons from one Atom to another, travelling from -ve terminal to +ve terminal of Applied voltage.



Note:- The direction of conventional current is always opposite to the direction of drifting electrons.

Diffusion current:

Gradient (Slope)

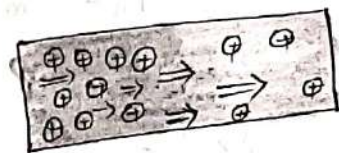
* In nonuniform doping of semiconductors, the electrons are move from the High carrier concentration to Low carrier concentration.

→ Such movement of charge carriers, due to the concentration ^{gradient} in a semiconductor is called process of diffusion.

→ When charge carriers move, the current is constituted in a bar. The current due to the Diffusion is called Diffusion current.



(a) Non uniform concentration

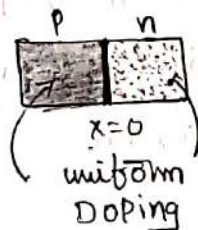


(b) Process of Diffusion

Note:- Diffusion is observed in non uniformly doped semiconductors & Not in in conductors.
open circuited -

P-N Junction (Qualitative Theory of PN Junction)

⇒ first points in previous page



The interface b/w the two regions at $x=0$ is called Metallurgical Junction.

Two Regions are at thermal equilibrium, $W \ll L_{De}$

Say,

on p side:- $p_p \rightarrow$ majority charge carrier concentration - N_A

$n_p \rightarrow$ minority charge carrier concentration - $\frac{n_i^2}{N_A}$

As $\oplus$ are majority & $\ominus$ are minority, $n_p \ll p_p$

on n side:-

$n_n \rightarrow$ majority charge carrier concentration = N_D

$p_n \rightarrow$ minority charge carrier " = $\frac{n_i^2}{N_D}$

As $\ominus$ are majority & $\oplus$ are minority, $p_n \ll n_n$.

→ At junction $x=0$, large changes in the carrier concentration.

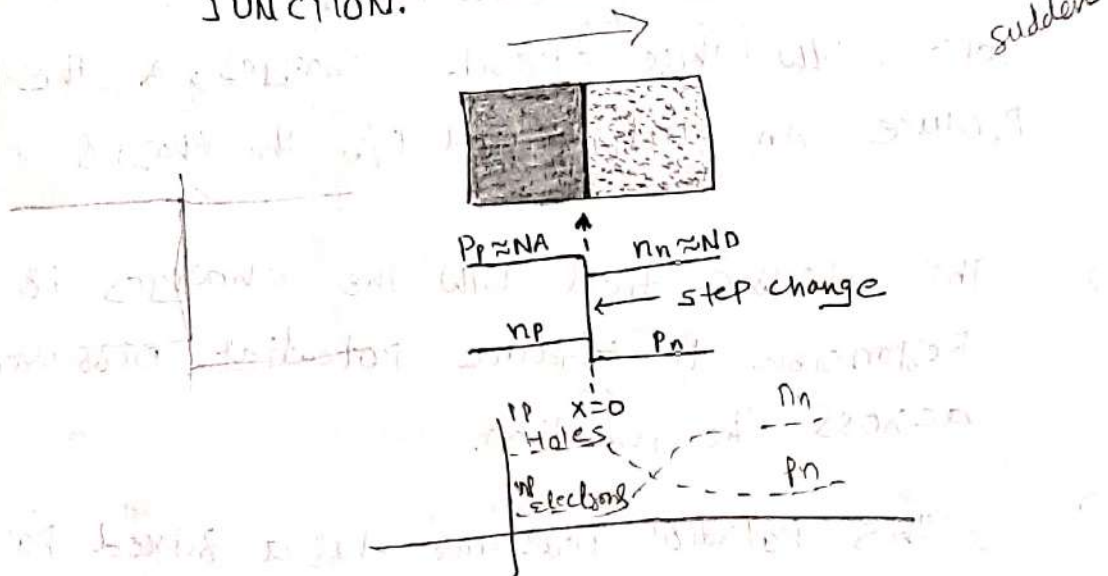
→ As the Junction is crossed from p-side to n-side, there is sudden decrease in the hole concentration from p_p to p_n . Similarly there is sudden increase in the electron concentration from n_p to n_n .

→ These sudden changes appear as the STEP type changes.

→ for the holes, there is step change from p_p to p_n , while the electrons there is a step ~~is a~~ change from n_p to n_n .

* Due to this, the P-N junction is called

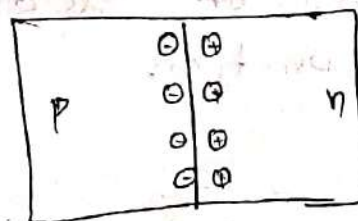
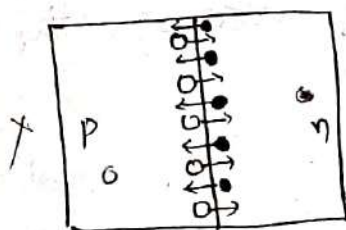
STEP GRADE P-N JUNCTION (or) ABRUPT P-N JUNCTION.



Depletion Region:-

In thermal equilibrium, in the region near the junction, there exists a wall of negative immobile charges on p side & a well of the immobile charges on n-side.

in this region, there is no mobile charge carriers, such a region is ^(reduction) depleted of the free mobile charge carriers & hence called depletion region or depletion layer.



→ width of depletion region is very small 0.5 to $1 \times 10^{-6} \text{ m}$.

Barrier Potential:-

→ Opposite charges existing near the junction creates a potential difference [Voltage] across the junction.

→ According to Coulomb's law, there exists a force b/w these opposite charges, & this force produces an electric field b/w the charges.

→ The electric field b/w the charges is responsible to produce potential difference across the junction.

→ This potential difference has a fixed polarity and acts as a barrier to the flow of electron & holes, across the junction.

Hence the potential is called barrier potential, junction potential or built-in potential barrier of P-n Junction.

* it is also called as cut-in voltage.

Note:-

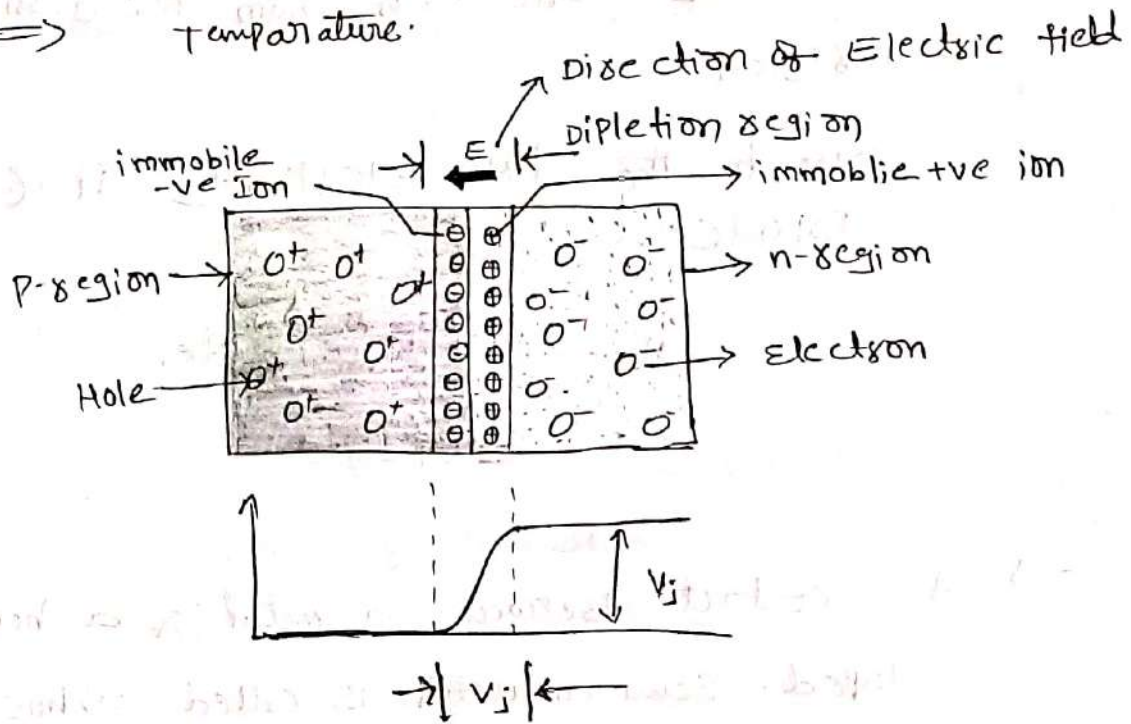
Barrier potential also indicates the amount of voltage with proper polarity, to be applied across the P-n junction, to start the flow of electrons & holes across the junction.

Barrier Potential depends up on following factors:-

$\Rightarrow$ Type of semiconductor used

$\Rightarrow$ concentration.

$\Rightarrow$ temperature.



$\rightarrow$ if doping increases the width of the depletion region is decreases on their side either P or n side.

Si - 0.7V
Ge - 0.3V } cut-in-voltage



The P-N Junction Diode:-

→ The P-n junction has two terminals called electrodes, one each from P-region & n-region.

→ Due to the two electrodes it is called Diode.

i.e. di + electrode.

= Diode

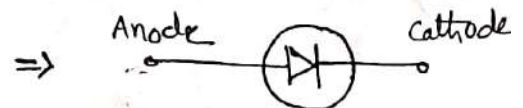
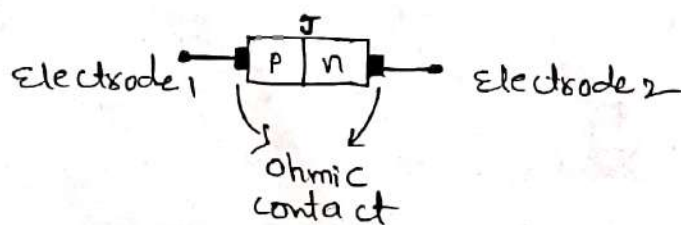
→ A contact between a metal & a heavily doped semiconductor is called ohmic contact.

ohmic contact has 2 important properties

* it conducts current equally in both the directions.

* The drop across the contact is

very small, which does not affect the performance of the device.



→ direction of current.

fig:- P-n junction Diode

fig:- Symbol P-n junction diode

* The P-region acts as a "Anode" while the n-region acts as a "Cathode."

Biased PN Junction :-

→ Applying external D.C. voltage to any electron device is called biasing.

→ it's classified into two

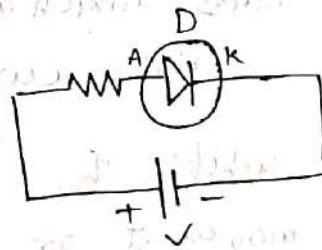
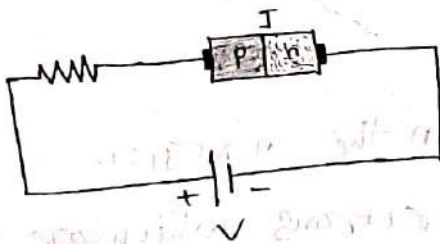
1) Forward biasing.

2) Reversing biasing.

FORWARD Biasing of P-n Junction Diode :-

→ An external D.C. voltage is Applied in such a way that the P-region terminal is connect to the +ve of Battery & the n-region is connected to the -ve of the Battery

— The biasing condition is called Forward biasing, as shown in fig.



→ Series connection of Resistor is limited current to the Device.

operation :-

→ When the Applied voltage is "less than" barrier potential (cut-in-volt), there is no conduction in F.b.

→ When the Applied voltage over come the barrier potential, it's reduce the width of the depletion Region.

→ Forward voltage is increased, At a particular value of the depletion region becomes very much narrow such that large no. of majority charge carriers can cross the junction.

→/ The large no. of majority carriers constitute a current called forward current.

→ once the conduction electrons enter the P-region, they become valence electrons.

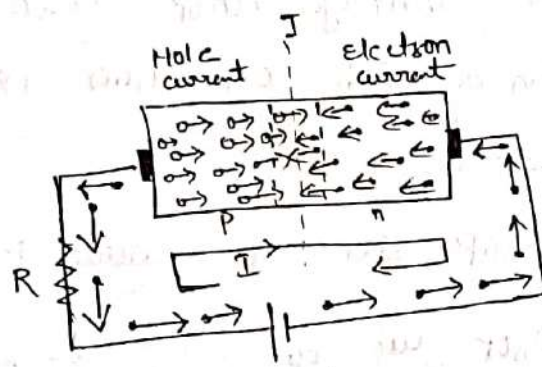
→ Then they move from hole to hole towards the positive terminal of the battery.

→ The movement of valence electrons is nothing but movement of holes in the opposite direction electrons. - in P-region.

→/ current in the P-region is the movement of holes which are majority carriers - called HOLE current.

→/ while the current in the n-region is the movement of free electrons which are majority carriers. This is the electron current.

* Hence the overall FORWARD current is due to the majority charge carriers.

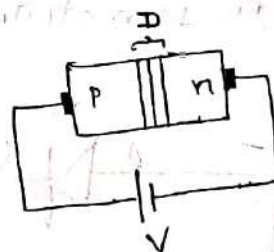
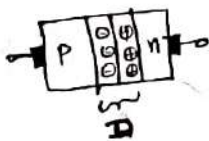


→ These majority carriers can then travel around the closed circuit and a relatively large current flows.

* The direction of the flow of electrons is opposite direction of the conventional current.

→ ~~the~~ forward biased voltage effect on the Depletion Region.

* Depletion Region narrows due to the FORWARD bias voltage.



→ The forward biasing voltage effect on the barrier potential.

* Due to the internal resistance, there is additional small voltage drop across the Diode.

Thus the total voltage drop across P-n junction diode in a F.b condition is V_f & it is made up of

- 1) Drop due to barrier potential
- 2) Drop due to internal resistance

$$\therefore V_f = V_B + I_f r_f$$

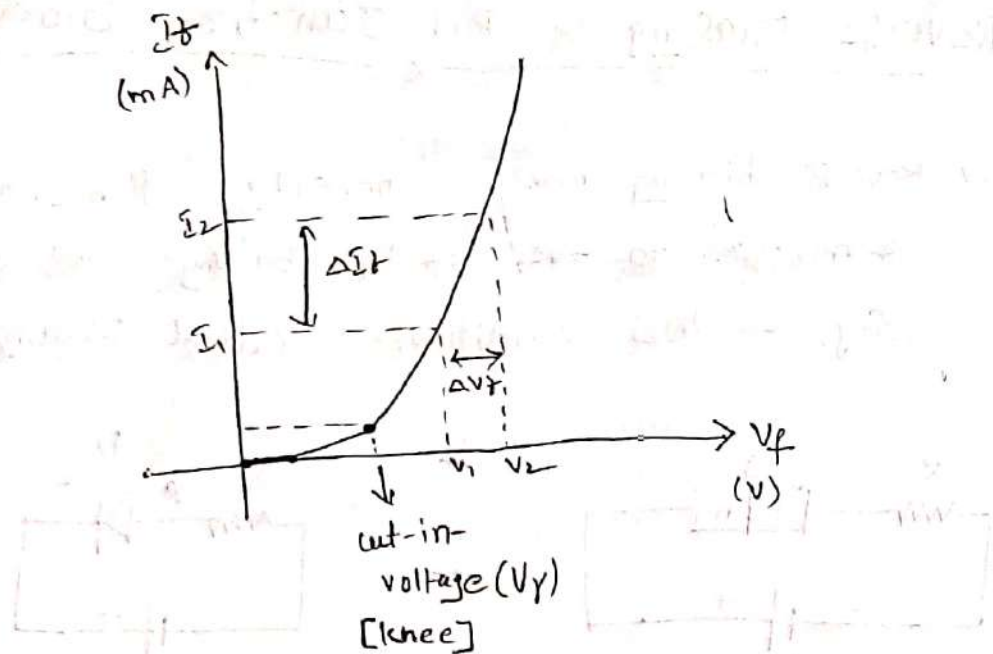
$\Rightarrow$ Total V_f is of the order of 0.7V for Si & 0.3V for Ge

Forward V-I characteristics of Diode:-

$\Rightarrow$ It is graph b/w the Applied voltage across the P-n junction & the flow of current through the P-n junction.



The graph of forward current I_f against the forward voltage V_f across the Diode is called forward characteristics of Diode.



→ Less than cut-in voltage, the current flow is very small, practically this current is assumed to be zero.

→ V_f increases towards V_f , the width of the depletion is reducing, it exceeds V_f then I_f increases suddenly in exponential as shown in above fig.

Resistance in forward bias:-

in 2 ways

→ static forward Resistance. $[R_f]$

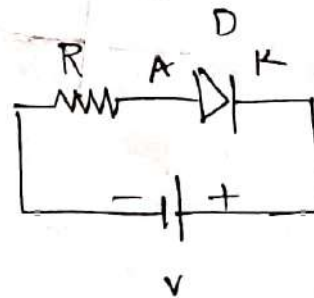
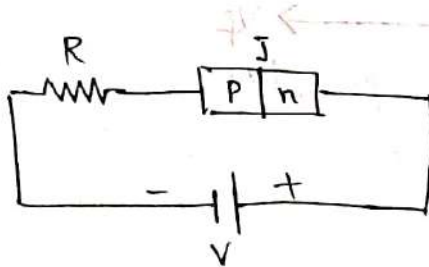
→ Dynamic forward Resistance. $[r_f]$

$$\therefore R_f = \frac{V_1}{I_1}$$

$$\therefore r_f = \frac{V_2 - V_1}{I_2 - I_1}$$

Reverse Biasing of P-N Junction Diode:-

* Reverse biasing means connecting P-region to -ve & n-region to +ve of the battery, as shown in fig. — this condition is called Reverse biasing.



operation:-

- The P-n junction is in reverse biased, the -ve terminal attracts the holes & +ve terminal attracts the electrons away from the junction.
- As electrons & holes both move away from the junction, the depletion region widens.
- creates the +ve ions in n-region & -ve ions in p-region.
- * Reverse biasing increase the width of the depletion region.
- As depletion region increases, barrier potential across the junction also increases.

→ The Reverse current flows due to minority charge carriers which are small in number. Hence reverse current is always very small.

→ The reverse current is ~~at~~ almost constant through reverse voltage is increased upto a certain limit. — it is called reverse saturation current & denoted as I_0 .

→ Reverse saturation current is very small, for Ge in mA & for Si in μA .

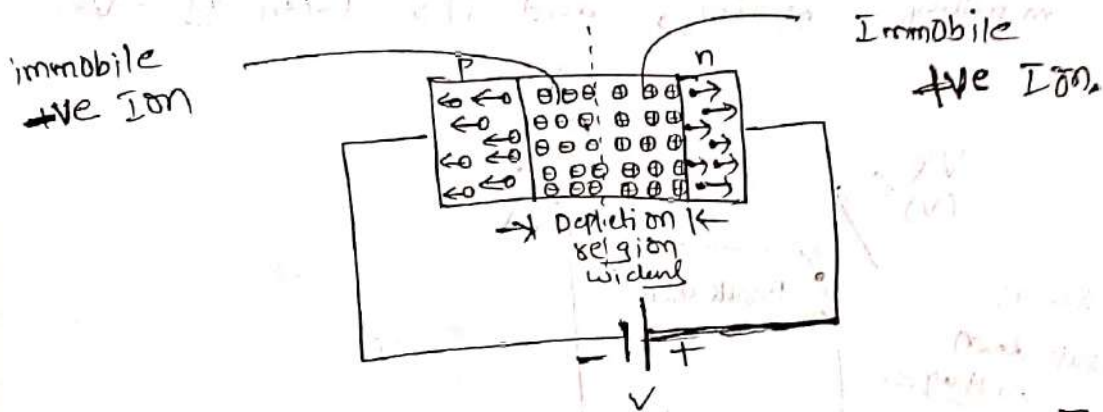


fig:- Depletion Region widens in R.B.

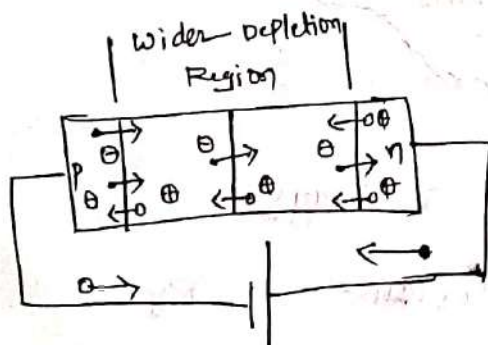


fig:- flow of minority charge carriers

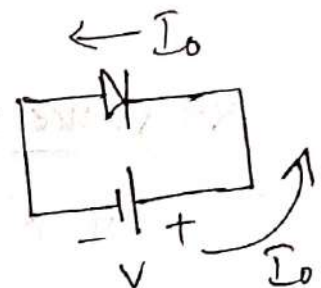
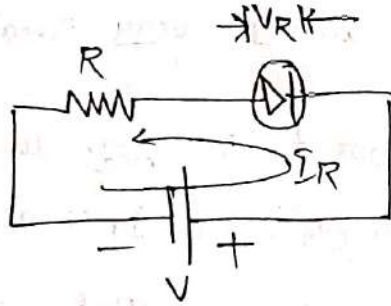


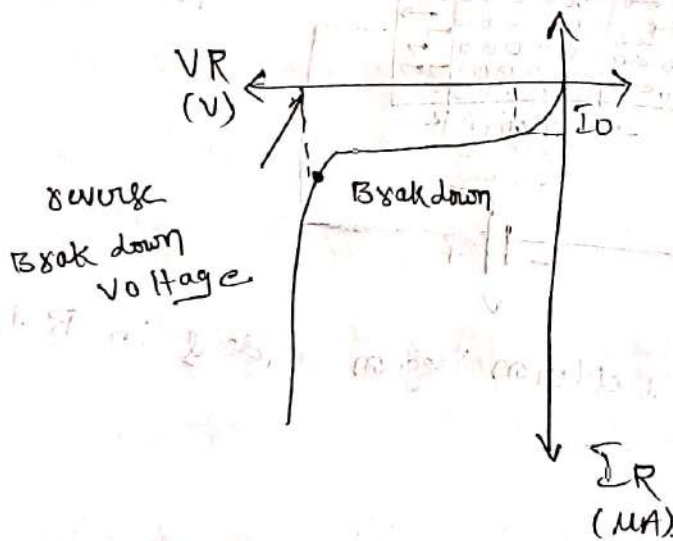
fig:- direction of Reverse current.

Reverse biased V-I characteristics of P-n :-



→ The graph of I_R against V_R is called Reverse characteristics of Diode.

→ The Reverse saturation current is due to minority carriers, and it's taken as -ve



Resistance :-

it is also defined in 2 ways

- Reverse Static resistance R_s
- Reverse Dynamic resistance r_s

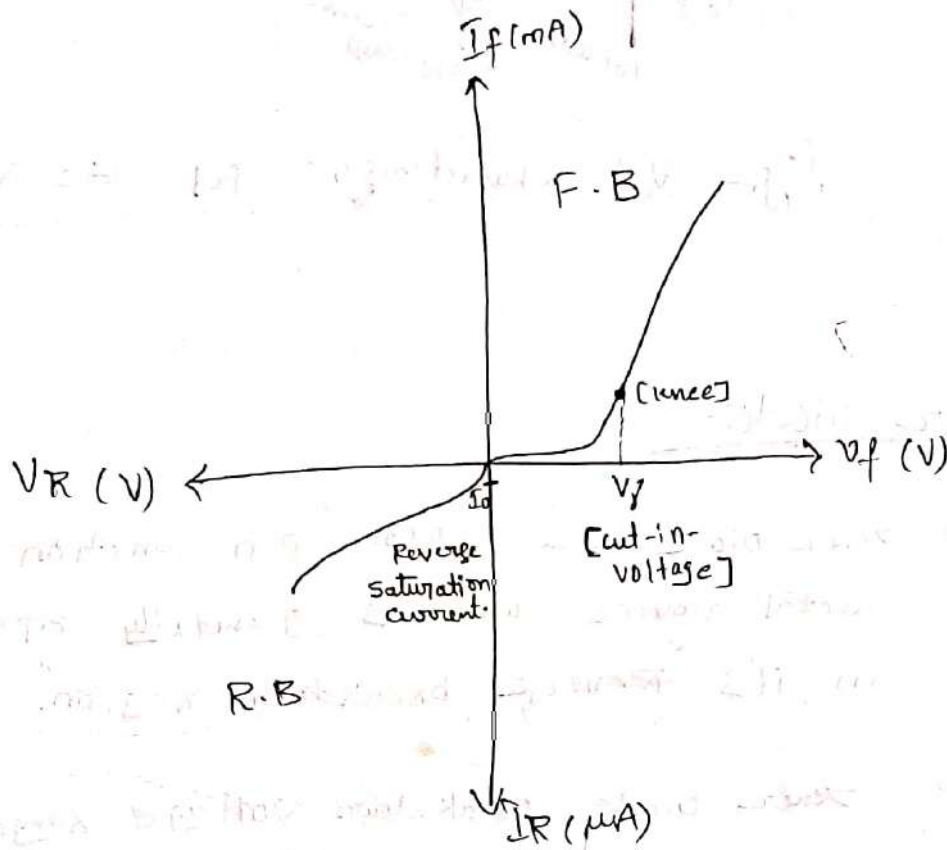
$$R_s = \frac{V_1}{I_1}$$

$$r_s = \frac{\Delta V_R}{\Delta I_R}$$

Complete V-I characteristics of Diode:-

→ The complete V-I characteristics of a Diode is the combination of its Forward as well as Reverse characteristics.

- shown in below fig.



→ Less than barrier potential, seen that initially forward current is small.

→ The voltage at which diode current starts increasing rapidly is called as cut-in-voltage is denoted by V_f .

V_f for Ge - 0.3V

Si - 0.7V

→ in Reverse biasing the Reverse saturation current is very small.

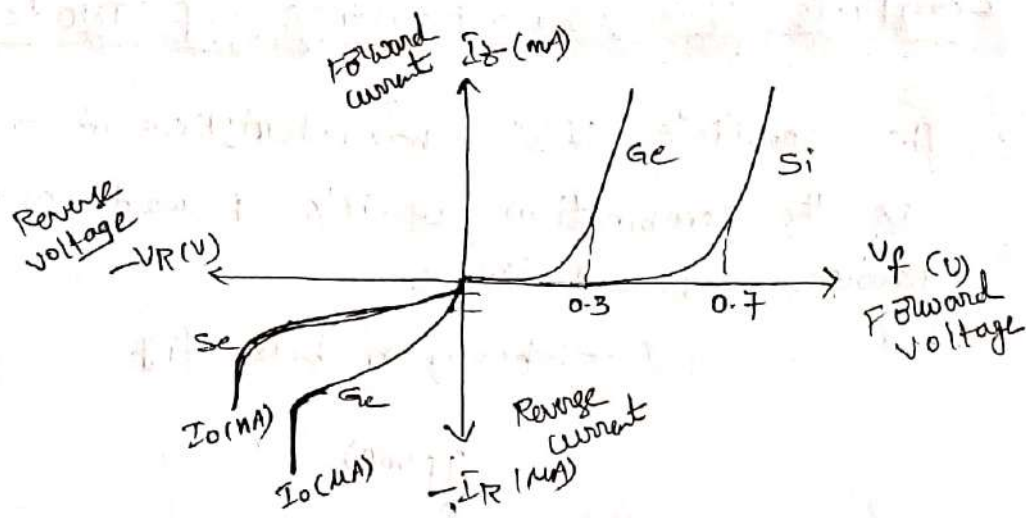
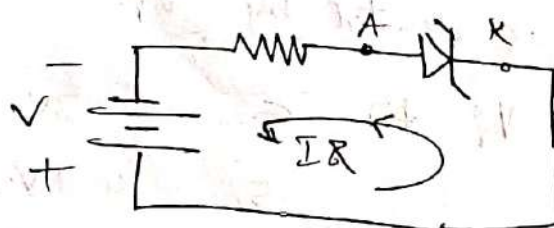
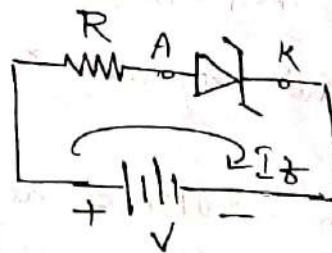
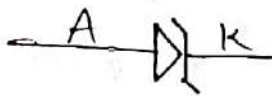


Fig. V-I characteristic for Ge & Si

Zener Diode:-

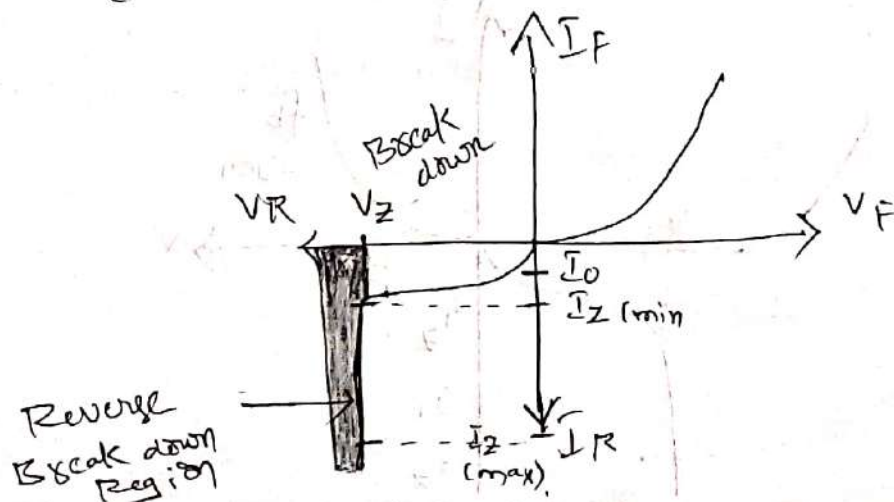
- Zener Diode is a Silicon p-n junction semiconductor device which is generally operated in its "Reverse breakdown region".
- Zener Diode breakdown voltage range B/w 3V to 200V.



- it is a special kind of Diode which permits current to flow in the F.D. as normal, but it also allows to flow in the R. direction. at certain voltage.

V-I characteristics of Zener Diode:-

- in forward condition, both normal P-n junction diode & Zener diode operation is same.
- But the Zener Diode is designed to be operated in the reverse biased condition.
- Reverse voltage applied to a Zener Diode is increased, initially the current through it is very small — it's called reverse leakage current (I_0).
- At a certain reverse voltage, current through Zener Diode increases rapidly.
- The change from low value to large value of current is very sharp — it's called "knee".
- At this knee, a breakdown is said to occur in the device, the reverse bias voltage at which the breakdown occurs is called Zener breakdown voltage (V_Z).



→ The voltage V_Z is set by carefully controlling the doping level during manufacturing process

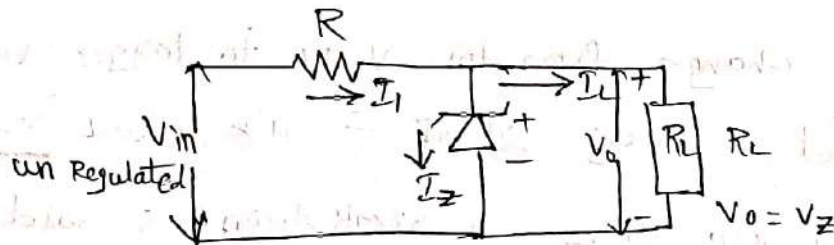
Application:-

→ AS a voltage regulating element in voltage regulators.

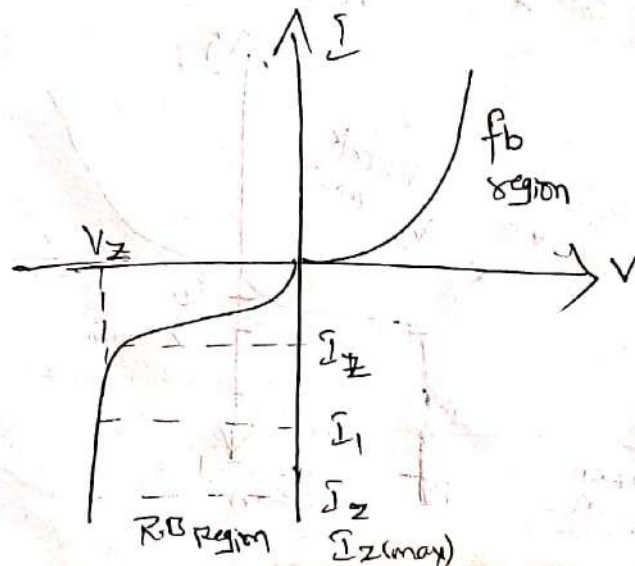
→ in various protection circuits

Zener Diode Regulator:-

→ voltage regulator circuit by using a Zener Diode - to Regulate the load Voltage



To understand working of circuit, we know the $V-I$ characteristics of Zener Diode.



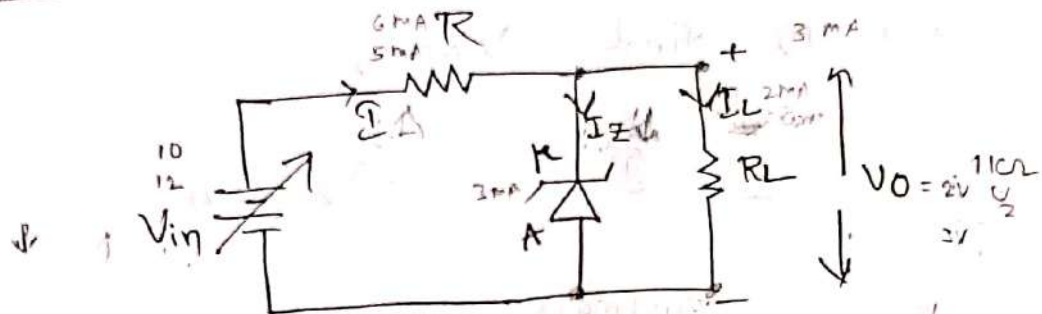
→ Zener Diode is used in Reverse biased region.

- In this Region current is very small in the order of few μA , up to certain limit.

→ After certain limit of voltage, large current flows through the Zener Diode. That voltage is called break down voltage (V_Z).

Regulation with Varying input voltage:-

I_{Zmin} & I_{Zmax}



Varying input condition.

→ it can be seen that the output is constant

$$V_o = V_Z$$

$$I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L}$$

$$I = I_Z + I_L$$

When V_{in} increases, then the total current I increases. But I_L is constant as V_Z is constant.

Steps

$$\rightarrow I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L}$$

$\rightarrow$ To find $V_{in}(\min)$, the current through Zener must be $I_{Z \min}$.

$$I = I_L + I_{Z \min}$$

$$V_{in}(\min) = V_Z + (I \times R)$$

$\rightarrow$ To find $V_{in}(\max)$

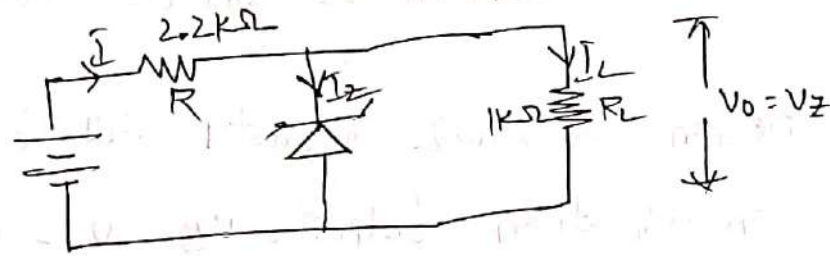
$$I = I_L + I_{Z(\max)}$$

$$V_{in}(\max) = V_Z + (I \times R)$$

The maximum power dissipation in the Zener diode is given by

$$P_D = V_Z I_{Z(\max)}$$

Prob:- for a zener regulator shown in the fig, calculate the range of i/p voltage for which o/p will remain constant



$$V_Z = 6.1 \text{ V}, \quad I_{Z\min} = 2.5 \text{ mA}, \quad I_{Z\max} = 25 \text{ mA}$$

$$r_Z = 0 \Omega$$

Sol:-

$$R_L = 1 \text{ k}\Omega, \quad V_Z = 6.1 \text{ V}$$

$$I_L = \frac{V_Z}{R_L} = \frac{6.1}{1 \times 10^3} = 6.1 \text{ mA} \quad \text{constant}$$

$$V_{in}(\min) \Rightarrow$$

$$I_Z = I_{Z(\min)} = 2.5 \text{ mA}$$

$$I = I_{Z(\min)} + I_L = 2.5 + 6.1 = 8.6 \text{ mA}$$

$$V_{in}(\min) = V_Z + IR$$

$$= 6.1 + 8.6 \times 10^{-3} \times 2.2 \times 10^3$$

$$= 25.02 \text{ V}$$

$$V_{in}(\max) \Rightarrow$$

$$I_Z = I_{Z(\max)} = 25 \text{ mA}$$

$$I = I_{Z(\max)} + I_L = 25 + 6.1 = 31.1 \text{ mA}$$

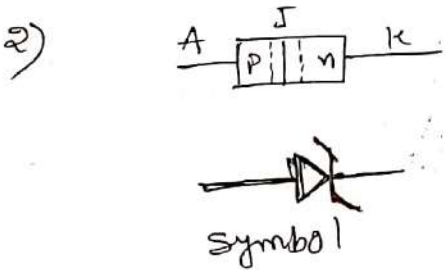
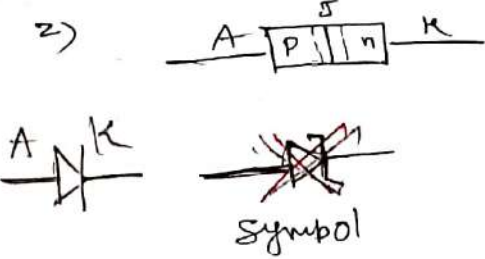
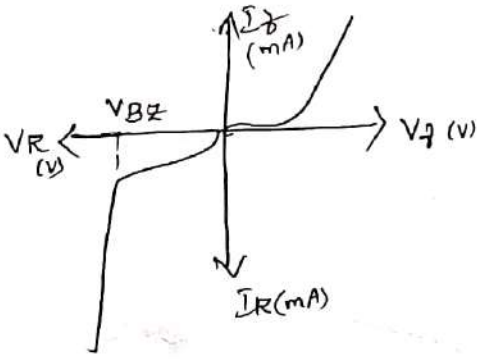
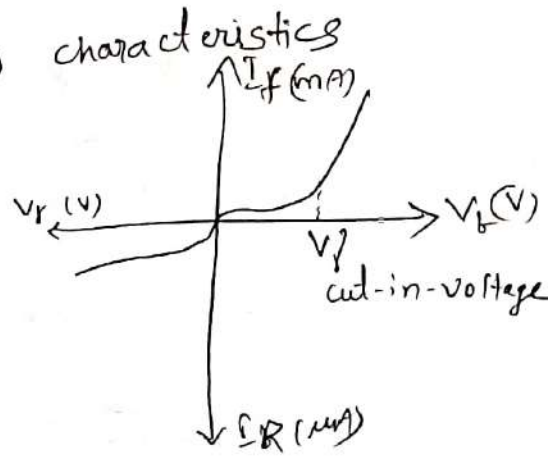
$$25.02 \text{ V}$$

$$24.52 \text{ V}$$

$$V_{in}(\max) = V_Z + IR =$$

$$= 6.1 + 31.1 \times 10^{-3} \times 2.2 \times 10^3 = 74.52 \text{ V}$$

Comparison of Zener Diode & P-n Junction Diode

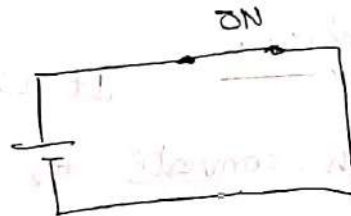
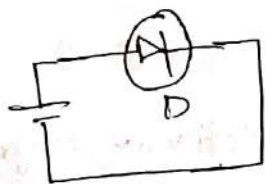
Zener Diode	P-n Junction Diode
1) operated in reverse break down condition, and forward condition also.	1) operated in Forward biased condition only.
2) 	2) 
3) characteristics 	3) characteristics 
4) Dynamic Zener resistance is very small in reverse break down condition.	4) The diode resistance in reverse biased condition is very high.
5) Power Dissipation capability is very high.	5) Power Dissipation capability is very low.
6) It is heavily doped device.	6) It is a lightly doped device.
7) Application - * Rectifier * Clipping * clamping.	7) Application - * voltage regulators. * protection circuits

Diode as Switch:-

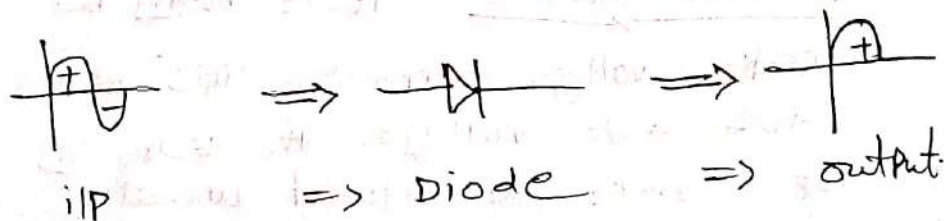
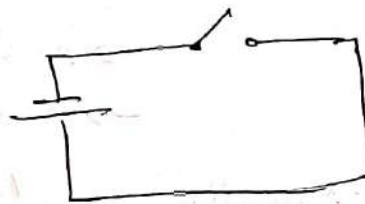
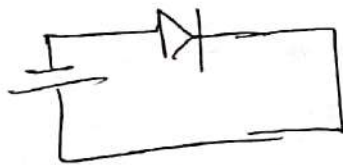
- The P-n Junction Diode act as a Switch. — Application of switch is ON & OFF.
- In the forward biased condition — the forward voltage Applied to the Diode.
- When we are Apply the voltage to the Diode it will goes to ON condition & it allows the forward current.



- ~~when~~ the below fig show the ON condition of Diode.



- When we are Apply the -ve voltage to the Diode, it will goes to OFF condition & it not allow the -ve current through Diode



Introduction:

* The most fundamental unit of all materials is an atom. An atom can be thought of as consisting of a central nucleus surrounded by orbiting electrons.

* It has been found that electrons can occupy only certain shells at fixed distances from the nucleus and each shell can contain only a particular number of electrons.

* Each electron has a negative electrical charge of $1.602 \times 10^{-19} \text{ C}$. The nucleus of an atom consists of two types of particles. They are protons and neutrons. The neutrons have no charge at all.

* The protons in the nucleus have the positive charge of same magnitude as that of electron i.e. $1.6 \times 10^{-19} \text{ Coulombs}$. Since the opposite charges attract, there exists a force of attraction between the electrons and the nucleus.

* For a given atom the number of protons and the number of orbiting electrons is same.

* Protons and neutrons each have the masses about 1800 times the mass of an electron.

* Because the protons and electrons in a given atom are equal in number and equal and opposite in charge they neutralize each other electrically. For this reason all atoms are normally electrically neutral.

* The process of losing or gaining an electron which converts an electrically neutral atom to a charged ion is called as "ionization".

* If an atom loses an electron, it has lost some negative charge. Hence it becomes positively charged and is referred to as a "positive ion". Similarly if an atom gains an additional electron it becomes negatively charged and is termed as a "negative ion".

* The number of protons in an atom is referred to as the "atomic number" of the atom. The "atomic weight" is approximately equal to the total number of protons and neutrons.

- in the nucleus of the atom. The atom of the semiconductor material silicon has 14 protons and 14 neutrons in the nucleus and also it has 14 electrons. Therefore the atomic number of silicon is 14 and the atomic weight is approximately 28.

* The electrons which are revolving around the nucleus are arranged in different orbits/shells at fixed distances from the nucleus. Each orbit contains a fixed number of electrons.

There are $2n^2$ electrons in each orbit.

Ex:- 1st orbit - $2(1)^2 = 2$

2nd orbit = $2(2)^2 = 8$

3rd orbit - $2(3)^2 = 18$ and so on.

* The electrons in the outermost shell determine the electrical characteristics of a particular type of atom. These electrons are usually referred to as "Valence Electrons". An atom may have its valance shell, completely filled or only partially filled.

Concept of Energy Level:

The closer an electron is to the nucleus, the stronger are the forces of attraction between the nucleus and electron. Each shell/orbit has an energy level associated with it that represents the amount of energy required to extract the electron from the atom. Farther an electron from the nucleus higher is the energy level.

The electrons in the valence shell are farthest from the nucleus, they require the least amount of energy to extract them. Similarly the electrons that are closest to the nucleus require greatest energy to extract them from the atom.

The energy levels of the orbiting electrons are measured in electron volts (eV). An electron volt is defined as the amount of energy required to move one electron through 1V potential difference.

$$1 \text{ eV} = 1.602 \times 10^{-19} \text{ Joules}$$

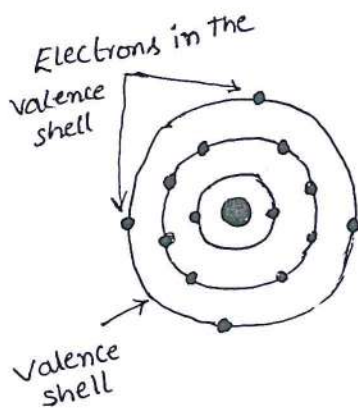


fig:- electrons in the valence shell.

When an atom absorbs energy from a heat source or from light due to high atmospheric temperature, the energy levels of the electrons are raised. If the electrons of valence shell gets adequate energy they are completely removed from the force of attraction of the nucleus. Such electrons are called as free electrons.

Free electrons are responsible for the flow of current. More the number of free electrons better is the conductivity.

Energy bands:

The electrons of an isolated atom are acted upon only by the forces within that atom. When atoms are brought closer together, the electrons come under the influence of forces from other atoms. Under these circumstances the energy levels that may be occupied by the electrons merge into bands of energy levels.

There are two distinct energy bands in which electrons may exist. They are valence band and conduction band. The energy gap that separates valence band and conduction band is known as forbidden gap, in which the electrons cannot exist normally.

Conduction band: It is a band of energy levels formed by merging all the energy levels of the free electrons.

Valence band: It is a band of energy levels formed by merging all the energy levels of the valence electrons.

Energy gap (or) Forbidden gap: It is the gap between the conduction band and valence band. Depending upon particular material the energy gap may be large, small or non-existent.

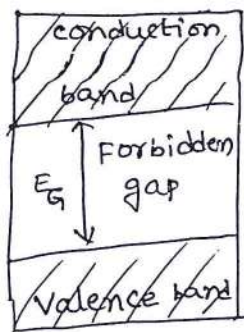


Fig:- Energy band diagram,

as shown in above fig.

To move the electrons present in the conduction band usually small amount of energy is sufficient where as to move the electrons present in the valence band relatively larger amount of energy is required. The energy band diagram is the graphical representation of -

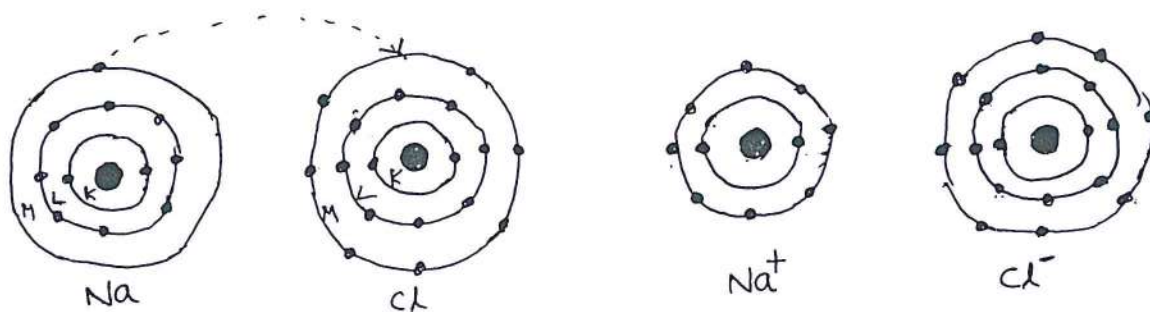
- the energy levels associated with electrons,

The forbidden gap is denoted by ' E_g '

Ionic bonding and Covalent bonding :

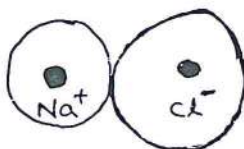
The crystals in which ionic bonding is involved are known as ionic crystals. In ionic crystals one or more electrons of one type of atom are transferred to another type of atom and the result being a crystal that is composed of positive and negative ions.

Ex:-



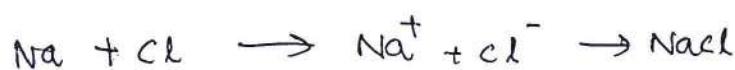
(a) Atoms

(b) Ions



(c) Ionic molecules

Sodium gives up its valence electron to the Chlorine atom. When Sodium atom loses one electron it becomes a positive ion and Chlorine atom gains one electron and becomes a negative ion. The two ions attract with each other, leads to the formation of the ionic bond between Na and Cl atoms.



The covalent bonds are formed by the shared electron pairs between the valence electrons of the neighbouring atoms.

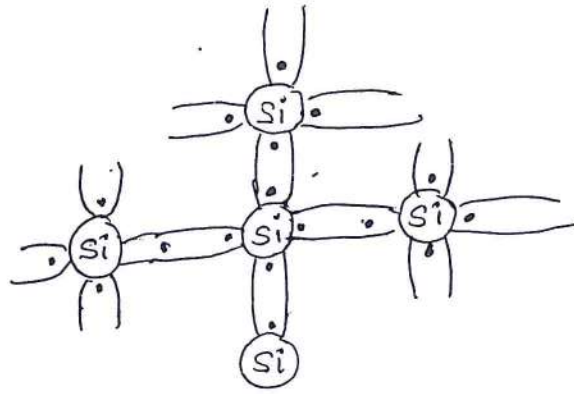


fig: Covalent bonding

Classification of Solidstate material:

The solidstate material can be classified into 3 types.

- 1) Conductors 2) Insulators 3) Semiconductors.

1) Conductors:

A conductor is a material which easily allows the flow of electric current. The examples for the best conductors are Copper, Silver, gold and aluminium.

For conductors the valence band and conduction band overlaps with each other and there is no forbidden gap.

For conductors the conductivity is very high, and the value of resistivity is very low.

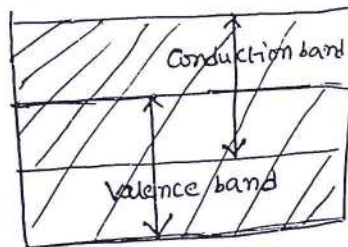


Fig:- Energy band diagram of a conductor.

2) Insulators:

An insulator is a material that does not allow the flow of electric current through it. In these materials the valence electrons are tightly bound to the atoms. A large -

forbidden region is present in between the Valence band and Conduction band. Hence a very high electric field is required (approximately 6 eV) to make the electrons to go from Valence band to Conduction band.

In insulators the Valence band is full and Conduction band is empty.

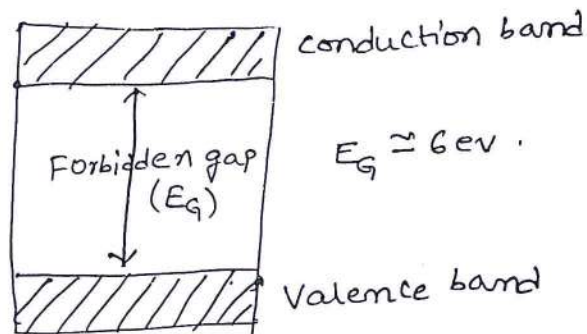


fig:- Energy band diagram of an insulator.

Examples for insulators are diamond, rubber etc.

3) semiconductors :

A semiconductor is a material which has electrical - conductivity that lies between conductors and insulators. A semiconductor in its pure form is neither a good conductor, nor a good insulator.

The most commonly used semiconductors are silicon and Germanium.

The forbidden energy gap is relatively small ($\approx 1 \text{ eV}$). Si has the energy gap of 1.2 eV and Ge has 0.785 eV at 0°K .

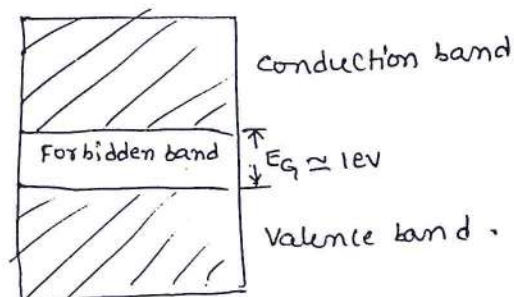


fig:- Energy band diagram of a Semiconductor.

As the temperature is increased some of the valence electrons acquire thermal energy greater than E_g and move to conduction band.

Classification of Semiconductors:

Semiconductors are classified into two types. They are

- i) Intrinsic (pure) semiconductor
- ii) Extrinsic (Impure) semiconductor.

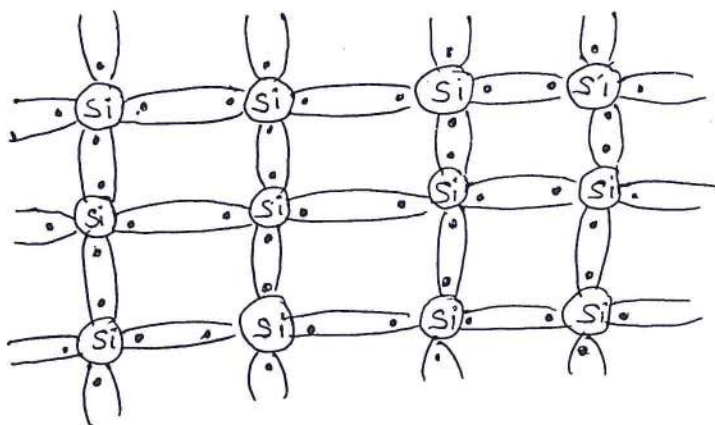
Intrinsic Semiconductor:

The pure form of semiconductor material is known as intrinsic semiconductor. Examples are 100% pure germanium and silicon.

At 0°K the intrinsic semiconductor behaves as an insulator, since no free electrons are available.

Even at room temperature 27°C (i.e. 300K), some of the valence electrons may acquire sufficient energy to enter the conduction band to form free electrons. Under the influence of electric field, these electrons constitute electric current.

A missing electron in the valence band leaves a vacant space there, which is known as a "hole". A combination of such a free electron and hole is referred to as "electron hole pair".



Ex:- Two dimensional representation of Silicon crystal.

At room temperature of 27°C (i.e. 300K), the number of valence electrons absorb the thermal energy, due to which they break the covalent bond and drift to the conduction band.

Once the electrons are dislodged from the covalent bonds, then they become free. Such free electrons wander in a random fashion in the crystal.

The energy required to break a covalent bond for Ge atom is 0.72 eV and for Si atom it is 1.21 eV at room temperature.

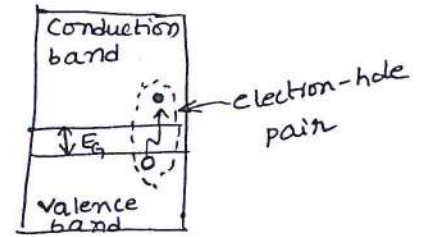
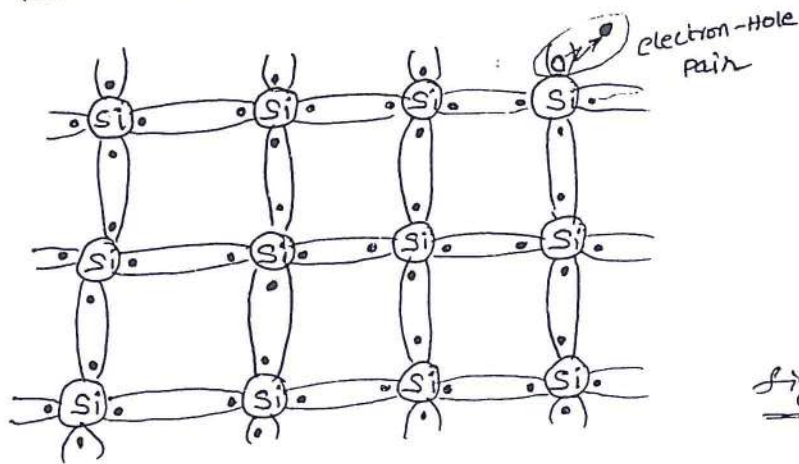


fig: Energy band diagram

fig: Electron-hole pair formation in a silicon crystal

Concentration of free electrons and holes always equal in the intrinsic semiconductors.

Conductivity in intrinsic semiconductor :-

In intrinsic semiconductors the conductivity is due to both electrons and holes.

The mechanism by which a hole contributes to the conductivity is as follows: when a bond is incomplete there exist a hole. There is tendency for a valence electron of the neighbouring atom to leave it's covalent bond to fill this hole. An electron moving from a bond to fill a hole leaves a hole in it's position. Hence the hole effectively moves in the direction opposite to that of the electron.

occasionally a free electron approaches a hole and falls into it. This merging of a free electron and a hole is called recombination.

After recombination the electron-hole pair gets disappeared.

Due to recombination the number of charge carriers gets decreased.

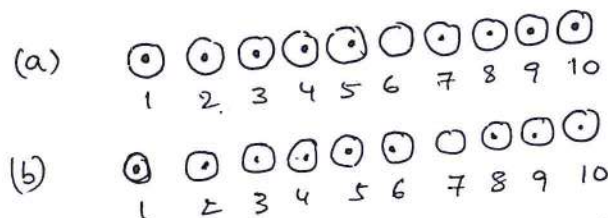


fig:- mechanism by which hole contributes to the conductivity.

In the above figure, a circle with a dot represents complete covalent bond and an empty circle represents a hole (incomplete covalent bond). Figure (a) shows a row of 10 ions with a hole at ion 6. Now imagine that an electron from ion 7 moves into the hole at ion 6, by leaving a hole at ion 7. Comparing fig (a) and figure (b) we can say that the movement of hole in one direction means the movement of electron in the opposite direction. Therefore the conductivity in intrinsic semiconductor is due to both holes and electrons.

Fermi Level in an intrinsic semiconductor: In an intrinsic semiconductor - is at room temperature the maximum energy level occupied by an electron is at the middle of the forbidden energy gap, it is known as "Fermi Level" of that intrinsic semiconductor.
$$E_F = \frac{E_C + E_V}{2}$$

Mean Lifetime of a Charge Carrier:

The amount of time between the creation and disappearance of a free electron or a hole is called the "mean Lifetime" of the charge carrier.

EXTRINSIC SEMICONDUCTORS: (IMPURE SEMICONDUCTORS)

As pure intrinsic semiconductor has poor conductivity, some impurity is added to it to increase the conductivity. Such impure semiconductors are called as extrinsic semiconductors.

The process of adding some impurity to an intrinsic semiconductor to improve its conductivity is called as "Doping" and - the impurity added is called 'Dopant'.

The amount of impurity added is extremely small, say 1 to 2 atoms for 10^6 intrinsic atoms.

The impurity having five valence electrons is called Pentavalent impurity. When pentavalent impurities are added, each atom donate one free electron and hence pentavalent impurities are also called as donor atoms. The examples for pentavalent impurities are Phosphorous, arsenic, bismuth.

The impurities having three valence electrons are called as Trivalent impurities. When trivalent impurities are added, each atom creates one hole which is ready to accept an electron and hence trivalent impurities are also called as acceptor atoms.

There are two types of extrinsic semiconductors. They are

1. N-type semiconductor
2. P-type semiconductor.

When a pentavalent impurity is added to intrinsic semiconductor, n-type semiconductor is obtained. While when trivalent impurity is added to intrinsic semiconductor, p-type semiconductor is obtained.

N-Type Semiconductor:

A small amount of pentavalent impurities such as Arsenic, antimony or phosphorous is added to an intrinsic semiconductor to get an N-type semiconductor.

Germanium atom has four valence electrons and antimony (Sb) has five valence electrons. Each antimony atom can form a covalent bond with ~~the~~ surrounding four germanium atoms. Thus four valence electrons of antimony atom form covalent bond with four valence electrons of individual germanium atom and fifth valence electron is loosely bound to the antimony atom and hence it enters the conduction band to become free electron.

Thus every antimony atom contributes (or donates) one electron,

such pentavalent impurities are also called as donor impurities.

Because the free electrons have negative charges, the donor doped semiconductor is also known as N-type material.

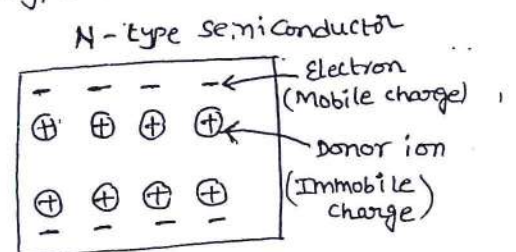
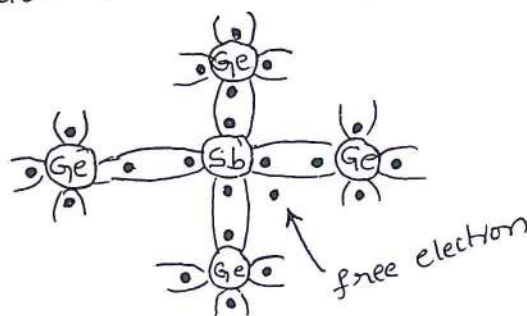


fig: Charged carriers.

fig: formation of covalent bonds in n-type semiconductor

P-TYPE semiconductor:

A small amount of trivalent impurities such as aluminium or boron is added to the intrinsic semiconductor to get p-type semiconductor.

Germanium (Ge) has four valence electrons and Boron (B) has three valence electrons as shown in below figure. The three valence electrons in boron atom form covalent bond with four surrounding atoms of Ge leaving one bond incomplete which gives rise to a hole.

Thus trivalent impurity (boron) when added to the intrinsic semiconductor (Germanium) introduces a large number of holes in the valence band. These positively charged holes increase the conductivity of p-type semiconductor.

Trivalent impurities such as boron is called acceptor impurity because it accepts free electrons in the place of holes.

As each boron atom donates a hole for conduction it becomes a negatively charged ion. As the number of holes is very much greater than the number of free electrons in a p-type material the holes are termed as majority charge carriers and electrons as minority charge carriers.

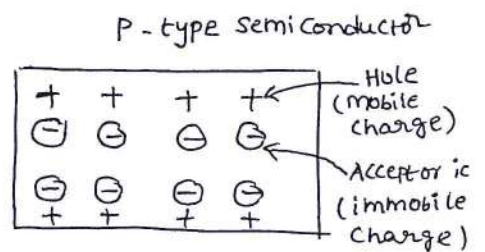
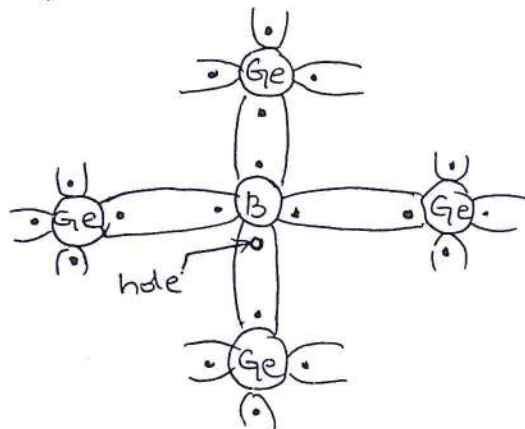


fig: Charge carriers

fig:- p-type semiconductor: formation of covalent bond

In p-type material holes are mobile charges and acceptor ions are immobile charges. Since holes have positive charge, the acceptor-doped semiconductor is named as p-type semiconductor.

Conductivity of Semiconductor:

In a pure semiconductor the number of holes is equal to the number of free electrons. In each electron hole pair, there are two charge carrying particles. one is negatively charged free-electron with mobility μ_n and the other is positively charged hole with mobility μ_p . These particles move in opposite direction to each other under the electric field 'E'.

Thus, in a pure semiconductor the total current density is the sum of the current density due to free electrons and current density due to holes.

$$J = J_n + J_p$$

$$\Rightarrow J = q n \mu_n E + q p \mu_p E$$

$$\Rightarrow J = (n \mu_n + p \mu_p) q E$$

$$\Rightarrow \boxed{J = \sigma E}$$

where $\sigma = (n \mu_n + p \mu_p) \cdot q$ = The conductivity of semiconductor

n = The number of electrons per unit-volume i.e. concentration of free electrons

p = The number of holes per unit-volume i.e. concentration of holes.

The resistivity of semiconductor is the reciprocal of the conductivity (σ) which is given by

$$\text{resistivity } \rho = \frac{1}{\sigma}$$

In an intrinsic semi-conductor $n = p = n_i$, where n_i is the intrinsic carrier concentration.

$$\therefore J = n_i (\mu_n + \mu_p) q E$$

Conductivity of an N-type semiconductor:

The conductivity of an intrinsic semiconductor is

$$\sigma_i = q \cdot n_i (\mu_n + \mu_p) = q (\eta \mu_n + p \mu_p) \quad \dots \quad (1)$$

For n-type semiconductor as $n \gg p$, the conductivity is

$$\boxed{\sigma_n = q n \mu_n}$$

In n-type material $n \approx N_D$, where N_D = Concentration of donor atoms.

$$\therefore \boxed{\sigma_n = N_D \mu_n q}$$

For p-type semiconductor as $p \gg n$, the conductivity is

$$\boxed{\sigma_p = q p \mu_p}$$

In p-type material $p \approx N_A$, where N_A = Concentration of acceptor atoms

$$\therefore \boxed{\sigma_p = N_A \mu_p q}$$

Mass action law:

If 'n' is the concentration of free electrons and 'p' is the concentration of holes, then the law of mass action states that

"The product of concentrations of electrons and holes is always constant at a fixed temperature".

$$\boxed{n \cdot p = n_i^2} \quad \text{where } n_i = \text{intrinsic concentration}$$

At a fixed temperature, the intrinsic concentration is also fixed. Hence the product of concentrations of electrons and holes is constant, irrespective of the amount of donor (or) acceptor impurity.

For 'n' type material $n = n_n$ and $p = p_n$, hence law can be stated as $n_n p_n = n_i^2$

For 'p' type material $n = n_p$, $p = p_p$ hence $n_p \cdot p_p = n_i^2$

Drift Current and Diffusion Current: Drift Current:-

When an electric field is applied across the semiconductor material, the holes move towards the negative terminal of the battery and electrons move towards the positive terminal. This combined effect of movement of the charge carriers constitutes a current known as drift current.

Thus the drift current is defined as the flow of electric current due to the motion of the charge carriers under the influence of an external electric field.

When an electric field is applied across the semiconductor material, the velocity attained by the charge carriers is known as drift velocity (v_d).

The current density due to drift current in an n-type material is $J_n = q n \mu_n E$ A/cm²

For p-type material it is $J_p = q p \mu_p E$ A/cm².

Diffusion Current:

In a semiconductor material, the charge carriers have the tendency to move from the region of higher concentration to that of lower concentration of the same type of charge carriers. Thus the movement of charge carriers takes place resulting in a current called diffusion current.

The diffusion current density due to holes is given by

$$J_p = -q D_p \frac{dp}{dx} \text{ A/cm}^2$$

The diffusion current density due to electrons is given by

$$J_n = +q D_n \frac{dn}{dx} \text{ A/cm}^2$$

where D_n and D_p are diffusion coefficients of electrons and holes respectively. $\frac{dp}{dx}$ and $\frac{dn}{dx}$ are concentration gradients of holes and electrons.

$\therefore$ The total current density due to both drift current and

diffusion current in a p-type semiconductor is given by

$$J_p = q p \mu_p E - q D_p \frac{dp}{dx}$$

lly In an n-type semiconductor it is given by

$$J_n = q n \mu_n E + q D_n \frac{dn}{dx}$$

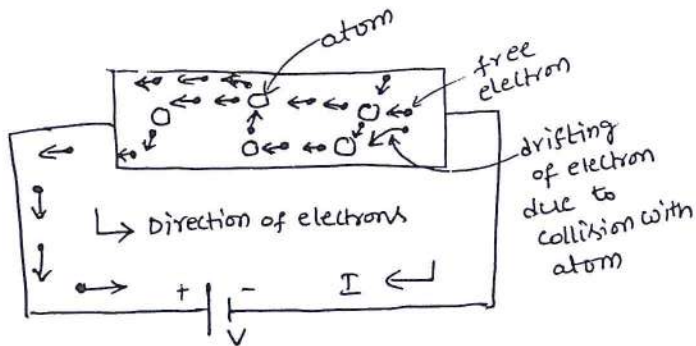


fig:- Drift mechanism causing - drift current

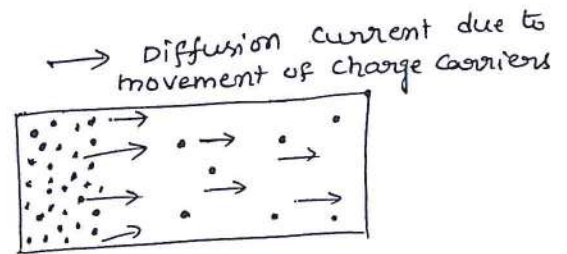
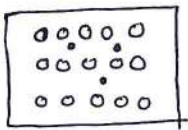


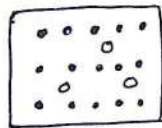
fig:- Diffusion process causing diffusion current

Open Circuited PN Junction (or) Qualitative theory of PN Junction:

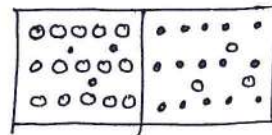
* If donor impurities are introduced into one side and acceptors into the other side of a semiconductor crystal, a PN Junction is formed.
(or) A junction that is formed when a sample of p-type semiconductor and a sample of n-type semiconductor joined together is called as PN Junction.



a) p-type semiconductor



b) n-type semiconductor



c) P-N Junction.

* At the junction there is a tendency for the free electrons to move towards p-side and holes towards the n-side. This process is known as diffusion. The diffusion is the process by which the charge carriers move from high concentration area to low concentration area. The current due to diffusion is known as diffusion current.

* When the free electrons diffusing from 'n'-side into 'p'-side, they recombine with the holes and leave negatively charged immobile ions near the junction of p-side.

* Similarly the holes diffusing from p-side into n-side they

recombine with the electrons and leaves positively charged immobile ions near the junction of n-side.

* After a certain extent the immobile positive ions near the junction, that are present in n-side prevents further charge carrier diffusion from p-region into n-region. Similarly the immobile negative ions near the junction, that are present in p-side prevents the further charge carrier diffusion from n-region into p-region. These immobile ions forms a region known as depletion region.

* Since the region of the junction is depleted of mobile charge carriers it is called as depletion region (or) space charge region (or) transition region (or) charge free region.

* The existence of these immobile ions develops the potential difference across the junction, this potential acts as a barrier for further conduction between the junction. Thus this potential is known as barrier potential (or) cut in voltage of semiconductor diode (or) junction potential (or) built-in potential barrier.

The potential barrier for germanium diodes is 0.3V and for silicon diodes it is 0.7V.

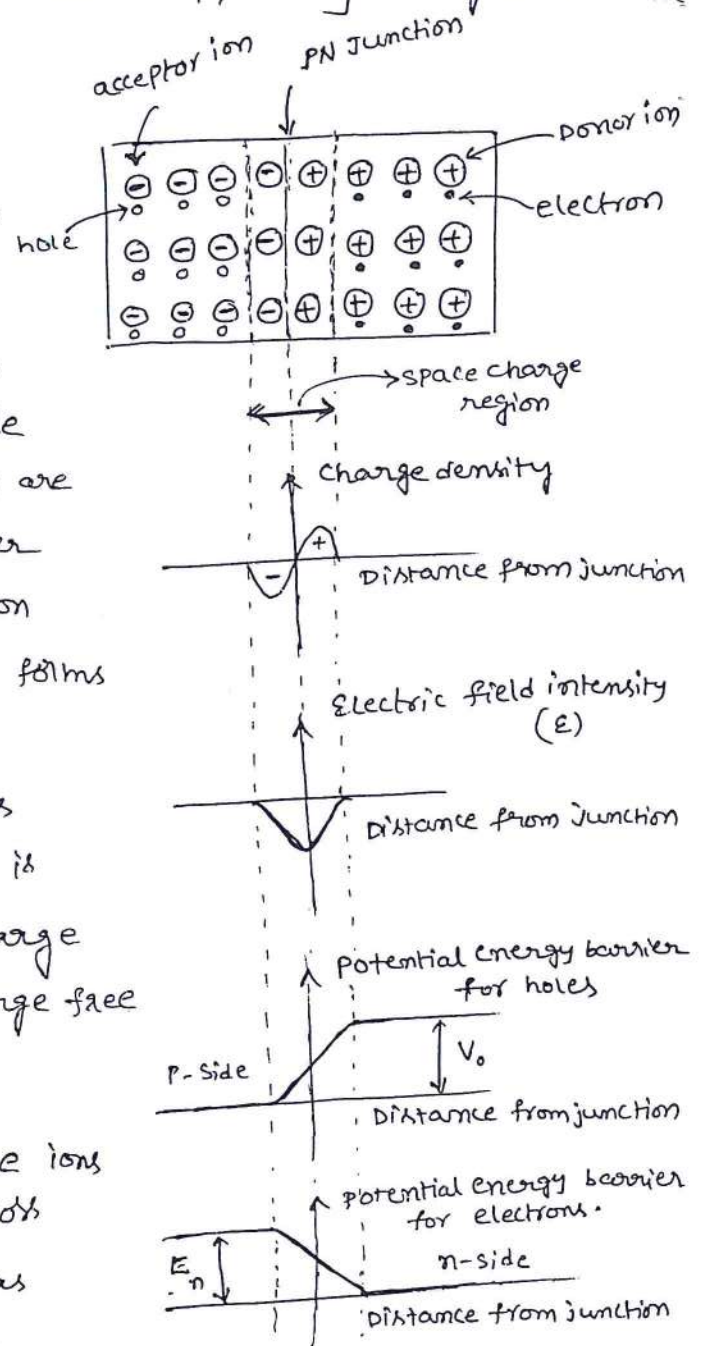


fig: Schematic diagram of open circuited PN Junction, including charge density, electric field intensity and potential energy barriers for holes & electrons.

ENERGY BAND DIAGRAM OF AN OPEN CIRCUITED PN JUNCTION DIODE;

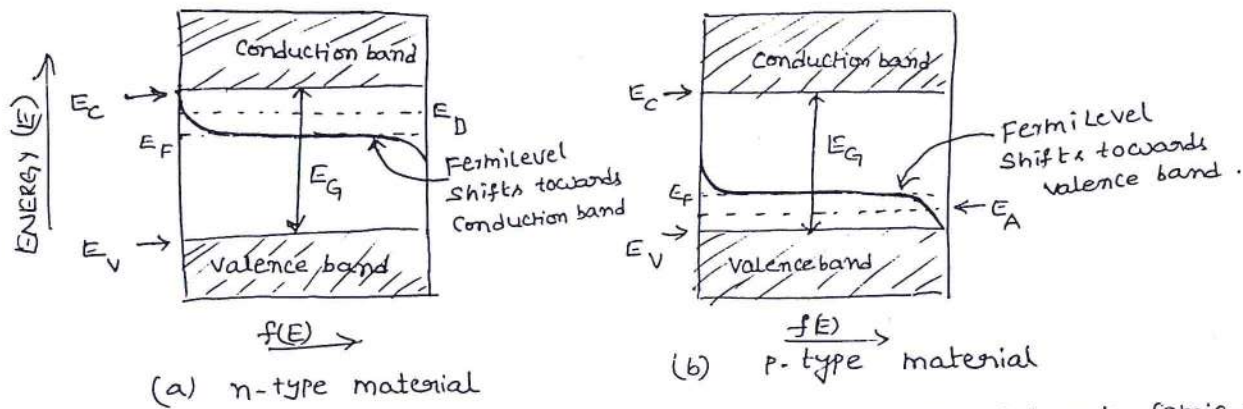


fig:- Energy band diagrams of Extrinsic Semiconductors.

The Fermi level Energy (E_F) depends on the temperature and the Concentration of impurity atoms. In case of no impurities (i.e. in intrinsic semiconductor) the E_F lies in the middle of the energy gap, indicating equal concentrations of free electrons and holes.

In n-type material the Fermi level is nearer to the conduction band and in p-type material it is nearer to the valence band.

Calculation of exact position of Fermi level in an n-type semiconductor material is given by

$$N_D = N_C e^{-(E_C - E_F)/kT}$$

solving for E_F we get

$$E_F = E_C - kT \ln\left(\frac{N_C}{N_D}\right)$$

Similarly for p-type material $N_A = N_V \cdot e^{(E_F - E_V)/kT}$

$$\text{solving for } E_F \text{ we get } E_F = E_V + kT \ln\left(\frac{N_V}{N_A}\right)$$

where k = Boltzmann Constant, T = Temperature in $^{\circ}K$; N_C = Concentration of electrons in conduction band, N_V = Concentration of electrons in valence band, N_D = concentration of donor atoms, N_A = Concentration of acceptor atoms.

A P-N Junction is formed by placing a P-type material and an n-type material closely together, having a contact between them.

When the P-N Junction is formed, the energy levels of P-region and the energy levels of n-region undergo relative shift to make the Fermi level constant throughout the specimen.

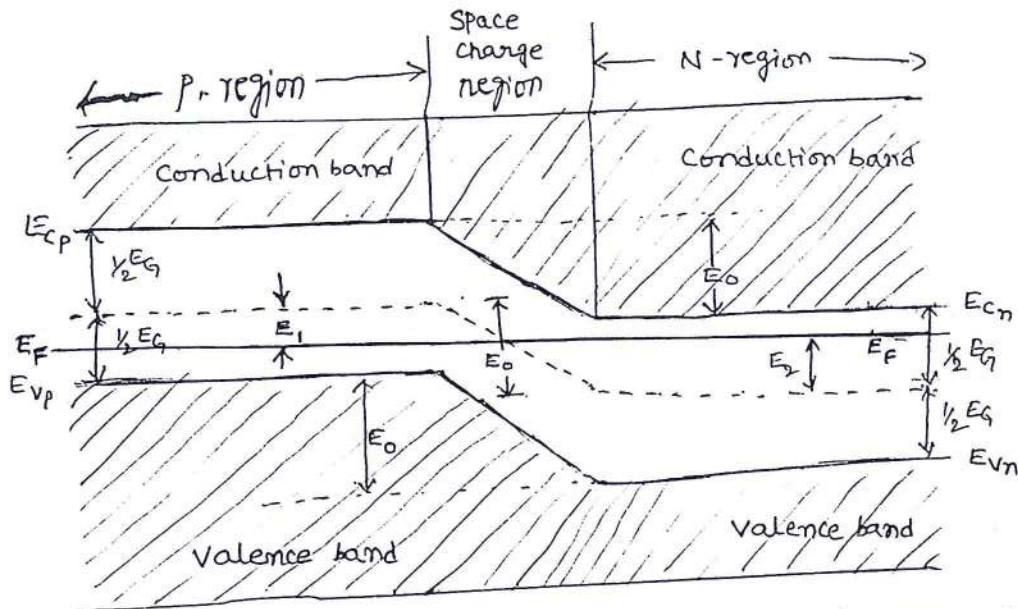


fig: Energy band diagram for open circuited PN Junction diode.

The shift in the energy levels E_p is given by

$$E_0 = E_{cP} - E_{cN} = E_{vP} - E_{vN} = E_1 + E_2 \rightarrow (1)$$

where E_{vP} , E_{cP} are edges of valence band and conduction band of p-type material and E_{vN} , E_{cN} are the edges of valence band and conduction band of n-type material respectively.

From the figure $E_F - E_{vP} = \frac{1}{2} E_g - E_1 \rightarrow (2)$

$$E_{cN} - E_F = \frac{1}{2} E_g - E_2 \rightarrow (3)$$

Adding (2), (3) we get $E_0 = E_1 + E_2 = E_g - (E_{cN} - E_F) - (E_F - E_{vP}) \rightarrow (4)$

we know that $E_g = KT \ln \left(\frac{N_c N_v}{n_i^2} \right) \rightarrow (5)$

$$E_{cN} - E_F = KT \ln \left(\frac{N_c}{N_D} \right) \rightarrow (6)$$

$$E_F - E_{vN} = KT \ln \left(\frac{N_v}{N_A} \right) \rightarrow (7)$$

substituting eq (5), (6), and (7) in eq (4) we get

$$E_0 = KT \ln \left(\frac{N_c N_v}{n_i^2} \right) - KT \ln \left(\frac{N_c}{N_D} \right) - KT \ln \left(\frac{N_v}{N_A} \right)$$

$$E_0 = KT \ln \left(\frac{N_c N_v}{n_i^2} \times \frac{N_D}{N_c} \times \frac{N_A}{N_v} \right)$$

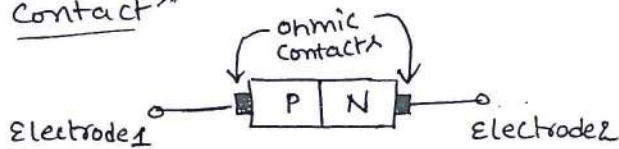
$$\therefore E_0 = KT \ln \left(\frac{N_D N_A}{n_i^2} \right)$$

PN Junction Diode:

* The P-N Junction forms a popular semiconductor device called P-N Junction diode.

* The P-N Junction has two terminals called electrodes, one is anode (from P-region) and the other is Cathode (N-region). Since there are two electrodes it is called as a diode (i.e. di-electric).

* To connect the n and P-regions to the external terminals a metal contact is applied to the n-region as well as P-region. Such a contact between a metal and the semiconductor is called "Ohmic Contact".



* The following figure shows the symbol of a diode

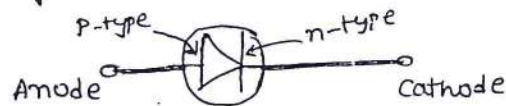


fig: symbol of a diode.

Biased P-N Junction Diode:

Applying external d.c voltage to any electronic device is called biasing.

Depending upon the polarity of DC voltage externally applied to PN-Junction, the biasing is classified as forward biasing and reverse biasing.

(i) Forward biasing of PN Junction diode:

* When an external dc voltage is connected in such a way that the P-region of a diode is connected to positive and the n-region to negative of the dc voltage, then the biasing is called as "forward biasing". It is shown in below fig

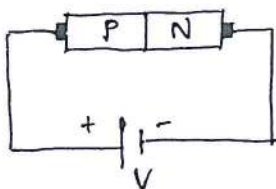


fig: Forward biasing

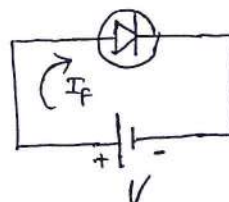


fig: Symbolic representation

I_F = forward current

The negative terminal of the battery pushes the free electrons against the barrier from n-region to p-region, while the positive terminal of the battery pushes holes against the barrier from p-region to n-region.

As the applied bias voltage is increased from zero, the width of the depletion region reduces and consequently the barrier potential also reduces. As the bias voltage is progressively increased, at a particular value, the depletion region becomes very narrow and hence the majority carriers from either sides of the junction can easily cross the junction. This large number of majority carriers constitute a current called forward current.

The current in the p-region is due to movement of holes, so it is hole current. The current in the n-region is due to the movement of electrons, so it is electron current. The majority carriers in p-region and in n-region are holes and electrons respectively.

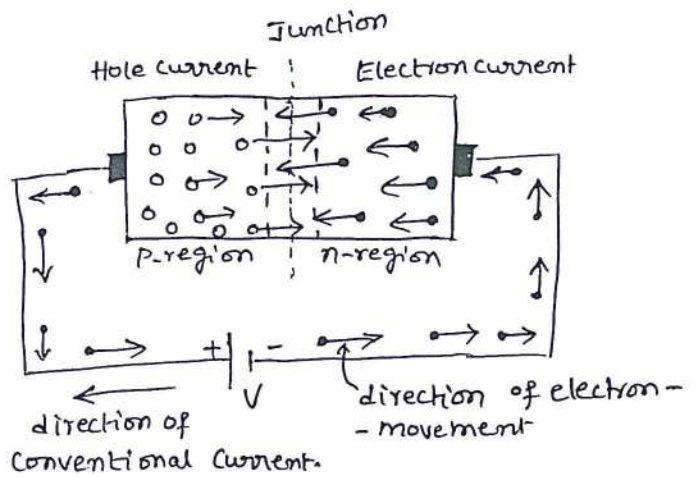


fig:- forward current in a diode

NOTE:

1. The effect on the depletion region in forward bias condition - The depletion region gets narrowed due to its forward bias voltage.

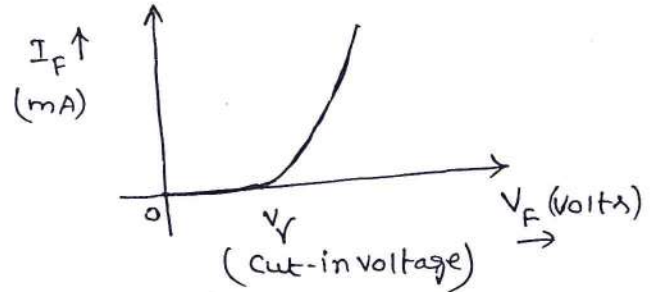
2. The total voltage drop across the PN junction diode in forward biased condition is the sum of the drop due to barrier potential and the drop due to internal resistance.

$$V_f = V_Y + I_f r_f ; \quad \begin{array}{l} \text{where } r_f = \text{forward resistance} \\ V_Y = \text{barrier potential} \\ I_f = \text{forward current} \end{array}$$

V-I characteristics in forward bias:

In forward bias of a PN Junction, on varying the forward voltage slowly, at some forward voltage the potential barrier is eliminated completely and current starts flowing. This voltage is known as cut-in voltage (or) threshold voltage (or) knee voltage, denoted by ' V_r '. Practically It is same as the barrier voltage. For $V_F < V_r$ the current flow is very negligible.

When forward voltage (V_F) is increased beyond ' V_r ', i.e. when $V_F > V_r$, the forward current I_F increases very rapidly.



The above figure shows the V-I characteristics of forward biased PN junction diode.

(2) Reverse biasing of a PN Junction diode:

When an external D.C. voltage is connected in such a way that P-region is connected to negative terminal and n-region is connected to positive terminal of the d.c. voltage, then the biasing is called "reverse biasing". It is shown in below figure.

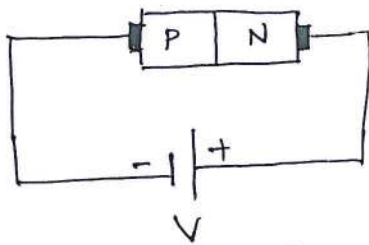
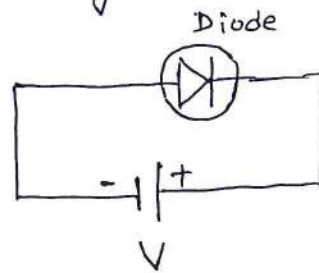


fig (a): Reverse biasing



fig(b): Symbolic representation.

In reverse biasing, negative terminal of the battery attracts the holes in P-region and the positive terminal attracts the electrons in n-region away from the junction. This causes the depletion region to become wider due to which the barrier potential gets increased. No majority charge carriers can cross the junction.

The free electrons on P-side are dragged towards the positive terminal and holes on n-side are dragged towards the negative terminal of the battery. This constitutes a current called as "reverse current". Since it flows due to the minority charge carriers, its magnitude is very very small. It is denoted by ' I_R '.

The reverse current ' I_R ' is of the order of few μA for Ge and few nA for Si diodes.

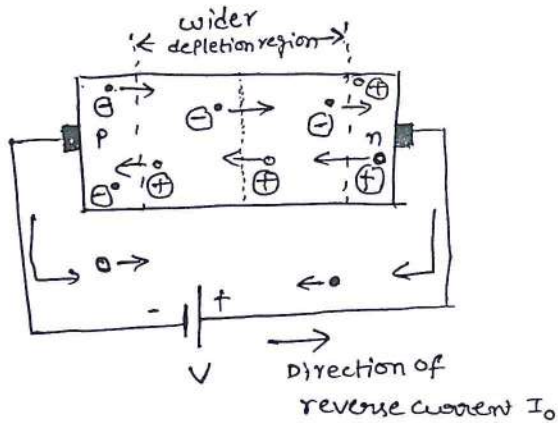


fig:- flow of minority charge carriers

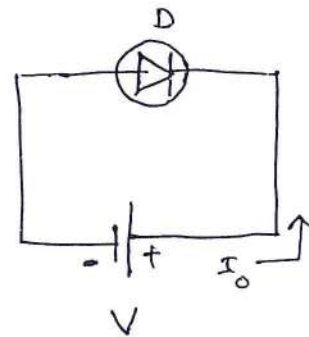


fig:- direction of reverse current.

V-I Characteristics in reverse biased condition:-

The V-I characteristics under reverse biased condition is as shown in below figure.

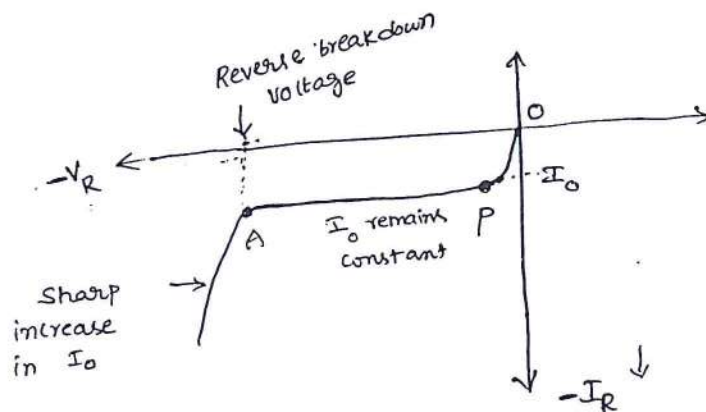


fig:- Reverse characteristics of P-N Junction diode

As reverse voltage is increased, the reverse current increases initially. But after a small voltage, the reverse current becomes constant though applied reverse voltage is increased upto certain limit. This current is called as reverse saturation current denoted by ' I_0 '.

At certain point A, this reverse current increases rapidly. The voltage at this point is known as breakdown voltage (or) reverse break down voltage denoted by V_{BR} .

NOTE:- The generation of minority carriers depends on the temperature but ^{not} on the applied reverse biased voltage. Therefore the reverse current depends on the temperature but not on the applied reverse biased voltage.

complete V-I Characteristics of P-N Junction diode:-

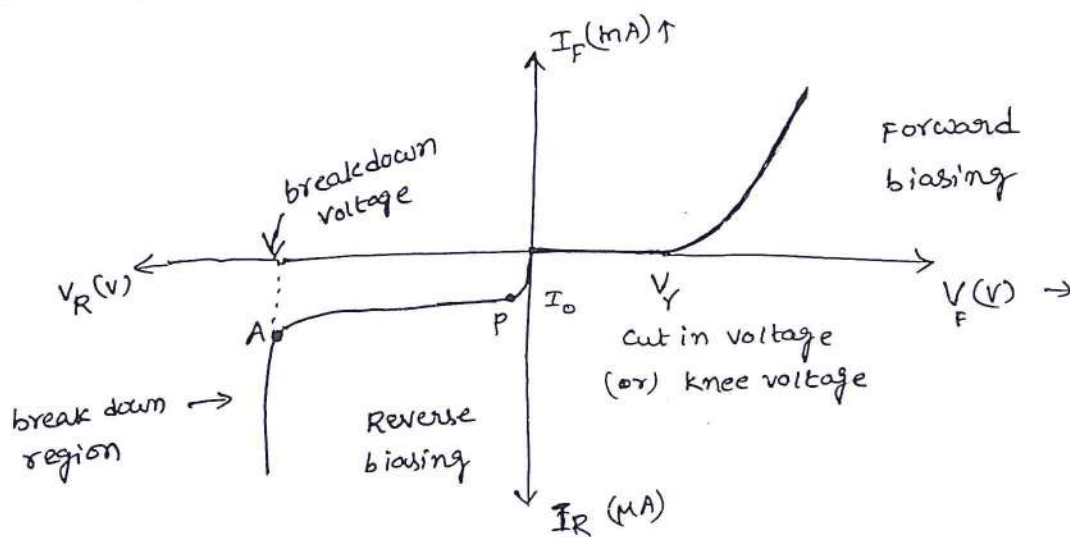


fig:- V-I Characteristics of P-N Junction diode.

Break down mechanisms in PN Junction diode:

Though the reverse saturation current does not depend on the applied reverse voltage, if the reverse bias voltage is increased beyond a certain limit, a large reverse current can flow through the diode, that can cause a damage to the diode.

This is called reverse breakdown of the diode.

The reverse breakdown of a diode can occur due to

two reasons

- 1) Avalanche breakdown effect
- 2) Zener breakdown effect.

1) Breakdown due to Avalanche effect :-

* If the reverse voltage is increased, at a particular value, velocity of minority charge carriers increases. Due to kinetic energy associated with the minority charge carriers, more minority charge carriers are generated when there is collision of minority charge carriers with the atoms. The collision makes the electrons to break the covalent bonds.

* These electrons are available as minority charge carriers and get accelerated due to high reverse voltage. They again collide with some other atoms and generate more minority carriers. This is called as "Carrier multiplication" (or) "Avalanche multiplication".

* Finally a large number of minority charge carriers move across the junction, breaking the p-n junction. These large number of minority carriers give rise to a very high reverse - current. This effect is known as "Avalanche breakdown".

The mechanism of destroying the junction is called reverse breakdown of p-n junction. The voltage at which the breakdown of a p-n junction occurs is called as "reverse breakdown voltage".

2) Breakdown due to the Zener effect :-

When a p-n junction is heavily doped, the depletion region is very narrow.

The electric field is voltage per distance and due to narrow depletion region and high reverse voltage, the electric field is very high in this case.

Such an intense field is enough to pull the electrons out of the valence bands of the stable atoms present in p-region.

Such creation of free electrons is called "Zener effect". These minority carriers constitute a very large current that may destroy the junction. This mechanism of destroying the junction is called as Zener breakdown.

The current components in a P-N junction diode:

When the forward bias is applied to a diode, the holes are injected into the n-side and electrons into the p-side. The holes injected into n-side and the electrons injected into p-side are the minority charge carriers.

On p-side, the injected electrons constitute the diffusion current that decreases exponentially with respect to the distance measured from the junction. This current due to the electrons on p-side which are minority carriers is denoted as I_{np} .

Similarly the holes injected into n-side constitute the diffusion current that decreases exponentially with respect to the distance measured from the junction. This current due to the holes on n-side which are the minority carriers, is denoted as I_{pn} .

If the distance is denoted by ' x ', then

$I_{np}(x)$ = current due to the electrons in p-side as a function of ' x '

$I_{pn}(x)$ = current due to the holes in n-side as a function of ' x '.

At the junction i.e. at $x=0$, the electrons crossing from n-side to p-side constitute a current $I_{np}(0)$ & in the same direction as that of the current formed due to the crossing of holes from p-side to n-side, $I_{pn}(0)$.

$\therefore$ The total current at the junction = $I = I_{pn}(0) + I_{np}(0)$

As we move away from the junction on n-side, $I_{pn}(x)$ gets decreased, similarly $I_{np}(x)$ decreases on p-side as we move away from the junction.

But the circuit is a series circuit, hence the total current must be maintained ' I ', independent of ' x '.

Therefore on p-side there must be a second current component which is due to holes on p-side which are majority carriers in

P-side. It is denoted by $I_{pp}(x)$.

The addition of $I_{np}(x)$ and $I_{pp}(x)$ on P-side is equal to the total current I ,

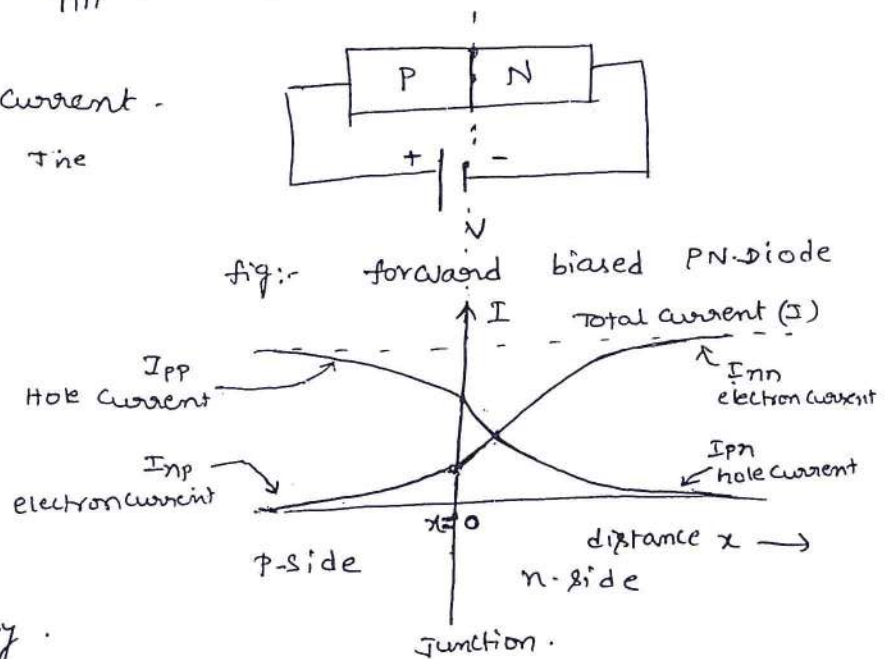
$$\text{i.e. } I = I_{pp}(x) + I_{np}(x)$$

Similarly on n-side there exists one more current component which is due to electrons on n-side which are majority carriers. It is denoted by $I_{nn}(x)$. The addition of $I_{pn}(x)$ and $I_{nn}(x)$ on n-side is equal to the total current I

$$\text{i.e. } I = I_{nn}(x) + I_{pn}(x)$$

The above discussed all current components are shown in the following graph.

The current I_{pp} decreases towards the junction, at the junction it enters n-side and becomes I_{pn} which also further decreases exponentially.



Similarly the current I_{nn} decreases towards the junction, at the junction it enters P-side and becomes I_{np} which also further decreases exponentially.

So the sum of the currents carried by electrons and holes at any point inside the diode is always constant equal to the forward current I .

* NOTE : At the junction i.e. at $x=0$

$$I_{pn}(0) = \frac{A q D_p P_n(0)}{L_p}$$

Similarly $I_{np}(0) = \frac{A q D_n N_p(0)}{L_n}$

where A = Cross sectional area of the junction

D_p = Diffusion Coefficient for holes

D_n = Diffusion Coefficient for electrons

q = Charge = 1.602×10^{-19} Coulombs

L_p = Diffusion length for holes

L_n = Diffusion length for electrons

$P_n(0)$ = Concentration of injected holes, from P-side into n-side

$N_p(0)$ = Concentration of injected electrons, from n-side to P-side

Diode current equation (or) V-I characteristic equation of a diode:

The relationship between applied voltage ' V ' and the diode current ' I ' is exponential and is mathematically given by the equation called diode current equation. It is expressed as

$$\text{Diode current } I = I_0 \left(e^{V/\eta V_T} - 1 \right)$$

where I_0 = Reverse Saturation Current in Amperes

V = Applied Voltage

η = a constant, '1' for Germanium diode and '2' for - diode

V_T = Voltage equivalent of temperature in Volts.

The voltage equivalent of temperature indicates the dependence of diode current on temperature.

The voltage equivalent of temperature ' V_T ' for a given diode at a temperature ' T ' is calculated as $V_T = kT$ volts.

where k = Boltzmann's Constant = $8.62 \times 10^{-5} \text{ eV/}^\circ\text{K}$.

T = temperature in $^\circ\text{K}$.

At room temperature of 27°C i.e. $T = 27 + 273 = 300^\circ\text{K}$

The value of V_T is $V_T = 8.62 \times 10^{-5} \times 300 = 25.86 \text{ mV} \approx 26 \text{ mV}$

The diode current equation is applicable for all the conditions of diode such as unbiased, forward biased and reverse biased.

For forward biased condition, ' V ' must be taken as positive

and we get the current I positive, which is nothing but the forward current. For reverse bias, V must be taken as negative and we get negative current I , which is nothing but the reverse current.

Nature of V-I characteristics from the diode current equation:

The diode current equation is $I = I_0 (e^{V/\eta V_T} - 1)$

For forward bias condition, the bias voltage ' V ' is considered as positive and hence the exponential index has positive sign. Due to this $1 \ll e^{V/\eta V_T}$. Therefore neglecting ' 1 ' we get the equation for forward current as

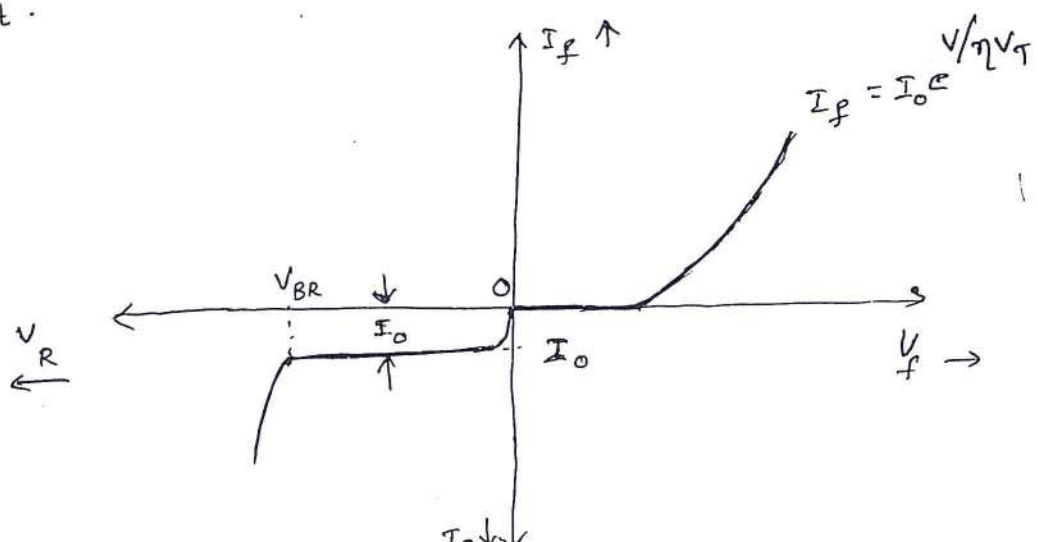
$$I_F = I_0 e^{V/\eta V_T}$$

This indicates that once bias voltage exceeds beyond cut-in voltage the forward current increases exponentially.

In reverse bias condition, the bias voltage ' V ' is treated as '-ve' and hence the index of exponential has -ve sign. Due to this $e^{-V/\eta V_T} \ll 1$. Hence neglecting exponential term we get

$$I_R \approx I_0(-1) \approx -I_0$$

The above equation indicates that the current in reverse bias is reverse saturation current which is negative, indicating that it flows in opposite direction to that of forward current and almost constant.



Problems

1) A silicon diode has reverse saturation current of 7.12 nA at room temperature $- 27^\circ\text{C}$. Calculate its forward current if it is in forward bias with a voltage of 0.7 V .

Sol) Given silicon diode, so $\eta = 2$
Reverse saturation current $I_0 = 7.12 \text{ nA} = 7.12 \times 10^{-9}$

Given Temperature = Room temperature $T = 27^\circ\text{C} = 27 + 273 = 300^\circ\text{K}$

forward bias voltage $V = 0.7 \text{ V}$

Voltage equivalent of temperature $V_T = kT = 8.62 \times 10^{-5} \times 300$
 $\therefore V_T = 26 \text{ mV}$

$$\therefore \text{Diode forward current } I = I_0 \left(e^{V/\eta V_T} - 1 \right)$$

$$\Rightarrow I = 7.12 \times 10^{-9} \left(e^{\frac{0.7}{2 \times 26 \times 10^{-3}}} - 1 \right)$$

$$\Rightarrow I = 4.997 \text{ mA}$$

$$\Rightarrow I \approx 5 \text{ mA}$$

2) The voltage across a silicon diode at room temperature of 300°K is 0.71 V , when 2.5 mA current flows through it. If the voltage increases to 0.8 V calculate the new diode current.

Sol) Given silicon diode, so $\eta = 2$

Voltage across the diode $= V = 0.71 \text{ V}$.

Temperature $T = 300^\circ\text{K}$.

Voltage equivalent of temperature $V_T = kT = 8.62 \times 10^{-5} \times 300$
 $\therefore V_T = 26 \text{ mV}$

Diode current $I = 2.5 \text{ mA}$.

Reverse saturation current $I_0 = ?$

$$\text{W.K.T } I = I_0 \left(e^{V/\eta V_T} - 1 \right)$$

$$\Rightarrow I_0 = \frac{I}{\left(e^{V/\eta V_T} - 1 \right)} = \frac{2.5 \times 10^{-3}}{\left(e^{0.71/(2 \times 26 \times 10^{-3})} - 1 \right)}$$

$$\Rightarrow I_0 = 2.938 \times 10^{-9} \approx 3 \text{ nA}$$

when the voltage increases to 0.8 V

i.e. Applied voltage $V = 0.8$

Diode current $I = ?$

$$I = I_0 (e^{V/\eta V_T} - 1)$$
$$= 3 \times 10^{-9} (e^{0.8/(2 \times 26 \times 10^{-3})} - 1)$$

$$I = 14.112 \text{ mA}$$

- 3) A Germanium diode has a reverse saturation current of $3 \mu\text{A}$. Calculate the forward bias voltage at the room temperature of 27°C and 1% of rated current is flowing through the forward biased diode. The diode forward rated current is 1 A .

4) Given Germanium diode, so $\eta = 1$

Reverse saturation current $I_0 = 3 \mu\text{A} = 3 \times 10^{-6} \text{ A}$

Temperature $= 27^\circ\text{C} = 27^\circ\text{C} + 273 = 300^\circ\text{K}$, so $V_T = 26 \text{ mV}$

Diode current $I = 1\%$ of rated current

Given rated current $= 1 \text{ A}$.

$$\therefore I = 1\% \text{ of } 1 \text{ A} = \frac{1}{100} \times 1 = 0.01 \text{ A}$$

$\therefore$ forward bias voltage $V = ?$

w.k.T $I = I_0 (e^{+V/\eta V_T} - 1)$

$$0.01 = 3 \times 10^{-6} (e^{\frac{V}{1 \times 26 \times 10^{-3}}} - 1)$$

$$\Rightarrow e^{\frac{V}{26 \times 10^{-3}}} - 1 = \frac{0.01}{3 \times 10^{-6}}$$

$$\Rightarrow e^{\frac{V}{26 \times 10^{-3}}} = 3333.33 + 1$$

Applying $\log_e$ on both sides

$$\ln_e e^{\frac{V}{26 \times 10^{-3}}} = \ln_e (3334.33)$$

$$\Rightarrow \frac{V}{26 \times 10^{-3}} = \ln_e (3334.33)$$

$$\Rightarrow V = 26 \times 10^{-3} \ln_e (3334.33) = \underline{\underline{0.21 \text{ V}}}_{\text{Ans}}$$

4) A diode operating at 300K at a forward voltage of 0.4V, which carries a current of 10mA. Then voltage is changed to 0.42V, the current becomes twice. Calculate the value of current of reverse saturation and Ideality factor (η).

Sol) Given forward voltage $V = 0.4V$
 Temperature $T = 300^\circ K$
 $\therefore$ Voltage equivalent of temperature $V_T = kT$
 $\Rightarrow V_T = 8.62 \times 10^{-5} \times 300 = 26 \text{ mV}$

Diode Current $I = 10 \text{ mA}$, $I_0 = ?$

$\therefore$ W.K.T $I = I_0 \left(e^{\frac{V}{\eta V_T}} - 1 \right)$

$10 \text{ mA} = I_0 \left(e^{\frac{0.4}{\eta \times 26 \times 10^{-3}}} - 1 \right) \dots \dots \textcircled{1}$

Given that at $V = 0.42 \text{ V}$, The diode current becomes twice.

$\therefore 2 \times 10 \text{ mA} = I_0 \left(e^{\frac{0.42}{\eta \times 26 \times 10^{-3}}} - 1 \right)$

$20 \text{ mA} = I_0 \left(e^{\frac{0.42}{\eta \times 26 \times 10^{-3}}} - 1 \right) \dots \dots \textcircled{2}$

$\frac{\textcircled{2}}{\textcircled{1}} \Rightarrow \frac{20 \text{ mA}}{10 \text{ mA}} = \frac{I_0 \left(e^{\frac{0.42}{\eta \times 26 \times 10^{-3}}} - 1 \right)}{I_0 \left(e^{\frac{0.4}{\eta \times 26 \times 10^{-3}}} - 1 \right)}$

$2 = \frac{e^{\frac{0.42}{\eta \times 26 \times 10^{-3}}} - 1}{e^{\frac{0.4}{\eta \times 26 \times 10^{-3}}} - 1}$

$2 \left(e^{\frac{0.4}{\eta \times 26 \times 10^{-3}}} - 1 \right) = \left(e^{\frac{0.42}{\eta \times 26 \times 10^{-3}}} - 1 \right)$

In forward bias condition '1' can be neglected.

$\therefore 2 e^{\frac{0.4}{\eta \times 26 \times 10^{-3}}} = e^{\frac{0.42}{\eta \times 26 \times 10^{-3}}}$

Applying natural logarithm on both sides we get
 $\ln_e \left(2 e^{\frac{0.4}{\eta \times 26 \times 10^{-3}}} \right) = \ln_e \left(e^{\frac{0.42}{\eta \times 26 \times 10^{-3}}} \right) \quad 16$

$$\ln_e^2 + \ln_e e^{0.4/(\eta \times 26 \times 10^{-3})} = \frac{0.42}{\eta \times 26 \times 10^{-3}}$$

$$\ln_e^2 + \frac{0.4}{\eta \times 26 \times 10^{-3}} = \frac{0.42}{\eta \times 26 \times 10^{-3}}$$

$$\frac{\ln_e^2 \times (\eta \times 26 \times 10^{-3}) + 0.4}{\eta \times 26 \times 10^{-3}} = \frac{0.42}{\eta \times 26 \times 10^{-3}}$$

$$\Rightarrow \eta \times \ln_e^2 \times 26 \times 10^{-3} = 0.42 - 0.4$$

$$\Rightarrow \eta = \frac{0.02}{\ln_e^2 \times 26 \times 10^{-3}} = 1.109$$

Substituting $\eta = 1.109$ in equation ① we get

$$10 \times 10^{-3} = I_0 \left(e^{\frac{0.4}{1.109 \times 26 \times 10^{-3}}} - 1 \right)$$

$$\Rightarrow I_0 = \frac{10 \times 10^{-3}}{\left(e^{\frac{0.4}{1.109 \times 26 \times 10^{-3}}} - 1 \right)}$$

$$I_0 = 9.4459 \times 10^{-9} \text{ A}$$

$\therefore$ Reverse saturation current $I_0 = 9.4459 \text{ nA}$

Ideality factor $\eta = 1.109$ Ans

⑤ Determine forward current with $I_0 = 10 \mu\text{A}$, $V_f = 0.8 \text{ V}$, $T = 300^\circ\text{K}$ assume silicon diode.

Sol

Given $I_0 = \text{Reverse saturation current} = 10 \mu\text{A} = 10 \times 10^{-6} \text{ A}$

$V_f = \text{forward bias voltage} = V = 0.8 \text{ V}$

$T = 300^\circ\text{K}$, $V_T = kT = 8.62 \times 10^{-5} \times 300 \approx 0.026 \text{ mV}$

$\eta = 2$ ($\because$ silicon diode)

$$I = I_0 \left(e^{\frac{V}{\eta V_T}} - 1 \right) = 10 \times 10^{-6} \left(e^{\frac{0.8}{2 \times 0.026}} - 1 \right)$$

$$\therefore I = 52.19 \text{ A}$$

Derivation of Diode Current Equation (or) Derivation of $v-i$ Characteristics of PN-Junction diode:

Let p_p = Concentration of holes in P-region
 n_n = Concentration of electrons in n-region
 p_n = Concentration of holes in n-region
 n_p = Concentration of electrons in P-region.

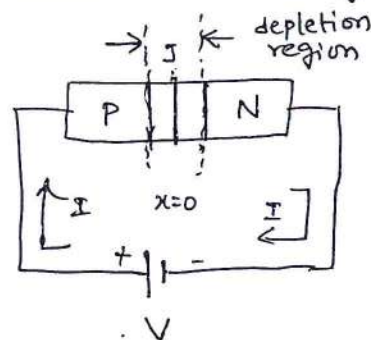
Under unbiased Condition, When holes move from P-side to n-side due to diffusion, the concentration of holes behaves in exponential manner. This is mathematically expressed as

$$p_{p0} = p_{n0} e^{V_F/V_T} \quad \rightarrow (1)$$

where p_{p0} = hole concentration in P-region under unbiased condition
 p_{n0} = hole concentration in n-region under unbiased condition
 V_F = barrier potential of PN Junction
 V_T = voltage equivalent of temperature, in volts

Now, Consider a forward biased diode as shown in below figure.

Under forward biased condition, even though the proportion of holes and electrons in constituting the current in P-region is changing, the hole concentration in P-region is constant that is equal to p_{p0} .



As the holes cross the junction, under forward bias the concentration behaves exponentially, it is given as at $x=0$

$$p_{p0} = p_n(0) \cdot e^{(V_F - V)/V_T} \quad \dots (2)$$

where $p_n(0)$ = hole concentration in n-region under forward bias at $x=0$ (i.e. at the junction exactly).

from equation ① and ②

$$p_{n0} e^{V_T/V_T} = p_n(0) e^{(V_T - V)/V_T}$$

$$p_{n0} e^{V_T/V_T} = p_n(0) e^{V_T/V_T} \dots e^{-V/V_T}$$

$$\Rightarrow \boxed{p_n(0) = p_{n0} e^{V/V_T}} \quad \dots \dots \dots \text{③}$$

This equation represents The boundary condition and called as law of junction.

① and the above equation ③ indicates that the hole concentration $p_n(0)$ at the junction (i.e at $x=0$) under forward bias condition is greater than that of the hole concentration under unbiased condition p_{n0} .

The difference between two concentrations at the junction under forward biased condition and unbiased condition is called as injected or Excess concentration. It is given by injected hole concentration at

n-region $p_n(0) = p_n(0) - p_{n0}$

From equation ③ we have $p_n(0) = p_{n0} e^{V/V_T}$

$$\therefore p_n(0) = p_{n0} e^{V/V_T} - p_{n0}$$

$$\Rightarrow \boxed{p_n(0) = p_{n0} (e^{V/V_T} - 1)} \quad \dots \dots \dots \text{④}$$

Similarly the injected electron concentration at the junction in p-region is $\boxed{N_p(0) = n_{p0} (e^{V/V_T} - 1)}$ $\dots \dots \dots \text{⑤}$

We know that the diode currents due to injected carriers at the junction because of diffusion, are given by

$$I_{np}(0) = \frac{A q D_n N_p(0)}{L_n}$$

$$I_{pn}(0) = \frac{AqD_p P_n(0)}{L_p}$$

where A = Area of cross sectional area of the junction

D_n, D_p = Diffusion coefficients of electrons and holes - respectively

q = charge = 1.602×10^{-19} Coulombs

L_n, L_p = Diffusion length for electrons and holes respective

The total current 'I' at the junction is given by

$$I = I_{pn}(0) + I_{np}(0)$$

$$= \frac{AqD_p P_n(0)}{L_p} + \frac{AqD_n N_p(0)}{L_n}$$

From eq (4), (5) we get

$$\Rightarrow I = \frac{AqD_p P_{n0} (e^{V/V_T} - 1)}{L_p} + \frac{AqD_n n_{p0} (e^{V/V_T} - 1)}{L_n}$$

$$\Rightarrow I = \left(\frac{AqD_p P_{n0}}{L_p} + \frac{AqD_n n_{p0}}{L_n} \right) (e^{V/V_T} - 1)$$

$$\Rightarrow \boxed{I = I_0 (e^{V/V_T} - 1)} \quad \text{--- --- --- --- --- (6)}$$

where $I_0 = \frac{AqD_p P_{n0}}{L_p} + \frac{AqD_n n_{p0}}{L_n}$ = reverse saturation current

when we consider the recombination effect, the equation (6) can be written as

$$\boxed{I = I_0 (e^{V/\eta V_T} - 1)} \quad \text{--- --- --- --- --- (7)}$$

where $\eta = 1$ for Germanium diode

$\eta = 2$ for silicon diode.

The above equation (7) is known as diode current equation (or) V-I characteristic equation of a diode.

Temperature dependence on VI Characteristics of Diode:-

The temperature has the following effects on the diode parameters

- 1) The cut-in voltage decreases as the temperature increases. The diode conducts even at a very smaller voltages at large temperature.
- 2) The reverse saturation current increases as the temperature increases. This increase in reverse current ' I_0 ' is such that it doubles at every 10°C rise in temperature.

$$\text{Mathematically } I_{02} = 2^{(\Delta T/10)} \cdot I_{01}$$

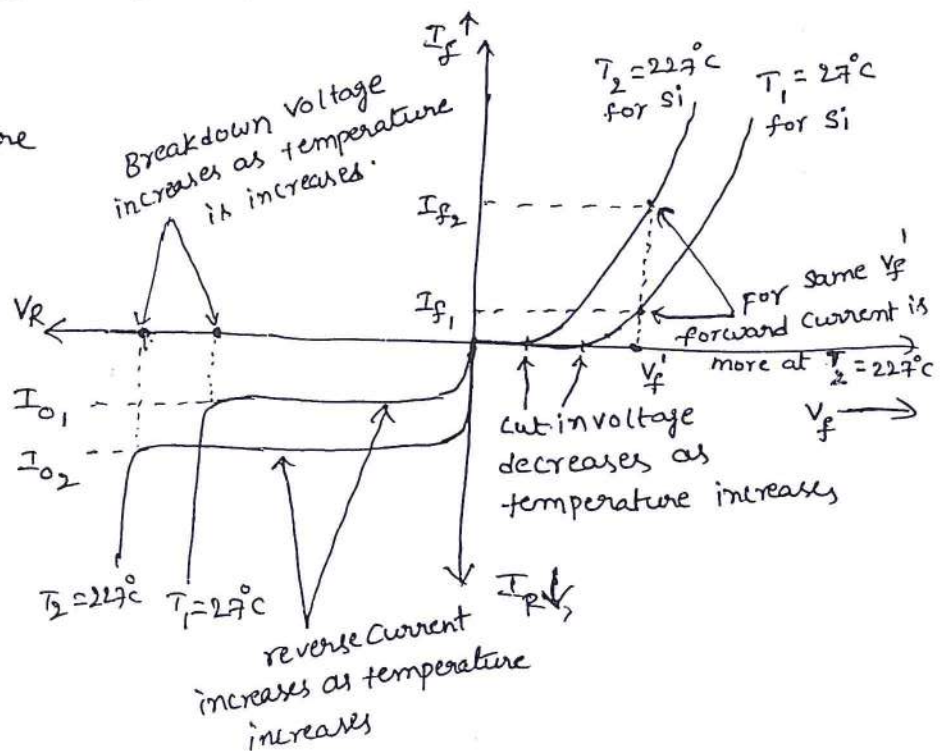
where $\Delta T = T_2 - T_1 = \text{change in temperature}$

$I_{02} = \text{reverse current at } T_2^\circ\text{C}$

$I_{01} = \text{reverse current at } T_1^\circ\text{C}$

- 3) The voltage equivalent of temperature V_T also increases as temperature increases.
- 4) The reverse break down voltage increases as temperature increases.
- 5) At higher temperatures, as the device junction temperature is also higher, the maximum power dissipation of the device decreases.

The effect of temperature on V-I characteristics of a Si-diode is shown in below graph.



Derivation for Temperature dependence on V-I Characteristics :

Since the reverse saturation current increases with the increase in temperature and also voltage equivalent of temperature (V_T) increases, we can say that the overall diode characteristics depends on temperature.

The reverse saturation current I_0 is given by

$$I_0 = KT^m e^{-V_{G0}/\eta V_T} \quad \text{--- (1)}$$

where K = Constant independent of temperature (not a Boltzmann constant)

$m = 2$ for Germanium diode

$= 1$ for Silicon Diode

V_{G0} = Forbidden Energy Gap which is equal to 0.785 eV for Germanium and 1.21 eV for Silicon

As temperature increases, the value of I_0 increases and hence the diode current increases. To keep the diode current 'I' constant it is necessary to change the applied voltage.

$$\text{The diode current } I = I_0 (e^{V/\eta V_T} - 1) \quad \text{--- (2)}$$

$$\text{For a forward bias condition } I \approx I_0 e^{V/\eta V_T} \quad \text{--- (3)}$$

substituting equation (1) in (3) we get

$$I = KT^m e^{-V_{G0}/\eta V_T} \cdot e^{V/\eta V_T}$$

$$I = KT^m e^{\frac{V-V_{G0}}{\eta V_T}} \quad \text{--- (4)}$$

For a constant diode current 'I', $\frac{dI}{dT} = 0$

$$\Rightarrow \frac{d}{dT} \left(KT^m e^{\frac{V-V_{G0}}{\eta V_T}} \right) = 0 \quad (\because \text{from (4)})$$

$$K \cdot \left[e^{\frac{V-V_{G0}}{\eta V_T}} \cdot m \cdot T^{m-1} + T^m \frac{d}{dT} \left(e^{\frac{V-V_{G0}}{\eta V_T}} \right) \right] = 0$$

substituting $V_T = kT$ in the second term

$$\Rightarrow k \cdot \left[m T^{m-1} e^{\frac{V-V_{G0}}{\eta V_T}} + T^m \cdot \frac{d}{dT} e^{\frac{V-V_{G0}}{\eta k T}} \right] = 0$$

$$\Rightarrow K \left[m \cdot T^{m-1} e^{\frac{V-V_{G0}}{\eta V_T}} + T^m e^{\frac{V-V_{G0}}{\eta k T}} \frac{d}{dT} \left(\frac{V-V_{G0}}{\eta k T} \right) \right] = 0$$

$$\Rightarrow k \left[m \cdot T^{m-1} e^{\frac{V-V_{G0}}{\eta V_T}} + T^m e^{\frac{V-V_{G0}}{\eta k T}} \frac{1}{\eta k} \left(\frac{T \cdot \frac{dV}{dT}}{T^2} - (V-V_{G0}) \cdot \frac{1}{T} \right) \right] = 0$$

$$\Rightarrow k e^{\frac{V-V_{G0}}{\eta V_T}} \left[m \cdot T^{m-1} + \frac{T^m}{\eta k T^2} \left(T \frac{dV}{dT} - (V-V_{G0}) \right) \right] = 0$$

($\because \eta k T^2 = \eta (k T) \cdot T$
 $= \eta V_T \cdot T$)

$$\Rightarrow k e^{\frac{V-V_{G0}}{\eta V_T}} \left[m \cdot T^{m-1} + \frac{T^m}{\eta V_T \cdot T} \left(T \frac{dV}{dT} - (V-V_{G0}) \right) \right] = 0$$

$$k e^{\frac{V-V_{G0}}{\eta V_T}} \left[\frac{m \cdot T^{m-1} \cdot T \cdot \eta V_T + T^m \left(T \frac{dV}{dT} - (V-V_{G0}) \right)}{\eta V_T \cdot T} \right] = 0$$

$$\frac{k e^{\frac{V-V_{G0}}{\eta V_T}}}{\eta V_T \cdot T} \left[m \cdot T^m \eta V_T + T^m \left(T \frac{dV}{dT} - (V-V_{G0}) \right) \right] = 0$$

$$\frac{k e^{\frac{V-V_{G0}}{\eta V_T}}}{\eta V_T \cdot T} \cdot T^m \left(m \eta V_T + T \frac{dV}{dT} - (V-V_{G0}) \right) = 0$$

$$\Rightarrow m \eta V_T + T \frac{dV}{dT} - (V-V_{G0}) = 0$$

$$T \frac{dV}{dT} = (V-V_{G0}) - m \eta V_T$$

$$\boxed{\frac{dV}{dT} = \frac{V-V_{G0} - m \eta V_T}{T}}$$

this is the required change in voltage which is necessary to keep the diode current constant.

For Germanium diode $\frac{dV}{dT}$ calculation:

Let the applied voltage $V =$ cut in voltage $= 0.3 \text{ V}$ for Germanium diode, assume the temperature as room temperature of 300°K . For Germanium $\eta = 1$, $m = 2$. $V_{G0} = 0.785 \text{ eV}$

$$V_T = kT = 8.62 \times 10^{-5} \times 300 = 26 \text{ mV.}$$

$$\therefore \frac{dV}{dT} = \frac{0.3 - 0.785 - 2(1)(26 \times 10^{-3})}{300} = -1.79 \text{ mV}/^\circ\text{C}$$

For Silicon diode $\frac{dV}{dT}$ calculation:

Let the applied voltage $V =$ cut in voltage $= 0.7 \text{ V}$ (for Si), assume the temperature as room temperature of 300°K .

$$\therefore V_T = kT = 8.62 \times 10^{-5} \times 300 = 26 \text{ mV.}$$

For Silicon $\eta = 2$, $m = 1.5$, $V_{G0} = 1.21 \text{ eV}$.

$$\therefore \frac{dV}{dT} = \frac{0.7 - 1.21 - (1.5)(2)(26 \times 10^{-3})}{300} = -1.96 \text{ mV}/^\circ\text{C}$$

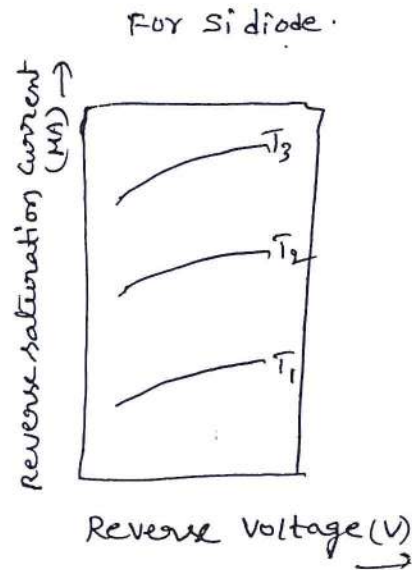
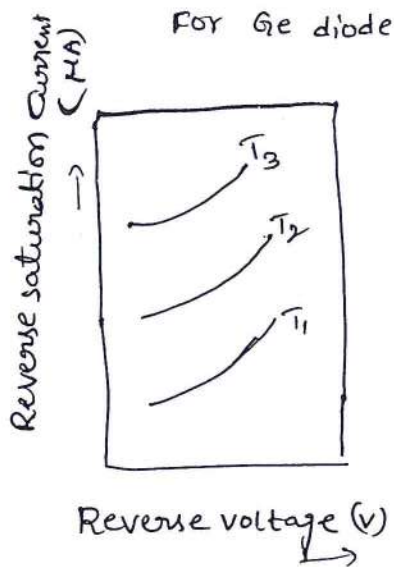
The effect of temperature on I_0 can be mathematically expressed as $I_{02} = I_{01} \cdot 2^{(\Delta T/10)}$

where $I_{01} =$ reverse saturation current at $T_1^\circ \text{K}$

$I_{02} =$ reverse saturation current at $T_2^\circ \text{K}$

$\Delta T = T_2 - T_1 =$ change in temperature

The temperature dependence on I_0 for Silicon diode and Germanium diode can be shown as given in below graph.



$$T_3 > T_2 > T_1$$

Problems:

- A silicon diode has a reverse saturation current of $7.5 \mu\text{A}$ at room temperature of 300°K . Calculate the saturation current at 400°K .

Sol) Given $T_1 = 300^\circ\text{K}$, $T_2 = 400^\circ\text{K}$, $\Delta T = T_2 - T_1 = 400 - 300 = 100^\circ\text{K}$
 $I_{01} = 7.5 \mu\text{A}$

$$I_{02} = ?$$

We know that $I_{02} = I_{01} \cdot 2^{\frac{\Delta T}{10}} = 7.5 \times 10^{-6} \times 2^{\frac{100}{10}}$

$$\Rightarrow I_{02} = 7.68 \text{ mA}$$

- Find the factor by which the reverse saturation current of a silicon diode will get multiplied when the temperature is increased from 27°C to 82°C .

Sol) Given temperature $T_1 = 27^\circ\text{C}$

Temperature $T_2 = 82^\circ\text{C}$

Change in temperature $\Delta T = 82^\circ\text{C} - 27^\circ\text{C} = 55^\circ\text{C}$

$$I_{02} = I_{01} \cdot 2^{\frac{\Delta T}{10}}$$

Let I_{01} is reverse saturation current at $T_1 = 27^\circ\text{C}$

and I_{02} is reverse saturation current at $T_2 = 82^\circ\text{C}$

$$\therefore I_{02} = I_{01} \cdot 2^{(55/10)}$$

$$= I_{01} \cdot 2$$

$$I_{02} = 45.2548 I_{01}$$

$\therefore$ The reverse saturation current will get multiplied by a factor of 45.25.

- ③ The reverse saturation current of a Ge diode is $100 \mu A$ at a room temperature of $27^\circ C$. Calculate the current in forward bias condition, if the forward bias voltage is $0.2 V$ at room temperature. When the temperature is increased by $20^\circ C$. Calculate the reverse saturation current and the forward current for the same forward voltage at new temperature.

Sol.) Given the temperature $T_1 = 27^\circ C = 300^\circ K$.

Given Ge diode, so $\eta = 1$

Reverse saturation current at $T_1 = 27^\circ C$ is $I_{01} = 100 \mu A$

Forward bias voltage $V = 0.2$

Voltage equivalent of temperature $V_T = kT = 8.62 \times 10^{-5} \times 300$
 $= 26 \text{ mV}$.

$$\therefore \text{Diode current } I = I_{01} \left(e^{\frac{V}{\eta V_T}} - 1 \right) = 100 \times 10^{-6} \left(e^{\frac{0.2}{1 \times 26 \times 10^{-3}}} - 1 \right)$$

$$\therefore I = 0.219 A$$

The temperature is increased by $20^\circ C$.

$$\therefore T_2 = 27^\circ C + 20^\circ C = 47^\circ C$$

$$\Delta T = T_2 - T_1 = 47^\circ C - 27^\circ C = 20^\circ C$$

The reverse saturation current $I_{02} = I_{01} \cdot 2^{\Delta T/10}$

$$\Rightarrow I_{02} = 100 \times 10^{-6} \cdot \left(2^{\frac{20}{10}} \right)$$

$$\Rightarrow I_{02} = 400 \mu A$$

The diode current 'I' at new temperature of $47^\circ C$ i.e. at 320° is $I = I_{02} \cdot \left(e^{\frac{V}{\eta V_T}} - 1 \right)$

$$= 400 \times 10^{-6} \times \left(e^{0.2 / (1 \times 8.62 \times 10^{-5} \times 320)} - 1 \right)$$

$$\therefore \text{Diode current } (I) = 0.563 \text{ A}$$

④ A P-N junction Ge diode has a saturation current of 0.1 mA at room temperature of 27°C . It is observed to be 30 mA , when the room temperature is increased, calculate the new room temperature.

sol) Given Ge diode, so $\eta = 1$

Given Reverse saturation current at $T_1 = 27^\circ\text{C} = 300 \text{ K}$ is

$$I_{01} = 0.1 \text{ mA}$$

$$T_2 = ?$$

The reverse saturation current at $T_2 = I_{02} = 30 \text{ mA}$.

$$\therefore I_{02} = I_{01} 2^{\frac{\Delta T}{10}}$$

$$\Rightarrow 30 \times 10^{-6} = 0.1 \times 10^{-6} 2^{\frac{(T_2 - 27^\circ\text{C})}{10}}$$

$$\Rightarrow 300 = 2^{\frac{(T_2 - 27^\circ\text{C})}{10}}$$

$$\Rightarrow \log_2 300 = \left(\frac{T_2 - 27^\circ\text{C}}{10} \right)$$

$$\Rightarrow T_2 = (10 \log_2 300) + 27^\circ\text{C}$$

$$\therefore T_2 = 109.28^\circ\text{C}$$

⑤ when a reverse bias is applied to a Ge diode, the reverse saturation current at room temperature is 0.3 mA . Determine the current flowing in the diode when 0.15 V forward bias is applied at room temperature

sol) Given Ge diode, so $\eta = 1$.

Reverse saturation current $I_0 = 0.3 \text{ mA}$, $T = 27^\circ\text{C} = 300^\circ\text{K}$

$$V_T = 26 \text{ mV}, \quad V = 0.15 \text{ V}$$

$$\therefore I = I_0 \left(e^{\frac{V}{\eta V_T}} - 1 \right) = 0.3 \times 10^{-6} \left(e^{\frac{0.15}{1 \times 0.026}} - 1 \right) = \underline{\underline{120.728 \text{ mA}}}$$

Diode Resistance:

An ideal diode has zero resistance in forward bias and infinite resistance in reverse bias. But in practice no diode can act as an ideal diode.

Forward resistance:

The resistance offered by a diode under forward biased condition is known as forward resistance. Forward resistance is of two types. They are

i) Static resistance (or) DC resistance

ii) Dynamic resistance (or) AC resistance.

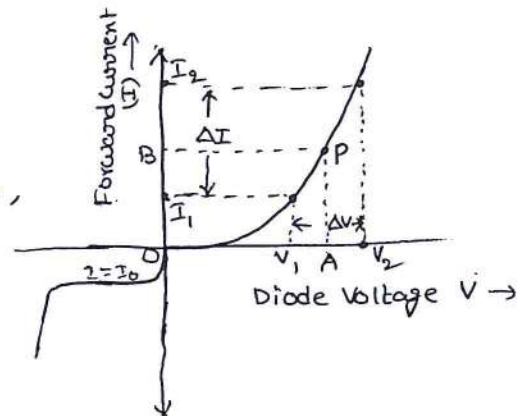
i) Static resistance (or) DC resistance: (R_f)

The static resistance (or) DC resistance is defined as the ratio of the voltage to the current ($\frac{V}{I}$) in the forward bias characteristics of the PN junction diode. As the static resistance varies widely with V and I , so it is not a useful parameter.

At any point 'P' on the V-I characteristics of the diode the voltage across the diode is $V = OA$, and the current $I = OB$ as shown in graph.

Then

$$\text{Static resistance } R_f = \frac{V}{I} = \frac{OA}{OB}$$



ii) Dynamic resistance (or) AC resistance: (r_f)

The dynamic resistance (or) AC resistance is defined as the reciprocal of the slope of the forward characteristics of the diode.

$$\text{Dynamic resistance } r_f = \frac{1}{\left(\frac{dI}{dV}\right)} = \frac{\eta V_T}{I_0 e^{V/\eta V_T}} = \frac{\eta V_T}{I + I_0}$$

$$\text{Since } I \gg I_0, \quad I + I_0 \approx I,$$

$$\therefore r_f = \frac{\eta V_T}{I}$$

From the V-I characteristics in forward bias

$$\text{The dynamic resistance } r_f = \frac{\Delta V}{\Delta I} = \frac{\text{change in forward voltage}}{\text{change in forward current}}$$

Reverse Resistance:

It is the resistance offered by the PN junction diode under reverse bias condition. It is very large compared to the forward resistance which is in the range of several $M\Omega$.

Diode Capacitance:

The diode capacitance is mainly classified into two types.

1) Transition Capacitance (C_T)

2) Diffusion Capacitance (C_D)

1) Transition Capacitance:

Consider a reverse biased PN Junction as shown in below figure.

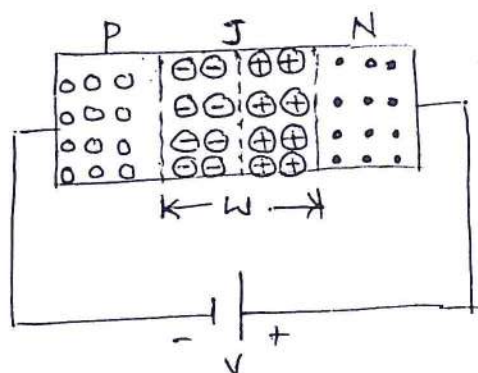


fig: Reverse biased PN junction diode

When a diode is reverse biased, a very small amount of ^{reverse} current flows through the diode which is due to minority charge carriers.

In reverse bias condition the majority charge carriers move away from the junction, this increases the width of the depletion region. The width of the depletion region increases as reverse bias voltage increases.

As the charge particles move away from the junction, there exists a change in charge with respect to the applied reverse voltage. So change in charge (dQ) with respect to the change in voltage (dV) is nothing but capacitive effect.

$$\text{i.e. } C = \frac{dQ}{dV}$$

Such a capacitance comes into picture under reverse biased -

- Condition is known as Transition Capacitance, denoted by ' C_T '.
 It is also called as Space charge Capacitance (or) barrier capacitor.
 (or) depletion region Capacitance. The Transition Capacitance
 is given by $C_T = \frac{\epsilon A}{W}$ Farads

where A = Area of cross section of PN Junction
 ϵ = Permittivity of semiconductor
 W = width of depletion region.

this transition Capacitance is not constant but it depends on the applied reverse voltage.

As the reverse voltage increases, the width of the depletion region is also increased due to which the value of C_T decreases. When the reverse voltage decreases, the width of the depletion region is also decreased, this causes the value of C_T to be increased.

2> Diffusion Capacitance:

During forward biased Condition a Capacitance comes into picture called as diffusion Capacitance denoted by (C_D). It is also called as Storage Capacitance.

In forward bias Condition of a diode, the width of the depletion region decreases as the holes from p-side diffuses into n-side while electrons from n-side diffuses into p-side. As the applied voltage increases the concentration of injected charge carriers increases. This rate of change of the injected charge carriers with applied voltage is defined as a capacitance called "Diffusion Capacitance".

$$\text{i.e. } C_D = \frac{dQ}{dV}$$

The diffusion capacitance is given by the expression

$$C_D = \frac{\tau \cdot I}{\eta V_T}$$

where τ = mean life time of injected charge carrier.

The graph between forward voltage (V_f) and diffusion-capacitance (C_D) and reverse voltage (V_R) and transition-capacitance (C_T) are as shown in below.

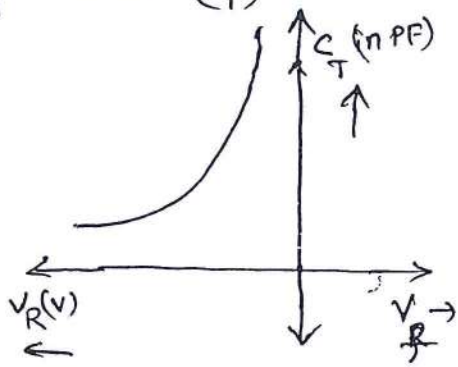


fig: Transition Capacitance against reverse voltage

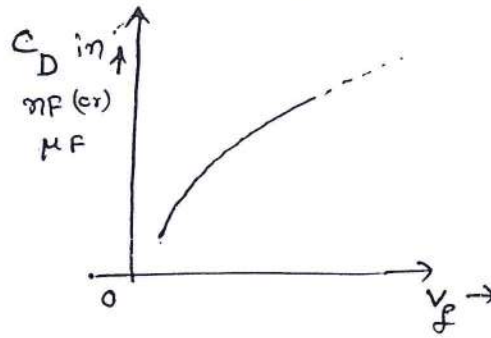


fig:- Diffusion Capacitance against forward voltage.

Zener Diode:

A zener diode is a heavily doped P-N junction diode, which is generally operated in reverse breakdown region.

The symbol for zener diode is as shown in below



fig:- Graphic symbol of zener diode.

In a normal PN junction diode, the doping level is light. As a result of this the breakdown voltage is high. If a P-N junction is heavily doped, the depletion region is thin. So the breakdown voltage will be less.

When the doping is heavy, even the reverse voltage is low the electric field at the barrier will be strong. Thus the electrons in the covalent bonds will break the bond and become free electrons. This effect is known as Zener effect.

and the diodes that exhibit Zener effect is called as Zener diode.

Zener breakdown mechanism:

When a P-N junction is heavily doped, the depletion region is very narrow. The electric field is voltage per distance and due to narrow depletion region at high reverse voltage, the electric field is very high.

Such a strong electric field is enough to pull the electrons out of covalent bonds. Hence under this strong electric field the electrons are released by breaking the covalent bonds, such a creation of free electrons is called Zener effect. These minority charge carriers constitute a large current at higher reverse voltage. At a particular reverse voltage a very large current is constituted that may destroy the junction. This is called as Zener breakdown.

V-I characteristics of Zener diode:

The following figure shows the V-I characteristics of Zener diode.

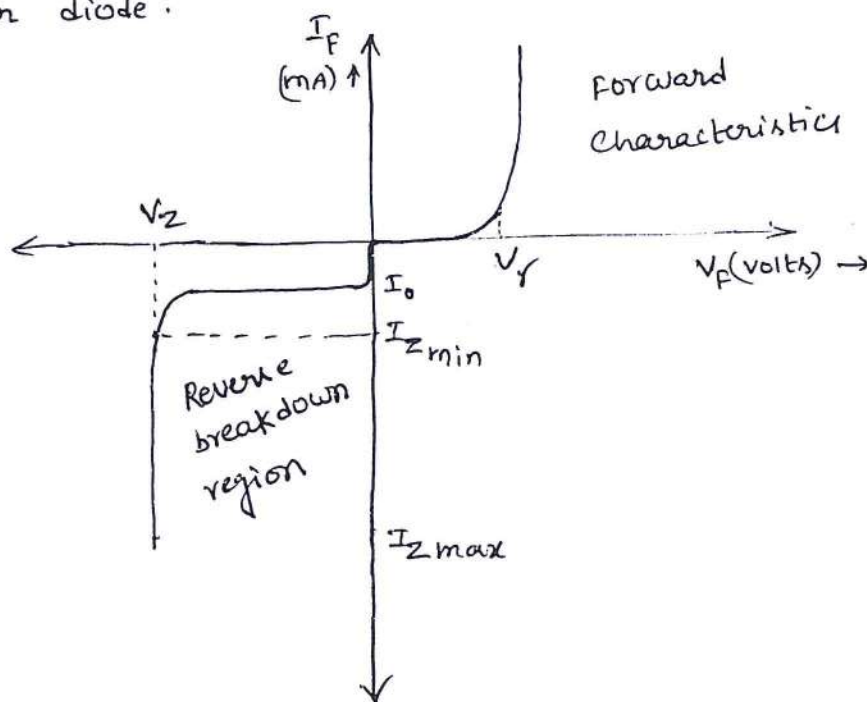


fig:- V-I characteristics of Zener diode

In the forward biased condition, a normal P-N junction diode and a zener diode both the forward characteristics are similar.

A zener diode is operated mainly in reverse bias. In reverse biased condition, the zener diode carries a reverse saturation current (I_0) till the reverse voltage is less than Zener voltage (V_Z). When the reverse voltage exceeds the Zener voltage (V_Z), the current increases drastically but the voltage across the diode remains constant. Usually the breakdown region is the normal operating region for a zener diode. As long as the current through the zener diode is in between I_{Zmin} and I_{Zmax} the voltage across the diode is maintained constant.

Applications of Zener diode:

- 1) As a voltage regulator
- 2) In voltage clipper circuits
- 3) In various protection circuits
- 4) As a reference voltage in comparator circuits.

Zener diode as a shunt regulator:

The following figure shows the shunt voltage regulator circuit that uses zener diode to regulate the load voltage.

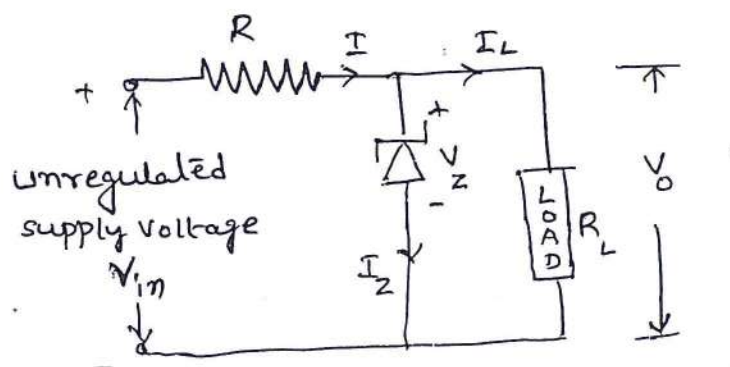


fig:- Zener diode as a shunt regulator.

The shunt regulator using Zener diode regulates the output voltage to a constant value irrespective of the changes in the input or Load.

The Zener diode has a characteristics that as long as the current through it is in between I_{Zmax} and I_{Zmin} , the voltage across it is constant, equal to Zener voltage V_Z .

As Zener diode is connected in shunt with the load resistance the output voltage is equal to the Zener voltage i.e. $V_o = V_Z$.

Voltage regulation with varying input voltage (Line regulation):

The following figure shows the Zener regulator under varying input voltage condition

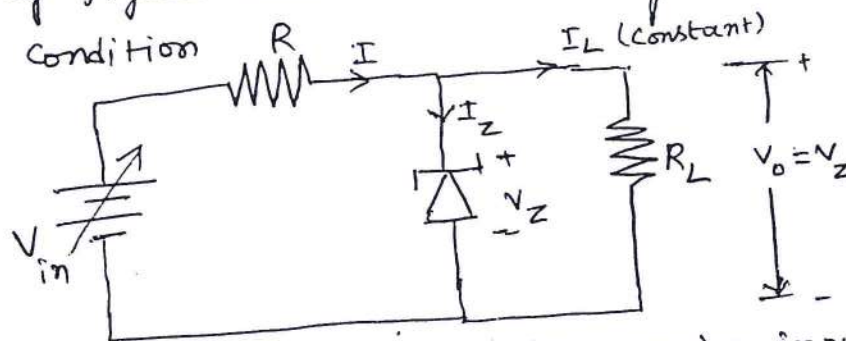


fig: Varying input condition

It is observed that

$$V_o = V_Z$$

$$I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} = \text{Constant}$$

$$I = I_Z + I_L$$

If V_{in} increases, the total current ' I ' increases. But I_L is constant as V_Z is constant. Hence the current I_Z increases to keep I_L as constant.

As long as the Zener current I_Z is in between I_{Zmax} and I_{Zmin} , the output voltage V_o is constant.

Similarly if V_{in} decreases, the total current ' I ' decreases. But to keep I_L constant I_Z decreases. As long as the

zener current (I_Z) is in between I_{Zmax} and I_{Zmin} , the output voltage (V_o) remains constant.

Analysis:

$$I = I_Z + I_L$$

$$I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} = \text{Constant}$$

when V_{in} is at maximum i.e. V_{inmax}

$$I = I_{max} = I_L + I_{Zmax}$$

when V_{in} is at minimum i.e. V_{inmin}

$$I = I_{min} = I_L + I_{Zmin}$$

$$P_{Dmax} = \text{Maximum power dissipation} = V_Z \cdot I_{Zmax}$$

Voltage regulation with varying load resistance:

The following figure shows the zener regulator under the varying load condition.

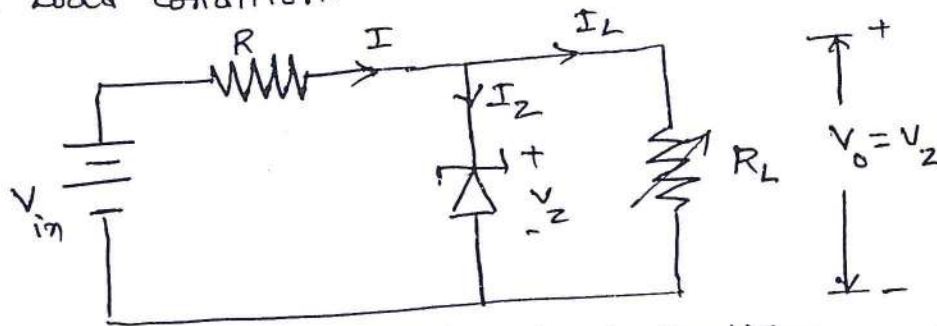


fig:- varying load condition

Here the input voltage V_{in} is constant. Hence I is also constant. The load resistance R_L is variable.

It is observed that $I = I_Z + I_L$

$$\text{and } I = \frac{V_{in} - V_Z}{R}$$

Now if R_L decreases, so I_L increases. But to keep 'I' constant I_Z decreases. As long as I_Z is in between

I_{Zmax} and I_{Zmin} , the output voltage $V_o = V_Z = \text{constant}$.

Similarly if R_L increases, then I_L decreases. But to keep 'I' as constant I_Z decreases. As long as I_Z is in between I_{Zmax} and I_{Zmin} the output voltage $V_o = V_Z = \text{constant}$.

Analysis :

since $V_{in} = \text{constant}$, $I = \frac{V_{in} - V_Z}{R} = \text{constant}$

$$I = I_Z + I_L$$

$$\Rightarrow I_L = I - I_Z$$

When the load resistance $R_L = R_{Lmin}$, $I_L = I_{Lmax}$, and $I_Z = I_{Zmin}$
 $\therefore I_{Lmax} = I - I_{Zmin}$

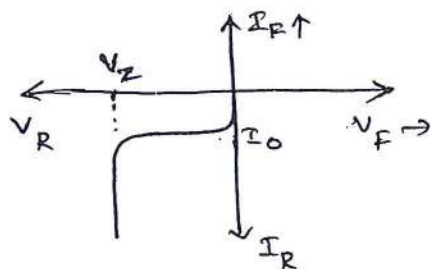
Similarly if $R_L = R_{Lmax}$, $I_L = I_{Lmin}$ and $I_Z = I_{Zmax}$

$$\therefore I_{Lmin} = I - I_{Zmax}$$

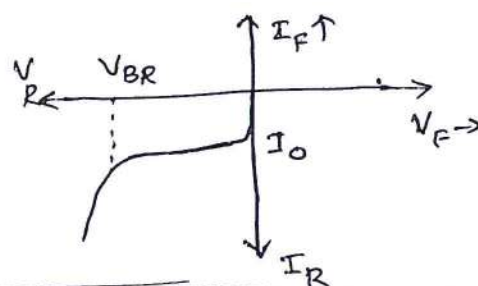
Comparison between Zener breakdown and Avalanche breakdown:

Zener breakdown	Avalanche breakdown
1. It occurs in a heavily doped PN junction diode.	1. It occurs in a lightly doped PN junction diode.
2. Temperature Coefficient is negative	2. Temperature Coefficient is positive
3. It occurs by breaking Covalent bonds due to strong electric field established by applied reverse voltage	3. It occurs by breaking covalent bond due to collision of minority carriers with atoms.
4. Break down Voltage decreases if junction temperature increases	4. Breakdown voltage increases if junction temperature increases
5. The reverse V-I characteristics is very sharp in breakdown region	5. The reverse V-I characteristics is not sharp in avalanche breakdown.

4. The reverse V-I characteristics is shown below



6. The reverse V-I characteristics is shown below.



Tunnel diode (Esaki Diode) :

In a normal PN junction diode, the impurity concentration is about 1 part in 10^8 . So the depletion region width is about 5 microns (5×10^{-4} cm).

In a tunnel diode, the impurity concentration is increased to 1 part in 10^3 . So the depletion region width is reduced from 5 microns to less than $100 \text{ \AA}$ (i.e. 10^{-8} m).

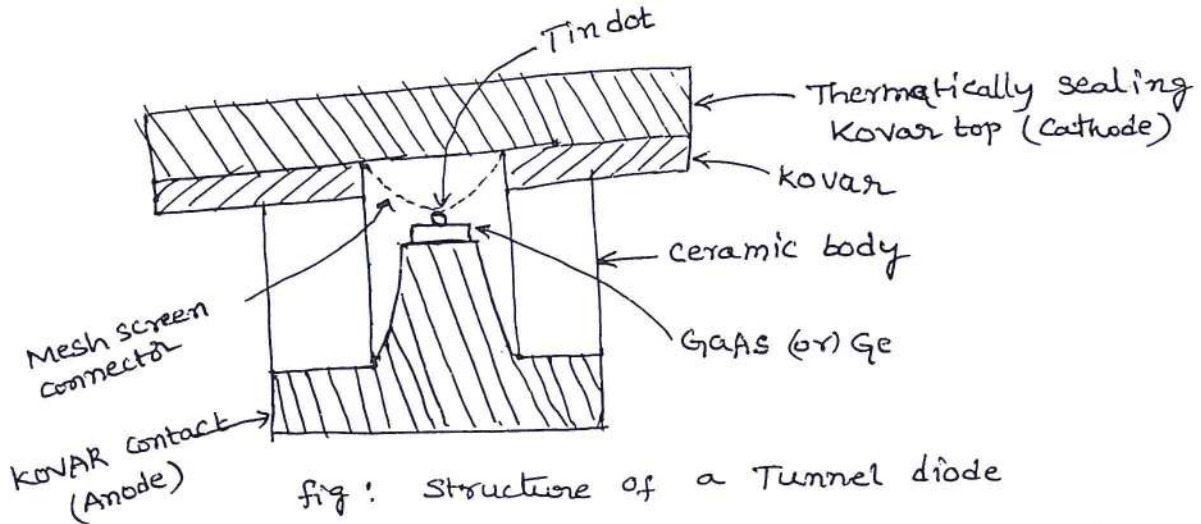
The tunnel diode was first introduced by Leo Esaki in 1958. So the tunnel diodes are also called as Esaki Diode.

Tunneling phenomenon:

Since the depletion region is extremely small, instead of crossing over the junction i.e. instead of surmounting the junction, they penetrate through the depletion region. This quantum mechanical behaviour of electrons is called as tunneling and hence these diodes are called as tunnel-diodes.

The construction of a tunnel diode is discussed below.

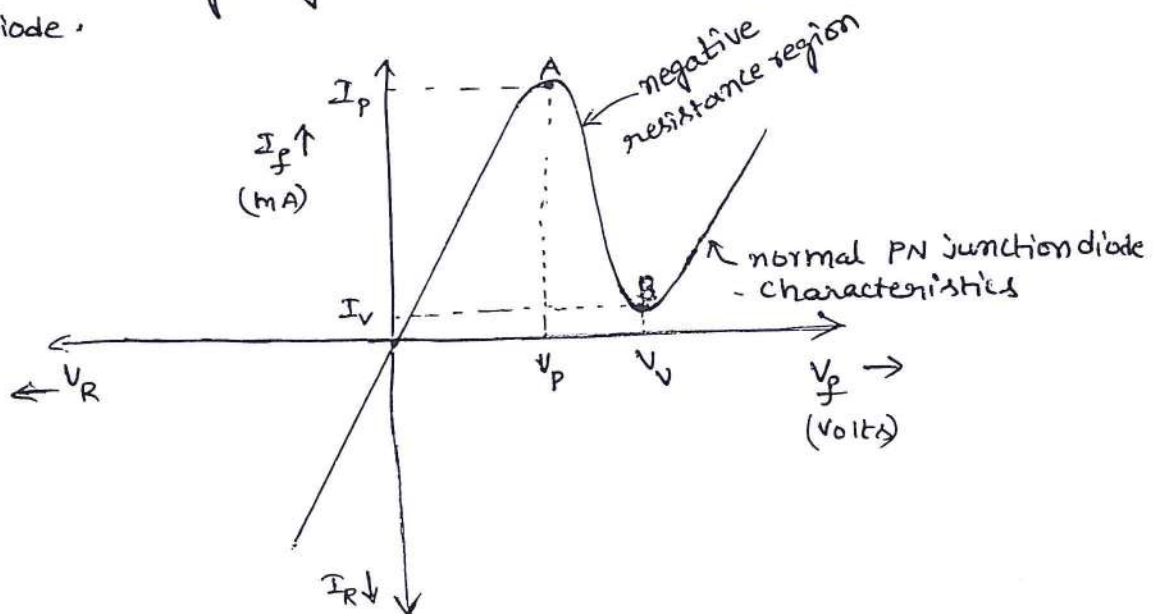
Construction and Symbol of a tunnel diode:



The above figure shows the construction of a typical tunnel diode. A very small tin dot is alloyed to a heavily doped n-type Ge (or) GaAs. It is then soldered to a Kovar pedestal used for heat dissipation which forms the anode contact. The cathode contact is also Kovar. It is connected to the tin dot via mesh screen. The diode has a ceramic body and thermally sealing to the top.

V-I Characteristics of a tunnel diode:

The following figure shows the V-I characteristics of a tunnel diode.



The tunnel diode is a heavily doped diode hence the depletion layer is very thin, hence it causes tunneling. We can clearly

observe that, for small rise in forward voltage, the forward current will be large.) The current rises sharply as the forward voltage is increased further and reaches a point 'A' at which peak current (I_p) is observed. The voltage at point 'A' is V_p .

When the forward voltage is increased further point 'A', the forward current drops and it continues to drop until a point 'B' is reached. The voltage at this point 'B', is known as valley voltage (V_v) and the current is valley current (I_v).

After the valley point if the forward voltage is further increased, the forward current varies as in the case of a normal PN junction diode.

The Tunnel diode exhibits negative resistance characteristics between peak current and valley current (I_p and I_v).

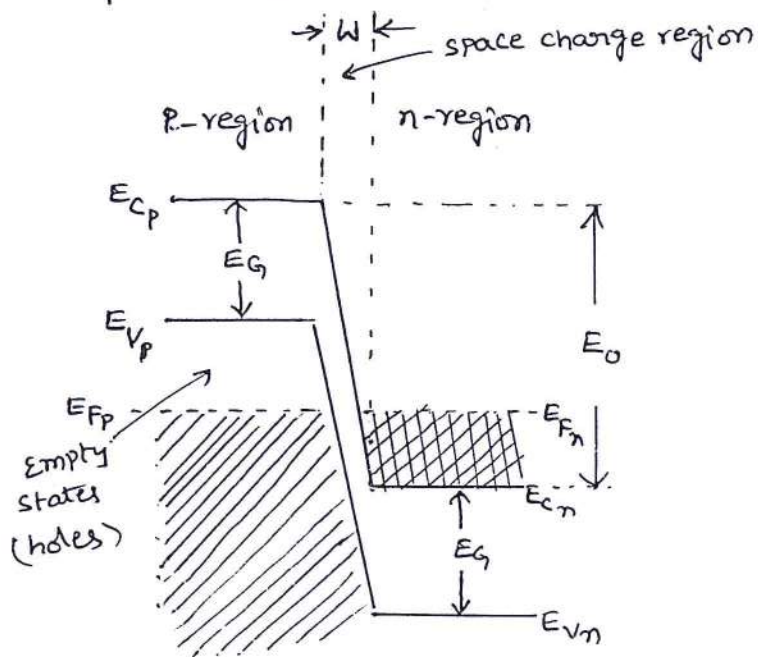
Energy band diagram of Tunnel diode

→ For a lightly doped P-type material the fermi level lies within the forbidden band and closer to valence band. Where as the fermi level for a heavily doped P-type material lies within the valence band i.e. outside the forbidden band.

→ For a lightly doped n-type material the fermi level lies within the forbidden band and closer to the conduction band. Where as in a heavily doped n-type material it lies within the conduction band i.e. outside the forbidden band.

→ Now For a heavily doped PN junction diode such as tunnel diode the fermi level of P-region lies in valence band and the fermi level of n-region lies in conduction band. Under open circuited condition the fermi level in P-side is at

the same energy level as that of the fermi level of the n-region as shown in below energy band diagram. Hence in open circuited condition there won't be any penetration of charge in either direction across the junction.

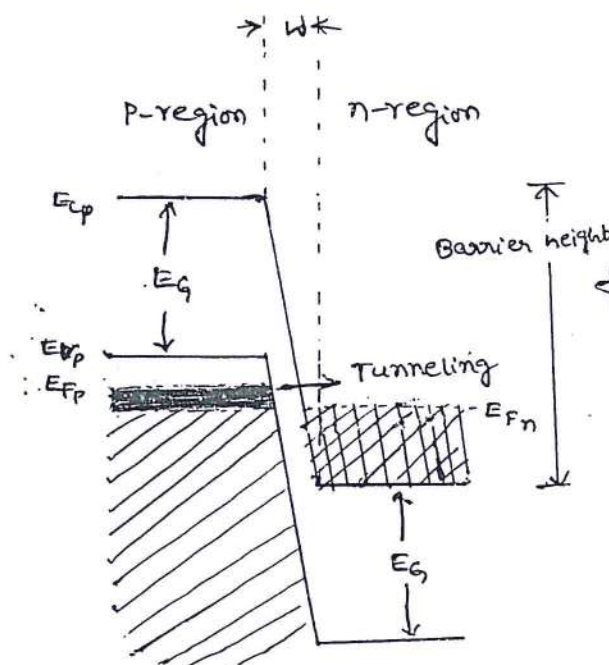


//// - energy states occupied by electrons in valence band of P-region

- energy states occupied by electrons in conduction band of n-region

fig(a): Energy band diagram of tunnel diode under open circuit condition.

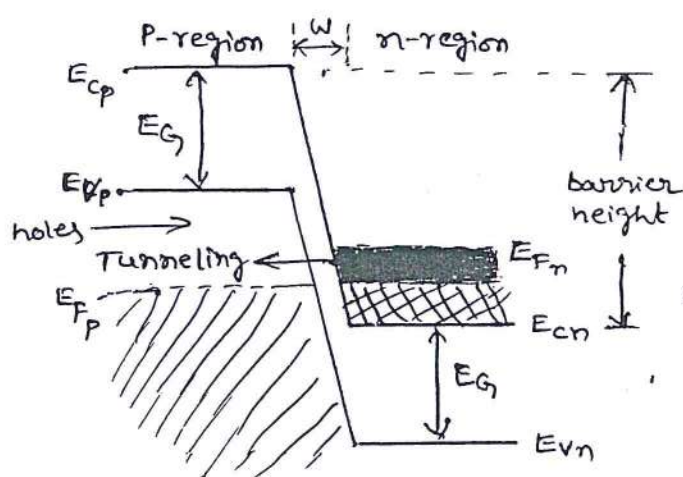
When reverse bias is applied the height of the barrier is increased above the open circuited value E_0 . Hence the n-side levels shift downwards with respect to the P-side levels as shown in below.



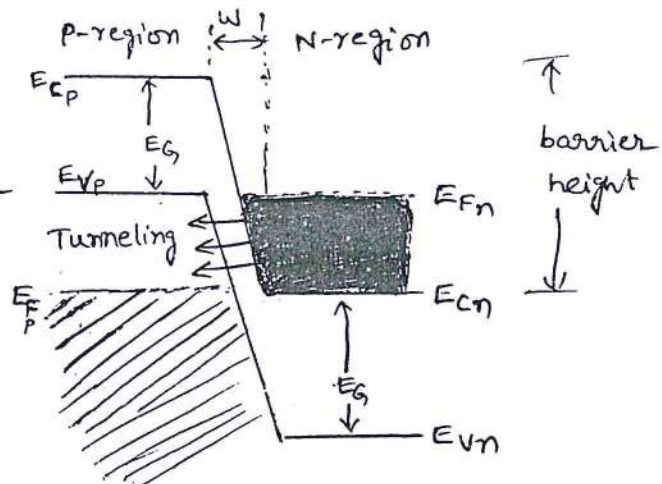
fig(b): Energy band diagram of tunnel diode under reverse biased condition.

We can notice that there are some energy states (portion in dark black colour) in valence band of P-side which lie at the same level as allowed empty states of conduction band of n-side. Hence these electrons will tunnel from P-side to n-side gives rise to a reverse diode current. As the reverse bias increases, the portion in dark black colour increases causing the reverse current to increase.

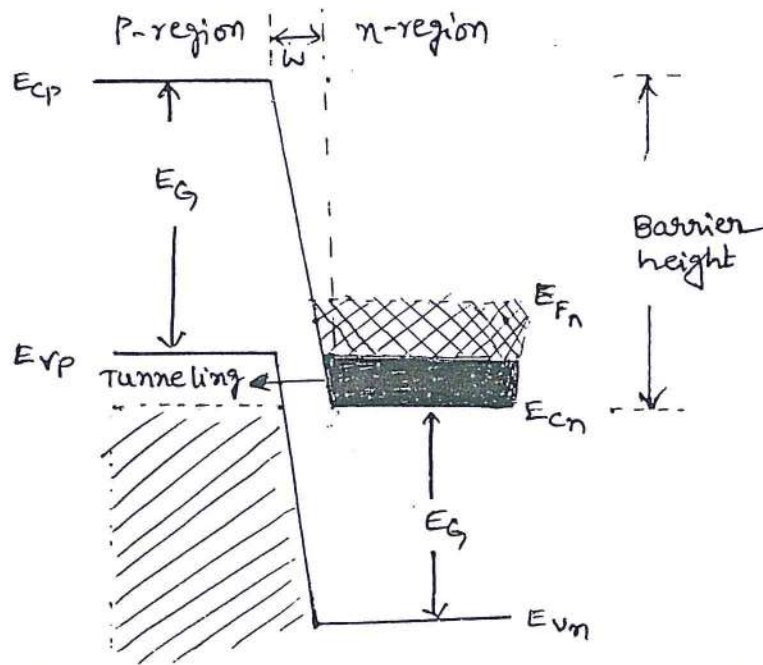
When forward bias is applied to the diode the barrier potential E_0 decreases. Hence the energy levels of n-side shift upwards with respect to those on P-side. Now there are some energy states in the conduction band of the n-side (portion in dark black colour) which are at same energy states as allowed empty states of valence band of P-side. Hence these electrons will tunnel from n-side to P-side gives rise to the forward current. As the forward bias is increased further, n-side level shifts further upward as shown in below figure(d). In this situation maximum number of electrons tunnel from n-side to P-side, that gives rise to peak current ' I_p '. If further more forward bias is applied the situation is shown in fig(e) and the tunnel current decreases.



fig(c): Energy band diagram when small forward voltage is applied across the diode

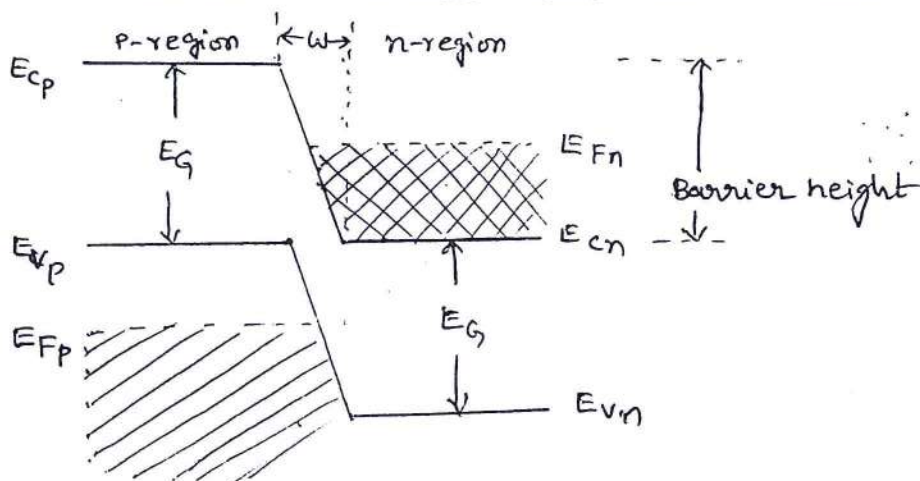


fig(d): Energy band diagram when peak current flows through the diode



fig(e): Energy band diagram when forward voltage is increased above peak voltage

When the forward voltage is increased further there will be no empty allowed states (holes) on P-side in valence band at the same level of energy as that of electrons in conduction band of n-side. So the tunneling current drops to zero as shown in fig(f). Thereafter if we increase the forward voltage, the further characteristics will be similar to that of normal PN junction diode that means the current increases with the increased forward voltage.



fig(f): Energy band diagram when forward voltage is at valley voltage (V_v).

Applications of a tunnel diode:

1. Tunnel diode is used as an ultra high speed switch with switching speed of the order of nsec or psec.
2. It is used in microwave oscillators
3. It is used in relaxation oscillator circuit
4. Can be used as an amplifier.

Photo diode:

The Photo diode is a light sensitive device. It is also called as a Photo detector. It converts light signals into electrical signals.

A Photo diode is essentially operated in reverse biased condition with light permitted to fall on one surface of the device across the junction, keeping the remaining sides unilluminated.

The light is incident through a small glass window on the P-N junction, the photons in the light bombard the P-N junction and some energy is acquired by some of the valence electrons,

Due to this, the valence electrons may break the covalent bonds and become free electrons. Thus the total number of minority charge carriers increases and hence the reverse current increases.

Photo diode symbol and the incidence of light on junction is as shown below.

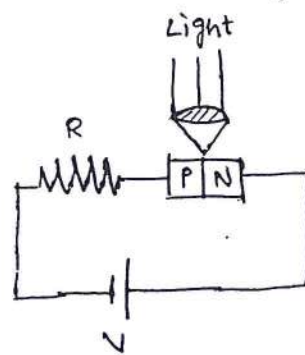
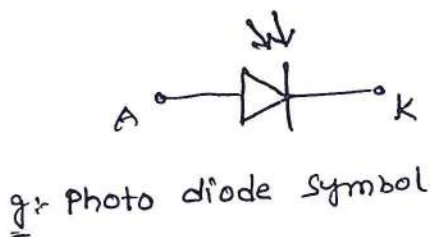


fig: principle of operation

Photo diode characteristics :

- * Photo diode is designed such that it is sensitive to the light.
- * When there is no light, the reverse biased Photo diode carries a current which is very small and called dark current.

The dark current is denoted by ' I_A '. It is purely due to thermally generated minority charge carriers.

* When light is allowed to fall on a P-N junction through a small window, photons transfer energy to the valence electrons using which they break their covalent bonds and become free. Hence the reverse current increases. The reverse current is directly proportional to the light intensity.

* The following figure shows the photodiode characteristics. fig(a) shows the relation between the reverse voltage and reverse current at different light intensities and fig(b) shows the relation between reverse current and light intensity.

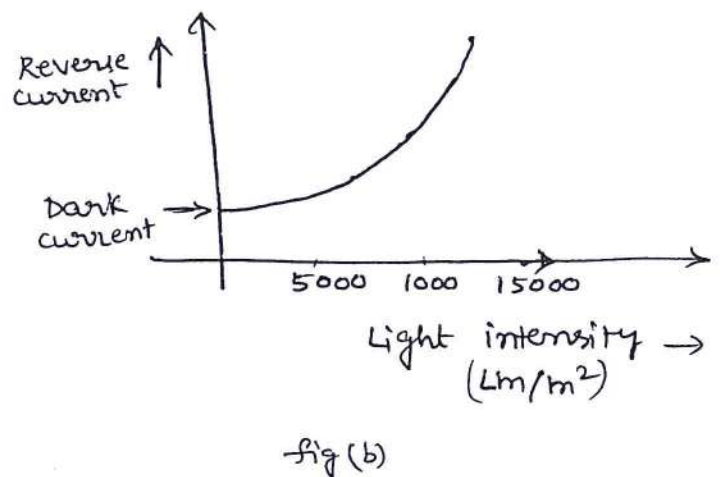
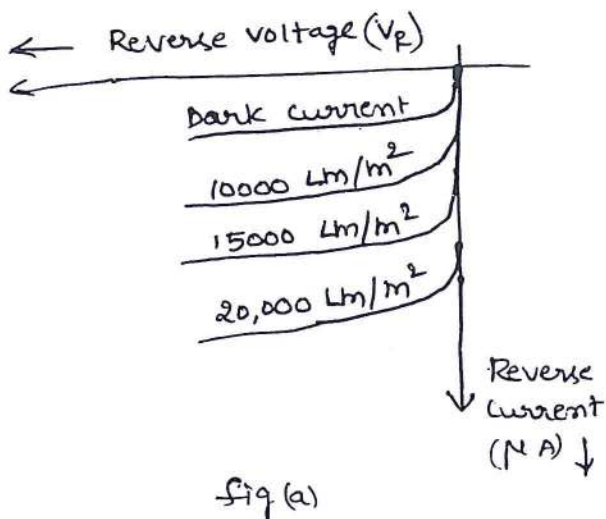


fig: Photodiode Characteristics

Photodiode characteristics tells us that the reverse current is not dependent on reverse voltage and totally depends on light intensity.

P.T.O

Photo diode as a variable resistance device:

Consider a photodiode that has dark current of $20\mu\text{A}$.

(i.e. $I_A = 20\mu\text{A}$) at $V_R = -2\text{V}$.

$$\therefore \text{Dark resistance} = \frac{V_R}{I_A} = \frac{2}{20 \times 10^{-6}} = 100\text{k}\Omega$$

If now photodiode is illuminated with $25,000 \text{ Lm/m}^2$, then the current changes to $350\mu\text{A}$ at same reverse voltage.

$$\therefore \text{Illuminated resistance} = \frac{2}{350 \times 10^{-6}} = 8.914\text{k}\Omega$$

This shows that the photodiode can be used as a variable resistance device controlled by light intensity. It is also called Photo conductive device.

Why photodiode is to be used in reverse bias only?

The reverse current through the diode in the absence of light is in the range of μA . The change in reverse current in the presence of light is also in the range of μA . So the change in reverse current due to incident light can be significantly observed.

If the photodiode is forward biased, the current flowing through it is in the order of mA . The applied forward biased voltage takes the control of the current instead of light. The change in forward current due to incident light is in μA and cannot be noticed. The resistance of forward biased diode is not affected by the light.

So to have a significant effect of light on current and to operate the photodiode as a variable resistance device, it is always connected in reverse biased condition.

Advantages of Photo diode:

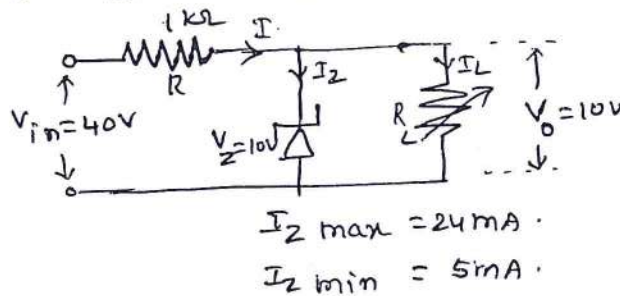
- 1) The photodiode can be used as a variable resistance device.
- 2) It is highly sensitive to the light.
- 3) The speed of operation is very high. The switching of current is fast and hence the resistance value from high to low is very fast.

Applications of photo diode:

- 1) As a variable resistance device
- 2) In light intensity meters
- 3) In high speed logic circuits
- 4) In optical communication system.

Problems on zener voltage regulator

- ① For a zener voltage regulator shown below, determine the range of R_L and I_L that gives a constant voltage of 10V.



Sol:

From the circuit $I = I_Z + I_L$

$$\text{and } I = \frac{V_{in} - V_Z}{R} = \frac{V_{in} - V_O}{R}$$

$$\Rightarrow I = \frac{40 - 10}{1 \times 10^3} = 30 \text{ mA}$$

when R_L is changed, I_L also gets changed.

when R_L is at $R_{L \text{ max}}$, I_L is at $I_{L \text{ min}}$

Then to maintain I constant I_Z will be at $I_{Z \text{ max}}$.

$$\therefore I = I_{L \text{ min}} + I_{Z \text{ max}}$$

$$30 \times 10^{-3} = I_{L \text{ min}} + 24 \text{ mA} \quad \left(\because I_{Z \text{ max}} = 24 \text{ mA} \text{ given} \right)$$

$$\Rightarrow I_{L \min} = 6 \text{ mA}$$

$$\text{But } I_{L \min} = \frac{V_0}{R_{L \max}}$$

$$\Rightarrow 6 \times 10^{-3} = \frac{10}{R_{L \max}}$$

$$\Rightarrow R_{L \max} = \frac{10}{6 \times 10^{-3}} = 1.667 \text{ k}\Omega$$

when R_L is at $R_{L \min}$, I_L will be at $I_{L \max}$. To maintain I constant I_Z will be at $I_{Z \min}$

$$\therefore I = I_{L \max} + I_{Z \min}$$

$$30 \times 10^{-3} = I_{L \max} + 5 \times 10^{-3}$$

($\because I_{Z \min} = 5 \text{ mA}$
given)

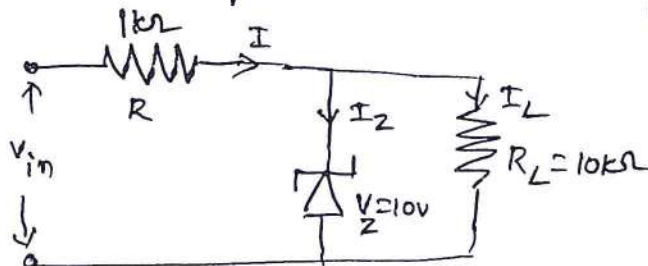
$$\Rightarrow I_{L \max} = 25 \times 10^{-3} \text{ A} = 25 \text{ mA}$$

$$\text{But } I_{L \max} = \frac{V_0}{R_{L \min}}$$

$$\Rightarrow R_{L \min} = \frac{V_0}{I_{L \max}} = \frac{10}{25 \times 10^{-3}} = 400 \Omega$$

$\therefore$ The range of R_L is 400Ω to $1.667 \text{ k}\Omega$ and the range of I_L is 6 mA to 25 mA .

- ② Determine the range of input voltage that maintains the output voltage of 10 V , for a regulator circuit shown below.



$$I_{Z \max} = 24 \text{ mA}, \quad I_{Z \min} = 5 \text{ mA}$$

Solution:

$$\text{As } V_0 = 10 \text{ V}, \quad V_Z = 10 \text{ V}. \quad \text{Given } R_L = 10 \text{ k}\Omega$$

$$\therefore I_L = \frac{V_0}{R_L} = \frac{10}{10 \times 10^3} = 1 \text{ mA}$$

when $V_{in} = V_{in \max}$, $I_Z = I_{Z \max}$, but I_L is constant .

$$I_{\max} = I_{Z \max} + I_L$$

$$\frac{V_{in \max} - V_Z}{R} = 24 \times 10^{-3} + 1 \times 10^{-3}$$

$$\frac{V_{in \max} - 10}{1 \times 10^3} = 25 \times 10^{-3}$$

$$V_{in \max} - 10 = 25 \times 10^{-3} \times 1 \times 10^3 = 25$$

$$\Rightarrow \therefore V_{in \max} = 35 \text{ V}$$

when $V_{in} = V_{in \min}$, $I_Z = I_{Z \min}$

$$I_{\min} = I_{Z \min} + I_L$$

$$\frac{V_{in \min} - V_Z}{R} = 5 \times 10^{-3} + 1 \times 10^{-3}$$

$$\frac{V_{in \min} - 10}{1 \times 10^3} = 6 \times 10^{-3}$$

$$\Rightarrow V_{in \min} = 16 \text{ V}$$

$\therefore$ The range of input voltage is 16V to 35V for which the output voltage will be of 10V.

* Applications PN junction diode:

- 1) PN junction diode is used in rectifiers in dc power supply
- 2) used as a switch in digital logic circuits
- 3) clippers can be designed with PN junction diode.
- 4) PN junction diodes can be used in clipper circuits.
- 5) They can be used in demodulation circuits.

Applications of zener diode:

- 1) zener diode can be used as voltage regulators.
- 2) They can be used in protection circuits to protect the circuit against the variations in the voltage supply.
- 3) The output of zener diode in some circuits, works as a reference voltage.
- 4) It is used for reshaping the wave forms.

Light Emitting Diode (LED):

* The Light Emitting Diode (LED) is a PN junction device which emits light when forward biased, by a phenomenon called electroluminescence.

* In all PN junctions, some of the energy is radiated as heat and some in the form of photons.

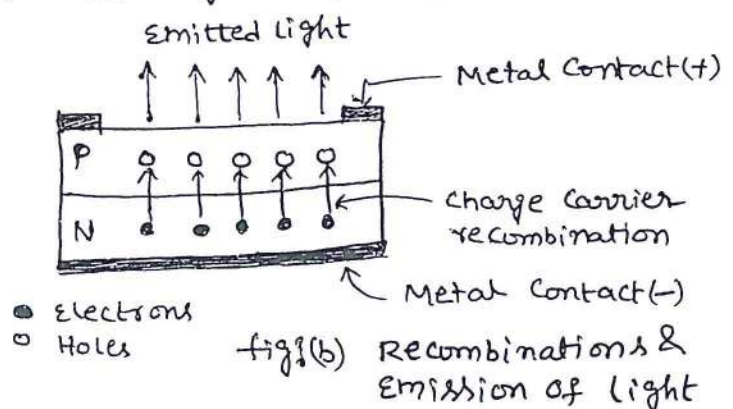
* In Si and Ge, PN junction diodes greater percentage of energy is radiated in the form of heat and the emitted light is insignificant because less amount of energy is radiated in the form of photons.

* In other materials such as Gallium Phosphide (GaP) or Gallium Arsenide Phosphide (GaAsP) the number of photons of light is sufficient to create visible light source.

That means most of the energy is radiated as photons in these kind of materials. The symbol for LED is shown in below in fig(a).



fig(a) LED symbol



Construction of LED:

The above fig(b) shows the basic structure of LED showing recombinations of charge carriers and emission of light. Here an N-type layer is grown on a semiconductor bar and P-layer is deposited on it. Since the carrier recombinations takes place in P-layer it is kept uppermost.

The metal anode connections are made at the outer edges of the P-layer so as to allow the emitted light from the surface area present in between the metal anodes.

LED's are manufactured with domed lenses in order to reduce the re-absorption problem.

A metal (Gold) film is applied at the bottom of the n-layer for providing cathode as well as for reflecting more light to the surface of the device.

Working principle:

* The LED works on the principle of electroluminescence.

* When an LED is forward biased the electrons in n-region cross the junction and recombine with the holes in p-region.

* As a result of recombination, the electrons lying in the conduction bands of N-region fall into the holes lying in the valence band of a P-region.

* For each recombination the difference of energy between the conduction band and valence band is radiated in the form of photon. Due to these emitted photons the light is generated.

* The brightness of the emitted light is directly proportional to the forward bias current.

* LEDs radiate different colours such as red, green, yellow, orange and white. The colour of the emitted light

depends on the type of the material used. Some LED's infrared also.

For example Gallium Arsenide (GaAs) - infrared radiation (invisible).

Gallium Phosphide (GaP) - red (or) green

Gallium Arsenide phosphide (GaAsP) - red or yellow.

* In order to protect LED's, resistance of $1\text{ k}\Omega$ or $1.5\text{ k}\Omega$ must be connected in series with LED.

* LEDs emit no light when reverse biased.

* They are operated at voltage levels from 1.5 V to 3.3 V

Advantages of LED's:

- 1) LEDs can be Switched ON and OFF at Very fast speed of 1 nsec.
- 2) Extremely long life of $1,00,000 +$ hours.
- 3) Very small in size and light weight. They are cheap.
- 4) Depending on the type of material, different colours of light is emitted.

Disadvantages of LED's:

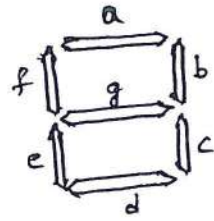
- 1) Very sensitive device i.e. it gets damaged when over voltage or over current occurs.
- 2) Low efficiency. Their characteristics are affected by temperature.
- 3) Need large power compared to normal PN junction diodes.

Applications of LED's:

- 1) As an ON-OFF indicator in various type of electronic circuits.
- 2) In burglar alarm systems
- 3) Multimeters
- 4) Calculators and digital watches, remote controls.
- 5) Optical communication systems and all kinds of visual displays.
- 6) Microprocessors and Digital Computers

Seven segment Display using LED's:

* A display consisting of Seven Segments a, b, c, d, e, f and g is shown in figure.

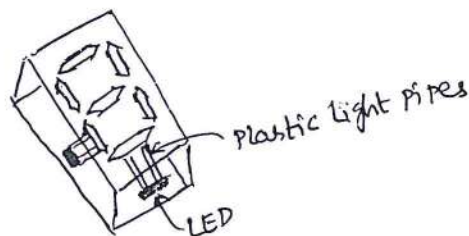


* It is Capable of displaying digits from 0 to 9.

* For each segment an LED⁺ is used. Hence 7 LED's are required for 7-segments.

* By Forward biasing proper segment LED's, we can display the digits from 0 to 9.

* Since the LED's are very small to enlarge the lighted surface solid plastic light pipes are employed.



Seven segment LED display

A two segment display is referred as a half digit. So three seven segment displays along with a two segment display can be used to display numerical values from 0 to 1999.

Problem: Calculate the total power supplied to $3\frac{1}{2}$ digit LED display when it indicates 1988. A 5V supply is used and each LED has current 10mA.

Sol Total number of segments = 2 segments for displaying '1' + 6 segments for 9 + 7 segments for 8 + 7 segments for 8

$$= 2 + 6 + 7 + 7$$
$$= 22$$

For each segment LED current = 10mA.

$$\therefore \text{Total Current} = 22 \times 10 \text{ mA} = 220 \text{ mA}$$

$$\text{voltage supply} = 3 \text{ V}$$

$$\begin{aligned} \therefore \text{Total Power} &= V \cdot I \\ &= 3 \times 220 \times 10^{-3} \\ &= 660 \text{ mW} \end{aligned}$$

$$\therefore \text{Total Power} = 0.66 \text{ Watts}$$

Liquid Crystal Display (LCD):

LCD's are the devices used for displaying numeric and alpha numeric characters.

There are two liquid crystal materials that are usually preferred in LCDs. They are Nematic and Cholesteric.

The molecules in ordinary liquids may have random - orientations, but in liquid crystals the molecules are oriented in a definite crystal pattern.

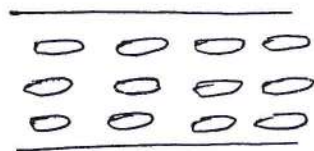


fig: Molecules in liquid crystal when no current flows.

When electric field is applied to the liquid crystal, the molecules tend to align perpendicular to the electric field, so the flow of (electrons) Charge carriers is disrupted by these molecules and causes a turbulence in the liquid.

The molecules in liquid crystal are as shown in below figure.

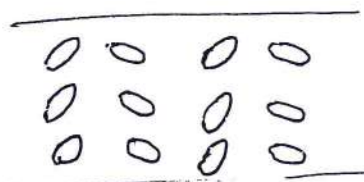


fig: Molecules in liquid crystal disturbed by the charge carriers under applied electric field.

Construction:

- * A liquid crystal cell consists of a very thin layer of liquid crystal material sandwiched between two glass sheets.
- * The glass sheets have transparent metal film electrodes deposited on the inner surface.
- * A polarizer is placed at the surface of each glass sheet.
- * When both the glass sheets of a liquid crystal cell are having transparent metal film electrodes, then that cell is said to be a transmittive type cell.
- * If only one of the glass sheet has the transparent metal film electrode and the other glass sheet has reflective coating, then that cell is said to be a reflective type cell.

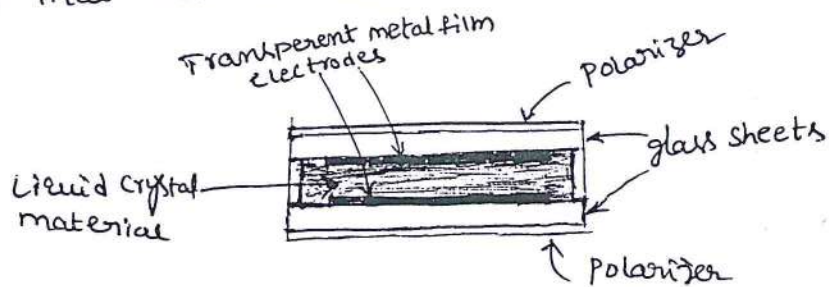


fig:- Liquid crystal cell cross section view.

Operation of LCD:

* Generally a liquid crystal cell is said to be activated when the electric field is applied. And it is not activated when proper electric field is not applied.

* In a transmittive type cell when the cell is not activated, the incident light is simply transmitted through the cell in a straight line manner. In this case the cell will not appear bright against the bright background.

* When the transmittive type cell is activated, the incident light is scattered in all the directions within the cell. Hence

it appears bright. This phenomenon is called dynamic - scattering. In transmittive type cell the light is incident from the back of the cell.

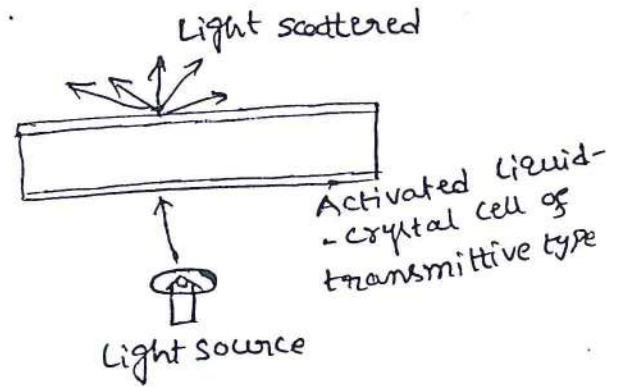
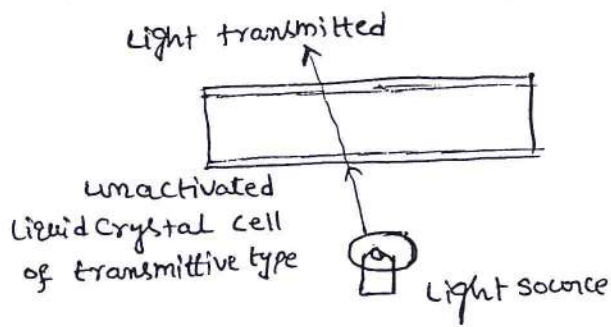


fig:- transmittive type

* In reflective type cell, when it is not activated the light is reflected from the surface and hence cell does not appear brightly.

* when a reflective type cell is activated the dynamic scattering phenomenon occurs and the cell appears brightly.

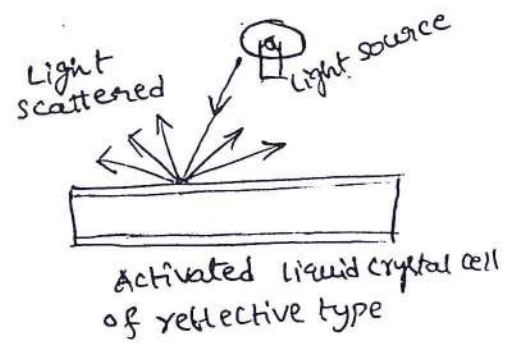
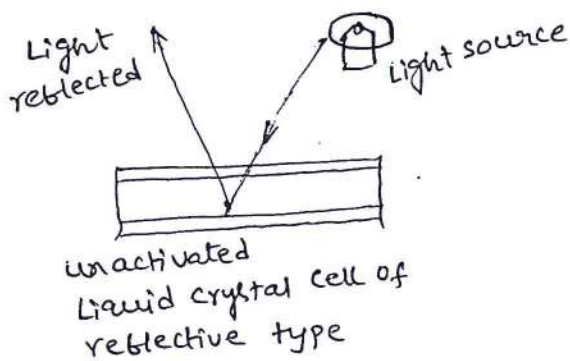


fig:- reflective type

Advantages of LCD :

- 1) It consumes very less amount of power when compared to LED.
- 2) It can be fabricated in almost any convenient size
- 3) The total current flow through 4 small 7-segment LCD displays is about 20mA only.

Disadvantages of LCD

- 1) The major disadvantage of LCD is its decay time 150ms or more. In fact the human eye can sometimes observe the fading out of LCD segments switching off.
- 2) The life time of LCD is very less when compared to LED.

Seven segment displays using LCD:

To design a seven segment display using LCD, we require seven Liquid crystal cells, each cell for a segment.

The LCD's require AC supply in the form of either sine wave or a square wave. Because the continuous DC supply may cause damage to LCD, AC supply is preferred.

The typical LCD supply is 3V to 8V peak to peak square wave with a frequency of 60Hz.

In 7-segment LCD display there is a back plane which is common to all the cells, is applied with a square wave.

Similar square waves are also applied to each of the cell.

The cells that are having the square waves in phase with the square wave of the back plane, have no voltage developed across them. Hence they are not energized and not bright.

The cells that are having square waves out of phase with the square wave of the back plane, have voltage that is developed across each of them. Hence they are energized and bright.

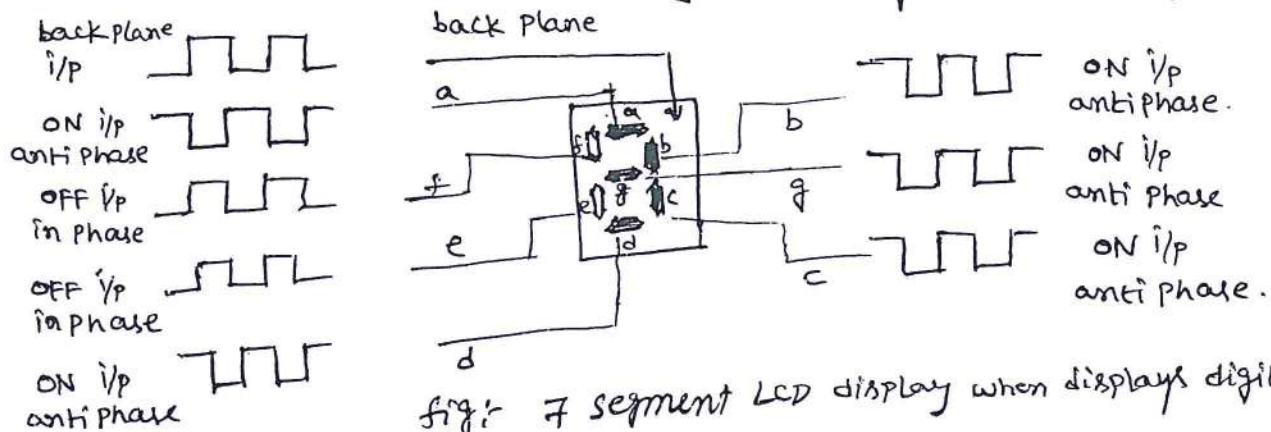


fig: 7 segment LCD display when displays digit '3'.

Problem : calculate the total power supplied to a $2\frac{1}{2}$ digit LCD display indicating 1999. The supply is a square wave with 8V peak level and the current to each segment is 5mA.

Sol Total segments in 1999 = 2 segments for '1' + 6 segments for each '9'

$$= 2 + (6 \times 3)$$

$$= 20$$

For each segment required Current = 5mA

For 20 segments total Current = $20 \times 5 \times 10^{-6} = 100 \mu A$

Voltage Supply = 8V.

$$\therefore \text{Total Power } P_{\text{total}} = V \cdot I = 8 \times 100 \mu$$

$$= 800 \times 10^{-6}$$

$$= 8 \times 10^{-4}$$

$$= 0.8 \text{ mW } \underline{A_3}$$

Applications of LCD:

- 1) The LCD's are widely used in electronic toys
- 2) Televisions
- 3) Calculators
- 4) Desktop Computers
- 5) Watches.
- 6) Portable instrument displays.

Varactor Diode:

The Varactor diode can also be called as a Varicap (or) tuning (or) Voltage variable capacitor diode. It is also a junction diode, but it has a useful property that its transition capacitance is easily varied.

The symbol for Varactor diode is shown in fig(a)



fig (a): Symbol

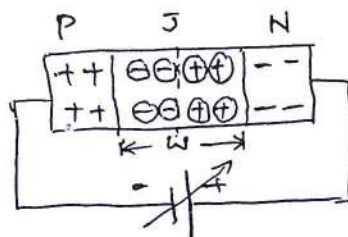


fig (b): Depletion region in a reverse biased PN Junction.

When any diode is reverse biased, the depletion region is formed as shown in above fig(b). The larger the reverse bias voltage, the width of the depletion region 'w' becomes wider. Conversely by decreasing the reverse bias voltage, the depletion region width 'w' becomes narrower. This depletion region is having no mobile charge carriers, having only immobile ions. Hence the depletion region acts like an insulator preventing the conduction between P-region and N-region just like a dielectric. The P-region and n-regions of the diode, act as plates of a capacitor. Hence there exist a capacitance at P-N junction, called Transition Capacitance (or) barrier capacitance (or) Space Charge Capacitance (or) depletion region capacitance denoted by C_T .

Mathematically C_T can be written as $C_T = \frac{\epsilon A}{w}$

ϵ = Permittivity of semiconductor

A = Cross sectional area of PN junction

w = width of depletion region.

As Capacitance C_T is inversely proportional to the width of the depletion region i.e. $C_T \propto \frac{1}{W}$. When reverse voltage is increased, that results an increased depletion region width due to which C_T decreases.

At zero volt, the diode depletion region width 'W' is small, and the capacitance is large approximately 600 pF.

When reverse voltage across the varactor diode is 15V, the capacitance is 30 pF. The characteristics of Varactor diode is shown in below fig.

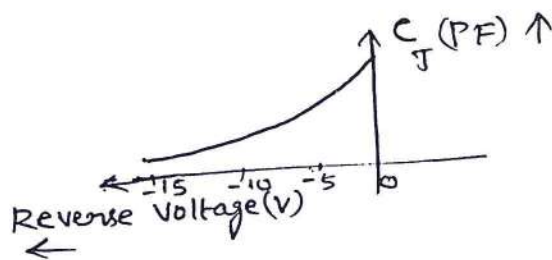


fig: characteristics of Varactor diode.

Applications :-

The Varactor diodes are used in

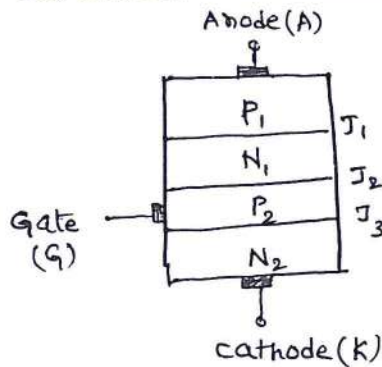
- 1) FM Radio 2) TV receivers 3) Automatic Frequency Control (AFC) circuits
- 4) Adjustable Band Pass filters
- 5) Self Adjusting bridge circuits 6) Tuning of LC resonant ckt's.

THYRISTORS :

A Thyristor in general is a semiconductor device having three or more junctions. Such a device acts a switch which is fabricated to operate under voltage range of several hundred volts and current range from few amperes to almost thousand amperes. The family of thyristors consists of PNPN diode (Shockley diode), SCR, DIAC, TRIAC, UJT, LASCR etc.

Silicon Controlled Rectifier:

The basic structure of SCR and its circuit symbol is as shown in below figure.



fig(a): basic structure of SCR



fig(b): circuit symbol of SCR

An SCR is a four layer, three terminal device, in which the outer layers are heavily doped (in figure P₁, N₂) and the inner layers are lightly doped (N₁, P₂).

The three terminals are namely Anode (A), Cathode (K), and Gate (G).

The outer P-layer acts as anode (A), the outer N-layer acts as Cathode (K) and the P-layer nearer to Cathode acts as gate (G).

The leakage current in Silicon is very small when we compare it with Germanium. SCR is made of Si, but not Ge.

The characteristics of SCR :

- * SCR acts as a switch when it is forward biased.
- * When the Gate terminal (G) is open, i.e. Gate current $I_G = 0$, then the operation of SCR is similar to PNP diode (Shockley diode).
- * When external voltage is applied to the SCR in such a way that anode is positive with respect to Cathode, the junctions J₁ and J₃ are forward biased but J₂ is reverse biased. In this case SCR is said to be forward biased.

so the current flowing through the device is only reverse saturation current. As the applied voltage is increased, the current increases slowly until a voltage called firing voltage (or) break over voltage denoted by V_{BO} . After V_{BO} if we increase the applied voltage the current increases abruptly and the voltage across the SCR decreases sharply. At this point the SCR switches from 'OFF' state to 'ON' state. Once the SCR is turned ON the minimum current known as holding current I_H has to be flown through the device, to keep it in ON state.

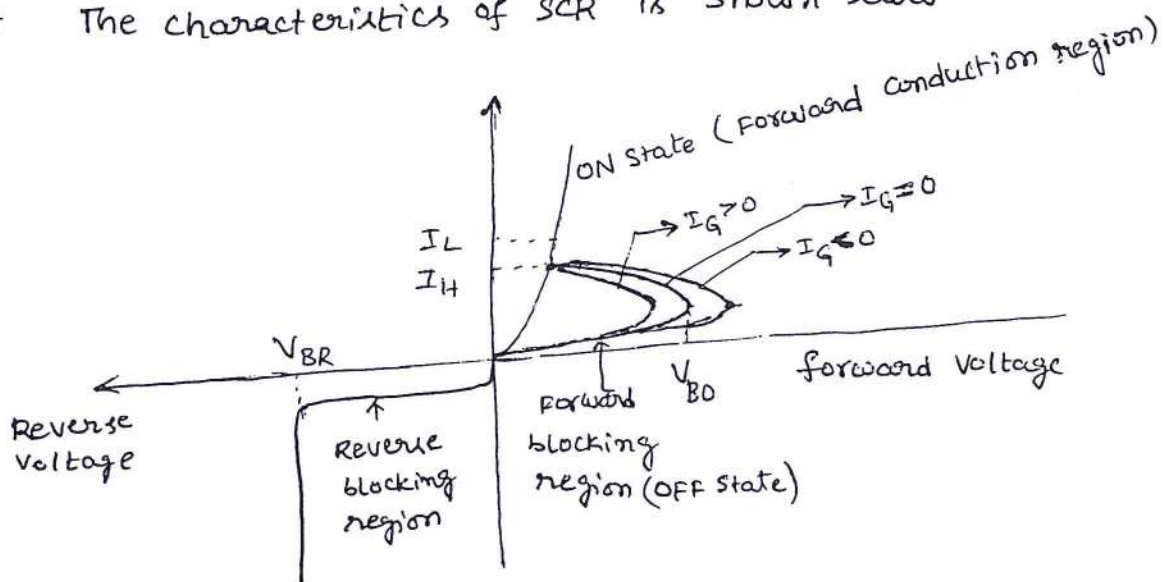
To turn the SCR from ON state to OFF state, the applied voltage has to be reduced such that the current is reduced below the holding current I_H . Thus SCR acts as a switch during forward biased condition while gate current $I_G = 0$.

- * when $I_G < 0$, and SCR is forward biased, the amount of reverse bias applied at junction J_2' is increased. So the break over voltage (V_{BO}) is increased than that of the case $I_G = 0$.
- * when $I_G > 0$ and SCR is forward biased, the amount of reverse bias applied to J_2' is decreased. So V_{BO} is decreased than that of the V_{BO} of the case $I_G = 0$.
- * At a very large positive gate current ' I_G ', V_{BO} may occur at very low voltage such that the characteristics of SCR is similar to that of ordinary PN Junction diode.
- * When the external voltage is applied to the SCR in such a way that the anode is negative with respect to cathode the SCR is said to be in reverse biased condition. In this case the junctions J_1 and J_3 are reverse biased and J_2 is forward biased. In this case a small reverse saturation

- Current flows through SCR. As the reverse voltage increases at a particular reverse voltage called break down voltage the current increases rapidly that may cause damage to the device.

* The SCR has its application only when it is connected in forward biased condition. As the voltage at which SCR is turned 'ON' can be controlled by varying gate current I_G , SCR is commonly called as Controlled switch.

* The characteristics of SCR is shown below.



* NOTE :

- 1) The region of reverse characteristics of SCR before breakdown is occurred is known as "reverse blocking region".
- 2) The region of reverse characteristics of SCR during which the breakdown is occurred is known as "reverse breakdown region".
- 3) The region of forward characteristics of SCR before the occurrence of break over voltage V_{BO} is called "Forward - blocking region".
- 4) The region of forward characteristics of SCR when it is switched 'ON' is known as forward conduction region.
- 5) Once the device turns 'ON' even if we remove the gate

current (I_G), it remains in ON state only. Hence the gate current loses its control when SCR turns 'ON'.

SCR Parameters

1) Forward break over voltage:-

It is the voltage above which the SCR enters the conduction region (ON state). The forward break over voltage in SCR, depends on gate current ' I_G '.

2) Holding current (I_H):

It is the current below which the SCR switches from the conduction state (ON state) to the forward blocking state (OFF state).

3) Latching current (I_L):

It is the minimum current flowing from anode to cathode when SCR goes from OFF to ON state and remains in ON state even if the gate current is removed. It is greater than I_H but very closer to I_H .

4) Reverse breakdown voltage (V_{BR}):

It is the reverse voltage above which the reverse break down occurs breaking the junctions J_1 and J_3 . Because J_1, J_3 are reverse biased when SCR is in reverse biased condition.

Applications of SCR:

1) It is used in AC voltage stabilizers

2) It is used as controlled rectifier.

3) Used as dimmerstats to control light intensity

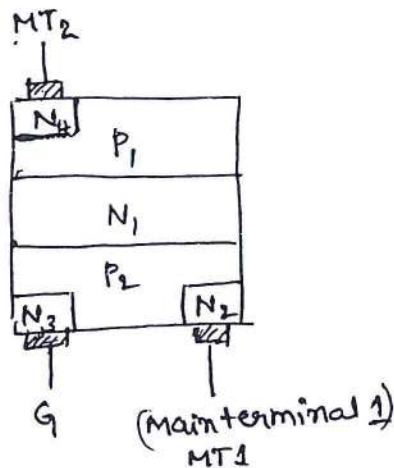
4) Used to control the speed of dc and ac motor

5) It can be used as a static switch

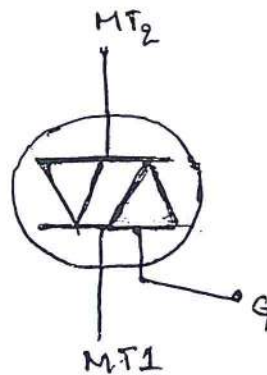
6) It is used in protection circuits and in heat controlling circuits.

TRIAC (TRIODE AC SWITCH) :

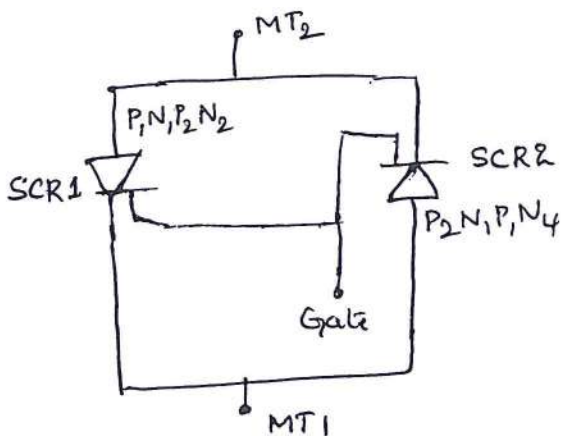
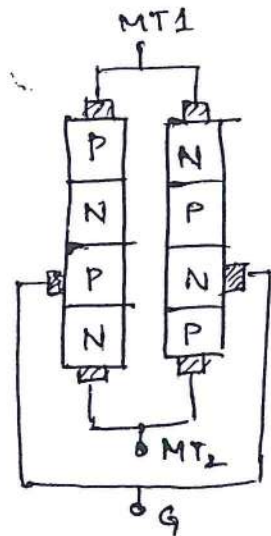
- * TRIAC is a 3 terminal device. It conducts in either direction when it is turned 'ON'. So TRIAC is a bidirectional semiconductor device.
- * An SCR Controls DC power where as a TRIAC Controls AC power.
- * The three terminals of TRIAC are named as Main terminal 1 (MT1), Main terminal 2 (MT2) and Gate.
- * A TRIAC is equivalent to two SCRs connected in parallel but in reverse direction. So a TRIAC will act as a switch for both directions.
- * The basic structure and circuit symbol of a TRIAC are shown in below figures (a), (b)



Fig(a) basic structure of TRIAC.



Fig(b) circuit symbol, Fig(c) TRIAC equivalent to two SCRs connected in parallel & in opposite manner



Fig(d) Equivalent circuit

- * SCR is more reliable when compared to TRIAC.
- * TRIACs are used in the field of power electronics for control purpose.

Working and V-I characteristics of TRIAC:

Like SCR, TRIAC also conducts only when the voltage is increased beyond the break over voltage. Earlier to that, only a very small leakage current flows through the device and therefore remains in OFF state. When the device starts conducting it allows a very large amount of current to flow through it.

During the positive half cycle of applied AC signal MT_1 is positive with respect to MT_2 , whereas MT_2 is positive with respect to MT_1 during negative half cycle. So during positive half cycle there is a flow of current in the direction $P_2N_1P_1N_4$. And during negative half cycle there is a current flow in the direction $P_1N_1P_2N_2$. So TRIAC is a bidirectional device. It can be triggered by either positive gate signal or by negative gate signal.

By applying proper signal at Gate, the break over voltage can be changed.

The characteristics of TRIAC are as shown below.

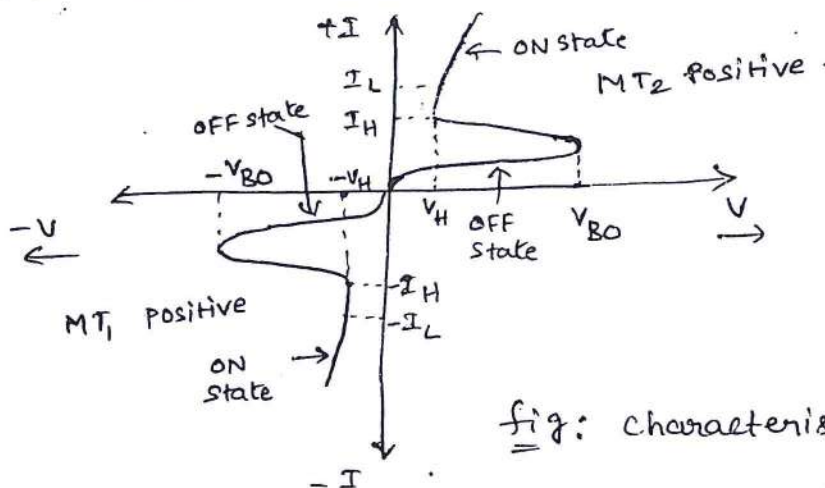


fig: characteristics of TRIAC.

APPLICATIONS OF TRIAC: TRIAC can be widely used in

- ① Temperature Control
- ② Liquid level Control
- ③ Motor speed - control
- ④ As a static switch to turn AC power ON and OFF.
- ⑤ For illumination control

DIAC (DIODE AC SWITCH) :

(41)

* DIAC is a two terminal, bidirectional semiconductor device. It has two terminals namely Main terminal 1 (MT₁) and main - terminal 2 (MT₂).

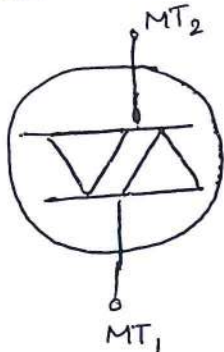
* DIAC has no control terminal such as Gate terminal.

* MT₁ and MT₂ are interchangeable.

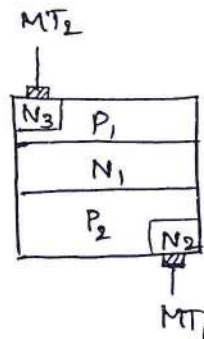
* As the doping level at the two ends of the device is same, the DIAC has identical characteristics for both positive and negative half of an a.c cycle.

* A DIAC can be considered as a parallel connection of two PNPN diodes but in opposite direction.

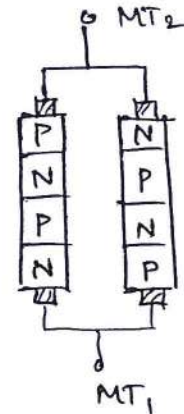
* The symbol and the basic structure of DIAC is as shown in below.



fig(a) circuit symbol of DIAC



fig(b) : basic structure of DIAC



fig(c): DIAC as a parallel connection of two PNPN diodes in reverse direction.

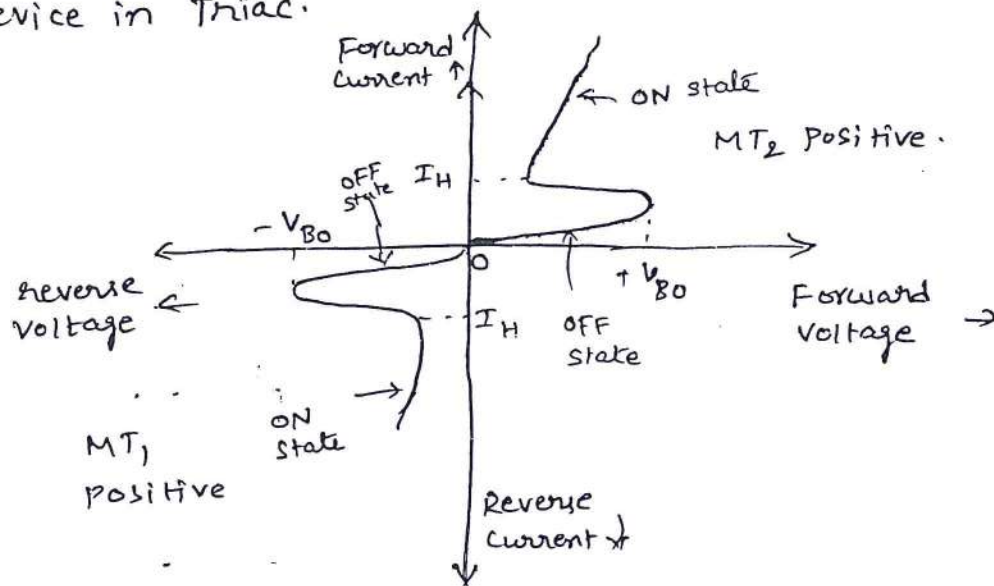
Working and characteristics of DIAC :

During positive half cycle of an AC signal MT₁ is positive with respect to MT₂ where as MT₂ is positive with respect to MT₁ during negative half cycle. During positive half cycle there is a current flow through the device in the direction of P₂N₁P₁N₃ and during negative half cycle the current flows through the device in the P₁N₁P₂N₂ direction. Hence DIAC is bidirectional.

At a voltage less than V_{BO} , a very small amount of current called leakage current flows through the device and the device remains in off state.

When the voltage level is increased beyond V_{BO} the device starts conducting and the current beyond V_{BO} increases rapidly and the voltage across the device decreases sharply.

The DIAC is not a control device. It is used as a triggering device in TRIAC.



Applications of DIAC:

DIAC can be used in

- 1) Triggering of TRIAC
- 2) Motor Speed Control
- 3) Temperature Control
- 4) Light dimming circuits

Disadvantages of TRIAC:

- 1) Not suitable for DC power applications
- 2) Gate has no control over the conduction when TRIAC is ON
- 3) TRIACs have very small switching frequencies
- 4) When compared to SCR, TRIAC has low power handling capacity
- 5) Reliability is less than SCR.

Uni Junction Transistor: (UJT)

- * UJT is a three terminal semiconductor switching device.
- * As UJT has only one PN-junction and three terminals it is commonly called as a uni junction transistor.
- * The three terminals are Base 1, Base 2, Emitter.
- * It consists of a highly doped N-type silicon bar with a heavily doped P-type material alloyed to its one side, closer to B_2 terminal for producing a PN junction.
- * The basic structure and circuit symbol is as shown below.
- * The arrow indicates the direction of the conventional current and the leg of the emitter is drawn at an angle to the vertical.

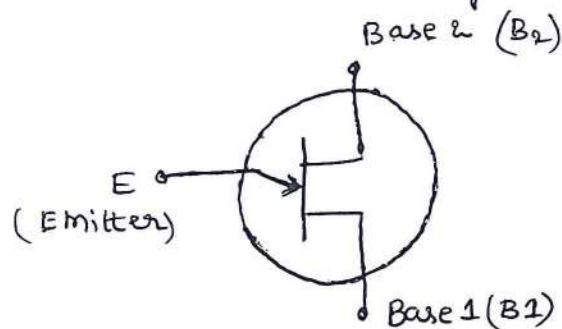
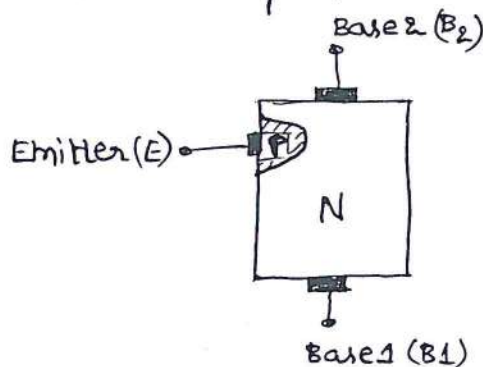


fig (a): Basic structure of UJT

fig(b): Circuit symbol of UJT.

characteristics of UJT:

The base resistance between two base terminals of UJT is $R_{BB} = R_{B1} + R_{B2}$.

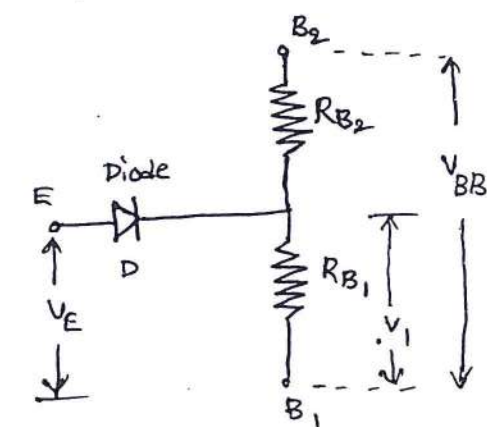
- ⊗ If Emitter terminal is open, and if V_{BB} is applied between base 1 and base 2 terminals, the voltage drop across R_{B1} is given by

$$V_1 = \frac{R_{B1}}{R_{B1} + R_{B2}} \cdot V_{BB}$$

$$V_1 = \eta V_{BB}$$

where $\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$

' η ' is known as intrinsic stand off ratio.



fig(c): Equivalent circuit of UJT.

The typical value of ' η ' is 0.56 to 0.75.

The voltage V_1 reverse biases the PN junction and a small leakage current flows from B_2 to emitter due to minority charge carriers.

⊗ If a positive voltage is applied to the emitter (i.e. V_E), the PN junction will remain reverse biased as long as V_E is less than V_1 . If V_E exceeds V_1 by cut-in voltage V_Y i.e. ($V_E > V_1 + V_Y$) the diode becomes forward biased. Under this condition, holes are injected into N-type bar. These holes are repelled by B_2 terminal and are attracted towards B_1 . Accumulation of holes from Emitter to B_1 region reduces the resistance in between the region^{of} emitter and B_1 . Hence the emitter current increases. The device is now in ON state.

⊗ If a negative voltage is applied to the emitter, PN junction remains in reverse biased and the emitter current is cut off. The device is now in 'OFF' state. The following figure shows the characteristics of UJT.

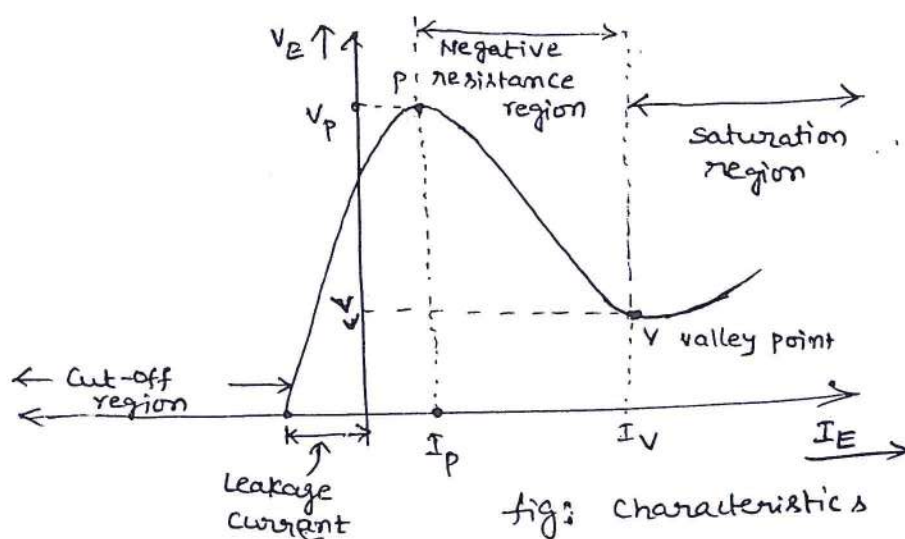


fig: characteristics of UJT

Here upto the peak point 'P', the diode is reverse biased. (P)

Hence the region left to the peak point_x is called as cut-off region.

At point 'P', the peak voltage $V_P = \eta V_{BB} + V_Y$ where the diode is

neither forward biased nor reverse biased. After Peak voltage ' V_P ' the diode starts conducting and holes are injected into N-layer towards B_1 terminal. Hence resistance decreases, thereby decreasing V_E for increase in ' I_E '. So the region between the points 'P' and 'V' is called as negative resistance region. After Valley point, the diode is driven into saturation region and behaves like conventional forward biased PN junction diode. The region to the right side of the valley point is called as saturation region.

Applications of UJT:

- * UJT is used in Sawtooth wave generator
- * It is used in pulse generator.
- * It is used in triggering of other devices like SCR.
- * UJT is used in a relaxation oscillator.
- * Timing and phase control circuits.

RECTIFIERS AND FILTERSIntroduction:

- * All electronic circuits need dc power supply which can be provided using batteries.
- * While using batteries there may be frequent replacement of the batteries is required. So we can not depend on batteries as they are not economical as well as inconvenient to replace every time.
- * So, many of the electronic equipment contain circuits, which convert the ac supply voltage into dc voltage at the required level.
- * In the absence of batteries also such circuits are very helpful.
- * The power supply unit that the circuits that converts the ac supply voltage to dc voltage is called as Linear Mode Power supply (LMPS).

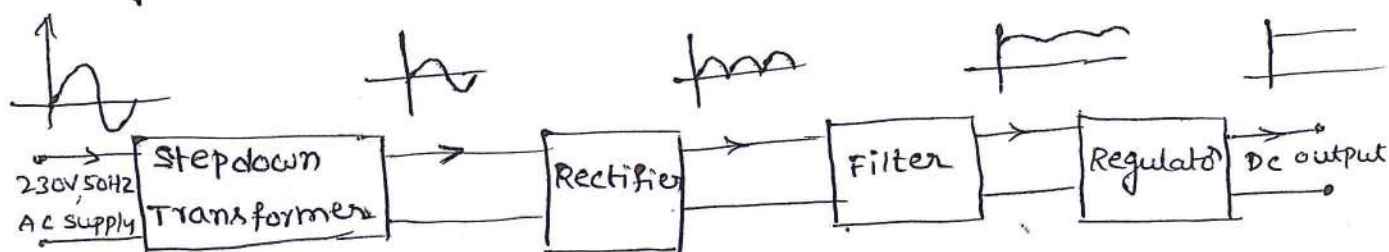
Basic rectifier setup (or) Linear mode power supply block diagram:

fig:- Basic block diagram of rectifier set up.

- * The basic block diagram of a rectifier set up is as shown in above figure.

When the AC supply is fed to a transformer, that AC signal level is made to the required level. Generally the stepdown transformer is most preferable. The stepdown transformer reduces the

voltage level of the AC supply to the desired level.

* The output of the transformer is passed to a rectifier. A rectifier may consist of one diode (or) two diodes (or) four diodes. The output of the rectifier is pulsating DC which is unidirectional, whereas the AC supply is bidirectional.

* This pulsating DC output of the rectifier contains unwanted AC components along with DC that can be removed (or) reduced by using filters, but not completely.

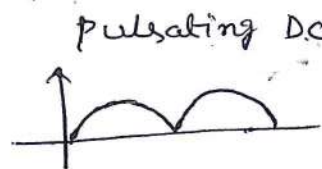
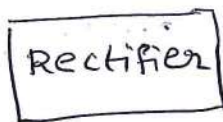
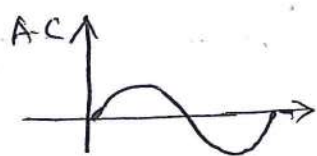
* The output of the filter is fed to a regulator which gives a steady DC output independent of load variations and input supply fluctuations. Usually the Zener diode is used as a voltage regulator.

Rectifiers:

A rectifier is defined as an electronic device which converts AC voltage into pulsating DC voltage.

(or)

A rectifier is defined as an electronic device which converts a bidirectional signal into unidirectional signal.



Rectifiers are classified into two types.

1. Half wave rectifier (HWR)
2. Full wave rectifier (FWR)

The full wave rectifier is again classified into two types.

- i) Centre tapped full wave rectifier
- ii) Full wave bridge rectifier.

1) Half wave Rectifier:

It converts an AC voltage into a pulsating DC voltage using only one half of the applied AC voltage. The rectifier circuit for Half wave Rectifier consists of a diode. This diode conducts during only one half of the ac cycle. Hence this rectifier is named as Half wave rectifier.

The below figure shows the half wave rectifier circuit and input, output wave forms of half wave rectifier.

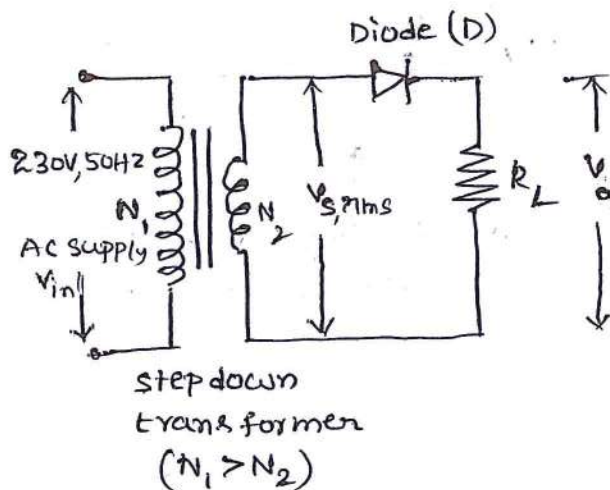


fig: Circuit diagram of a Half wave Rectifier

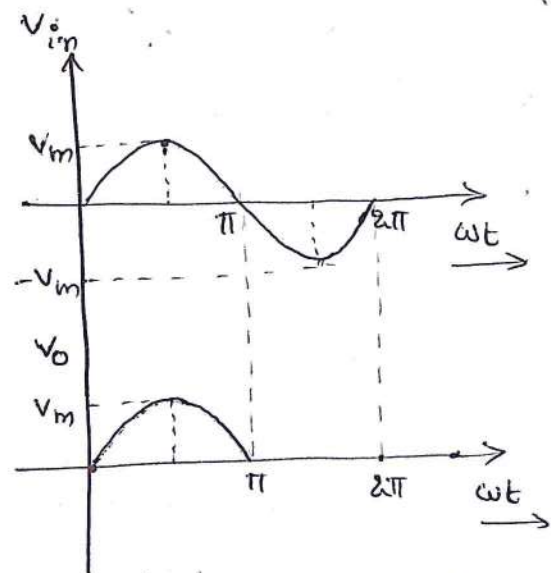


fig: input and output waveforms of Half wave rectifier.

Let V_{in} be the input voltage to the primary of the step-down transformer and given by the equation

$$V_{in} = V_m \sin \omega t ; V_m \gg \text{cut in voltage } V_f$$

The secondary rms voltage (or) secondary ripple voltage is given by

$$V_{ac} = V_{s,rms} = \frac{N_2}{N_1} \cdot V_{in}$$

The Peak voltage (or) the maximum voltage is given by

$$V_m = \sqrt{2} V_{s,rms} \quad \left(\because V_{s,rms} = \frac{V_m}{\sqrt{2}} \right)$$

Operation of Half wave rectifier:

During positive half cycle of the input ac voltage, the terminal 'A' of the secondary of the transformer becomes positive with respect to terminal 'B'. Hence the diode is forward biased and the current flows in the circuit through the load resistance (R_L). This current is denoted as I_L .

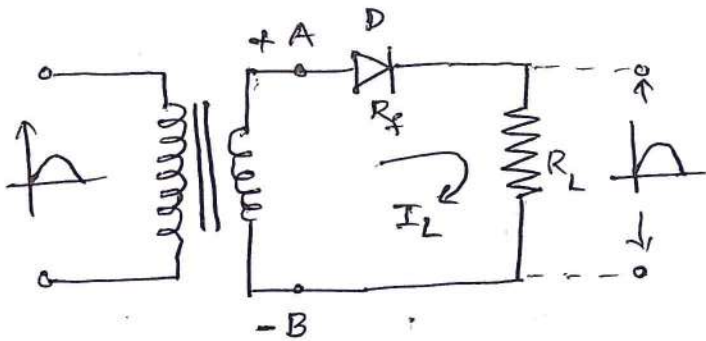


fig: HWR during positive half cycle of AC supply

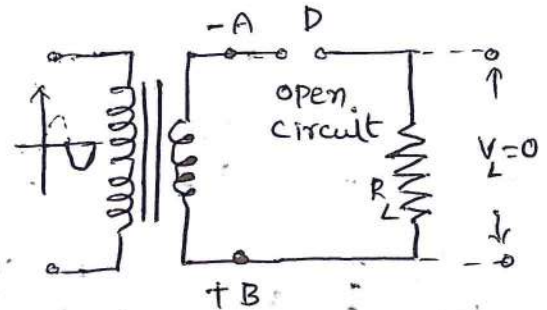


fig:- HWR during negative half cycle of AC supply

During negative half cycle of the ac supply, the terminal 'A' of the secondary of the transformer becomes negative with respect to the terminal B. Hence the diode is reverse biased. Hence no current flows in the circuit.

Derivation of characteristics of Half wave rectifier (or)

Parameters of Half wave rectifier (or) Analysis of HWR:

① Average (or) DC Value of load current (I_{avg} (or) I_{dc}):

$$\begin{aligned} \text{The load current } I_L &= I_m \sin \omega t \text{ for } 0 < \omega t < \pi \\ &= 0 \text{ for } \pi < \omega t < 2\pi. \end{aligned}$$

$$\text{Maximum current (or) peak current } I_m = \frac{V_m}{R_s + R_f + R_L}$$

R_f = forward resistance of the diode.

R_s = Secondary resistance of the transformer

R_L = Load resistance.

(3)

D

The average or dc value of load current

$$\begin{aligned}
 I_{dc} = I_{av} &= \frac{1}{T} \int_0^T I_L dt \\
 &= \frac{1}{2\pi} \int_0^{2\pi} I_L dt \\
 &= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin \omega t dt + \int_{\pi}^{2\pi} 0 dt \right] \\
 &= \frac{1}{2\pi} \left[I_m \int_0^{\pi} \sin \omega t dt \right] \\
 &= \frac{I_m}{2\pi} \left[-\cos \omega t \right]_0^{\pi} \\
 &= -\frac{I_m}{2\pi} (\cos \pi - \cos 0) \\
 &= -\frac{I_m}{2\pi} (-1 - 1)
 \end{aligned}$$

$$\therefore I_{dc} = \frac{I_m}{\pi}$$

(2) DC value of load voltage:

$$\begin{aligned}
 V_{dc} &= I_{dc} \cdot R_L \\
 &= \frac{I_m}{\pi} \cdot R_L \\
 &= \frac{V_m}{(R_s + R_f + R_L)} \cdot \frac{R_L}{\pi} \quad \left(\because I_m = \frac{V_m}{R_s + R_f + R_L} \right) \\
 &= \frac{V_m}{\pi} \cdot \frac{1}{\left(\frac{R_s + R_f}{R_L} + 1 \right)}
 \end{aligned}$$

$R_s + R_f \ll R_L$, hence neglecting $\frac{R_s + R_f}{R_L}$ in the above expression we get $V_{dc} = \frac{V_m}{\pi}$

(3) RMS Current :

$$\begin{aligned}
 I_{rms} &= \sqrt{\frac{1}{T} \int_0^T I_L^2 dt} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_L^2 d\omega t} \\
 &= \sqrt{\frac{1}{2\pi} \left[\int_0^{\pi} (I_m \sin \omega t)^2 d\omega t + \int_{\pi}^{2\pi} 0 d\omega t \right]} \\
 &= \sqrt{\frac{1}{2\pi} I_m^2 \int_0^{\pi} \sin^2 \omega t d\omega t} \\
 &= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \left(\frac{1 - \cos 2\omega t}{2} \right) d\omega t} \\
 &= \sqrt{\frac{I_m^2}{4\pi} \left(\omega t - \frac{\sin 2\omega t}{2} \right) \Big|_0^{\pi}} \\
 &= \sqrt{\frac{I_m^2}{4\pi} \left[\left(\pi - \frac{\sin 2\pi}{2} \right) - \left(0 - \frac{\sin 0}{2} \right) \right]} \\
 &= \sqrt{\frac{I_m^2}{4\pi}}
 \end{aligned}$$

$$\therefore \boxed{I_{rms} = \frac{I_m}{2}}$$

4) RMS Voltage :

Similarly RMS voltage across the load is given by

$$V_{rms} = I_{rms} \cdot R_L = \frac{I_m}{2} \cdot R_L$$

$$= \left(\frac{V_m}{R_s + R_f + R_L} \right) \frac{R_L}{2}$$

$$= \frac{V_m}{\left(\frac{R_s + R_f}{R_L} + 1 \right)} \times \frac{1}{2}$$

Since $R_s + R_f \ll R_L$ so neglecting the term $\frac{R_s + R_f}{R_L}$ we get

(4)

$$\therefore \boxed{V_{rms} = \frac{V_m}{2}}$$

(5) DC output power delivered to the load (P_{dc}) :-

$$P_{dc} = I_{dc}^2 \cdot R_L$$

$$P_{dc} = \left(\frac{I_m}{\pi} \right)^2 \cdot R_L$$

$$\boxed{P_{dc} = \frac{I_m^2}{\pi^2} R_L}$$

(6) AC input power (P_{ac}) :-

$$P_{ac} = I_{rms}^2 \cdot (R_s + R_f + R_L)$$

$$= \left(\frac{I_m}{2} \right)^2 (R_s + R_f + R_L)$$

$$\therefore \boxed{P_{ac} = \frac{I_m^2}{4} (R_s + R_f + R_L)}$$

(7) Rectifier efficiency (η)

$$\text{Rectifier efficiency } (\eta) = \frac{P_{dc}}{P_{ac}} = \frac{\frac{I_m^2 R_L}{\pi^2}}{\frac{I_m^2 (R_s + R_f + R_L)}{4}}$$

$$\Rightarrow \eta = \frac{\cancel{I_m^2} R_L}{\pi^2} \times \frac{4}{\cancel{I_m^2} (R_s + R_f + R_L)}$$

$$= \frac{4}{\pi^2} \times \frac{1}{\left(\frac{R_s + R_f}{R_L} + 1 \right)}$$

$R_s + R_f \ll R_L$, neglecting the term $\frac{R_s + R_f}{R_L}$, then

$$\% \text{ efficiency is } \% \eta = \frac{4}{\pi^2} \times 100 = 40.5\%$$

$$\therefore \boxed{\% \eta = 40.5\%}$$

⑧ Peak inverse voltage (PIV) :

* It is the maximum voltage applied to a diode when it is connected in reverse biased condition, with which the diode can withstand without destroying the junction.

* It is some times called as PIV rating.

* The PIV for a half wave rectifier $= V_m$.

$$\text{i.e. } \boxed{PIV = V_m}$$

⑨ Ripple factor (γ) :

The ratio of ac component of current to the dc value of the current is defined as ripple factor.
(or)

The ratio of ac value of voltage to the dc value of the voltage is defined as ripple factor.

$$\gamma = \frac{I_{ac}}{I_{dc}} = \frac{V_{ac}}{V_{dc}}$$

$$I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2} \Rightarrow I_{rms}^2 = I_{ac}^2 + I_{dc}^2$$

$$\Rightarrow I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\therefore \gamma = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}} = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}}$$

$$\Rightarrow \gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\gamma = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

(5)

$$\therefore \boxed{\gamma = \text{ripple factor for H.W.R} = 1.21}$$

(10) Transformer utilization factor (TUF):

Transformer Utilization factor (TUF) is given by

$$\text{TUF} = \frac{\text{DC Power delivered to the load}}{\text{AC rating of the transformer secondary}}$$

$$= \frac{P_{dc}}{P_{ac \text{ rated (secondary)}}$$

$$= \frac{\left(\frac{I_m^2}{\pi^2} \cdot R_L \right)}{V_{s,rms} \cdot I_{rms}} \quad \left(\begin{array}{l} \text{NOTE: } V_{s,rms} = \frac{V_m}{\sqrt{2}} \\ \text{is different from } V_{rms} \end{array} \right.$$

$$= \frac{\left(\frac{I_m^2}{\pi^2} \cdot R_L \right)}{\left(\frac{V_m}{\sqrt{2}} \right) \cdot \left(\frac{I_m}{2} \right)} \quad \because V_{s,rms} = \frac{V_m}{\sqrt{2}}$$

$$= \frac{I_m R_L}{\pi^2} \times \frac{2\sqrt{2}}{V_m} \quad \because V_m = I_m R_L$$

$$= \frac{V_m}{\pi^2} \times \frac{2\sqrt{2}}{V_m}$$

$$= \frac{2\sqrt{2}}{\pi^2}$$

$$= 0.2865$$

(11) Ripple frequency = f (for H.W.R)

(12) Form factor = $\frac{I_{rms}}{I_{dc}} = \frac{(I_m/2)}{(I_m/\pi)} = \pi/2 = 1.57$

Form factor is the ratio of rms value to dc value.

⑬ Peak factor :-

$$\text{Peak factor} = \frac{\text{Peak value}}{\text{rms value}}$$

$$= \frac{V_m}{(V_m/2)}$$

$$\therefore \text{Peak factor} = 2$$

⑭ % Regulation = $\frac{V_{\text{No Load}} - V_{\text{Full Load}}}{V_{\text{Full Load}}} \times 100$

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

Advantages of Half wave Rectifier:

1) It is simple and low cost circuit.

2) It does not require any center tapping to the transformer.

3) It requires only one diode in the circuit.

Disadvantages of Half wave Rectifier:

1) Low rectification efficiency i.e. $\% \eta = 40.5\%$.

2) Ripple factor is high 1.21.

3) Low TUF (0.286), that means transformer is not fully utilized.

Definition of Half wave Rectifier:

An electronic circuit that converts AC voltage into pulsating dc voltage during half the period of the input cycle is known as Half wave Rectifier.

2) Full Wave Rectifier;

An electronic circuit that converts an AC voltage into a pulsating DC voltage during both the half cycles of the input cycle is known as a full wave rectifier.

There are two types of Full wave Rectifiers

i) Center tapped Full wave Rectifier

ii) Full wave Bridge Rectifier.

i) Center tapped Full wave Rectifier:

In this rectifier two diodes and a center tapped transformer are required.

These two diodes are connected to a common load resistor (R_L) as shown in figure below.

Center tapped full wave rectifier conducts during both positive and negative half cycles of AC input voltage.

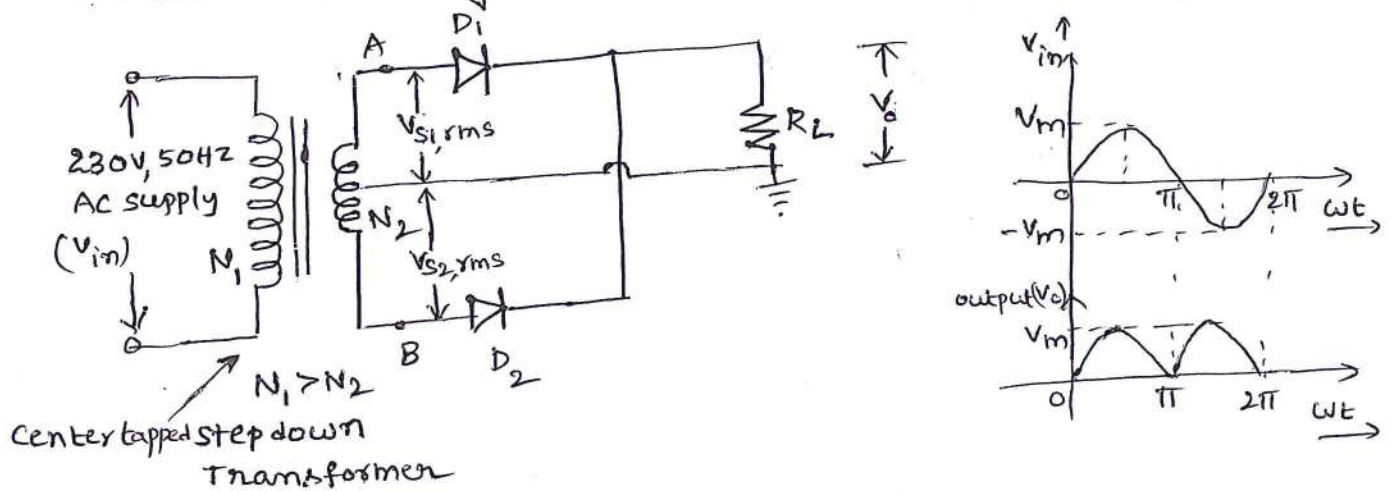


Fig: circuit diagram of center tapped full wave rectifier.

Operation:

During positive half cycle of AC input voltage, the terminal 'A' of the secondary of transformer becomes positive and 'B' is negative. Hence the diode D_1 is forward biased and D_2 is reverse biased. Hence the current

flows through the load resistor ' R_L ' in the circuit, due to D_1 is forward biased. This current is I_{D1} , flows in the circuit through the upper half of the secondary winding. while the lower half of the secondary winding carries no current. Because the diode D_2 is reverse biased and hence acts as open circuit. It is explained with the figure below.

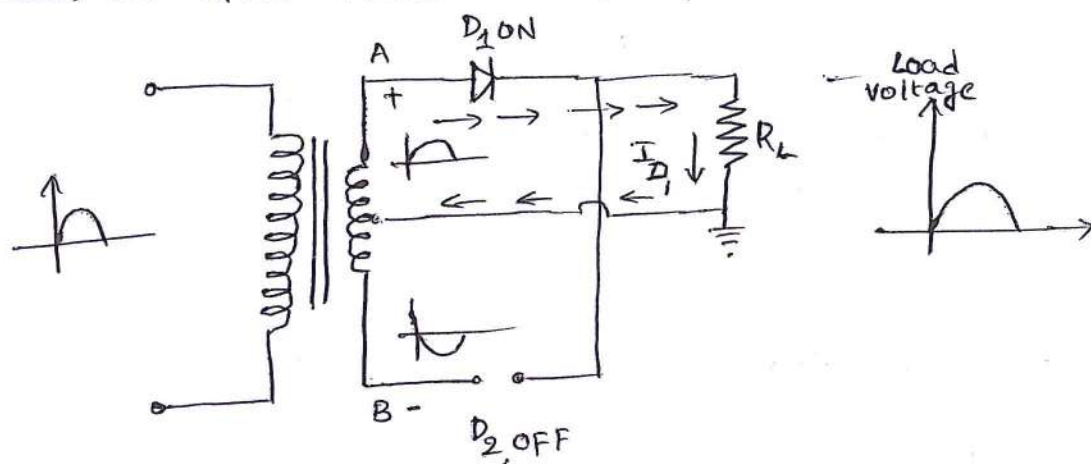


fig:- Current flow during Positive half Cycle.

During negative half cycle of AC input voltage, the terminal A of the secondary coil becomes negative and terminal B becomes positive. Hence the diode D_1 is ⁱⁿ reverse biased and D_2 is in forward biased condition. Hence the current flows through the load resistor ' R_L ' in the circuit due to D_2 is forward - biased. This current is I_{D2} , flows in the circuit through the lower half of the secondary winding. while the upper half of the secondary winding carries no current.

Because the diode D_1 is in reverse biased condition and hence acts as open circuit. It is explained with the following figure.

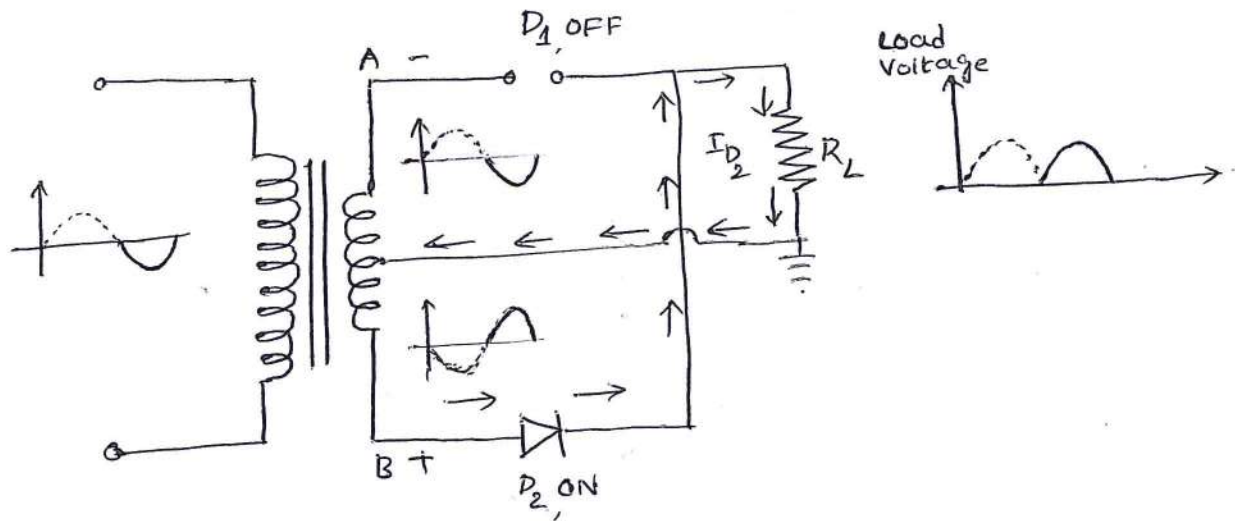
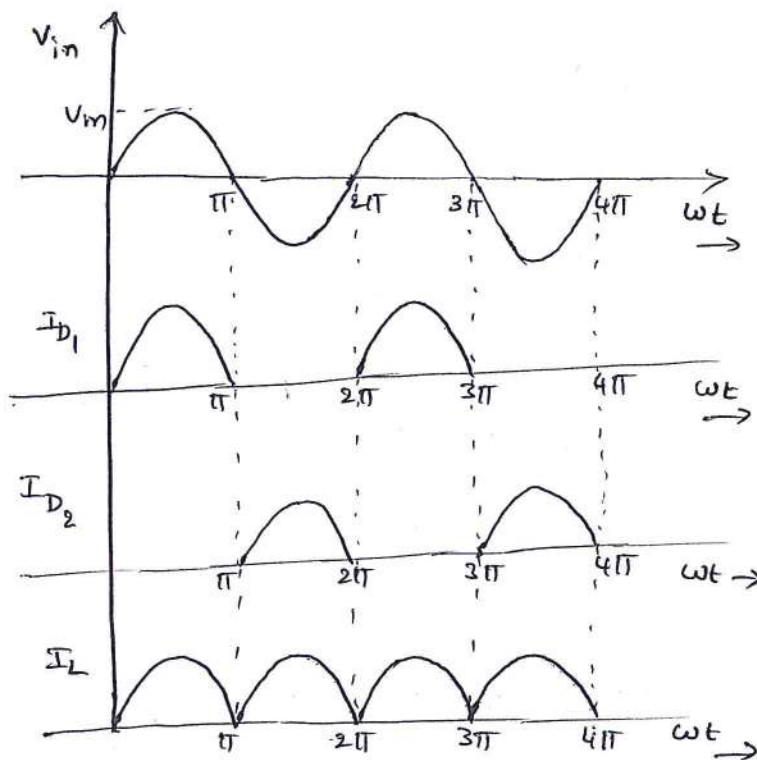


Fig: Current flow during negative half cycle

It is noted that the direction of current in both the half-cycle durations, through the load resistance is same. Hence the load current I_L is obtained by adding I_{D_1} and I_{D_2} .

$$I_L = I_{D_1} + I_{D_2}$$

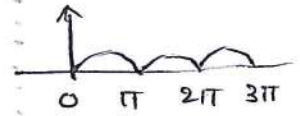


It is also observed that the diodes do not conduct simultaneously but in alternate half cycles.

Derivation of Full wave rectifier (center tapped FWR) characteristics (or) Parameters of FWR (or) Analysis of FWR :

1) Average or DC value of Load Current :

$$\begin{aligned} I_{avg} = I_{dc} &= \frac{1}{T} \int_0^T I_L dt \\ &= \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t dt \\ &= \frac{1}{\pi} (I_m) \cdot \left[-\cos \omega t \right]_0^{\pi} \\ &= -\frac{I_m}{\pi} [\cos \pi - \cos 0] \\ &= -\frac{I_m}{\pi} (-1 - 1) \end{aligned}$$



$$\therefore \boxed{I_{avg} = I_{dc} = \frac{2I_m}{\pi}}$$

2) DC value of load voltage :

$$\begin{aligned} V_{dc} &= I_{dc} \cdot R_L \\ &= \frac{2I_m}{\pi} \cdot R_L \end{aligned}$$

We know that $I_m = \frac{V_m}{R_s + R_f + R_L}$

$$\begin{aligned} \therefore V_{dc} &= \frac{2}{\pi} \left(\frac{V_m}{R_s + R_f + R_L} \right) \cdot R_L \\ &= \frac{2V_m}{\pi} \cdot \frac{1}{\left(\frac{R_s + R_f}{R_L} + 1 \right)} \end{aligned}$$

Since $R_s + R_f \ll R_L$, we can ignore $\frac{R_s + R_f}{R_L}$ in the above expression.

$$\therefore \boxed{V_{dc} = \frac{2V_m}{\pi}}$$

(3) RMS current (or) RMS value of load current:

(8)

$$\begin{aligned} I_{rms} &= \sqrt{\frac{1}{T} \int_0^T I_L^2 dt} = \sqrt{\frac{1}{\pi} \int_0^{\pi} (I_m \sin \omega t)^2 dt} \\ \Rightarrow I_{rms} &= \sqrt{\frac{I_m^2}{\pi} \int_0^{\pi} \left(\frac{1 - \cos 2\omega t}{2} \right) dt} \\ &= \sqrt{\frac{I_m^2}{2\pi} \left(\omega t - \frac{\sin 2\omega t}{2} \right) \Big|_0^{\pi}} \\ &= \sqrt{\frac{I_m^2}{2\pi} \left[\pi - \frac{\sin 2\pi}{2} - \left(0 - \frac{\sin 0}{2} \right) \right]} \\ &= \sqrt{\frac{I_m^2}{2\pi} \times \pi} \end{aligned}$$

$$\therefore I_{rms} = \frac{I_m}{\sqrt{2}}$$

(4) RMS Voltage (or) RMS value of load current:

$$V_{rms} = I_{rms} \cdot R_L = \frac{I_m}{\sqrt{2}} \cdot R_L$$

$$\Rightarrow V_{rms} = \left(\frac{V_m}{R_s + R_f + R_L} \right) \frac{1}{\sqrt{2}} R_L \quad \left(\because I_m = \frac{V_m}{R_s + R_f + R_L} \right)$$

$$\Rightarrow V_{rms} = \frac{V_m}{\sqrt{2}} \left(\frac{R_s + R_f + 1}{R_L} \right)$$

since $R_s + R_f \ll R_L$, neglecting $\frac{R_s + R_f}{R_L}$ we get

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

(5) Dc output power delivered to the load (P_{dc}):

$$P_{dc} = I_{dc}^2 R_L$$

$$= \left(\frac{2I_m}{\pi} \right)^2 R_L$$

$$\therefore \boxed{P_{dc} = \frac{4I_m^2}{\pi^2} R_L}$$

⑥ Ac input power (P_{ac}) :

$$P_{ac} = I_{rms}^2 (R_s + R_f + R_L)$$

$$= \left(\frac{I_m}{\sqrt{2}} \right)^2 (R_s + R_f + R_L)$$

$$\therefore P_{ac} = \frac{I_m^2}{2} (R_s + R_f + R_L)$$

⑦ Rectifier efficiency (η) :

$$\text{Rectifier Efficiency } \eta = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{4I_m^2 R_L}{\pi^2} \right)}{\frac{I_m^2}{2} (R_s + R_f + R_L)}$$

$$= \frac{4I_m^2 R_L}{\pi^2} \cdot \frac{(2)}{I_m^2 (R_s + R_f + R_L)}$$

$$= \frac{8}{\pi^2} \cdot \frac{1}{\left(\frac{R_s + R_f}{R_L} + 1 \right)}$$

neglecting $\frac{R_s + R_f}{R_L}$ as $R_L \gg R_s + R_f$

$$\therefore \eta = \frac{8}{\pi^2} = 0.81056$$

$$\% \text{ Efficiency} = \% \eta = 0.8105 \times 100$$

$$\Rightarrow \boxed{\% \text{ Efficiency} = \% \eta = 81.05\%}$$

⑧ Peak Inverse Voltage (PIV) :

It is the maximum voltage applied to a diode when it is connected in reverse biased condition, with which the diode can withstand without destroying the junction. PIV for full wave rectifier is $2V_m$...

i.e. $\boxed{PIV = 2V_m}$

⑨ Ripple factor (γ) :

The ratio of ac component of current to the dc value of the current is defined as the ripple factor.

$$\gamma = \frac{I_{ac}}{I_{dc}}$$

$$I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2} \Rightarrow I_{rms}^2 = I_{ac}^2 + I_{dc}^2$$

$$\Rightarrow I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\therefore \gamma = \frac{I_{ac}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}}$$

$$\Rightarrow \gamma = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left[\left(\frac{\frac{I_m}{\sqrt{2}}}{\frac{2I_m}{\pi}}\right)^2 - 1\right]}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$\therefore \gamma = 0.48$$

$$\therefore \text{Ripple factor } \boxed{\gamma = 0.48}$$

⑩ Ripple frequency = $2f$

⑪ Form factor = $\frac{\text{RMS value}}{\text{DC value}} = \frac{I_{rms}}{I_{dc}} = \frac{\frac{I_m}{\sqrt{2}}}{\frac{2I_m}{\pi}} = \frac{\pi}{2\sqrt{2}} = 1.11$

$$\star \boxed{\text{form factor} = 1.11}$$

(12) Transformer Utilization Factor (TUF) :

$$\text{FWR TUF} = \text{TUF}_{\text{FWR}} = \frac{\text{TUF}_{\text{primary}} + \text{TUF}_{\text{secondary}}}{2}$$

$$\begin{aligned} \text{TUF}_{\text{primary}} &= 2 \text{TUF}_{\text{HWR}} \\ &= 2 \times 0.2865 \end{aligned}$$

$$\text{TUF}_{\text{primary}} = 0.5731$$

$$\text{TUF}_{\text{secondary}} = \frac{P_{\text{dc}}}{\text{AC rating of the transformer - secondary}}$$

$$= \frac{\frac{4I_m^2}{\pi^2} \times R_L}{V_{\text{rms}} \cdot I_{\text{rms}}}$$

$$= \frac{\frac{4I_m^2}{\pi^2} R_L}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}}$$

$$= \frac{4I_m^2}{\pi^2} R_L \cdot \frac{2}{V_m I_m}$$

$$(\because I_m R_L = V_m)$$

$$= \frac{8}{\pi^2} \frac{V_m}{V_m}$$

$$= \frac{8}{\pi^2}$$

$$\therefore \text{TUF}_{\text{secondary}} = 0.8105$$

$$\therefore \text{TUF}_{\text{FWR}} = \frac{0.5731 + 0.8105}{2} = 0.6918$$

$$\therefore \boxed{\text{TUF}_{\text{FWR}} = 0.6918}$$

(13) Peak factor = $\frac{\text{Peak value}}{\text{RMS value}}$

$$= \frac{I_m}{\left(\frac{I_m}{\sqrt{2}}\right)}$$

$$\therefore \text{Peak factor} = \sqrt{2} = 1.414$$

(14) % Regulation = $\frac{V_{\text{No load}} - V_{\text{Full load}}}{V_{\text{Full load}}} \times 100$

$$\therefore \% \text{ regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

Advantages of center tapped Full wave rectifier:

- 1) Rectifier efficiency is higher than that of half wave rectifier
- 2) Ripple factor is less than half wave rectifier
- 3) TUF (Transformer Utilization Factor) is better than half wave rectifier. $TUF = 0.691$
- 4) DC load voltage and currents are more than half wave rectifier.

Disadvantages of Full wave rectifier:

- 1) PIV rating is high. Higher the PIV rating, larger the diode size is required, which increases the cost.
- 2) center tapped transformer is required.

ii) Bridge Rectifier (or) Full wave Bridge rectifier:

A bridge rectifier has four diodes, connected to form a bridge. The AC input voltage is applied to diagonally opposite ends of the bridge. The load resistance is connected to other two ends of the bridge. Bridge rectifier requires a step-down transformer but no center tapping is required.

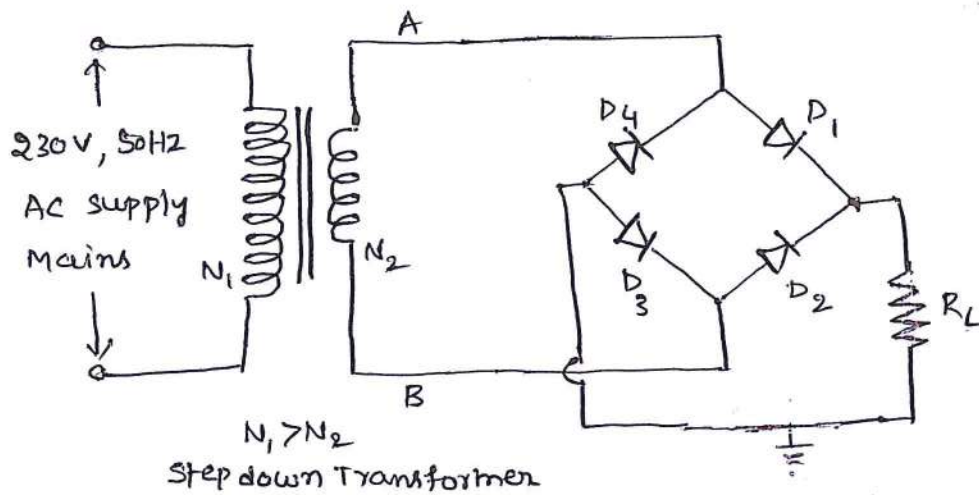


fig: Circuit diagram for Full wave Bridge - Rectifier.

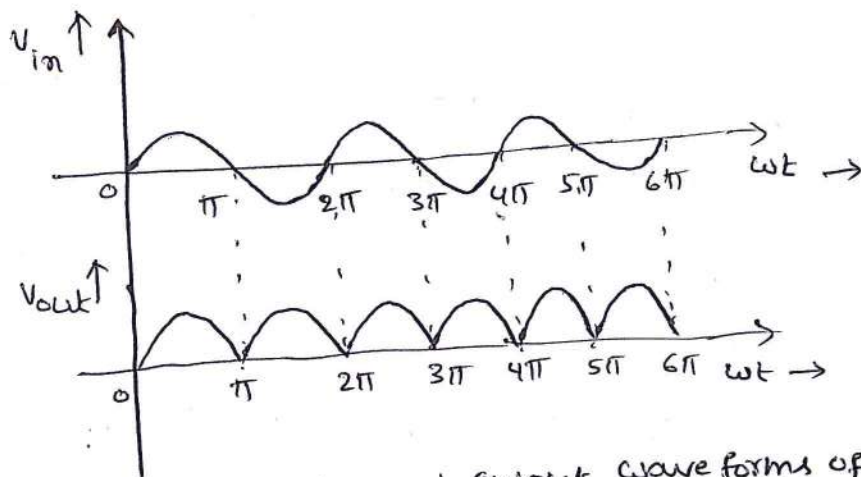


fig:- Input and Output wave forms of Full wave bridge rectifier.

Operation:

During the positive half cycle of AC input supply, the terminal point A of the secondary coil of the transformer is + and terminal B is -. In this case the diodes D_1 , D_3 are forward biased and D_2 , D_4 are reverse biased. The two diodes D_1 , D_3 conducts and the current

flows in the circuit, through the load resistor R_L as shown in below figure.

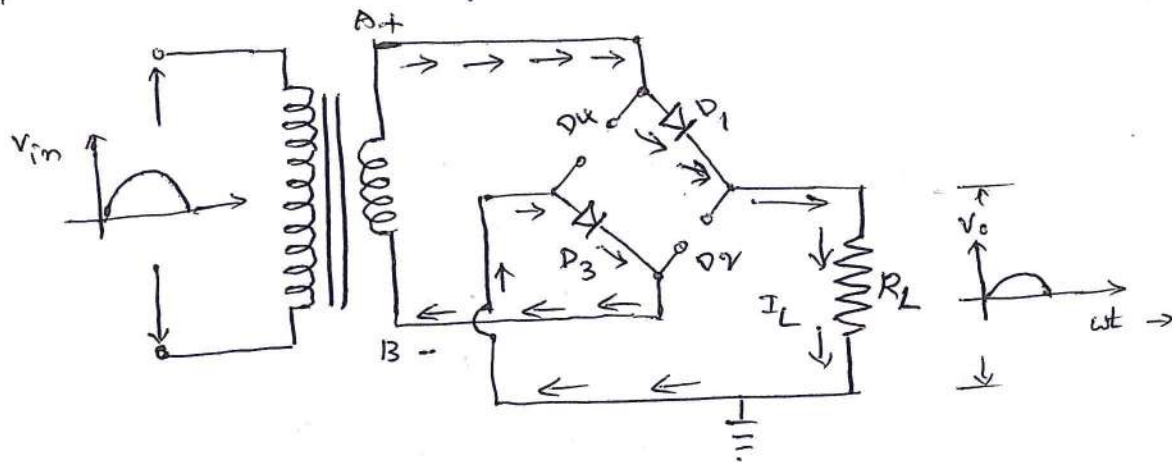


fig: Current flowing during positive half cycle

During negative half cycle of the AC input voltage, the terminal B becomes positive and terminal 'A' becomes negative. In this case the diodes D_2 and D_4 becomes forward biased and the diodes D_1 and D_3 are reverse biased. The two diodes D_2 , D_4 conducts and the current flows in the circuit through the load resistor R_L as shown in below figure.

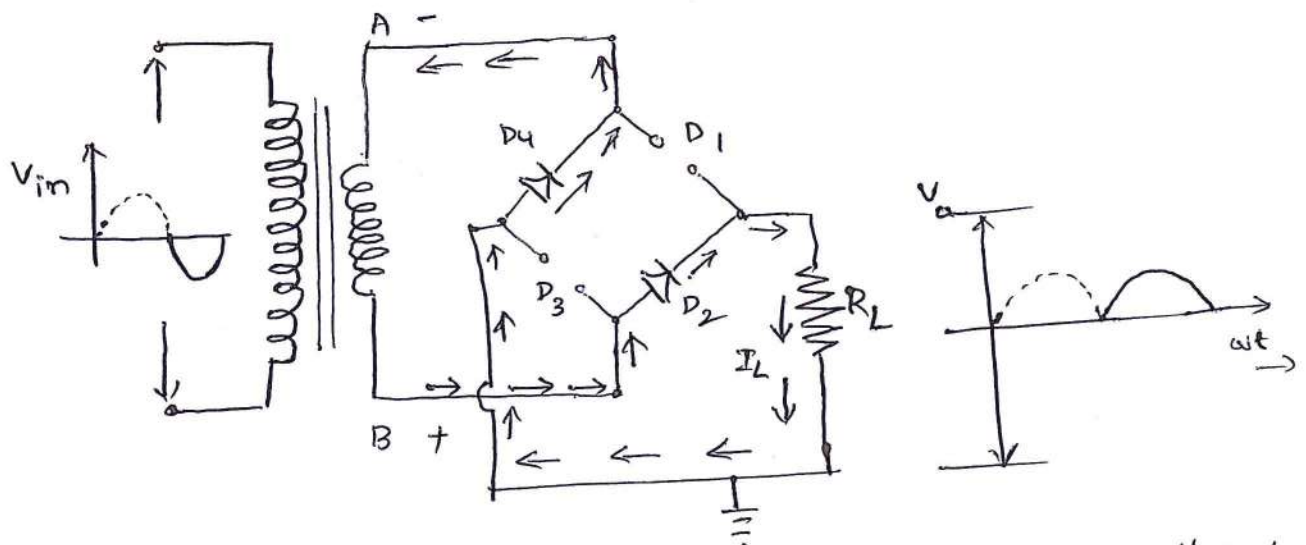


fig: Current flowing during negative half cycle.

It is noted that the current flow direction through load resistor R_L for both the half cycles of AC input supply is same.

Derivation of Bridge rectifier characteristics (or) parameters of bridge rectifier (or) the analysis of bridge rectifier:

1) DC value (or) Average value of Load current:

$$\begin{aligned} I_{dc} = I_{avg} &= \frac{1}{T} \int_0^T I_L dt \\ &= \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t dt \\ &= \frac{I_m}{\pi} \left[-\cos \omega t \right]_0^{\pi} \\ &= -\frac{I_m}{\pi} [\cos \pi - \cos 0] \\ &= -\frac{I_m}{\pi} [-1 - 1] \end{aligned}$$

$$\therefore \boxed{I_{dc} = \frac{2I_m}{\pi}}$$

2) DC value of Load voltage:

$$V_{dc} = I_{dc} \cdot R_L = \frac{2I_m}{\pi} \cdot R_L$$

$$\Rightarrow V_{dc} = \frac{2}{\pi} \left(\frac{V_m}{R_s + 2R_f + R_L} \right) \cdot R_L$$

$$\because I_m = \frac{V_m}{R_s + 2R_f + R_L}$$

$$= \frac{2V_m}{\pi} \cdot \frac{1}{\left(\frac{R_s + 2R_f}{R_L} + 1 \right)}$$

Since $R_s + 2R_f \ll R_L$, we can ignore $\frac{R_s + 2R_f}{R_L}$ in the above expression.

$$\therefore \boxed{V_{dc} = \frac{2V_m}{\pi}}$$

③ RMS Current (or) RMS value of load current:

$$I_{rms} = \sqrt{\frac{1}{T} \int_0^T I_L^2 dt} = \sqrt{\frac{1}{\pi} \int_0^\pi (I_m \sin \omega t)^2 d\omega t}$$

$$\Rightarrow I_{rms} = \sqrt{\frac{1}{\pi} I_m^2 \int_0^\pi \sin^2 \omega t d\omega t}$$

$$= \sqrt{\frac{I_m^2}{\pi} \int_0^\pi \left(\frac{1 - \cos 2\omega t}{2} \right) d\omega t}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \left(\omega t - \frac{\sin 2\omega t}{2} \right) \Big|_0^\pi}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \left[\left(\pi - \frac{\sin 2\pi}{2} \right) - \left(0 - \frac{\sin 0}{2} \right) \right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \times \pi}$$

$$\therefore \boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}$$

④ RMS voltage (or) RMS value of load voltage:

$$V_{rms} = I_{rms} \cdot R_L = \frac{I_m}{\sqrt{2}} \cdot R_L$$

$$\Rightarrow V_{rms} = \frac{V_m}{R_s + 2R_f + R_L} \times \frac{R_L}{\sqrt{2}} \quad \because I_m = \frac{V_m}{R_s + 2R_f + R_L}$$

$$= \frac{V_m}{\sqrt{2}} \cdot \frac{1}{\left(\frac{R_s + 2R_f}{R_L} + 1 \right)}$$

Since $R_s + 2R_f \ll R_L$, we can neglect $\frac{R_s + 2R_f}{R_L}$ in the above expression we get

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

⑤ DC output power delivered to the load (P_{dc}) :-

$$P_{dc} = I_{dc}^2 \cdot R_L = \left(\frac{2I_m}{\pi} \right)^2 R_L = \frac{4I_m^2}{\pi^2} R_L$$

$$\therefore \boxed{P_{dc} = \frac{4I_m^2}{\pi^2} R_L}$$

⑥ AC input power (P_{ac}) :-

$$P_{ac} = I_{rms}^2 (R_s + R_f + R_L)$$

$$= \left(\frac{I_m}{\sqrt{2}} \right)^2 (R_s + R_f + R_L)$$

$$\therefore \boxed{P_{ac} = \frac{I_m^2}{2} (R_s + R_f + R_L)}$$

⑦ Rectifier efficiency (η) :

$$\text{Rectifier efficiency } \eta = \frac{P_{dc}}{P_{ac}} = \frac{\left(\frac{4I_m^2}{\pi^2} R_L \right)}{\frac{I_m^2}{2} (R_s + R_f + R_L)}$$

$$\Rightarrow \eta = \frac{4I_m^2}{\pi^2} R_L \times \frac{2}{I_m^2 (R_s + R_f + R_L)}$$

$$= \frac{8}{\pi^2} \times \frac{1}{\left(\frac{R_s + R_f}{R_L} + 1 \right)}$$

Since $R_s + R_f \ll R_L$, neglecting $\frac{R_s + R_f}{R_L}$ we get

$$\eta = \frac{8}{\pi^2} = 0.81056 \Rightarrow \% \eta = 81.056\%$$

$$\boxed{\% \text{ Efficiency} = \% \eta = 81.056\%}$$

⑧ Peak Inverse voltage (PIV) :

It is the maximum voltage applied to a diode when it is connected in reverse bias, with which the diode can withstand without destroying the junction.

PIV for Bridge rectifier is V_m

i.e. $\boxed{PIV = V_m}$

⑨ Ripple factor (γ) :

The ratio of ac value of the current to the dc value of current is defined as the ripple factor.

$$\gamma = \frac{I_{ac}}{I_{dc}}$$

$$I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2} \Rightarrow I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\therefore \gamma = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\Rightarrow \gamma = \sqrt{\left[\frac{(I_m/\sqrt{2})}{(2I_m/\pi)}\right]^2 - 1}$$

$$= \sqrt{\frac{I_m^2}{2} \times \frac{\pi^2}{4I_m^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$\therefore \gamma = 0.48$$

$$\therefore \boxed{\text{Ripple factor } \gamma = 0.48}$$

⑩ Transformer utilization factor (TUF):

$$TUF = \frac{P_{dc}}{\text{AC rating of the transformer secondary}}$$

AC rating of the transformer secondary

$$\Rightarrow TUF = \frac{\left(\frac{4I_m^2}{\pi^2} \times R_L\right)}{V_{s,rms} \cdot I_{rms}} = \frac{\frac{4I_m^2}{\pi^2} \times R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

$$\Rightarrow TUF = \frac{4I_m^2 R_L}{\pi^2} \times \frac{2}{V_m I_m}$$

$$\Rightarrow TUF = \frac{8I_m R_L}{\pi^2 V_m} \quad \left[\because I_m R_L = V_m \right]$$

$$\Rightarrow TUF = \frac{8V_m}{\pi^2 V_m} = \frac{8}{\pi^2} = 0.8105$$

$$\therefore \boxed{\text{Bridge rectifier TUF} = 0.8105}$$

(11) Form factor:

$$\text{Form factor} = \frac{\text{RMS value}}{\text{DC value}} = \frac{I_{rms}}{I_{DC}} = \frac{(I_m/\sqrt{2})}{(2I_m/\pi)}$$

$$\Rightarrow \text{formfactor} = \frac{\pi}{2\sqrt{2}} = 1.11$$

$$\therefore \boxed{\text{formfactor} = 1.11}$$

(12) Peak factor:

$$\text{peak factor} = \frac{\text{Peak value}}{\text{RMS value}} = \frac{I_m}{I_{rms}} = \frac{I_m}{(I_m/\sqrt{2})} = \sqrt{2}$$

$$\therefore \boxed{\text{Peak factor} = \sqrt{2} = 1.414}$$

(13) Ripple frequency:

$$\text{Ripple frequency} = 2f$$

$$(14) \% \text{ Regulation} = \frac{V_{NoLoad} - V_{FullLoad}}{V_{FullLoad}} \times 100$$

$$\text{i.e. } \boxed{\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100}$$

Advantages of Bridge rectifier:

- ① Center tapped transformer is not required
- ② Transformer utilization factor is 0.8105 which is better than Center tapped full wave rectifier
- ③ % Efficiency is 81.05 %.
- ④ Better ripple factor i.e $\gamma = 0.48$.
- ⑤ Peak Inverse Voltage = V_m ; which is less than Center-tapped full wave rectifier.

Disadvantages of Bridge rectifier:

- 1) Four diodes are required

Comparison among HWR, FWR and bridge rectifier:

Half Wave Rectifier	Center tapped full-wave Rectifier	Bridge rectifier
1) $I_{dc} = \frac{I_m}{\pi}$	1) $I_{dc} = \frac{2I_m}{\pi}$	1) $I_{dc} = \frac{2I_m}{\pi}$
2) $V_{dc} = \frac{V_m}{\pi}$	2) $V_{dc} = \frac{2V_m}{\pi}$	2) $V_{dc} = \frac{2V_m}{\pi}$
3) % efficiency = 40.6 ($\% \eta$)	3) $\% \eta = 81.05$	3) $\% \eta = 81.05$
4) Ripple factor $\gamma = 1.81$	4) $\gamma = 0.48$	4) $\gamma = 0.48$
5) Ripple frequency is f	5) Ripple frequency is $2f$	5) Ripple frequency $2f$
6) TUF = 0.2865	6) TUF = 0.6918	6) TUF = 0.8105
7) PIV = V_m	7) PIV = $2V_m$	7) PIV = V_m
8) Low cost	8) Costly	8) Less Costly
9) one diode is required	9) Two diodes are required	9) 4 diodes are required.
10) $I_{rms} = I_m/2$	10) $I_{rms} = I_m/\sqrt{2}$	10) $I_{rms} = I_m/\sqrt{2}$

- > A Half wave rectifier circuit is supplied from a 230V, 50Hz AC supply with a step down ratio of 3:1 to a resistive load of $10k\Omega$. The diode forward resistance is 75Ω while the transformer secondary resistance is 10Ω . Calculate i) Maximum Current, average current and rms current ii) DC output voltage iii) efficiency of rectifier. iv) ripple factor v) Ripple frequency vi) PIV.

Sol: Given data $V_{in} = 230V$, frequency $= 50Hz$
 $N_1:N_2 = 3:1$, $R_L = 10k\Omega$, $R_S = 10\Omega$
 $R_F = 75\Omega$

i) Maximum Current $I_m = \frac{V_m}{R_S + R_L + R_F}$

we know that $V_{s,rms} = \frac{V_m}{\sqrt{2}}$ also

$$V_{s,rms} = \frac{N_2}{N_1} V_{in} = \frac{1}{3} \times 230 = 76.666V$$

$$\therefore V_{s,rms} = \frac{V_m}{\sqrt{2}} = 76.666V$$

$$\Rightarrow V_m = \sqrt{2} \times 76.666 = 108.42V$$

$$\text{maximum current } I_m = \frac{108.423}{10 + 75 + (10 \times 10^3)}$$

$$I_m = 0.0107509 A$$

$$I_{dc} = \text{Average current } I_{avg} = \frac{I_m}{\pi} = 3.422 \times 10^{-3} A$$

$$I_{rms} = \frac{I_m}{2} = \frac{0.01075}{2} = 5.3754 \times 10^{-3} A$$

ii) DC output Voltage $V_{dc} = I_{dc} R_L = (3.422 \times 10^{-3})(10 \times 10^3)$
 $\therefore V_{dc} = 34.22 V$

iii) Efficiency $\% \eta = \frac{P_{dc}}{P_{ac}} \times 100$

$$\begin{aligned}
 &= \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_s + R_f + R_L)} \times 100 \\
 &= \frac{(3.422 \times 10^{-3})^2 \times (10 \times 10^3)}{\left(\frac{I_m}{2}\right)^2 (10 + 75 + (10 \times 10^3))} \times 100 \\
 &= \frac{(3.422 \times 10^{-3})^2 \times 10^4}{\left(\frac{0.0107509}{2}\right)^2 (10085)} \times 100
 \end{aligned}$$

$$\therefore \% \eta = 40.184\%$$

$$\begin{aligned}
 \text{iv)} \text{ Ripple factor } \gamma &= \frac{I_{ac}}{I_{dc}} = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \\
 \Rightarrow \gamma &= \sqrt{\left(\frac{5.3754 \times 10^{-3}}{3.422 \times 10^{-3}}\right)^2 - 1}
 \end{aligned}$$

$$\therefore \gamma = 1.2114$$

$$\text{v)} \text{ Ripple frequency } f = 50 \text{ Hz}$$

$$\text{vi)} \text{ PIV} = V_m = 108.42 \text{ V}$$

- 2) A HWR having a resistive load of $1 \text{ k}\Omega$, rectifies an AC voltage of 325 V peak values and the diode has a forward resistance of 100Ω . Calculate i) Peak, average and rms values of current ii) DC output power iii) AC input power iv) Efficiency of the rectifier v) TUF.

$$\text{sol)} \text{ Given data } R_L = 1000 \Omega, V_m = 325 \text{ V}, R_f = 100 \Omega$$

$$\text{i)} \text{ Peak value of load current } = I_m = \frac{V_m}{R_f + R_s + R_L}$$

Since R_s is not given, ignore R_s as it is a very small resistance

$$\therefore I_m = \frac{325}{100 + 0 + 1000} = 0.295454 \text{ A}$$

Average value of Current $I_{avg} = \frac{I_m}{\pi} = \frac{0.2954}{\pi} = 0.094046 \text{ A}$

RMS Value of Current $I_{rms} = \frac{I_m}{2} = \frac{0.2954}{2} = 0.147727 \text{ A}$

ii) DC output Power $P_{dc} = I_{dc}^2 \cdot R_L = (0.094046)^2 \times 1000$
 $= 8.844669 \text{ watts}$

iii) AC input Power $P_{ac} = I_{rms}^2 (R_s + R_f + R_L)$
 $= (0.147727)^2 (6 + 100 + 1000)$
 $P_{ac} = 24.005593 \text{ watts}$

iv) % Rectifier efficiency $= \frac{P_{dc} \times 100}{P_{ac}} = \frac{8.844669 \times 100}{24.005593}$

$\therefore$ % rectifier efficiency $= 36.84\%$

v) Transformer utilization factor $= \frac{P_{dc}}{\text{AC rating of transformer secondary}}$
 $= \frac{8.844669}{V_{s,rms} I_{rms}}$
 $= \frac{8.844669}{\left(\frac{V_m}{\sqrt{2}}\right) \cdot \left(\frac{I_m}{2}\right)}$
 $= \frac{8.844669 \times 2\sqrt{2}}{325 \times 0.295454}$
 $\therefore \text{TUF} = 0.2605$

- 3) An AC supply of 230V is applied to a HWR through a S.I transformer. Assume the diode is an ideal one. The load resistance is 300Ω . Find i) DC output voltage ii) PIV
 iii) Maximum power delivered to the load iv) Average value of Power delivered to the load.

Sol). Given $V_{in} = 230V$, $N_1:N_2 = 5:1$, $R_L = 300\Omega$,

$R_f = 0$ ($\because$ Ideal diode is given)

$$V_m = \sqrt{2} V_{s,rms} ; V_{s,rms} = \frac{N_2}{N_1} \times 230 = \frac{1}{5} \times 230 = 46V$$

$$\therefore V_m = \sqrt{2} \times 46 = 65.0538V.$$

$$I_m = \frac{V_m}{R_s + R_f + R_L} = \frac{65.0538}{0+0+300} = 0.216846A$$

i) DC output voltage $V_{dc} = \frac{V_m}{\pi} = 20.7072V$

ii) $PIV = V_m = 65.0538V$

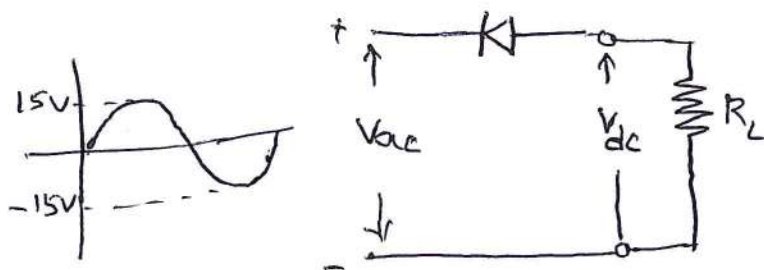
iii) Maximum power delivered to the load

$$P_m = I_m^2 R_L = 14.1066 \text{ watts}$$

iv) $P_{avg} = P_{dc} = I_{dc}^2 R_L = \left(\frac{0.216846}{\pi}\right)^2 \times 300 = 1.4293 \text{ watts.}$

$$\left[\because I_{dc} = \frac{I_m}{\pi} \right]$$

4) a) Assume Ideal diode, find the V_{dc} for the circuit shown in below b) Repeat part 'A' if ideal diode is replaced by a silicon diode having a Cut in Voltage $0.7V$, neglect forward resistance.



Sol) a) $V_{dc} = \frac{V_m}{\pi} = \frac{-15}{\pi} = -4.774648V$

b) $V_f = 0.7V$ (Silicon)

$$V_{dc} = \frac{-15 + 0.7}{\pi} = -4.55183V \quad \underline{\underline{Ans}}$$

Problems on FWR:

- i) In a center tapped FWR, the RMS half secondary voltage is 9V. Assume ideal diode, load resistance $1k\Omega$. i) find Peak, dc, rms values of current ii) DC load voltage iii) ripple factor iv) rectifier efficiency

Sol) Given $V_{s,rms} = 9V$, $R_L = 1k\Omega$, ideal diode i.e. $R_f = 0$.
 R_s is not given Assume $R_s = 0$

i) Peak current $I_m = ?$

$$V_m = \sqrt{2} V_{s,rms} = \sqrt{2} \times 9 = 12.72792V.$$

$$I_m = \frac{V_m}{R_s + R_f + R_L} = \frac{12.72792}{0+0+1000} = 0.0127279A$$

$$\text{dc value of current } I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 0.0127279}{\pi} = 0.008102 \times 10^{-3}A$$

$$\therefore I_{dc} = 8.1028468 \text{ mA}$$

$$I_{r,rms} = \frac{I_m}{\sqrt{2}} = 0.009 = 9 \text{ mA}$$

ii) DC load voltage $V_{dc} = I_{dc} \cdot R_L = 0.0081028648 \times 1000$
 $\therefore V_{dc} = 8.1028648V$

iii) Ripple factor
$$r = \frac{I_{ac}}{I_{dc}} = \frac{\sqrt{I_{r,rms}^2 - I_{dc}^2}}{I_{dc}}$$

$$r = \frac{\sqrt{0.009^2 - (8.1028468 \times 10^{-3})^2}}{8.1028468 \times 10^{-3}}$$

$$r = 0.483424$$

iv) Rectifier efficiency
$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 \cdot R_L}{I_{r,rms}^2 (R_s + R_f + R_L)}$$

$$\Rightarrow \eta = \frac{(8.1028468 \times 10^{-3})^2 \times 1000}{(0.009)^2 (0+0+1000)} = 0.810573$$

$$\therefore \% \eta = 81.0573 \%$$

2) A Full wave rectifier circuit is fed from a transformer having a center tapped secondary. The rms voltage from either end of secondary is 30V. If the diode forward resistance is 2Ω and that of the half secondary is 8Ω . For a load resistance of $1k\Omega$. Calculate i) Power delivered to the load ii) Percent regulation at full load iii) Efficiency iv) TUF of secondary v) V

Sol) Given $V_{S,rms} = 30V$, $R_f = 2\Omega$, $R_s = 8\Omega$, $R_L = 1k\Omega$

$$V_{S,rms} = 30V \Rightarrow \frac{V_m}{\sqrt{2}} = 30V \Rightarrow V_m = 30\sqrt{2} = 42.4264V$$

i) Power delivered to the load $P_{dc} = I_{dc}^2 \cdot R_L$

$$\therefore P_{dc} = \left(\frac{2I_m}{\pi} \right)^2 \cdot R_L = \left(\frac{2V_m}{\pi R_s + R_f + R_L} \right)^2 \times R_L$$

$$\Rightarrow P_{dc} = \left[\frac{2 \times 42.4264}{\pi \times (8 + 2 + 1000)} \right]^2 \times 1000 = 0.71513W$$

ii) $V_{NoLoad} = \frac{2V_m}{\pi} = \frac{2 \times 42.4264}{\pi} = 27.00948V$

$$V_{Fullload} = V_{NoLoad} \times \frac{R_L}{R_s + R_f + R_L} = 27.00948 \times \frac{1000}{8 + 2 + 1000}$$

$$\therefore V_{Fullload} = 26.74206V$$

$$\therefore \% \text{regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$$= \frac{27.00948 - 26.74206}{26.74206} \times 100$$

$$= 0.99996\%$$

$$\therefore \% \text{regulation} \approx 1\%$$

iii) Rectifier efficiency $\eta = \frac{P_{dc}}{P_{ac}}$

4 (18)

$$P_{ac} = I_{rms}^2 (R_s + R_f + R_L) = \left(\frac{I_m}{\sqrt{2}} \right)^2 (R_s + R_f + R_L)$$

$$\Rightarrow P_{ac} = \left(\frac{\frac{V_m}{R_s + R_f + R_L}}{\sqrt{2}} \right)^2 (R_s + R_f + R_L)$$

$$P_{ac} = \frac{V_m^2}{2(R_s + R_f + R_L)} = \frac{(42.4264)^2}{2(8+2+1000)} = 0.89082 \text{ W}$$

$$\therefore \eta = \frac{0.71513}{0.89082} = 0.8025$$

$$\Rightarrow \% \eta = 80.25\%$$

iv) TUF = $\frac{P_{dc}}{\text{Ac rating of the transformer secondary}}$

$$= \frac{0.71513}{V_{s,rms} I_{rms}}$$

$$= \frac{0.71513}{30 \times I_{rms}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{V_m}{(R_s + R_f + R_L) \sqrt{2}} = \frac{42.4264}{(8+2+1000)\sqrt{2}} = 0.0297029 \text{ A}$$

$$\therefore \text{TUF} = \frac{0.71513}{30 \times 0.0297029} = 0.8025$$

v) Ripple factor $\gamma = \frac{I_{ac}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}}$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2}{\pi} \frac{V_m}{R_s + R_f + R_L} = \frac{2 \times 42.4264}{\pi \times (8+2+1000)} = 0.02674$$

$$\therefore \gamma = \frac{\sqrt{0.0297029^2 - 0.02674^2}}{0.02674} = 0.4836$$

Problems on bridge rectifier:-

- A $5k\Omega$ load is fed from a bridge rectifier connected across a transformer secondary whose primary is connected to $460V$, $50Hz$ supply. The ratio of number of primary turns to secondary is $2:1$. Calculate i) dc load current ii) dc load voltage iii) ripple voltage and iv) PIV rating of diode.

Sol)

Given $R_L = 5k\Omega = 5000\Omega$, $f = 50Hz$

$V_{in} = 460V$, $N_1:N_2 = 2:1$

$$V_{s,rms} = \frac{V_m}{\sqrt{2}} \quad \text{and} \quad V_{s,rms} = \frac{N_2}{N_1} \cdot V_{in}$$
$$= \frac{1}{2} \times 460$$
$$= 230V$$

$\therefore 230 = \frac{V_m}{\sqrt{2}} \Rightarrow V_m = 230\sqrt{2} = 325.2691193V$

$\therefore V_m = 325.2691193V$

i) dc load current $I_{dc} = 2 \frac{I_m}{\pi}$

$$I_m = \frac{V_m}{R_s + 2R_f + R_L}$$
$$= \frac{325.2691193}{0 + 0 + 5000}$$

$\therefore$ Assume ideal diode as R_f not given and assume $R_s = 0$.

$$I_m = 0.0650538 A$$

$$\therefore I_{dc} = \frac{2 \times 0.0650538}{\pi} = 0.04141455 A$$

ii) dc load voltage $V_{dc} = I_{dc} \times R_L = 0.04141455 \times 5000$
 $\therefore V_{dc} = 207.07275V$

iii) ripple voltage $V_{ac} = ?$

w.k.T Ripple factor $\gamma = 0.48$ (for bridge rectifier)

$$\text{ie } \frac{V_{ac}}{V_{dc}} = 0.48$$

$$V_{ac} = 0.48 \times V_{dc}$$

$$= 0.48 \times 207.07275$$

$$\therefore V_{ac} = 99.3949 \text{ V.}$$

$$\text{iv)} \text{ Peak inverse voltage} = V_m = 325.2691193 \text{ V.}$$

2) The four semiconductor diodes used in a bridge rectifier circuit, each having a forward resistance of 0.1Ω and infinite reverse resistance, feed a dc current of 10 A to a resistive load from a sinusoidally varying AC supply of 30 V rms . Determine the load resistance and efficiency of the circuit.

$$\text{Sol)} \quad R_f = 0.1 \Omega, \quad I_{dc} = 10 \text{ A}, \quad V_{s, \text{rms}} = 30 \text{ V}$$

$$R_L = ? \quad \eta = ?$$

$$V_{s, \text{rms}} = \frac{V_m}{\sqrt{2}} \Rightarrow V_m = \sqrt{2} \cdot V_{s, \text{rms}} = \sqrt{2} \times 30 = 42.4264 \text{ V}$$

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 42.4264}{\pi} = 27.00948 \text{ V}$$

$$\text{we know that } I_{dc} = \frac{V_{dc}}{R_L} = \frac{27.00948}{R_L}$$

$$\text{but } I_{dc} = 10 \text{ A} \quad \Rightarrow \quad 10 = \frac{27.00948}{R_L}$$

$$\therefore R_L = 2.700948 \Omega$$

$$P_{dc} = I_{dc}^2 \cdot R_L = 10^2 \times 2.700948 = 270.0948 \text{ W.}$$

$$P_{ac} = I_{\text{rms}}^2 (R_s + 2R_f + R_L)$$

$$I_m = \frac{V_m}{R_s + 2R_f + R_L} = \frac{42.4264}{0 + 2(0.1) + 2.7009} \quad \left(\text{let } R_s = 0, \text{ since not given} \right)$$

$$I_m = 14.62 \text{ A}$$

$$\begin{aligned} \therefore P_{ac} &= \left(\frac{I_m}{\sqrt{2}} \right)^2 (R_s + 2R_f + R_L) = \left(\frac{14.625}{\sqrt{2}} \right)^2 (0 + 2(0.1) + 2.7) \\ &= \frac{(14.625)^2}{2} \times 2.9 \\ &= 310.1419 \text{ watts} \end{aligned}$$

$$\therefore \text{Efficiency } \eta = \frac{P_{dc}}{P_{ac}} = \frac{270.034}{310.1419} = 0.8708$$

$$\therefore \% \eta = 87.08\%$$

Filters:

* The output of a rectifier circuit is a Pulsating DC. That means the output contains some unwanted AC components called ripples along with DC. These unwanted AC components have to be removed by using a suitable circuit such as Filters.

Definition for filter:

A filter is defined as a circuit or a device that removes the unwanted AC components of the rectifier output and allows only DC components to appear at the load.

Some of the important filters used in the power supply circuits

- are
- 1) Inductor filter (choke filter)
 - 2) Capacitor filter
 - 3) L-section filter (or) LC filter (choke input)
 - 4) π -section filter (or) CLC filter
 - 5) Multiple L-section filter
 - 6) Multiple π -section filter.

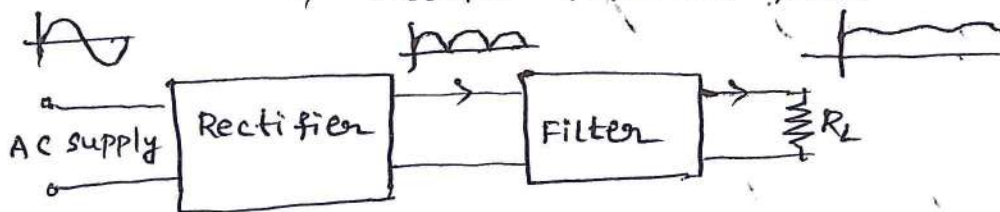


fig. Block diagram of a rectifier with filter.

1) Inductor filter : (choke filter)

Basic principle of inductor filter:

* An inductor filter opposes any change in current and allows the current which does not change. i.e. usually the inductor filter opposes AC components and allows DC components and some low frequency AC components.

i) Inductor filter with Half Wave Rectifier :

This circuit consists of a step down transformer, a diode and an inductor and a load resistor (R_L) .

The inductor filter is connected in series with the diode and load resistance . usually it is connected between the diode and load resistance of a half wave rectifier.

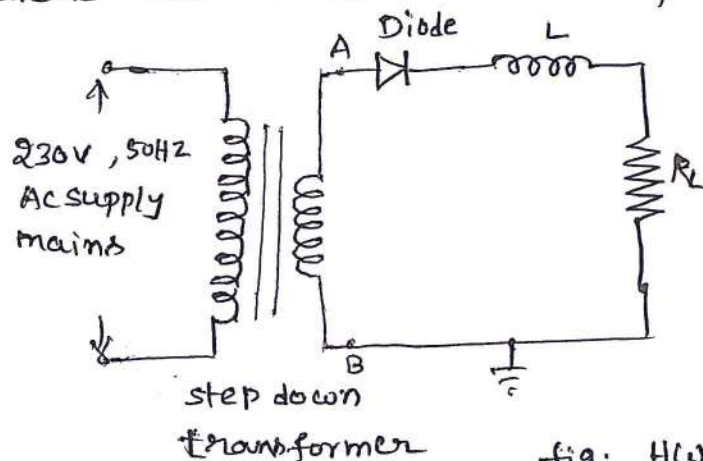


fig: HWR with Inductor filter

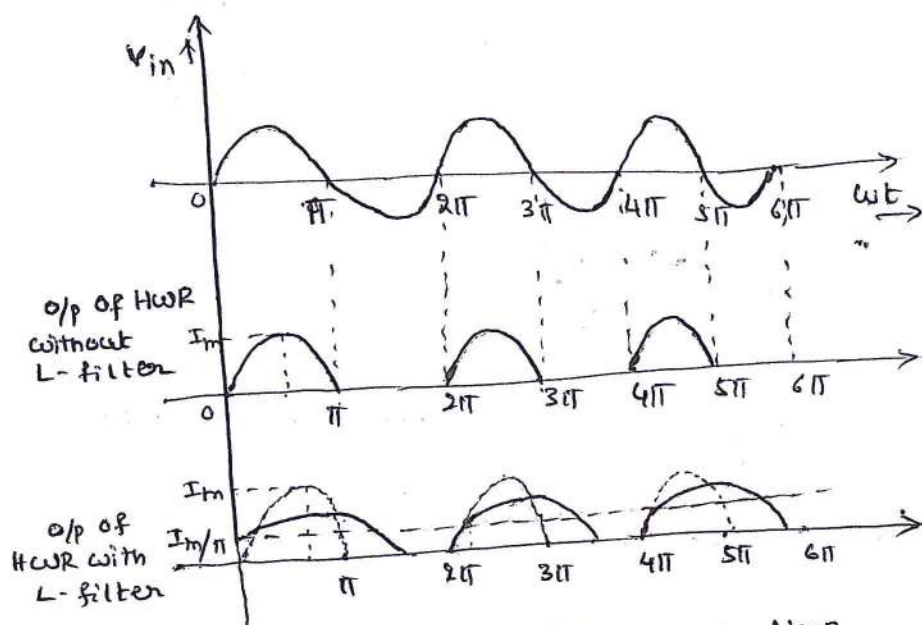


fig:- wave forms of HWR

operation:

During positive half cycle of the input, the terminal A of the secondary coil of the transformer is positive with respect to terminal B. so the diode is forward biased and hence starts conducting .

* The output of the diode is passed through the inductor. but the inductor does not allow any variation in current passing through it. Because the o/p of diode contains both ac and dc components.

for DC and low frequency components $X_L = 2\pi fL$ is low, thus it permits DC and low frequency components.

For high frequency AC components $X_L = 2\pi fL$ is very high thus it does not permit high frequency components.

* When the o/p of the rectifier increases above the average value (i.e dc value), the inductor starts storing magnetic energy. This stored energy tends to decrease, when the rectifier o/p falls below the average value

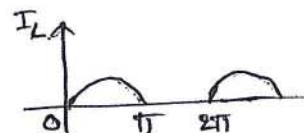
* During the negative half cycle of input the terminal 'B' is positive with respect to the terminal 'A' of the secondary coil of the transformer. Thus the diode is reverse biased and it does not permit any current to flow through it. During this the inductor filter continues discharging the stored energy. The amount of discharging energy depends on the time constant.

Expression for ripple factor for H.W.R with inductor filter:

we know that the load current I_L for Half wave Rectifier is

$$I_L = I_m \sin \omega t \quad \text{for } 0 \leq \omega \leq \pi$$

$$= 0 \quad \text{for } \pi < \omega \leq 2\pi$$



The Fourier series expansion of a half wave rectifier load

$$\text{Current is, } I_L = \frac{I_m}{\pi} + \frac{I_m}{2} \sin \omega t - \frac{2I_m}{3\pi} \cos 2\omega t - \dots \rightarrow (1)$$

The first term in the above expression represents the DC or average value of load current i.e $I_{dc} = \frac{I_m}{\pi} = \frac{V_m}{\pi R_L} \rightarrow (2)$

The 2nd and 3rd terms represent the 1st and 2nd order ripples.

neglecting the higher order terms, we can write

$$I_{ac} = \frac{I_m \sin \omega t}{2} - \frac{2I_m \cos 2\omega t}{2\pi} \rightarrow (3)$$

let the RMS value of 1st ripple is $I_{1r,rms}$ and 2nd ripple RMS value as $I_{2r,rms}$.

$$\text{w.k.T RMS value of a ripple} = \frac{\text{Peak value}}{\sqrt{2}}$$

$$\therefore I_{1r,rms} = \frac{\left(\frac{I_m}{2}\right)}{\sqrt{2}} = \frac{I_m}{2\sqrt{2}} = \frac{V_m}{(R_L + j\omega L) 2\sqrt{2}} \rightarrow (4)$$

$$I_{2r,rms} = \frac{\left(\frac{2I_m}{3\pi}\right)}{\sqrt{2}} = \frac{2I_m}{3\sqrt{2}\pi} = \frac{\sqrt{2}}{3\pi} \left(\frac{V_m}{R_L + j2\omega L}\right) \rightarrow (5)$$

when $\omega L \gg R_L$,

$$\text{Then } (3) \Rightarrow I_{1r,rms} = \frac{V_m}{\omega L 2\sqrt{2}} = \frac{V_m}{2\sqrt{2} \omega L}$$

$$(4) \Rightarrow I_{2r,rms} = \frac{\sqrt{2}}{3\pi} \left(\frac{V_m}{2\omega L}\right) = \frac{V_m}{3\sqrt{2} \pi \omega L}$$

$$I_{ac} = \sqrt{I_{1r,rms}^2 + I_{2r,rms}^2}$$

$$I_{ac} = \sqrt{\left(\frac{V_m}{2\sqrt{2} \omega L}\right)^2 + \left(\frac{V_m}{3\sqrt{2} \pi \omega L}\right)^2} = \sqrt{\frac{V_m^2}{4 \times 2 \omega^2 L^2} + \frac{V_m^2}{9 \times 2 \pi^2 \omega^2 L^2}}$$

$$= \frac{V_m}{\omega L} \sqrt{\frac{1}{8} + \frac{1}{18\pi^2}}$$

$$I_{ac} = 0.36142 \frac{V_m}{\omega L} \rightarrow (6)$$

$$\text{Ripple factor } \gamma = \frac{I_{ac}}{I_{dc}} = \frac{0.36142 \frac{V_m}{\omega L}}{\frac{V_m}{\pi R_L}} \quad \left[\because \text{from (6), (2)} \right]$$

$$\Rightarrow \gamma = \frac{0.36142 V_m}{\omega L} \times \frac{\pi R_L}{V_m}$$

$$\Rightarrow \gamma = \frac{0.36142 \times \pi R_L}{\omega L}$$

$$\therefore \gamma = \frac{1.135 R_L}{\omega L}$$

This expression clearly shows that the reduced ripple factor can be obtained either for a small value of load resistance (R_L) or for a larger value of inductance (L).

ii) Inductor filter with full wave rectifier:

This circuit consists of a center tapped transformer, or a bridge rectifier, an inductor and a load resistor R_L . Inductor, the load resistor are connected in series to each other as shown in below circuit diagram.

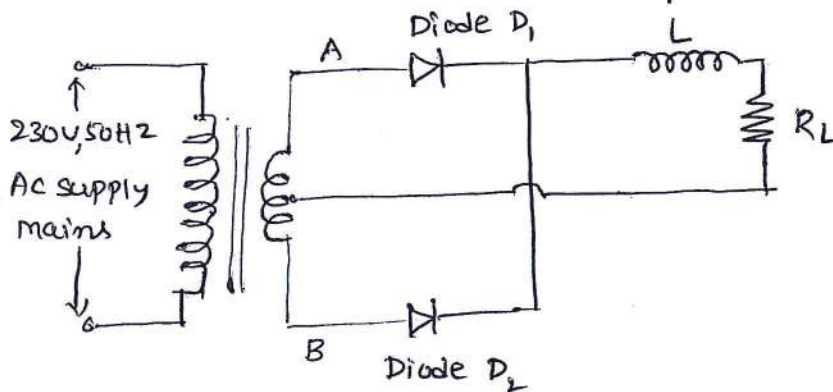


fig:- Full wave rectifier with inductor filter

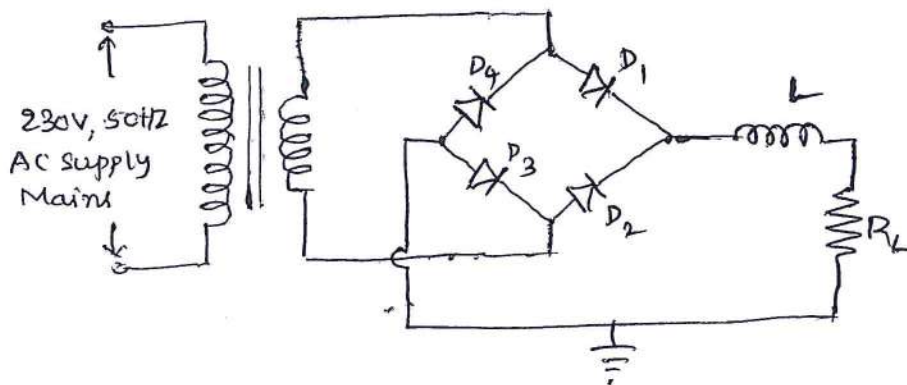
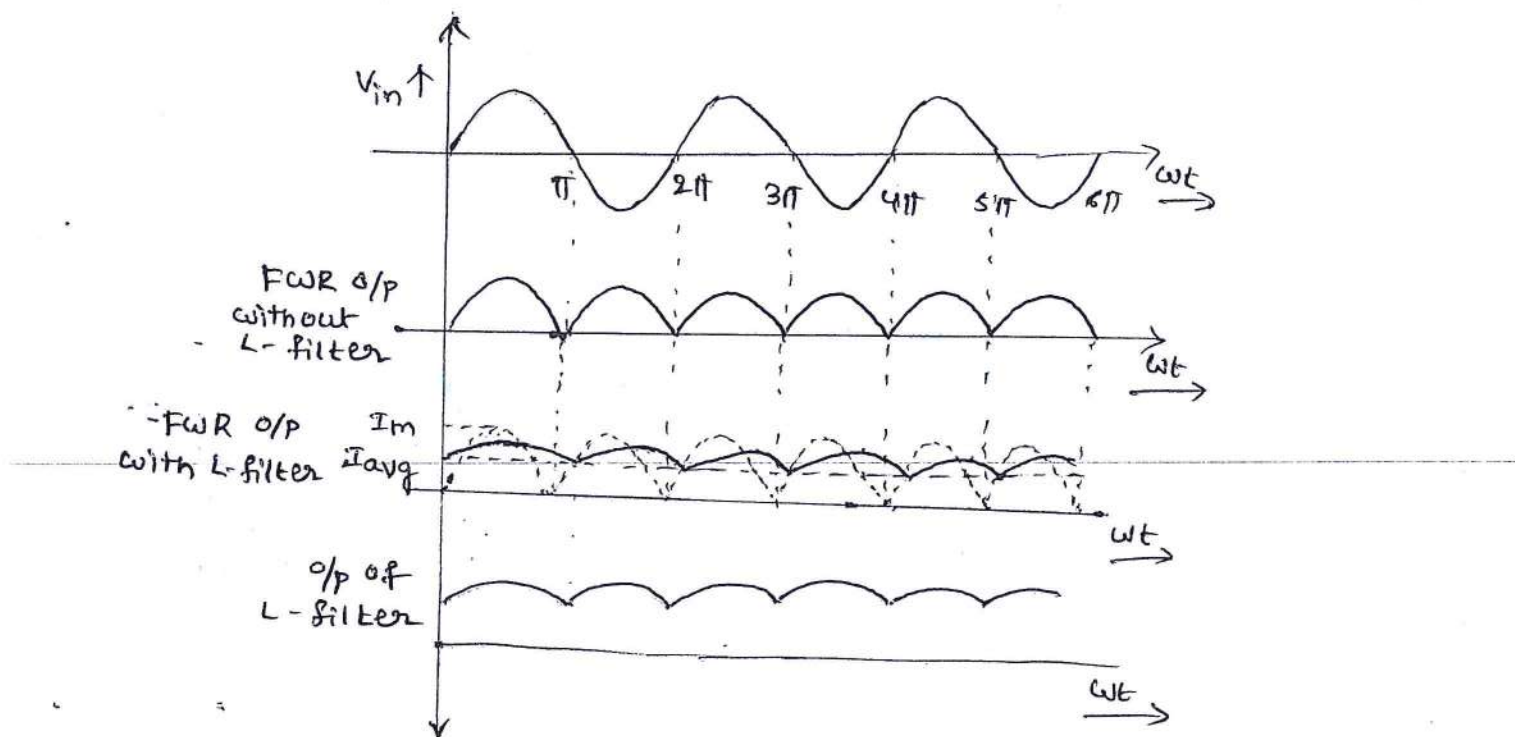


fig:- Full wave bridge rectifier with inductor filter.



Operation :

- * During positive half cycle of the input, the terminal A of the secondary coil of the transformer is positive with respect to terminal B. So the diode D_1 is forward biased and D_2 is reverse biased. Hence D_1 starts conducting. The diode output current contains dc component and ac components.
- * During negative half cycle of the input, the terminal B of the secondary coil of the transformer is positive with respect to the terminal A. So the diode D_2 is forward biased and D_1 is reverse biased. Hence D_2 starts conducting.
- * The output of the diode is passed through the inductor but the inductor does not permit any changes in the current passing through it.
- * For dc and low frequency ripple components X_L is low, thus it permits dc and low frequency ripple components.
- For high frequency ripple components X_L is large, thus it does not permit high frequency ripple components.

$$\Rightarrow \gamma = \frac{0.36142 \times \pi R_L}{\omega L}$$

$$\therefore \gamma = \frac{1.135 R_L}{\omega L}$$

This expression clearly shows that the reduced ripple factor can be obtained either for a small value of load resistance (R_L) or for a larger value of inductance (L).

ii) Inductor filter with full wave rectifier :

This circuit consists of a center tapped transformer, or a bridge rectifier, an inductor and a load resistor R_L . Inductor, the load resistor are connected in series to each other as shown in below circuit diagram.

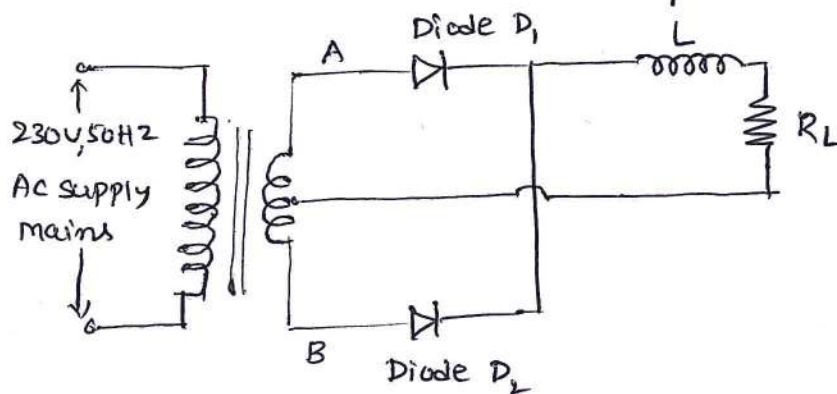


fig:- Full wave rectifier with inductor filter

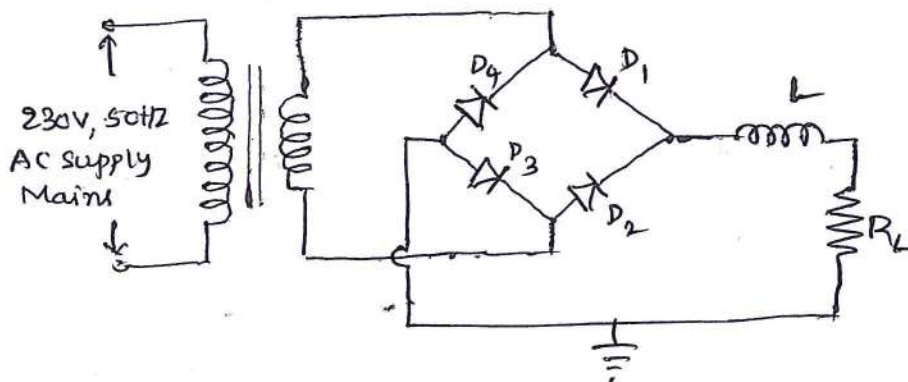
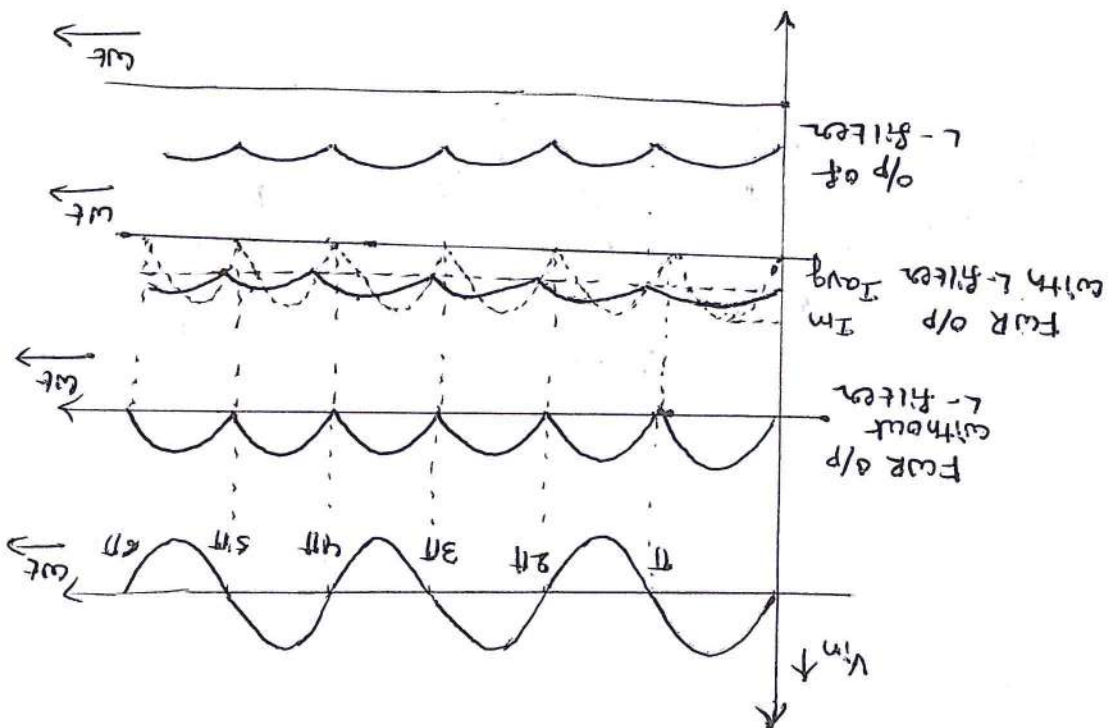


fig: Full wave bridge rectifier with inductor filter.

operation :



* During positive half cycle of the input, the terminal A of the secondary coil of the transformer is positive with respect to terminal B. So the diode D_1 is forward biased and D_2 is reverse biased. Hence D_1 starts conducting. The diode output current contains dc component and ac components.

* During negative half cycle of the input, the terminal B of the secondary coil of the transformer is positive with respect to the terminal A. So the diode D_2 is forward biased and D_1 is reverse biased. Hence D_2 starts conducting.

* The output of the diode is passed through the inductor but the inductor doesn't permit any changes in the current passing through it.

* For dc and low frequency ripple components X_L is low, thus it permits dc and low frequency ripple components.

* For high frequency ripple components X_L is large, thus it doesn't permit high frequency ripple components.

* When the output of the rectifier increases above average value, then the inductor starts storing the magnetic energy. This stored energy tends to decrease when the rectifier o/p falls below the average value. The stored energy prevents the current to fall down to zero. Thus the o/p current is maintained at average value as its minimum current.

Expression for ripple factor for full wave rectifier with inductor filter (or) bridge rectifier

We know that the load current I_L for Full wave current

$$I_L = I_m \sin \omega t \quad (\text{For } 0 \leq \omega t \leq \pi)$$

It can be written in Fourier series representation

$$\text{as } I_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos 2\omega t + \dots \rightarrow (1)$$

The first term in the above expression represents the dc or average value of load current. i.e. $I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi R_L} \rightarrow (2)$

The 2nd term in equation (1) represents the 2nd order ripple. Neglecting the higher order terms we can write

$$I_{ac} = \frac{4I_m}{3\pi} \cos 2\omega t \rightarrow (3)$$

Let the rms value of the ripple is $I_{r,rms}$.

We know that RMS Value of a ripple = $\frac{\text{Peak value}}{\sqrt{2}}$

$$\therefore I_{r,rms} = \frac{\left(\frac{4I_m}{3\pi}\right)}{\sqrt{2}} = \frac{2\sqrt{2} I_m}{3\pi}$$

$$\Rightarrow I_{r,rms} = \frac{2\sqrt{2}}{3\pi} \left(\frac{V_m}{R_L + j2\omega L} \right)$$

$$\left(\because \text{the ripple is 2nd order ripple } I_m = \frac{V_m}{R_L + j2\omega L} \right)$$

when $\omega L \gg R_L$

$$I_{r,rms} = \frac{2\sqrt{2}}{3\pi} \left(\frac{V_m}{2\omega L} \right)$$

$$I_{r,rms} = \frac{\sqrt{2}}{3\pi} \frac{V_m}{\omega L} \rightarrow (4)$$

$$I_{ac} = \sqrt{(I_{r,rms})^2} = I_{r,rms} = \frac{\sqrt{2}}{3\pi} \frac{V_m}{\omega L} \rightarrow (5)$$

$$\text{Ripple factor } \gamma = \frac{I_{ac}}{I_{dc}} = \frac{\left(\frac{\sqrt{2} V_m}{3\pi \omega L} \right)}{\left(\frac{2 V_m}{\pi R_L} \right)} \quad (\because \text{from (2), (5)})$$

$$\Rightarrow \gamma = \frac{\sqrt{2} V_m}{3\pi \omega L} \times \frac{\pi R_L}{2 V_m}$$

$$\therefore \text{Ripple factor } \gamma = \frac{R_L}{3\sqrt{2} \omega L}$$

This expression clearly shows that the reduced ripple factor is obtained when R_L value is smaller or when inductor value is larger.

2) Capacitor Filter :

Basic Principle of capacitor filter :

*

A capacitor filter allows

AC components of high frequencies and blocks dc components and low frequency components.

*

so, when a capacitor filter is connected in parallel to the load resistor the capacitor makes the dc components to be appearing at the load.

Half Wave Rectifier with C-filter:

A Half wave rectifier with Capacitor filter is as shown in figure below. The Capacitor filter is connected in parallel with the load resistance ' R_L '.

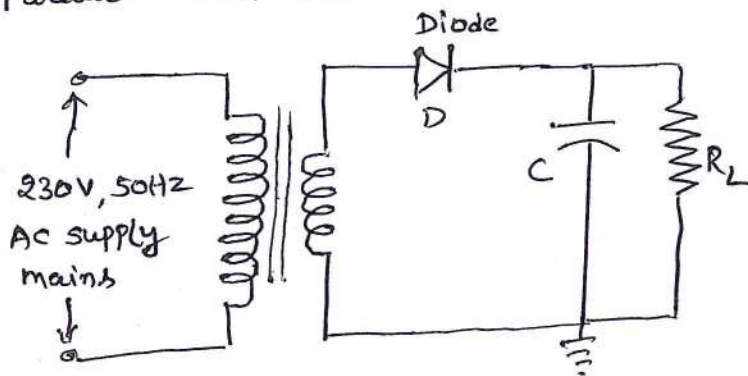


fig: Half wave rectifier with C-filter

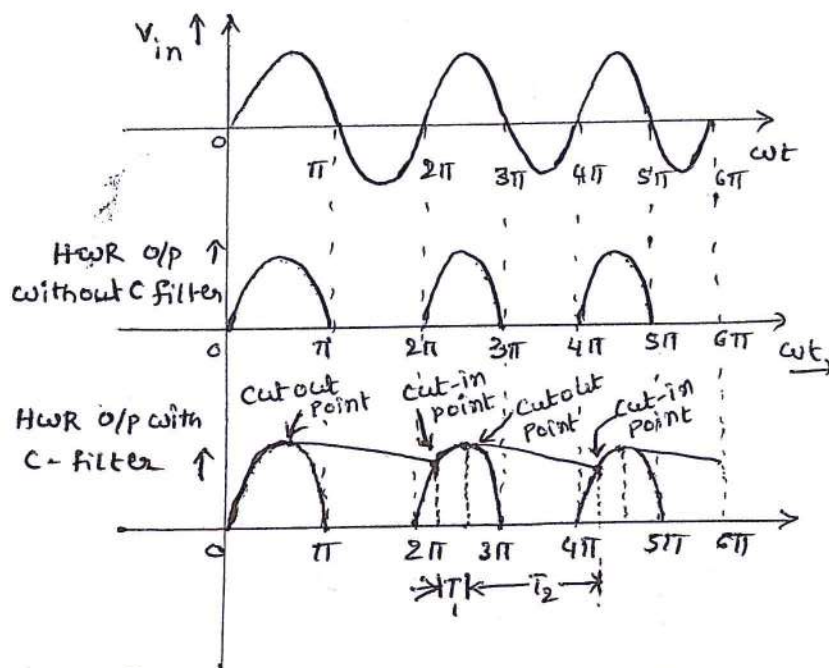


fig: Input and o/p wave forms of HWR with C-filter.

operation :

* During the (first quarter of) positive half cycle of AC supply, the diode D is forward biased, hence it starts conducting.

During this period the capacitor quickly charges to a voltage V_m .

* when the input voltage of AC supply (of positive half-cycle) falls below the voltage V_m i.e. $V_{in} < V_c$, the diode becomes reverse biased, due to which the capacitor starts to discharge

through the load resistance R_L .

* During the negative half cycle, the diode D becomes reverse biased, hence it does not conduct. so the capacitor C continues discharging through R_L .

As the discharging time constant " $R_L \cdot C$ " is very large the capacitor does not get sufficient time to discharge completely. Due to this the voltage of the capacitor C decreases slightly.

* During the next positive half cycle when the input voltage V_{in} increases above the voltage of the capacitor (i.e. $V_{in} > V_C$) the diode again comes into forward bias hence the capacitor gets charged to it's maximum value. The process is repeated, for each cycle of the input voltage.

* It is important to know, over what portion of the full cycle is the diode conducting. The instant (or) point at which the diode stops conduction is known as cut-out point.

The point at which the diode starts conduction is known as cut-in point.

* The current flowing through the diode in the duration between the cut in point to cut-out point is known as "Surging current".

Expression for Ripple Factor :

From the output waveform of Half wave rectifier with C-filter, it is observed that the capacitor discharges over the period T_2 . The amount of charge lost by the

capacitor is $Q_{\text{discharge}} = I_{dc} \cdot T_2$

The capacitor charges to maximum value by replacing

the same amount of charge during the period ' T_1 '.

$$Q_{\text{charge}} = C \cdot V_{r,PP}$$

where $V_{r,PP}$ is the peak to peak voltage of the ripple, in the C-filter o/p.

$$\therefore Q_{\text{charge}} = Q_{\text{discharge}}$$

$$C V_{r,PP} = I_{dc} \cdot T_2$$

It is observed that $T_2 \gg T_1$, let $T_1 + T_2 = T$
then $T_2 \approx T \approx \frac{1}{f}$

$$\therefore C V_{r,PP} = I_{dc} \cdot T$$

$$V_{r,PP} = \frac{I_{dc}}{C \cdot f}$$

The o/p of the C-filter looks like a triangular wave form. Hence it's rms value ^{of ripple} obtained by $V_{r,rms} = \frac{\text{Maximum value}}{2\sqrt{3}}$

$$\therefore V_{r,rms} = \frac{V_{r,PP}}{2\sqrt{3}} = \frac{1}{2\sqrt{3}} \frac{I_{dc}}{C \cdot f}$$

$$\Rightarrow V_{r,rms} = \frac{I_{dc}}{2\sqrt{3} f \cdot C}$$

$$V_{ac} = \sqrt{V_{r,rms}^2} = V_{r,rms} = \frac{I_{dc}}{2\sqrt{3} f C}$$

$$\text{W.K.T } V_{dc} = I_{dc} \cdot R_L$$

$$\therefore \text{Ripple factor } \gamma = \frac{V_{ac}}{V_{dc}} = \left(\frac{I_{dc}}{2\sqrt{3} f C} \right) \frac{1}{I_{dc} R_L}$$

$$\Rightarrow \boxed{\gamma = \frac{1}{2\sqrt{3} f C R_L}}$$

Full wave Rectifier with Capacitor filter:

A full wave rectifier can be either a center tapped full wave rectifier or full wave bridge rectifier. The circuit diagram for full wave rectifier with capacitor filter is as shown in below figure.

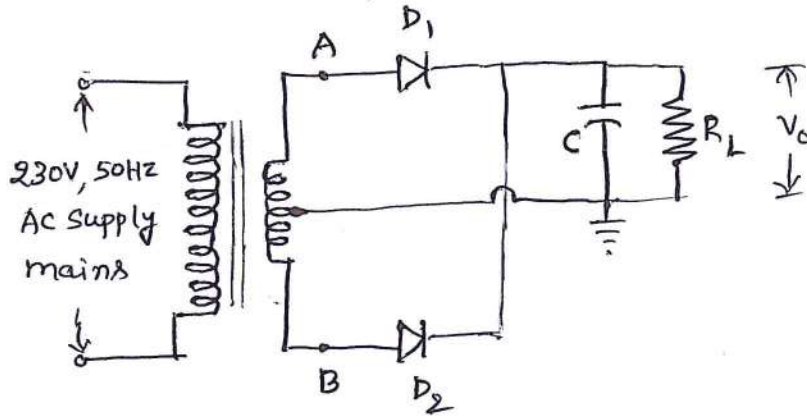


fig: center tapped full wave rectifier with capacitor filter.

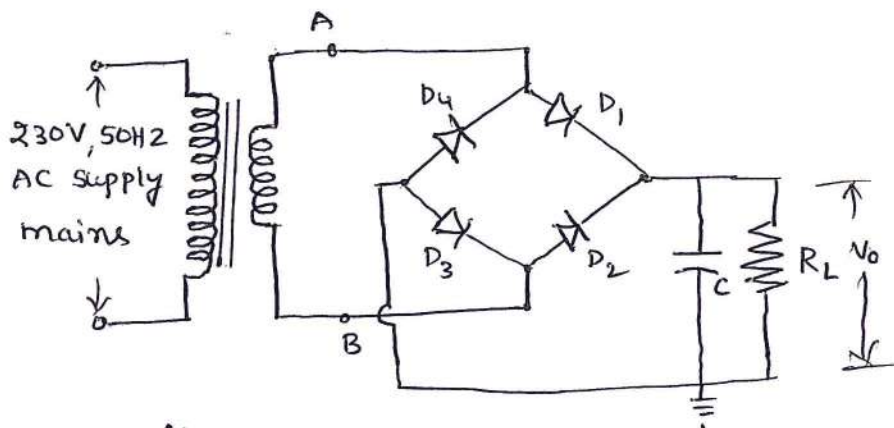
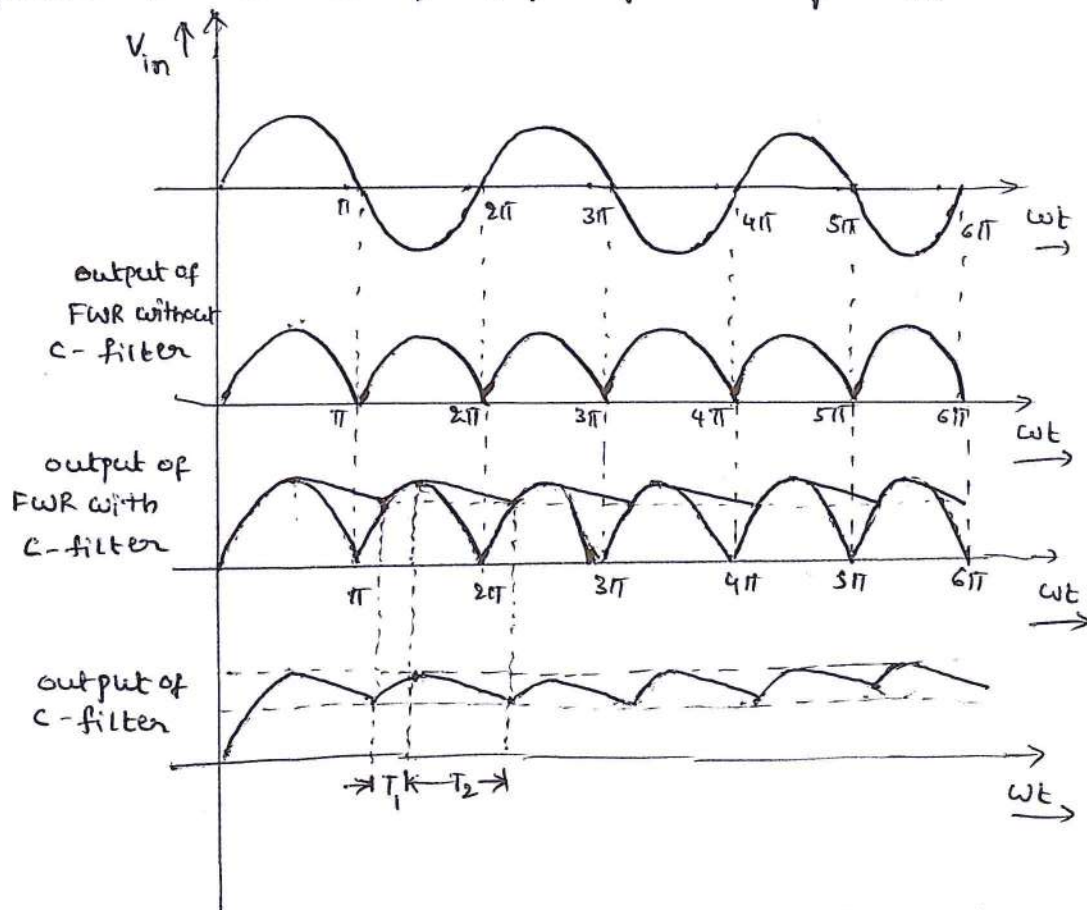


fig: full wave bridge rectifier with capacitor filter.

Operation

- * During the first half of the positive half cycle the diode D_1 is forward biased and D_2 is reverse biased. So the capacitor C charges up to the peak value of the input voltage V_m .
- * During the second half of the positive half cycle the diode D_2 is reverse biased during which input voltage V_{in} is less than capacitor voltage V_C i.e. $V_C < V_{in}$. Thus the capacitor starts discharging through the load resistor. This is continued till the voltage of V_{in} becomes greater than V_C .

* During negative half cycle D_2 is forward biased and D_1 is reverse biased. When the input voltage exceeds the capacitor voltage, the capacitor starts charging. Same procedure is repeated for all the cycles of input voltage V_{in} .



Expression for ripple factor for a FWR with filter:

The average value of the capacitor discharge over time period T_2 , is $Q_{discharge} = I_{dc} \times T_2$.

This charge lost by the capacitor, is replaced during ' T_1 ' during which the capacitor is charged to the peak to peak voltage of the ripple V_{rpp} .

$$\therefore Q_{charge} = V_{rpp} \cdot C$$

$$\Rightarrow Q_{charge} = C V_{rpp}$$

$$Q_{charge} = Q_{discharge}$$

$$C V_{rpp} = I_{dc} T_2$$

$$V_{rpp} = \frac{I_{dc} T_2}{C}$$

$$\text{If } T_1 = T_2 \text{ then } T_1 + T_2 = T \Rightarrow T_1 = T_2 = T/2$$

$$\therefore V_{rpp} = \frac{I_{dc} \cdot T}{2C} = \frac{I_{dc}}{2Cf} \quad \left(\because T = \frac{1}{2f} \right)$$

$$\therefore V_{rpp} = \frac{I_{dc}}{2fC}$$

It is observed from the wave form of FWR with filter that, it looks like a triangular wave form. Hence, the RMS value of a ripple is obtained by

$$V_{r,rms} = \frac{\text{Maximum value}}{2\sqrt{3}}$$

$$\therefore V_{r,rms} = \frac{V_{rpp}}{2\sqrt{3}} = \frac{\left(\frac{I_{dc}}{2fC} \right)}{2\sqrt{3}}$$

$$\therefore V_{r,rms} = \frac{I_{dc}}{4\sqrt{3}fC}$$

$$\therefore V_{ac} = \sqrt{V_{r,rms}^2} = V_{r,rms} = \frac{I_{dc}}{4\sqrt{3}fC}$$

$$\text{W.K.T } V_{dc} = I_{dc} \cdot R_L$$

$$\therefore \text{Ripple factor} = \gamma = \frac{V_{ac}}{V_{dc}} = \frac{\left(\frac{I_{dc}}{4\sqrt{3}f \cdot C} \right)}{I_{dc} \cdot R_L}$$

$$\Rightarrow \gamma = \frac{1}{4\sqrt{3}f \cdot C \cdot R_L}$$

$$\therefore \boxed{\text{Ripple factor} = \gamma = \frac{1}{4\sqrt{3}f \cdot C \cdot R_L}}$$

3) LC - Filter (or) L-section filter:

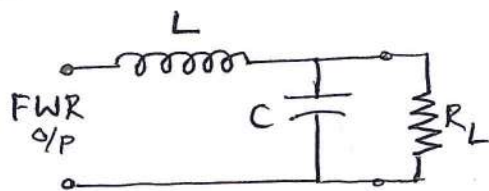
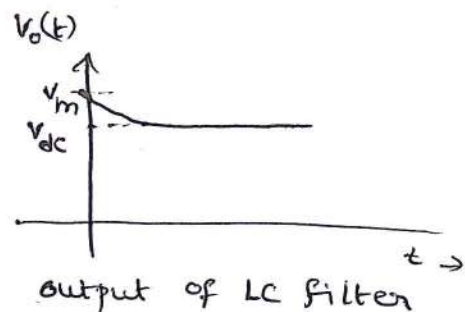


Fig: L-section (or) LC-filter



We know that the ripple factor of inductor filter is directly proportional to the load resistance R_L and inversely proportional to the load resistance R_L in capacitor filter. When these two filters are combined to form LC filter as shown in the above circuit, the ripple factor will become independent of load resistance (R_L).

If the value of the inductor is increased, it will increase the time of conduction. At some critical value of inductance either D_1 diode (or) D_2 diode of FWR will always remain in conduction.

Expression for ripple factor:

The fourier series expansion of the output voltage is expressed as $V_L = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos 2\omega t$

The dc value of load voltage is $V_{dc} = \frac{2V_m}{\pi}$

RMS value of the ripple, present in $V_L = \left(\frac{4V_m}{3\pi} \right) / \sqrt{2}$

$$\text{i.e. } V_{r, rms} = \frac{4V_m}{3\pi\sqrt{2}}$$

$$I_{r, rms} = \frac{V_{r, rms}}{X_L} = \left(\frac{4V_m}{3\pi\sqrt{2}} \right) \frac{1}{X_L} = \frac{4V_m}{3\pi\sqrt{2} X_L}$$

$$\Rightarrow I_{r, rms} = \left(\frac{2V_m}{\pi} \right) \frac{2}{3\sqrt{2} X_L} = V_{dc} \cdot \frac{2}{3\sqrt{2} X_L}$$

$$I_{r, rms} = \frac{\sqrt{2}}{3X_L} V_{dc}$$

This current $I_{n,rms}$ flows through X_C , creates the ripple voltage in the o/p.

$$V_{ac} = I_{n,rms} \cdot X_C = \frac{\sqrt{2}}{3X_L} \cdot V_{dc} \cdot X_C$$

$$V_{ac} = \frac{\sqrt{2}}{3} \frac{X_C}{X_L} \cdot V_{dc}$$

$$r = \text{Ripple factor} = \frac{V_{ac}}{V_{dc}} = \frac{\frac{\sqrt{2}}{3} \frac{X_C}{X_L} V_{dc}}{V_{dc}}$$

$$\Rightarrow \boxed{r = \frac{\sqrt{2}}{3} \frac{X_C}{X_L}}$$

$$X_C = \frac{1}{2\omega C}, \quad X_L = 2\omega L, \quad \text{then}$$

$$r = \frac{\sqrt{2}}{3} \frac{1}{(2\omega C)(2\omega L)}$$

$$\Rightarrow \boxed{r = \frac{1}{6\sqrt{2} \omega^2 LC}}$$

Bleeder resistor (R_B):

It was assumed in the analysis that, for a critical value of inductance either diode D_1 or diode D_2 will always remain in conduction and the current will never fall to zero.

The incoming current consists of two components:

$$i) I_{dc} = \frac{2I_m}{\pi} \quad \text{and} \quad ii) \text{ ripple content } I_{rms} = \frac{I_m}{\sqrt{2}}$$

The peak value of AC current must always be less than dc current

$$\sqrt{2} I_{rms} \leq I_{dc}$$

$$\Rightarrow I_{rms} \leq \frac{I_{dc}}{\sqrt{2}}$$

$$\Rightarrow I_{rms} \leq \frac{V_{dc}}{\sqrt{2} R_L} \quad \left[\because I_{dc} \cdot R_L = V_{dc} \right]$$

We know that $I_{n,rms}$ of LC filter is

$$I_{n,rms} = \frac{\sqrt{2} V_{dc}}{3X_L}$$

$$\therefore \frac{\sqrt{2} V_{dc}}{3X_L} \leq \frac{V_{dc}}{\sqrt{2} R_L}$$

$$\Rightarrow 2R_L \leq 3X_L$$

$$\Rightarrow X_L \geq \frac{2R_L}{3}$$

$$\Rightarrow 2\omega L \geq \frac{2R_L}{3} \quad (\because \text{For } 2^{\text{nd}} \text{ order ripple frequency} = 2\omega)$$

$$\Rightarrow L \geq \frac{R_L}{3\omega}$$

$$\boxed{\text{Critical Inductance } L_c = \frac{R_L}{3\omega}}$$

At no load i.e. when the load resistance is 'infinity', the value of inductance tends to ' ∞ ', hence X_L becomes ' ∞ ' due to which the current becomes '0'. To overcome this problem a bleeder resistor (R_B) is connected across the load resistance as shown in below fig, so that minimum current will always be present in the circuit.

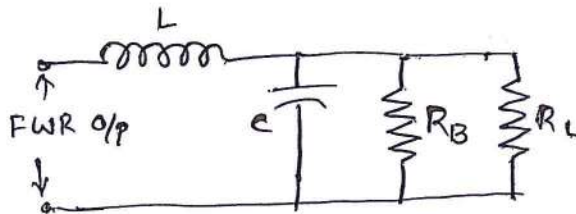


Fig: LC filter with bleeder resistor.

Advantages of bleeder resistor:

- 1) It improves the voltage regulation of the supply
- 2) It provides safety by acting as a discharging path for the capacitor.

4) Multiple L-section filters:

To achieve better ripple factor we can use two or more L-section filters as shown in below figure.

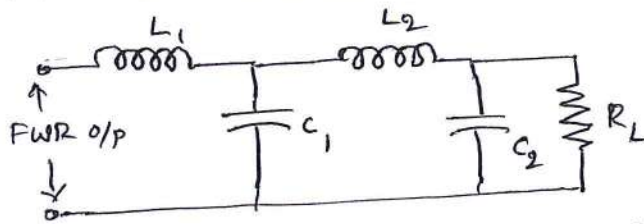


fig:- Multiple L-section filter.

The ripple factor
$$\gamma = \frac{\sqrt{2}}{3} \frac{X_{C1}}{X_{L1}} \frac{X_{C2}}{X_{L2}}$$

5) CLC (or) Π -section filter:

The CLC filter or Π -section filter basically consists of a capacitor filter followed by an LC section as shown in below.

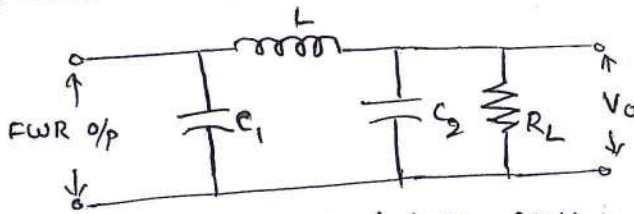


fig: CLC (or) Π -section filter.

The ripple factor
$$\gamma = \sqrt{2} \cdot \frac{X_{C1}}{R_L} \cdot \frac{X_{C2}}{X_L}$$

6) Multiple Π -section filters:

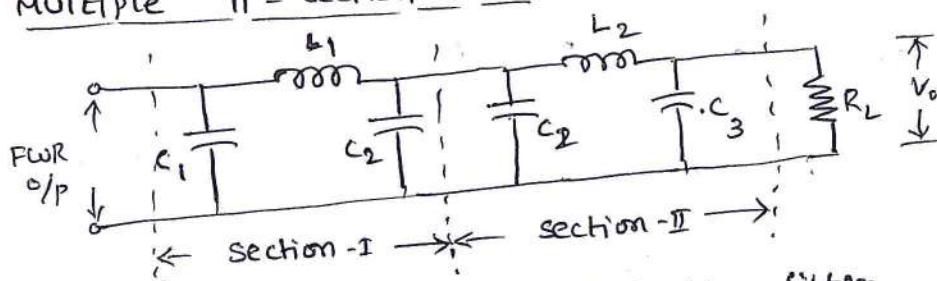


fig: Multiple Π -section filter.

Ripple factor
$$\gamma = \sqrt{2} \frac{X_{C1}}{R_L} \frac{X_{C2}}{X_{L1}} \frac{X_{C3}}{X_{L2}}$$

(10)

Comparison of Various filters in terms of ripple factor
considering each filter with full wave rectifier

Filter	Ripple factor (γ)
1) Inductor filter (or) choke filter	$\gamma = \frac{R_L}{3\sqrt{2} \omega L}$
2) Capacitor filter	$\gamma = \frac{1}{4\sqrt{3} f C R_L}$
3) LC - filter (or) L-section filter	$\gamma = \frac{\sqrt{2}}{3} \frac{X_C}{X_L} = \frac{\sqrt{2}}{3} \frac{1}{(2\omega C)(2\omega L)}$ $= \frac{\sqrt{2}}{3} \frac{1}{4\omega^2 LC}$ $\therefore \gamma = \frac{1}{6\sqrt{2} \omega^2 LC}$ $\therefore \gamma = \frac{\sqrt{2}}{3} \frac{X_C}{X_L} = \frac{1}{6\sqrt{2} \omega^2 LC}$
4) CLC filter (or) π -section filter	$\gamma = \sqrt{2} \frac{X_{C_1}}{R_L} \frac{X_{C_2}}{X_L}$ $\Rightarrow \gamma = \sqrt{2} \frac{1}{(2\omega C_1) R_L} \cdot \frac{1}{(2\omega C_2)(2\omega L)}$ $\gamma = \frac{1}{4\sqrt{2} \omega^3 C_1 C_2 L R_L}$
5) Multiple L-section filter	$\gamma = \frac{\sqrt{2}}{3} \frac{X_{C_1}}{X_{L_1}} \cdot \frac{X_{C_2}}{X_{L_2}}$ $\Rightarrow \gamma = \frac{\sqrt{2}}{3} \frac{1}{(2\omega C_1)(2\omega C_2)(2\omega L_1)(2\omega L_2)}$ $\Rightarrow \gamma = \frac{\sqrt{2}}{3 \times 16 \omega^4 C_1 C_2 L_1 L_2}$

6) Multiple π -Section

$$\therefore Y = \frac{1}{24\sqrt{2}} \omega^4 C_1 C_2 L_1 L_2$$

$$Y = \sqrt{2} \frac{X_{C1}}{R_L} \frac{X_{C2}}{X_{L1}} \frac{X_{C3}}{X_{L2}}$$

$$\Rightarrow Y = \frac{\sqrt{2}}{(2\omega C_1)(2\omega C_2)(2\omega C_3)R_L(2\omega L_1)(2\omega L_2)}$$

$$Y = \frac{1}{16\sqrt{2} \omega^5 L_1 L_2 C_1 C_2 C_3 R_L}$$

In the output of Full wave rectifier, the 2nd order ripple is considered and all the higher order ripples are neglected. So, for a 2nd order ripple, $X_L = 2\omega L$. Similarly for a 2nd order ripple $X_C = \frac{1}{2\omega C}$. So in the above table there two formulas are used.

Problems

i) Calculate the value of inductance to use as an inductor-filter connected to a FWR operating at 60Hz, to provide a dc op with 4% ripple for a 100 Ω load.

Sol

Given frequency $f = 60\text{Hz}$

ripple factor $\gamma = 0.04$ ($\because$ 4% is given)

Load resistance $R_L = 100\Omega$

Inductance $L = ?$

We know that, for an inductor filter $\gamma = \frac{R_L}{3\sqrt{2} \omega L}$

$$\Rightarrow L = \frac{R_L}{3\sqrt{2} \omega \cdot \gamma} = \frac{100}{3\sqrt{2} \times (2\pi \times 60) \times 0.04}$$

$$\Rightarrow L = 1.563 \text{ H}$$

2) Calculate the value of Capacitance to use as a capacitor filter connected to a full wave rectifier operating at 400Hz, if the ripple factor is 10% for a load of 500Ω.

Sol) Given $f = 400\text{Hz}$, $R_L = 500\Omega$

$$\gamma = 10\% = 0.1$$

For full wave rectifier with C-filter

$$\gamma = \frac{1}{4\sqrt{3} f C R_L}$$

$$\Rightarrow C = \frac{1}{4\sqrt{3} f R_L \gamma} = \frac{1}{4\sqrt{3} \times 400 \times 500 \times 0.1}$$

$$C = 7.2168 \times 10^{-6} = 7.2168 \mu\text{F}$$

③ A full wave rectified voltage of 18V peak is applied across a 500μF filter capacitor. Calculate the ripple and dc voltage if the load takes a current of 100mA.

Sol)

Given, Peak voltage of the rectifier o/p $V_m = 18\text{V}$.

Capacitance $C = 500\mu\text{F} = 500 \times 10^{-6}\text{F}$

$f = 50\text{Hz}$ (assume)

Given $I_{dc} = 100\text{mA}$.

For a full wave rectifier with C-filter, dc value of load voltage is given by

$$V_{dc} = V_m - \frac{I_{dc}}{4fC} = 18 - \frac{100 \times 10^{-3}}{4 \times 50 \times 500 \times 10^{-6}}$$

$$V_{dc} = 17\text{V}$$

We know that $V_{dc} = I_{dc} \cdot R_L \Rightarrow R_L = \frac{V_{dc}}{I_{dc}} = \frac{17}{100 \times 10^{-3}}$

$$\Rightarrow R_L = 170\Omega.$$

$\therefore \gamma$ for FWR with C-filter = $\frac{1}{4\sqrt{3} (f C R_L)}$

$$\Rightarrow R_L = \frac{1}{4\sqrt{3} (f C \gamma)} = \frac{1}{4\sqrt{3} \times \frac{1}{50 \times 500 \times 10^{-6} \times 0.1}}$$

$$\therefore \gamma \approx 0.03396 = 3.39\%$$

NOTE: In full wave rectifier with C-filter dc value of load voltage $V_{dc} = V_m - \frac{V_{r,pp}}{2}$

$$\text{where } V_{r,pp} = \frac{I_{dc}}{2fC}$$

$$\therefore \boxed{V_{dc} = V_m - \frac{I_{dc}}{4fC}}$$

4) A 15-0-15 V (rms) ideal transformer is used with a full wave rectifier circuit with diodes having forward drop of 1V. The load is a resistance of 100 ohm and a capacitor of 10,000 μF is used as a filter across the load resistance. Calculate the dc load current and dc load voltage.

sol) Given that transformer secondary rms voltage = 15V.

$$V_{s,rms} = 15V, \text{ w.k.t } \sqrt{2} \cdot V_{s,rms} = V_m$$

$$\therefore V_m = 15 \times \sqrt{2} = 21.2132V$$

Given $C = 10000 \mu F = 0.01F$, Let $f = 50Hz$, Given $R_L = 100 \text{ ohms}$
We know that in full wave rectifier with C-filter,

$$V_{dc} = V_m - \frac{V_{r,pp}}{2}$$

$$V_{dc} = V_m - \frac{I_{dc}}{4fC}$$

$$V_{dc} = V_m - \frac{V_{dc}}{4fC R_L} \quad \left[\because I_{dc} = \frac{V_{dc}}{R_L} \right]$$

$$V_{dc} + \frac{V_{dc}}{4fC R_L} = V_m$$

$$V_{dc} = \frac{V_m}{\left[1 + \frac{1}{4fC R_L} \right]} = \frac{21.2132}{1 + \frac{1}{4 \times 50 \times 0.01 \times 100}} = 21.107V$$

If the voltage drop across the diode is considered,
then dc load voltage $V_{dc} = 21.107 - 1V = 20.107V$.

D

$$\text{Dc load Current } I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.1076}{100} = 0.201076 \text{ A}$$

5) Design an LC filter for FWR circuit, to provide an o/p voltage of 10V with a load current of 200mA and ripple is limited to 2%.

Sol:

Given $V_{dc} = 10\text{V}$,

$$I_{dc} = 200\text{mA}$$

$$r = 2\% = 0.02$$

we know that the critical inductance for an LC filter is

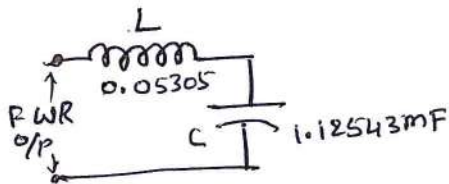
$$L_c = \frac{R_L}{3\omega} = \frac{(V_{dc}/I_{dc})}{3\omega} = \frac{\left(\frac{10}{200 \times 10^{-3}}\right)}{3 \times 2\pi \times 50} = 0.05305\text{H}$$

we know that the ripple factor for an LC filter is

$$r = \frac{1}{6\sqrt{2} \omega^2 L C} \Rightarrow C = \frac{1}{6\sqrt{2} \omega^2 L r}$$

$$\Rightarrow C = \frac{1}{6\sqrt{2} (2\pi \times 50)^2 \times 0.05305 \times 0.02}$$

$$\therefore C = 1.12543\text{mF}$$



6) Design a π -section filter for a FWR, to get $V_{dc} = 10\text{V}$, $I_L = 200\text{mA}$ and $r = 2\%$, Assume $C_1 = C_2 = C$

Sol)

Given $V_{dc} = 10\text{V}$, $I_L = 200\text{mA} = I_{dc}$

$$r = 2\% = 0.02$$

w.k.t for π -section filter $r = \sqrt{2} \frac{X_{C1}}{R_L} \frac{X_{C2}}{X_L}$

The FWR o/p has a ripple of 2nd order, so $X_L = 2\omega L$, $X_C = \frac{1}{2\omega C}$

$$\therefore V = \sqrt{2} \frac{1}{2\omega C_1 R_L} \cdot \frac{1}{2\omega C_2 \cdot 2\omega L}$$

$$V = \frac{1}{4\sqrt{2} \omega^3 C_1 C_2 L \cdot R_L} \quad [\text{given } C_1 = C_2 = C]$$

$$\therefore V = \frac{1}{4\sqrt{2} \omega^3 C^2 L R_L} \rightarrow \textcircled{1}$$

$$R_L = \frac{V_{dc}}{I_{dc}} = \frac{10}{200 \times 10^3} = 50 \, \Omega$$

$$L = \text{critical inductance} = \frac{R_L}{3\omega} = \frac{50}{3 \times 2\pi \times 50} = 0.05305 \, \text{H}$$

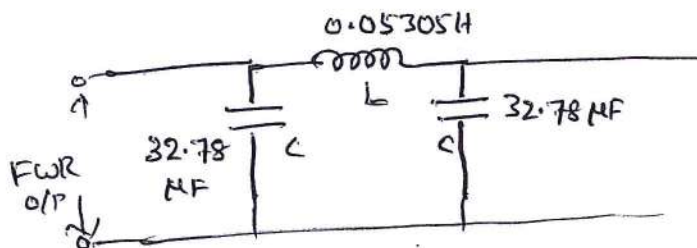
Substituting all parameters in equation ① we get

$$0.02 = \frac{1}{4\sqrt{2} (2\pi \times 50)^3 \times C^2 \times 0.05305 \times 50}$$

$$\Rightarrow C^2 = \frac{1}{4\sqrt{2} \times (2\pi \times 50)^3 \times 0.05305 \times 50 \times 0.02}$$

$$C = 3.278 \times 10^{-4} \, \text{Farads}$$

$$\Rightarrow C = 32.78 \, \mu\text{F}$$



①

UNIT-III
TRANSISTOR CHARACTERISTICS

Bipolar Junction Transistor: (BJT)

- * A Bipolar junction transistor (BJT) is a three terminal semiconductor device in which the current conduction is due to both majority charge carriers and minority charge carriers. Hence it is named bipolar.
- * In BJT the output current is controlled by input current and hence BJT is a Current Controlled device.
- * BJT is a three terminal device. The three terminals are namely Emitter (E), Base (B) and Collector (C).
- * Bipolar junction transistor is of two types. They are
 1. NPN Transistor
 2. PNP transistor

Structure and Symbol of BJT:

- * If a thin layer of an N-type silicon is sandwiched between two layers of P-type silicon, a PNP transistor is formed.
- * Similarly if a thin layer of a P-type silicon is sandwiched between two layers of n-type silicon, an NPN transistor is formed.
- * Germanium (Ge) can also be used in the place of silicon. The structures of NPN and PNP transistors are as shown in below

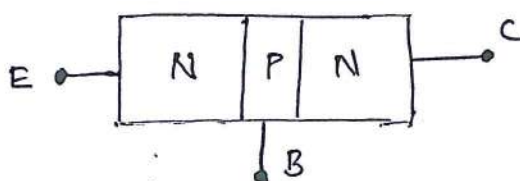


fig: Structure of NPN transistor

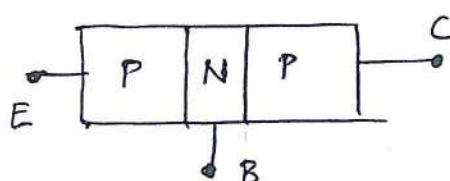


fig: structure of PNP transistor.

* BJT has 3 terminals. They are Emitter, Base and Collector, E, B and C respectively.

* The symbols of NPN and PNP transistors are as shown below.

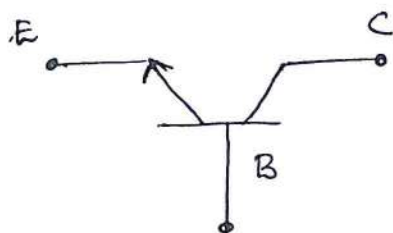


fig: NPN Transistor Symbol

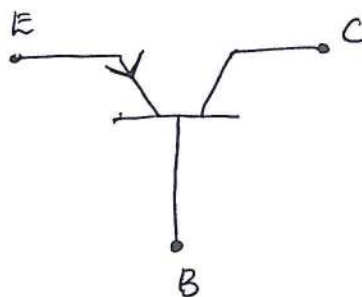


fig: PNP transistor Symbol.

* The arrow on the emitter terminal in the symbol of a BJT represents the direction of current flow.

* A BJT has two junctions namely emitter base junction (also known as emitter junction J_E) and collector base - junction (also known as collector junction J_C).

* The base region is very thin and usually it is very lightly doped.

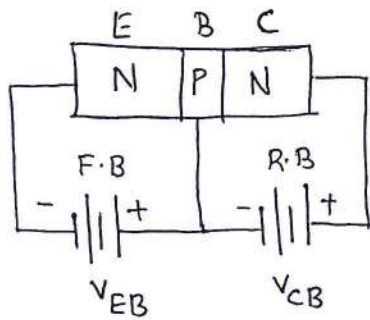
* Emitter region is larger than base region but smaller than collector region. Usually emitter is heavily doped whereas collector is moderately doped.

Transistor biasing:

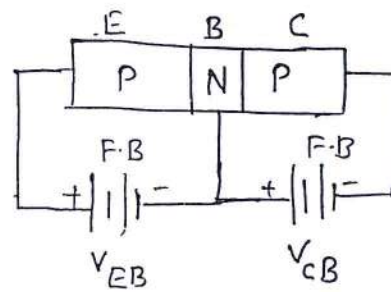
Most of the times, generally the emitter - base junction is forward biased and collector - base junction is reverse biased.

Since the emitter - base junction is forward biased, the emitter current flows through the base, into the collector region. Though the collector base junction is reverse biased, almost the entire emitter current flows in the collector region.

(2)



fig(a): NPN Transistor biasing



fig(b): PNP transistor biasing.

Operation of an NPN Transistor:

In an NPN transistor, when the emitter base junction is forward biased, it causes a lot of electrons from the emitter region to cross the emitter-base junction towards the base region, which constitutes the emitter current I_E . As the base is thin and lightly doped with P-type impurity, the number of holes in the base region is very less and hence a few electrons (say 5%) will recombine with the holes that are present in the base region and constitute a base current I_B . The remaining electrons (95% of electrons) cross the collector base junction and reach the collector region to constitute collector current ' I_C '. Thus the base current and collector current, when summed up gives the emitter current i.e. $I_E = I_B + I_C$

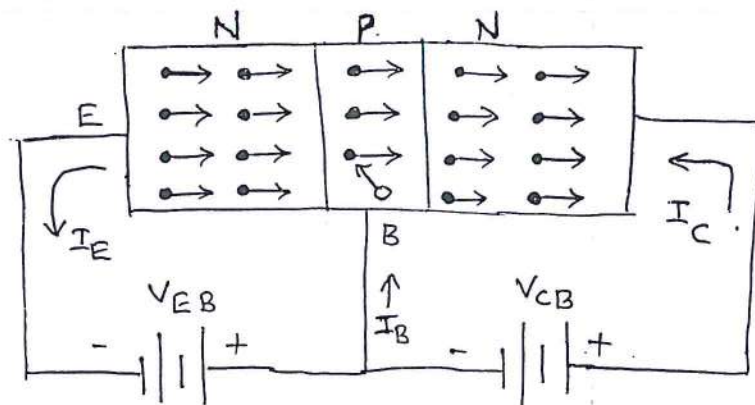


fig: Current in an NPN Transistor.

operation of a PNP transistor:

In a PNP transistor, when emitter base junction is forward biased, it causes a lot of holes from emitter region to cross the emitter base junction towards the base region, which constitutes the emitter current I_E . As the ^{base} is thin and lightly doped with n-type impurity, the number of electrons in the base region is very less and hence a few holes (say 5%) will recombine with the electrons that are present in the base region and constitute a base current I_B . The remaining holes (95% of holes) cross the collector base junction and reach the collector region to constitute the collector current I_C . Thus the base current and collector current when summed up, gives the emitter current i.e. $I_E = I_B + I_C$

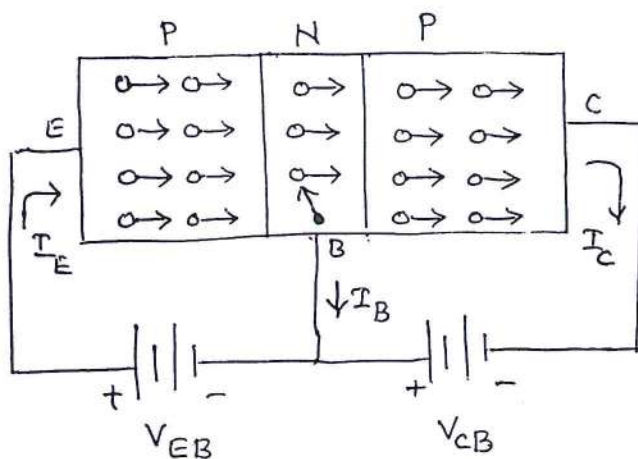


fig:- Current in a PNP transistor.

Transistor Configurations:

Depending on the input terminal, output terminal and common terminal there are three configurations for a transistor. They are

1. Common Base (CB) Configuration
2. Common Emitter (CE) Configuration
3. Common Collector (CC) Configuration.

1) Common base Configuration :

* It is also called as grounded base configuration.

In this configuration Emitter is the input terminal, Collector is the output terminal and Base is the common terminal (grounded terminal).

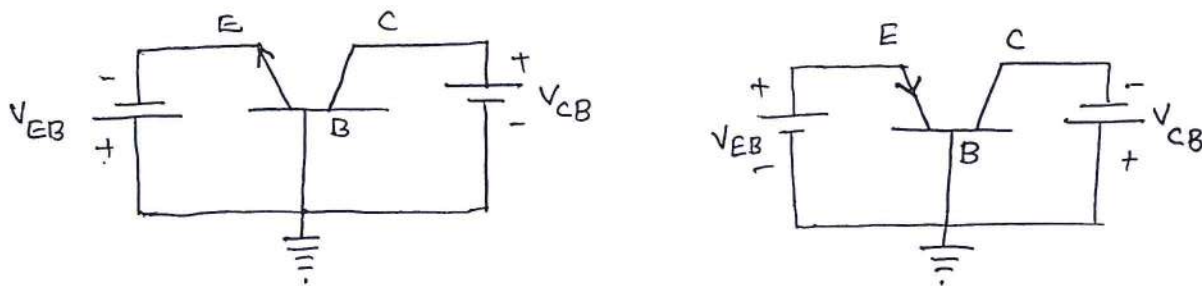


fig: common base configuration for NPN and PNP transistors.

* The current amplification factor (or) gain in CB Configuration is denoted by α (or) α_{dc} . It is defined as the ratio of collector current (I_C) to the emitter current (I_E).

$$\text{i.e. } \boxed{\alpha = \alpha_{dc} = \frac{I_C}{I_E}}$$

* If the AC supply is given at the i/p, the current amplification factor is denoted by α_{ac} and is defined as the ratio of change in collector current (I_C) to the change in emitter current (I_E).

$$\text{i.e. } \boxed{\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}}$$

2) Common Emitter Configuration :

* It is also called as grounded emitter configuration.

In this configuration base is the input terminal, collector is the output terminal and emitter is the common terminal (grounded).

terminal).

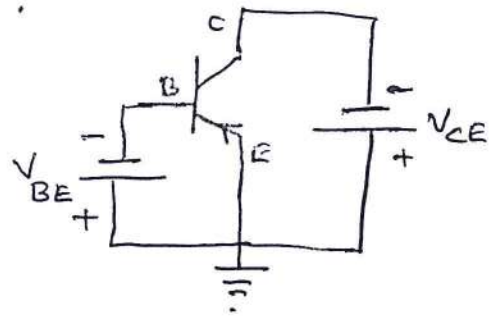
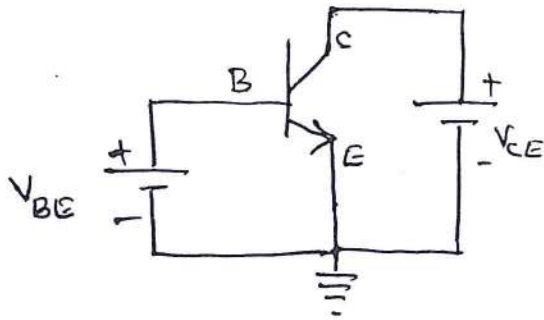


fig: Common Emitter Configuration for NPN and PNP transistors.

* The current amplification factor (or) Current Gain in CE Configuration is denoted by β (or) β_{dc} . It is defined as the ratio of collector Current (I_C) to the base Current (I_B).

i.e.
$$\beta = \beta_{dc} = \frac{I_C}{I_B}$$

* If the AC supply is given in the CE Configuration, the current amplification factor is denoted by β_{ac} and is defined as the ratio of change in collector Current to the change in base Current.

i.e.
$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

3) Common Collector Configuration:

* It is also called as grounded Collector Configuration. In this configuration base is the input terminal, emitter is the output terminal and Collector is the common terminal (or) grounded terminal.

* The current amplification factor (or) Current Gain in CC Configuration is denoted by γ (or) γ_{dc} . It is defined as

(4)

the ratio of the Emitter Current (I_E) to the base current (I_B).

i.e.
$$\gamma = \gamma_{dc} = \frac{I_E}{I_B}$$

* If the AC supply is used in CC Configuration, then the current amplification factor is denoted by γ_{ac} and is defined as the ratio of change in Emitter Current to the change in base current.

i.e.
$$\gamma_{ac} = \frac{\Delta I_E}{\Delta I_B}$$

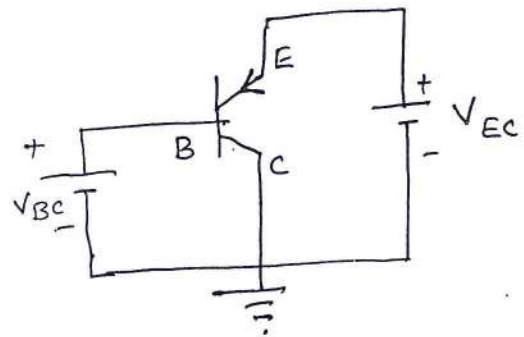
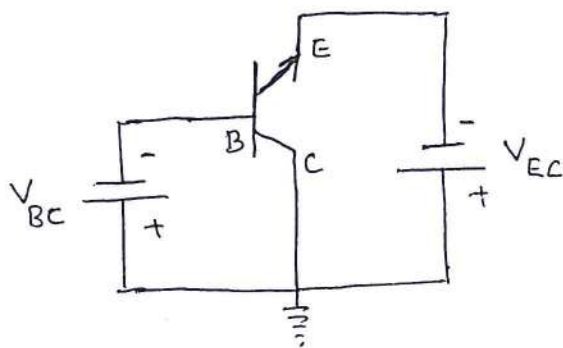


fig: Common Collector Configuration for NPN, PNP Transistors.

Relationship between α_{dc} , β_{dc} and γ_{dc} :-

α in terms of β :

we know that $\alpha_{dc} = \alpha = \frac{I_C}{I_E}$

$$\Rightarrow \alpha = \frac{I_C}{I_B + I_C} \quad \left(\because I_E = I_B + I_C \right)$$

Dividing both numerator and denominator by I_B
we get

$$\alpha = \frac{\left(\frac{I_C}{I_B} \right)}{\left(\frac{I_B + I_C}{I_B} \right)} \Rightarrow \alpha = \frac{\left(\frac{I_C}{I_B} \right)}{1 + \left(\frac{I_C}{I_B} \right)}$$

$$\Rightarrow \boxed{\alpha = \frac{\beta}{1+\beta}}$$

$$\left(\because \beta = \frac{I_C}{I_B} \right)$$

β in terms of α :

we know that $\beta_{dc} = \beta = \frac{I_C}{I_B}$

we know that $I_E = I_B + I_C$

$$\Rightarrow I_B = I_E - I_C$$

$$\therefore \beta = \frac{I_C}{I_B} = \frac{I_C}{I_E - I_C}$$

By dividing both numerator and denominator with I_E

we get

$$\beta = \frac{\left(\frac{I_C}{I_E} \right)}{\left(\frac{I_E - I_C}{I_E} \right)} = \frac{\left(\frac{I_C}{I_E} \right)}{1 - \left(\frac{I_C}{I_E} \right)}$$

$$\Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$\left(\because \alpha = \frac{I_C}{I_E} \right)$$

γ in terms of α :

we know that $\gamma_{dc} = \gamma = \frac{I_E}{I_B}$

we know that $I_E = I_B + I_C$

$$\Rightarrow I_B = I_E - I_C$$

$$\therefore \gamma = \frac{I_E}{I_E - I_C}$$

Dividing both numerator denominator with I_E , we get

(5)

$$\gamma = \frac{\left(\frac{I_E}{I_E}\right)}{\left(\frac{I_E - I_C}{I_E}\right)} = \frac{1}{1 - \frac{I_C}{I_E}}$$

$$\Rightarrow \boxed{\gamma = \frac{1}{1 - \alpha}} \quad \left(\because \alpha = \frac{I_C}{I_E}\right)$$

γ in terms of β

We know that $\gamma_{dc} = \gamma = \frac{I_E}{I_B}$

We know that $I_E = I_B + I_C$

$$\therefore \gamma = \frac{I_B + I_C}{I_B} = \frac{I_B}{I_B} + \frac{I_C}{I_B} = 1 + \frac{I_C}{I_B}$$

$$\Rightarrow \boxed{\gamma = 1 + \beta} \quad \left(\because \beta = \frac{I_C}{I_B}\right)$$

$$\therefore \boxed{\gamma = \frac{1}{1 - \alpha} = 1 + \beta}$$

** Large signal current gain, Transport factor and emitter efficiency :

i) Large signal current gain (α) :

The large signal current gain (α) is defined as the ratio of negative of the collector current increment to the emitter current.

$$\text{i.e. } \alpha = - \frac{(I_C - I_{C_{B_0}})}{I_E}$$

* I_{CB0} is the reverse saturation current flowing through the reverse biased collector base junction when emitter is open circuited. The magnitude of I_{CB0} is very negligible. So by neglecting I_{CB0} , the large signal current gain ' α ' becomes

$$\alpha = \frac{I_C}{I_E}$$

* Since I_C and I_E are flowing in opposite directions α is always positive. The α ranges from 0.90 to 0.99

* α is not constant. It varies with emitter current I_E , collector voltage V_{CB} and temperature.

ii) Transport factor (β^*):

Transport factor (β^*) is defined as the ratio of injected carrier current reaching collector junction (I_C) to the injected carrier current reaching emitter junction (I_E).

$$\text{Transport factor } (\beta^*) = \frac{\text{Injected carrier current reaching } I_C}{\text{injected carrier current reaching } I_E}$$

In the case of PNP transistor

$$\beta^* = \frac{I_{PC}}{I_{PE}}$$

iii) Emitter efficiency (or) emitter injection efficiency (γ):

Emitter efficiency (or) emitter injection efficiency (γ) is defined as the ratio of injected carrier current reaching emitter junction (I_E) to the total emitter current (I_E).

(6)

Emitter Efficiency $\gamma = \frac{\text{Injected Carrier Current reaching Emitter Junction}}{\text{Total Emitter Current}}$

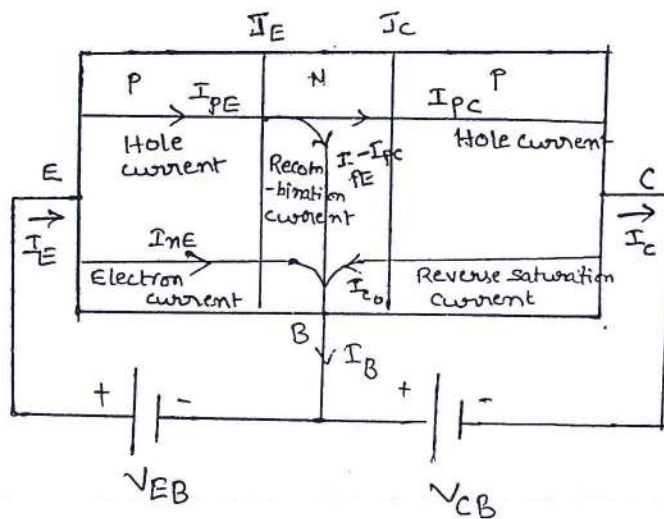
$$\gamma = \frac{I_{PE}}{I_E}$$

$$\therefore \gamma = \frac{I_{PE}}{I_{PE} + I_{NE}}$$

Emitter Efficiency represents the measure of how efficiently the emitter is injecting the charge carriers to the base.

Transistor Current Components:

The following figure shows the various current components in the PNP transistor in which emitter base junction is forward biased and the collector base junction is reverse biased.



I_{PE} , I_{NE} and I_{PC} :

The emitter current I_E consists of the hole current I_{PE} (holes crossing from emitter to base) and electron current I_{NE} (due to electrons crossing from base to emitter). The ratio of holes to electron current is I_{PE}/I_{NE} is proportional to the ratio of

the conductivity of p type material to that of n-type material. Conductivity is proportional to the level of doping. Generally in BJT, the doping level of the emitter is much larger than the doping level of base.

The holes crossing the emitter base junction J_E causes the current I_{PE} in emitter region. Some of the holes that crossed the emitter base junction recombines with the electrons in the base region. All the remaining holes cross the collector base junction J_C causes the current I_{PC} in base region. Hence the base current due to recombination of electrons and holes in the base region is $I_{PE} - I_{PC}$.

I_{CB_0} (or) I_{C_0} : Reverse saturation current :

When emitter is open circuited $I_E = 0$ and hence $I_{PC} = 0$.

In such a condition, the collector base junction acts as a reverse-biased diode, hence there exists a reverse saturation current ' I_{C_0} '.

From the figure, total collector current $I_C = I_{PC} - I_{CB_0}$

Transistor Current Equation : (Generalised Current equation of a transistor) :

When a transistor is connected to be operated in active region, the emitter base junction is forward biased and the collector base junction is reverse biased. The generalised current equation of the transistor is obtained as follows.

We know that the large signal current gain

$$\alpha = \frac{I_{PC}}{I_E} = \frac{I_C - I_{CB_0}}{I_E}$$

$$\Rightarrow \boxed{I_C = \alpha I_E + I_{CB_0}} \longrightarrow \textcircled{1}$$

Relation among I_C , I_B and I_{CB_0} :

From equation ① $I_C = \alpha I_E + I_{CB_0}$

we know that $I_E = I_B + I_C$

$$\therefore I_C = \alpha (I_B + I_C) + I_{CB_0}$$

$$\Rightarrow I_C (1 - \alpha) = \alpha I_B + I_{CB_0}$$

$$\Rightarrow I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{I_{CB_0}}{1 - \alpha}$$

we know that $\frac{\alpha}{1 - \alpha} = \beta$, $\frac{1}{1 - \alpha} = 1 + \beta$

$$\therefore \boxed{I_C = \beta I_B + (1 + \beta) I_{CB_0}} \longrightarrow \textcircled{2}$$

In CE configuration the large signal current gain

$$\beta = \frac{I_{PC}}{I_B} = \frac{I_C - I_{CE_0}}{I_B}$$

$$\Rightarrow \boxed{I_C = \beta I_B + I_{CE_0}} \longrightarrow \textcircled{3}$$

Relation between I_{CB_0} and I_{CE_0} :-

From ②, ③ we have $I_C = \beta I_B + (1 + \beta) I_{CB_0}$

$$I_C = \beta I_B + I_{CE_0}$$

From these two equations

$$\boxed{I_{CE_0} = (1 + \beta) I_{CB_0}}$$

Early Effect (or) Base width modulation:

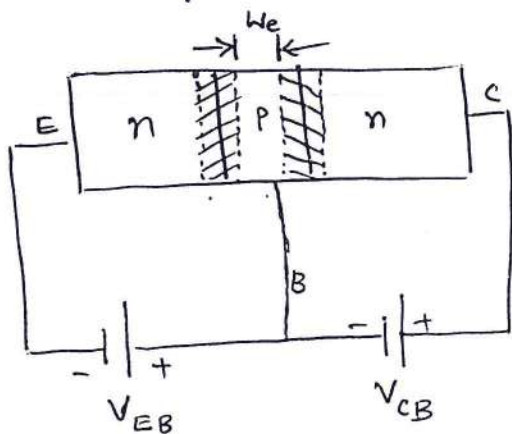
As the collector base junction is reverse biased in a transistor, the width of the depletion^{region} increases when the reverse voltage across the collector base junction V_{CB} is increased. Due to this, the effective base width of the base region decreases.

Definition for early effect:

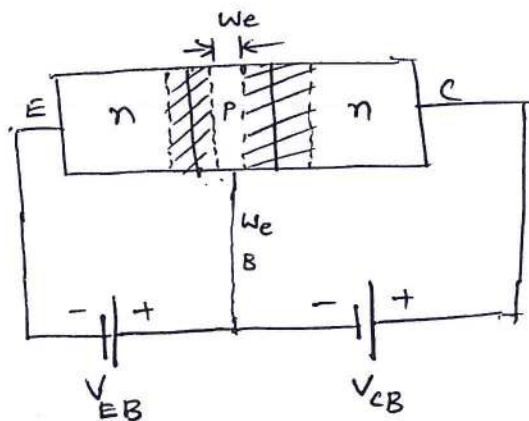
The variation in the effective width of the base in a bipolar junction transistor due to the variation in^{the} applied collector to base voltage (V_{CB}) is known as Early effect (or) base width modulation.

The decrease in effective base width has the following consequences.

- 1) It reduces the recombination of holes and electrons in the base region which may cause I_C to become approximately equal to I_E i.e. $I_C \approx I_E$ i.e. $\alpha \approx 1$
- 2) For extremely large voltages of V_{CB} , the effective base width may be reduced to zero, causing the voltage breakdown in the transistor. This phenomenon is called the punch-through effect.



fig(a) Transistor with I_E in F.B and I_C in R.B



fig(b): The decrement in effective base width (W_B) due to increased V_{CB} i.e. (early effect)

The above illustration shows the decrease in effective base width due to increased V_{CB} .

Punch Through Effect (or) Reach through effect:

* In the active region, the collector base junction is reverse biased. For every transistor there is certain limit on the maximum value of the collector to base voltage V_{CB} .

* When V_{CB} increases, the width of the depletion region at the collector base junction increases.

* When V_{CB} increases above $V_{CB \text{ max}}$, the increase in depletion region is such that it penetrates more into base until it makes contact with the depletion region of emitter base junction. This condition is called as punch through effect (or) reach through effect.

* When this situation occurs the transistor breakdown occurs.

Input and output characteristics of transistor Configurations:

i) Common Base (CB) Configuration:

In this configuration emitter is the input terminal, collector is the output terminal and base is the common terminal (or) grounded terminal.

The current amplification factor (α) of CB configuration

$$\text{i.e. } \alpha_{dc} = \alpha = \frac{I_C}{I_E}$$

where α ranges from 0.95 to 0.995.

Input characteristics of common base Configuration:

To determine the input and output characteristics, the circuit diagram of CB configuration is given below.

For Input characteristics, the collector to base voltage V_{CB} is kept constant at zero volts and the emitter current

I_E is noted for different values of V_{EB} . This is repeated for different fixed values of V_{CB} . The graph is drawn between the emitter base voltage V_{EB} and emitter current I_E at constant collector base voltage V_{CB} .

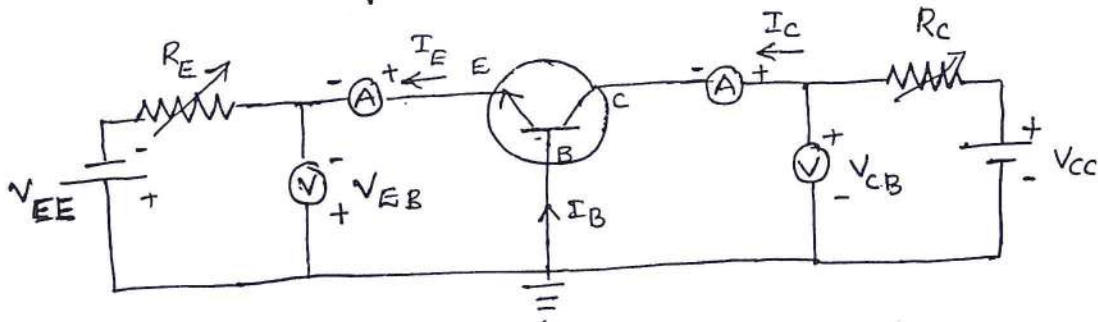


fig: Circuit to determine CB characteristics.

When V_{CB} is equal to zero and the emitter base junction is forward biased, the emitter base junction behaves as a forward biased diode so the emitter current I_E increases rapidly with the increase in V_{EB} .

When V_{CB} is increased keeping V_{EB} constant, the width of the depletion region of collector base junction increases, due to which the effective base width decreases, hence I_E increases. Therefore the curve shifts towards the left as V_{CB} is increased.

The input characteristics of CB configuration is as shown in below figure.

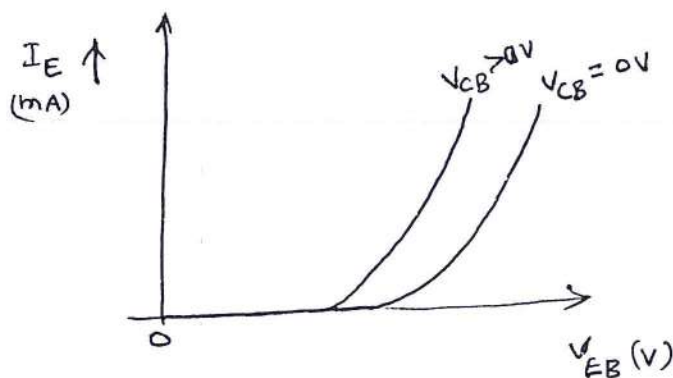


fig: CB input characteristics.

Output characteristics of common base configuration:

To determine the output characteristics, the emitter current I_E at the input side is kept constant by adjusting the emitter base voltage V_{EB} . Now the collector current I_C is noted for different values of collector to base voltage V_{CB} . This is repeated for different values of fixed I_E . Now the graph between V_{CB} and I_C is drawn for constant I_E .

The output characteristics of CB configuration is as shown in below figure.

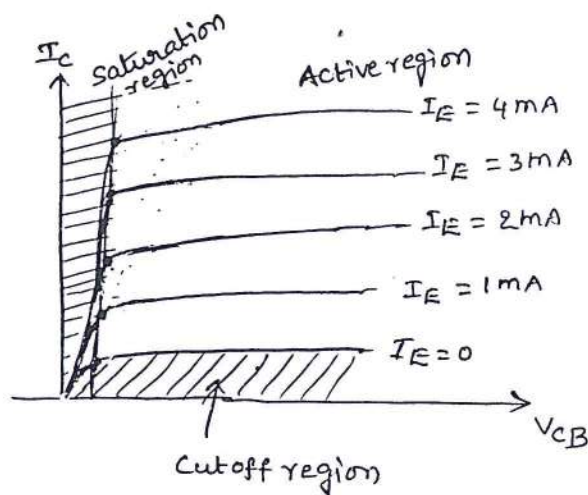


fig:- CB output characteristics.

From the output characteristics we can observe three different regions. They are cut off region, Saturation region and active region.

Cut off region:

The region along the horizontal axis, below the curve $I_E = 0$ is known as cut off region. In this region both the emitter-base junction as well as collector base junction are reverse biased. In this region the transistor is said to be the OFF switch.

Saturation region:

The region present at the left side of the vertical line is called the saturation region. In this region the emitter base junction (I_E) and collector base junction (I_C) are forward biased i.e. both the junctions are forward biased.

In this region a transistor is said to be an "ON" switch.

Active region:

The central region where the curves are uniformly spaced and slope is also of uniform, is called as Active region. In this region, the emitter base junction is forward biased and the collector base junction is reverse biased.

If the transistor is required to be worked as an amplifier it should be operated in the active region.

Transistor Parameters (or) Hybrid parameters of transistor in CB configuration:

i) Input impedance (h_{ib}) (or) R_i :

The ratio of change in (input) emitter to base voltage (V_{EB}) to the change in (input) emitter current (I_E) is called as input impedance denoted by h_{ib} . To get this input impedance the output collector-base voltage is kept constant.

$$\text{Therefore } h_{ib} = R_i = \frac{\Delta V_{EB}}{\Delta I_E}, \quad V_{CB} \text{ Constant}$$

The typical value of h_{ib} ranges from 20Ω to 50Ω .

ii) output Admittance (h_{ob}) (or) $\frac{1}{R_o}$:

It is defined as the ratio of the change in (output) collector current (I_C) to the change in (output) collector to base voltage (V_{CB}) with

the (input) emitter current (I_E) kept constant.

Therefore
$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, \quad I_E \text{ Constant}$$

The typical value of this parameter is of the order of 0.1 to $10 \mu\text{mhos}$.

iii) Forward current gain (h_{fb}) (or) α_{ac} :

It is defined as the ratio of change in (output) collector current (I_C) to the change in (input) emitter current (I_E) with constant (output) collector to base voltage V_{CB} . Therefore

$$h_{fb} = \alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}, \quad V_{CB} \text{ Constant}$$

The typical value varies from 0.9 to 1.

iv) Reverse voltage gain (h_{rb}):

It is defined as the ratio of the change in (input) emitter to base voltage (V_{EB}) to the change in (output) collector to base voltage (V_{CB}) with constant (input) emitter current (I_E).

Therefore
$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, \quad I_E \text{ Constant}$$

The typical value is of the order of 10^{-5} to 10^{-4} .

2) COMMON EMITTER CONFIGURATION: (CE Configuration)

In this configuration, base is the input terminal and collector is the output terminal and emitter is the common terminal (i.e. grounded terminal).

The current amplification factor of CE configuration is

$$\beta_{dc} = \frac{I_C}{I_B}$$

Generally β value ranges from 20 to 200.

Input characteristics of Common Emitter Configuration

The circuit diagram for determining the input and output characteristics is shown in below figure.

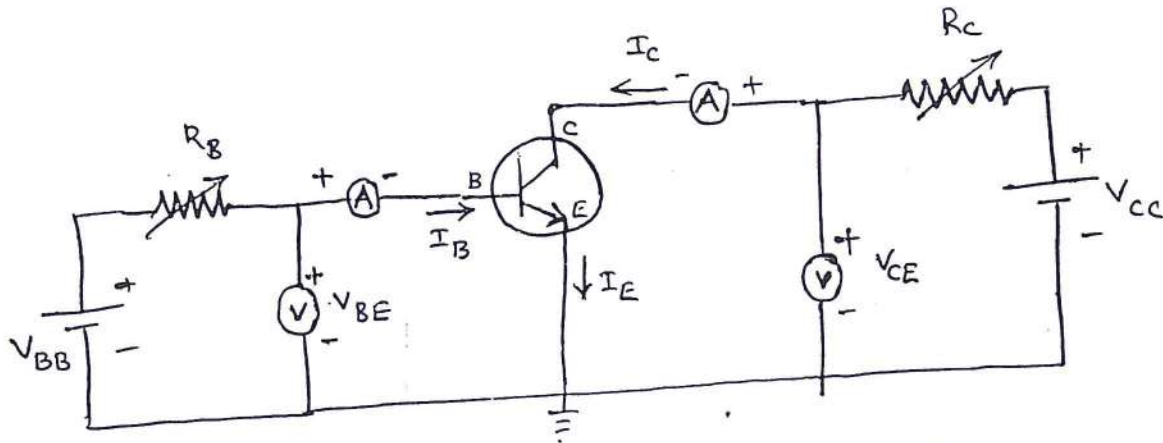


fig: circuit to determine CE characteristics.

To determine the input characteristics, the collector to emitter voltage V_{CE} (output voltage) is kept constant at zero volt. Now for different values of base to emitter voltage (V_{BE}), note down the values of corresponding base current (I_B). This procedure is repeated for different values of fixed V_{CE} and the graph between V_{BE} and I_B at constant V_{CE} is drawn.

When $V_{CE} = 0$, the emitter base junction is forward biased and the junction J_E behaves as forward biased diode. Hence the input characteristics for $V_{CE} = 0$ is similar to that of a forward biased diode. When V_{CE} is increased, the width of the depletion region across the collector-base junction increases due to which the effective base width decreases hence the recombination in the base region decreases due to which the base current I_B decreases. Hence the curve shifts to the right as V_{CE} increases. The input characteristics of CB configuration is as shown below.

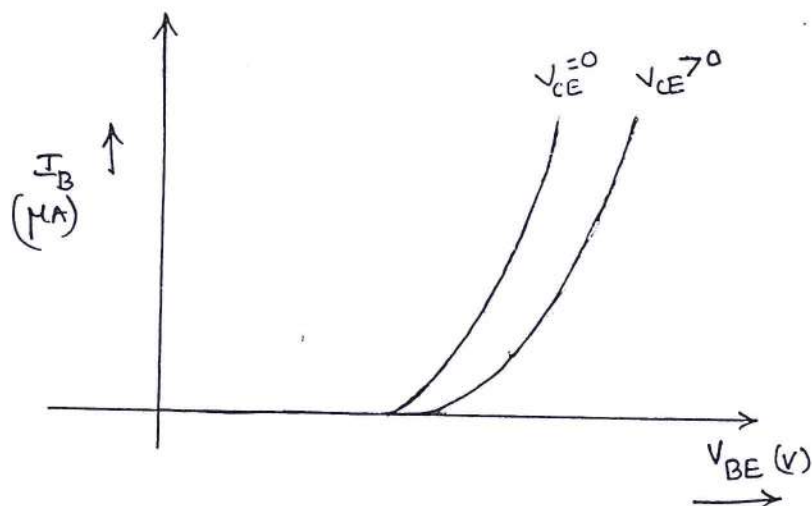


fig: CE input characteristics

output characteristics of CE configuration:

To determine the output characteristics, the base current (I_B) is kept constant by adjusting the base to emitter voltage (V_{BE}). Now the collector current I_C is noted down for different values of collector to emitter voltage V_{CE} . This is repeated for different values of fixed (I_B). Now the graph between V_{CE} and I_C is drawn at constant I_B .

The output characteristics of CE configuration is as shown in below figure.

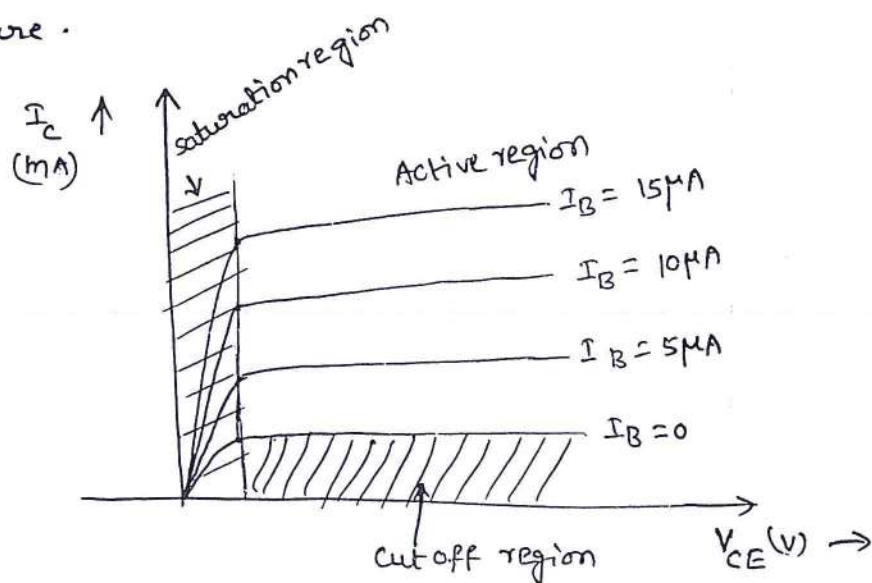


fig: CE output characteristics.

From the o/p characteristics we can observe three different regions. They are cut off region, saturation region and active region.

Cut-off region:

The region along the horizontal axis below the curve $I_B = 0$ is known as cut off region. In this region both the emitter-base junction and collector base junction are reverse biased. The transistor is said to be the OFF switch in cut off region.

Saturation region:

The region present at the left side of the vertical line is called as saturation region. In this region both the emitter base junction and collector base junction are forward biased. The transistor is said to be the ON switch in this region.

Active region:

The central region where the curves are uniformly spaced and the slope is also uniform is called as active region. In this region emitter base junction is forward biased and the collector base junction is reverse biased. If the transistor is required to be used as an amplifier, it should be operated in the active region.

Transistor parameters (or) Hybrid parameters of transistor in CE Configuration:

i) Input impedance (h_{ie}) or (R_i):

It is defined as the ratio of the change in (input) base to emitter voltage to the change in (input) base current with the (output) collector to emitter voltage V_{CE} kept constant.

Therefore
$$h_{ie} = R_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad , \quad V_{CE} \text{ Constant.}$$

The typical value of h_{ie} ranges from 500Ω to 2000Ω .

ii) output Admittance: (h_{oe}) or $\frac{1}{R_o}$:

It is defined as the ratio of the change in the (output) collector current to the change in the (output) collector to emitter voltage with the (input) base current I_B kept constant.

Therefore
$$h_{oe} = \frac{1}{R_o} = \frac{\Delta I_c}{\Delta V_{CE}} \quad I_B \text{ Constant}$$

The typical value of this parameter is in the order of 0.1 to $10 \mu\text{mhos}$.

iii) Forward Current gain (h_{fe}) or (β_{ac}) :

It is defined as the ratio of the change in the (output) collector current to the change in the (input) base current with the (output) collector to emitter voltage V_{CE} kept constant.

Therefore
$$h_{fe} = \frac{\Delta I_c}{\Delta I_B} = \beta_{ac} \quad , \quad V_{CE} \text{ Constant}$$

The typical value of this parameter is in the range of 20 to 200 .

iv) Reverse Voltage gain (h_{re}) :

It is defined as the ratio of the change in the (input) base to emitter voltage to the change in the (output) collector to emitter voltage with the (input) base current I_B kept constant.

Therefore
$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \quad I_B \text{ Constant}$$

The typical value of this parameter is of the order of 10^{-5} to 10^{-4} .

3) Common collector configuration (CC configuration):

In this configuration base is the input terminal, emitter is the output terminal and collector is the common terminal (grounded terminal).

The current amplification factor of CC configuration is

$$\beta_{dc} = \frac{I_E}{I_B}$$

Input characteristics of Common collector Configuration:

The circuit diagram for determining the characteristics of both input and output is shown in below figure.

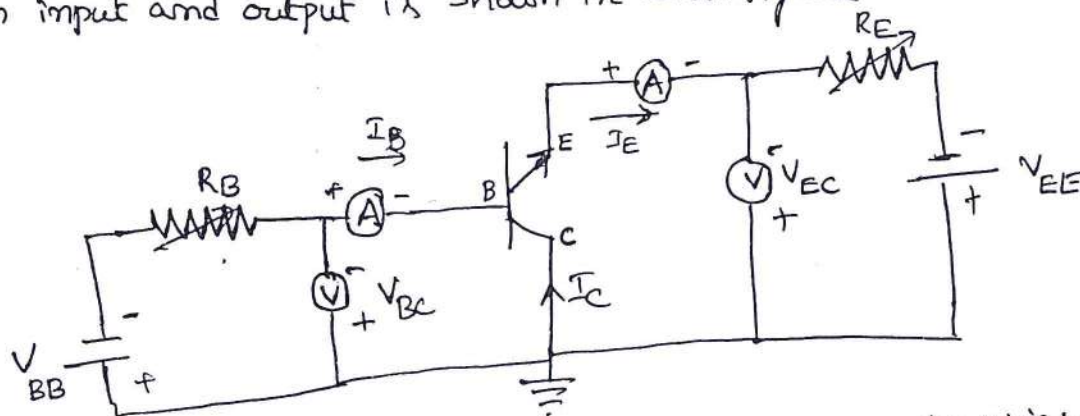


Fig: circuit to determine CC characteristics

To determine the input characteristics, V_{EC} is kept at constant. The base current I_B is noted for different values of base to collector voltage (V_{BC}). This is repeated for different fixed values of V_{EC} . The graph between V_{BC} versus I_B for different values of V_{EC} is drawn.

The common collector input characteristics are quite different from either CB (or) CE input characteristics. This is due to the i/p voltage V_{BC} is dependent on the output voltage V_{EC} .

The relation between them is given by $V_{EC} = V_{EB} + V_{BC}$

The following figure shows the input characteristics of common collector configuration.

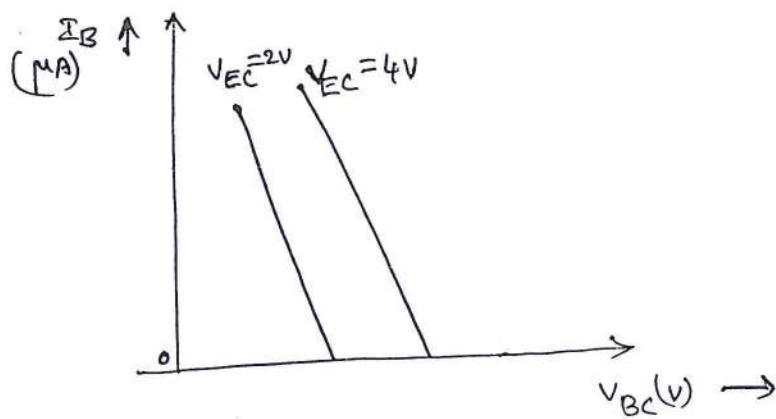


fig: CE input characteristics

Output characteristics of CE configuration:

To determine the output characteristics of CE configuration, the base current I_B is kept constant by adjusting the base to collector voltage V_{BC} . Now the emitter current I_E is noted down for different values of emitter to collector voltage V_{EC} . This is repeated for different values of fixed I_B . Now the graph between V_{EC} and I_E is drawn for constant I_B .

The output characteristics of CE configuration is as shown in below figure

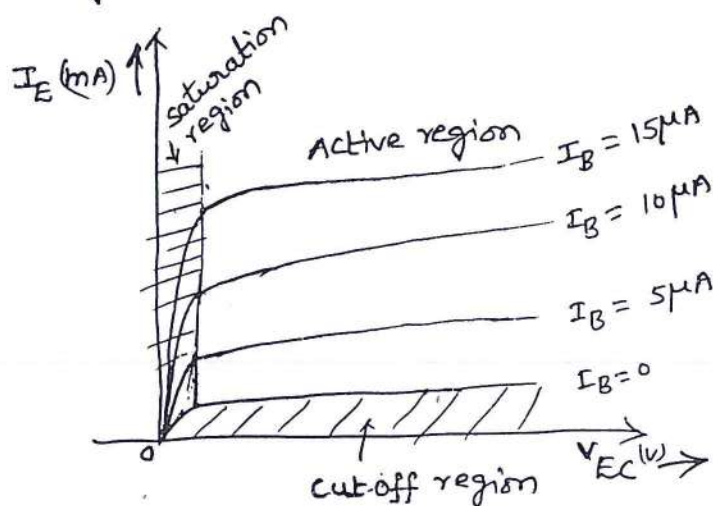


fig: CE output characteristics

From the output characteristics we can observe three different regions. They are cut off region, saturation region and active region.

Cut-off region:

The region along the horizontal axis below the curve $I_B = 0$ is known as cutoff region. In this region the emitter-base junction and the collector-base junction both are reverse biased. The transistor is said to be the off switch in this region.

Saturation region:

The region present at the left side of the vertical line is called saturation region. In this region both emitter-base junction as well as the collector base junctions are forward biased. The transistor is said to be the ON switch in this region.

Active region:

The central region where the curves are uniform in spacing and slope, is called as active region. In this region the emitter-base junction is forward biased and the collector-base junction is reverse biased. If the transistor is required to be used as an amplifier, it should be operated in this region.

Transistor Parameters (or) hybrid parameters of transistor in CC -

- Configuration:

i) Input Impedance h_{ic} (or) R_i :

It is defined as the ratio of the change in ^(i/p) base to collector voltage V_{bc} to the change in ^(i/p) base current with the (output) emitter to collector voltage V_{ec} kept at constant.

Therefore
$$h_{ic} = R_i = \frac{\Delta V_{bc}}{\Delta I_B}, \quad V_{ec} \text{ constant}$$

The input impedance of Common collector Configuration is very high when compared to the remaining two configurations.

ii) output admittance h_{oc} (or) $\frac{1}{R_o}$:

It is defined as the ratio of the change in (output) emitter current to the change in (output) emitter to collector voltage, with

constant (input) base current.

(14)

Therefore
$$h_{oc} = \frac{1}{R_o} = \frac{\Delta I_E}{\Delta V_{EC}} \quad , \quad I_B \text{ Constant}$$

iii) forward current gain : h_{fc} (or) γ_{ac} :-

It is defined as the ratio of the change in (output) emitter - current to the change in (input) base current with (output) emitter to collector voltage V_{EC} at constant.

$$h_{fc} = \gamma_{ac} = \frac{\Delta I_E}{\Delta I_B} \quad , \quad V_{EC} \text{ Constant}$$

iv) Reverse voltage gain h_{rc} :-

It is defined as the ratio of the change in (input) base to collector voltage (V_{BC}) to the change in (output) emitter to collector voltage (V_{EC}) with (input) base current I_B at constant.

$$h_{rc} = \gamma_{ac} = \frac{\Delta V_{BC}}{\Delta V_{EC}} \quad , \quad I_B \text{ Constant.}$$

comparison of CB, CE, CC configurations :

Property	CB	CE	CC
Input resistance	Low (about 100Ω)	Moderate (about 750Ω)	High (about $750k\Omega$)
output resistance	High (about $450k\Omega$)	Moderate (about $45k\Omega$)	Low (about 25Ω)
Current gain	Low (1)	High	High
Voltage gain	about 150	about 500	less than 1
Applications	For high frequency ckt's	For Audio frequency circuits	For Impedance Matching

Important Formulae:

- 1) $I_E = I_B + I_C$
- 2) $\alpha_{dc} = \frac{I_C}{I_E}$, $\beta_{dc} = \frac{I_C}{I_B}$, $\gamma_{dc} = \frac{I_E}{I_B}$
- 3) $\alpha = \frac{\beta}{1+\beta}$
- 4) $\beta = \frac{\alpha}{1-\alpha}$
- 5) $\gamma = \frac{1}{1-\alpha}$, $\gamma = \beta + 1$
- 6) $I_C = \alpha I_E + I_{CB0} = \beta I_B + (1+\beta) I_{CB0}$
- 7) $I_C = \beta I_B + I_{CE0}$
- 8) $I_{CE0} = (1+\beta) I_{CB0}$

Problems:

1) In a common base transistor circuit, the emitter current is 6.28 mA, the collector current is 6.20 mA. Find the value of I_B and α_{dc} .

Sol) Given data $I_E = 6.28 \text{ mA}$, $I_C = 6.20 \text{ mA}$

We know that $I_E = I_B + I_C$

$$\Rightarrow I_B = I_E - I_C = 6.28 \times 10^{-3} - 6.20 \times 10^{-3}$$

$$\Rightarrow I_B = 0.08 \times 10^{-3} \text{ A}$$

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{6.20 \times 10^{-3}}{6.28 \times 10^{-3}} = 0.98$$

$$\therefore I_B = 0.08 \text{ mA} , \alpha_{dc} = 0.98$$

2) The common base DC current gain of a transistor is 0.967. If the emitter current is 10 mA. Then find base current.

Sol) Given DC current gain of a transistor in CB configuration

$$\alpha_{dc} = 0.967 , \text{ Given } I_E = 10 \times 10^{-3} \text{ A}$$

$$\Rightarrow \frac{I_C}{I_E} = 0.967 \Rightarrow I_C = 0.967 \times 10 \times 10^{-3}$$
$$I_C = 9.67 \text{ mA}$$

W.K.T $I_E = I_B + I_C$

$$10 \times 10^{-3} = I_B + 9.67 \times 10^{-3}$$

(15)

$$\Rightarrow \therefore I_B = 0.33 \text{ mA}$$

- 3) i) If a transistor has $\alpha = 0.97$, find the value of β .
 ii) If $\beta = 200$. Find the value of α .

sol) Given $\alpha = 0.97$

$$i) \beta = \frac{\alpha}{1-\alpha} = \frac{0.97}{1-0.97} = 32.333$$

$$ii) \text{ given } \beta = 200, \alpha = ?$$

$$\alpha = \frac{\beta}{1+\beta} = \frac{200}{1+200} = 0.99502$$

- 4) A transistor has $\beta = 150$, find the collector and base currents, if $I_E = 10 \text{ mA}$.

sol) Given $\beta = 150$, $I_E = 10 \text{ mA} = 10 \times 10^{-3} \text{ A}$
 we know that $\alpha = \frac{\beta}{1+\beta} = \frac{150}{1+150} = 0.99337$

W.K.T $\alpha = \frac{I_C}{I_E} = \frac{I_C}{10 \times 10^{-3}}$

$$\therefore 0.99337 = \frac{I_C}{10 \times 10^{-3}}$$

$$\Rightarrow I_C = 0.0099337 = 9.9337 \text{ mA}$$

W.K.T $I_E = I_B + I_C \Rightarrow I_B = I_E - I_C$

$$\Rightarrow I_B = (10 - 9.9337) \text{ mA} = 0.0663 \text{ mA}$$

$$\therefore I_C = 9.9337 \text{ mA}, I_B = 0.0663 \text{ mA} = 66.3 \mu\text{A}$$

- 5) If a transistor circuit has $\alpha = 0.98$, $I_{CB0} = I_{C0} = 5 \mu\text{A}$,
 $I_B = 100 \mu\text{A}$, find I_C and I_E .

sol) Given $\alpha = 0.98 \Rightarrow \beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$

Given $I_B = 100 \mu\text{A} = 100 \times 10^{-6} \text{ A} = 10^{-4} \text{ A} = 0.1 \text{ mA}$

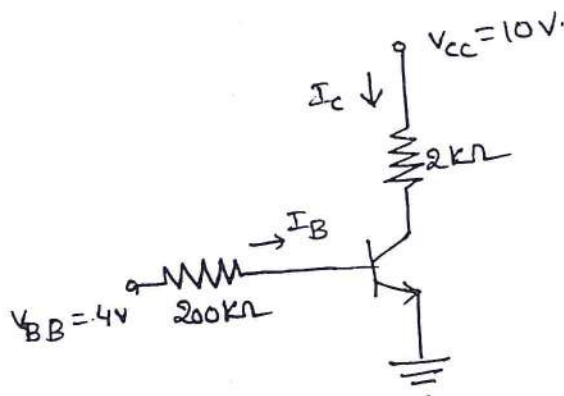
$$\begin{aligned}
 \text{w.k.T } I_C &= \beta I_B + (1 + \beta) I_{C_0} \\
 &= 49 \times 10^{-4} + (1 + 49)(5 \times 10^{-6}) \\
 &= 10^{-6} (49 \times 100 + (50)(5)) \\
 &= 5150 \times 10^{-6} \text{ A}
 \end{aligned}$$

$$I_C = 5.15 \text{ mA}$$

$$\text{w.k.T } I_E = I_B + I_C = 0.1 + 5.15 = 5.25 \text{ mA}$$

$$\therefore I_C = 5.15 \text{ mA}, I_E = 5.25 \text{ mA}$$

6) Determine base, collector, and emitter currents and V_{CE} for the circuit shown in below figure. $V_{BE \text{ ON}} = 0.7 \text{ V}$, $\beta = 200$.



sol)

$$\text{Given } V_{BE \text{ (ON)}} = 0.7 \text{ V}, \beta = 200$$

$$\text{From the input circuit } I_B = \frac{V_{BB} - V_{BE}}{200 \text{ k}\Omega} = \frac{4 - 0.7}{200 \times 10^3}$$

$$\Rightarrow I_B = 16.5 \mu\text{A}$$

$$\text{we know that } \beta = \frac{I_C}{I_B}$$

$$\Rightarrow 200 = \frac{I_C}{16.5 \times 10^{-6}}$$

$$\Rightarrow I_C = 200 \times 16.5 \times 10^{-6} = 3.3 \text{ mA}$$

$$\text{we know that } I_E = I_B + I_C = (16.5 \times 10^{-6}) + (3.3 \times 10^{-3})$$

$$I_E = 0.0165 \times 10^{-3} + 3.3 \times 10^{-3}$$

$$I_E = 3.3165 \text{ mA}$$

$$\text{From the output circuit } V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow 10 - (3.3 \times 10^{-3} \times 2 \times 10^3) - V_{CE} = 0 \Rightarrow V_{CE} = 10 - 6.6 \quad (16)$$

$$\Rightarrow \therefore V_{CE} = 3.4 \text{ V}$$

$$\therefore I_B = 16.5 \mu\text{A}, I_E = 3.3165 \text{ mA}, I_C = 3.3 \text{ mA}, \\ V_{CE} = 3.4 \text{ V} \quad \underline{A}$$

7) If $\alpha_{dc} = 0.99$ and $I_{CB0} = 50 \mu\text{A}$. Find the emitter current
sol)

$$\text{Given } \alpha_{dc} = 0.99, I_{CB0} = 50 \times 10^{-6} \text{ A}.$$

$$\text{Assume } I_B = 1 \mu\text{A}$$

$$\text{W.K.T } \beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99.$$

$$\text{W.K.T } I_C = \beta I_B + (1+\beta) I_{CB0} \\ = 99 \times 1 \times 10^{-6} + (1+99) 50 \times 10^{-6} \\ = 10^{-6} [99 + 5000]$$

$$I_C = 5.099 \text{ mA}$$

$$\text{W.K.T } I_E = I_B + I_C = 1 \times 10^{-6} + 5.099 \times 10^{-3} \\ I_E = 0.001 \times 10^{-3} + 5.099 \times 10^{-3}$$

$$\therefore \text{Emitter current } (I_E) = 5.1 \text{ mA}.$$

8) A Germanium Transistor used in a complementary symmetry amplifier has $I_{CB0} = 10 \mu\text{A}$, at 27°C and $h_{FE} = 50$.

a) find I_C when $I_B = 0.25 \text{ mA}$ and

b) Assume h_{FE} does not increase with temperature, find the value of new Collector Current if the transistor's temperature raises to 50°C .

$$\text{sol) Given } I_{CB0} = 10 \mu\text{A}, T_1 = 27^\circ\text{C}, h_{FE} = \beta = 50.$$

$$\text{a) } I_B = 0.25 \text{ mA}, I_C = ?, \text{ W.K.T } I_C = \beta I_B + (1+\beta) I_{CB0}$$

$$\Rightarrow I_C = 50 \times 0.25 \times 10^{-3} + (1+50)(10 \times 10^{-6})$$

$$\Rightarrow I_C = 13 \text{ mA}$$

b) $h_{fe} = \beta = 50$

Temperature $T_2 = 50^\circ\text{C}$.

New reverse saturation current $I_{CB0}' = I_{CB0} \cdot 2^{\frac{\Delta T}{10}}$
 $= 10 \times 10^{-6} \times 2^{\frac{50-27}{10}}$
 $= 49.2 \mu\text{A}$

New collector current $I_C' = \beta I_B + (1+\beta) I_{CB0}'$

$$\Rightarrow I_C' = 50 \times (0.25 \times 10^{-3}) + (1+50)(49.2 \times 10^{-6})$$

$$\therefore I_C' = 15 \text{ mA}$$

$\therefore$ New collector current = 15 mA.

Q) The reverse leakage current of a transistor when connected in CB Configuration is $0.2 \mu\text{A}$ and it is $18 \mu\text{A}$ when the same transistor is connected in CE Configuration. Calculate α_{dc} and β_{dc} when $I_B = 30 \mu\text{A}$.

Sol) Given $I_{CB0} = 0.2 \mu\text{A}$, $I_{CE0} = 18 \mu\text{A}$.

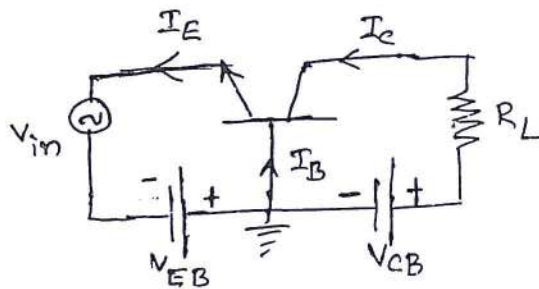
w.k.T $I_{CE0} = (1+\beta) I_{CB0} \Rightarrow 18 \times 10^{-6} = (1+\beta) 0.2 \times 10^{-6}$
 $\Rightarrow \therefore \beta_{dc} = 89$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{89}{1+89} = \frac{89}{90}$$

$$\therefore \alpha_{dc} = 0.988$$

$$\therefore \alpha_{dc} = 0.988, \beta_{dc} = 89$$

Transistor as an amplifier:



The emitter base junction is forward biased generally. Therefore V_{EB} is used, just to forward bias the transistor.

The above figure shows a CB amplifier. When there is a small change in input voltage it causes a change in input emitter current. This change in emitter current causes a change in collector current (I_C) that flows through R_L resulting a large voltage drop across it. Thus a small input change results a large output voltage. So the transistor can be used as an amplifier.

For example if there is a change of 0.1 V in the input, which further produces a change in emitter current of 1 mA . This change in emitter current of 1 mA will cause a change in collector current also by 1 mA approximately, that flows through the load.

If the load resistance is of $5\text{ k}\Omega$ then the voltage drop across R_L is $= 1 \times 10^{-3} \times 5 \times 10^3 = 5\text{ V}$.

$\therefore$ For a small change of 0.1 volts in input there is a 5 V change in the output. This means the voltage level of the signal is amplified.

Typical Transistor Junction voltage values:

- * Generally a transistor is operated in active region. That means the emitter base junction is forward biased and the collector base junction is reverse biased.
- * The typical values for the emitter to base junction voltage is V_{BE} , for a transistor made of silicon it is $0.7V$.
- * If the transistor is made of germanium it is $0.3V$.
- * The typical values for collector to base junction voltage V_{CB} can be anywhere between $3V$ to $20V$ for both npn and pnp transistors.
- * Junction voltages for different conditions such as active, saturation and cutoff, for an npn transistor at $25^{\circ}C$ are listed below

Type	$V_{CE sat}$	$V_{BE sat}$	$V_{BE active}$	$V_{BE cutoff}$
Si	0.2	0.8	0.7	0.0
Ge	0.1	0.3	0.2	-0.1

- * The entries in the table are for npn transistor. They may change for pnp transistor.

Photo transistor :

- * A Photo transistor is a much more sensitive semiconductor Photo device than Photo diode.
- * It is a light detector that permits a greater flow of current when the light is illuminated onto it.
- * A Photo transistor is usually connected in a CE configuration with base is open circuited. Even though there are three regions in a Photo transistor, only two regions emitter and collector are used.
- * A lens focuses the light on the base to collector junction.
- * In this device the base current is produced by the light falling on the collector to base junction of the photo transistor.
- * The following figures shows the circuit of a NPN Photo-transistor and it's symbol.

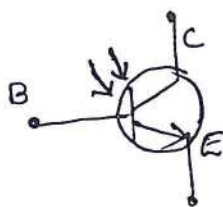


fig:- NPN Photo Transistor symbol

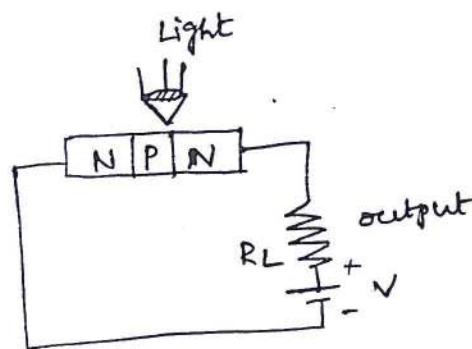


fig:- biasing arrangement.

- * when there is no light exposed onto the photo transistor collector to base junction, the minority charge carriers are generated thermally which causes the reverse saturation current I_{C0} . with $I_B = 0$, The collector current I_C is

$$\text{given by } I_C = \beta I_B + (1 + \beta) I_{C0} = \beta(0) + (1 + \beta) I_{C0}$$

$$\Rightarrow I_C = (1 + \beta) I_{C0}$$

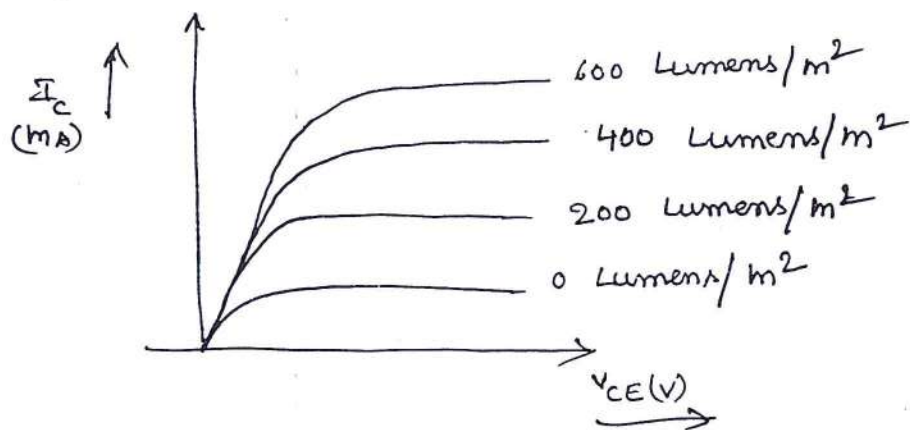
- * Now, when the light is illuminated onto the photo transistor,

the additional minority carriers are generated and the total collector current I_C becomes $I_C = (\beta + 1)(I_{C0} + I_L)$.

where I_L is the reverse saturation current due to the illumination of light.

* The current in photo transistor is dependent mainly due to illuminated light. So the collector current I_C increases, when the light intensity of the illuminated light is increased.

* The characteristics of photo transistor is as shown in below. The light intensity is measured in lumens/m^2 (or) Lux



Applications of Photo transistor:

1. Photo transistors are used in light detection systems.
2. Light operated switches
3. Reading of film soundtrack
4. High speed reading of computer punched cards and tape

NOTE :-

* Light intensity is measured in lumens/m^2 (or) Lux

$$1 \text{ Lux} = 1 \text{ lumen/m}^2$$

* The current produced by photo sensitive devices is very low which cannot be directly used for controlling applications. Therefore the current is amplified before applying to control circuits.

Eber's - MOLL Model :

* The general expression for collector current (I_C) of a transistor for any voltage across collector junction V_C and emitter current ' I_E ' is

$$I_C = -\alpha_N I_E - I_{C_0} \left(e^{\frac{V_C}{V_T}} - 1 \right)$$

where α_N is the current gain in normal operation of CB Configuration and I_{C_0} is the collector junction reverse saturation current.

* In inverted mode of operation of CB Configuration (where collector base junction is forward biased and emitter base junction is reverse biased), the above equation becomes

$$I_E = -\alpha_I I_C - I_{E_0} \left(e^{\frac{V_E}{V_T}} - 1 \right)$$

Where α_I is the current gain in inverted common base configuration and I_{E_0} is the reverse saturation current of emitter base junction.

* The Ebers-Moll model for a PNP transistor is given below.

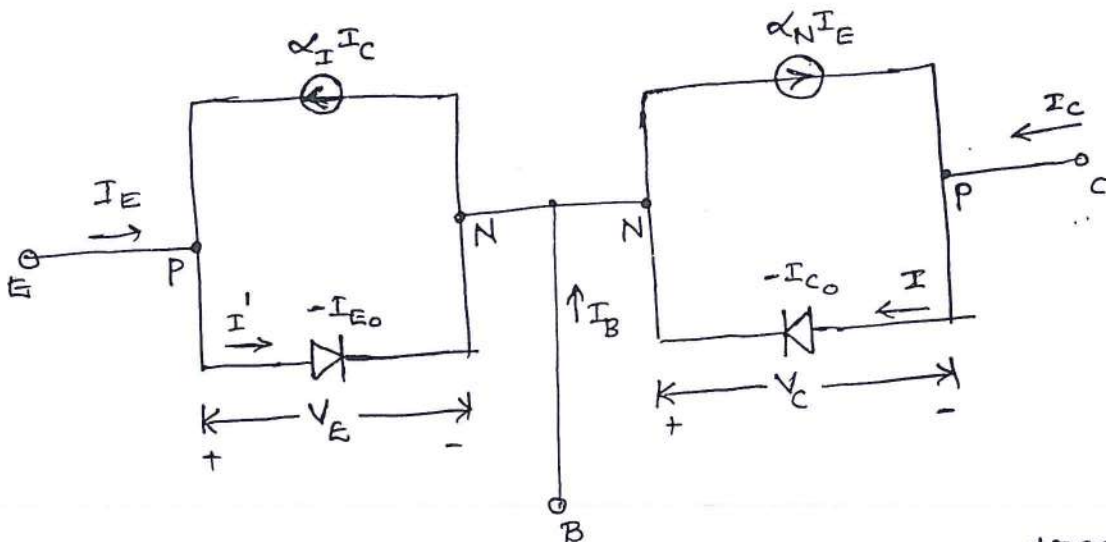


fig: Ebers-Moll Model for a PNP transistor.

* In Ebers Moll model of a transistor, two separate ideal diodes are connected back to back with saturation currents $-I_{E_0}$ and $-I_{C_0}$ and there are two dependent current sources as shown in above figure. Applying KCL to the above circuit we get

$$I_C = -\alpha_N I_E + I = -\alpha_N I_E - I_{C_0} \left(e^{V_C/V_T} - 1 \right)$$

Therefore the Ebers-Moll model is valid for both forward and reverse voltages applied across the transistor junctions.

Q) Is it possible to construct a transistor by simply placing two isolated diodes back to back?

Ans) The dependent current sources may be removed from the Ebers-Moll model of a transistor, if $\alpha_N = \alpha_I = 0$. If the base width is made much larger than the diffusion length of the minority charge carriers in the base, all the minority charge carriers will recombine in the base and no minority carrier will be available to reach the collector. Therefore, the transistor amplification factor α becomes zero. As a result the transistor action ceases. Hence it is not possible to construct a transistor by simply placing two isolated diodes back to back.

NOTE: Diffusion length is the distance travelled by an injected carrier before recombining ^{with} other kind of carrier.

Field Effect Transistor (FET):

→ The FET is a unipolar device, as the current conduction is only due to majority charge carriers.

→ FET is a voltage controlled device.

→ Like BJT, FET is also a 3 terminal device.

→ Based on the construction, the FET can be classified into two types. They are

1. Junction Field Effect Transistor (JFET)

2. Metal oxide semiconductor Field Effect Transistor (MOSFET)

→ The MOSFET some times called as Insulated Gate Field-Effect Transistor (IGFET) or Metal oxide silicon Transistor (MOST).

→ Depending on the majority charge carriers JFET has been

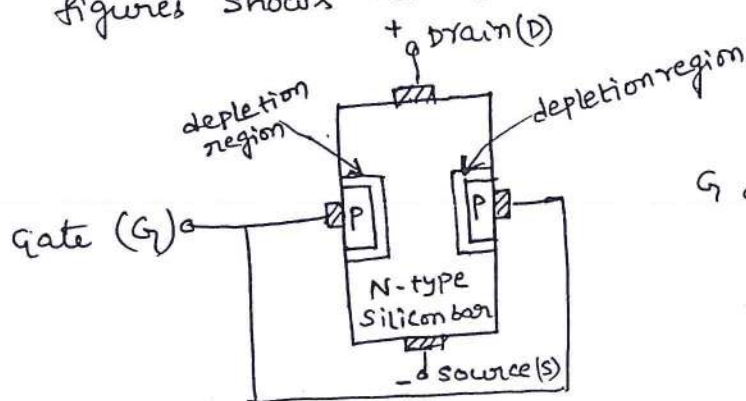
Classified into two types. They are

- 1) N-channel JFET with electrons as majority carriers.
- 2) P-channel JFET with holes as majority carriers.

N-channel JFET:

Construction of N-channel JFET:

- * It consists of an N-type silicon bar to which the ohmic contacts are made at the two ends of the bar to take the terminals out, called source and drain.
- * on either sides of the N-type silicon bar, heavily doped P-type silicon is diffused, by which PN junctions are formed. These layers are joined together and called as gate (G).
- * The source is a terminal which is connected to the negative pole of the battery. The electrons which are the majority charge carriers in N-type bar enter the bar through this terminal.
- * The drain is a terminal which is connected to the positive pole of the battery. The majority charge carriers leave the bar through this terminal.
- * The region of N-type silicon bar between the depletion regions of the two PN junctions is called as the channel. The below figures shows the structure of n-channel JFET and its symbol.



fig(a) Structure of an N-channel JFET

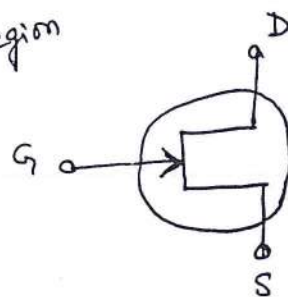


fig: symbol of an N-channel JFET.

** Operation of N-channel JFET (2) (Drain characteristics of N-channel JFET)

1) When $V_{GS} = 0$ and $V_{DS} = 0$:

When no voltage is applied between drain and source and gate and source (i.e. when $V_{GS} = 0$, $V_{DS} = 0$),

the thickness of the depletion regions round the PN junctions is uniform, as shown in figure (a)

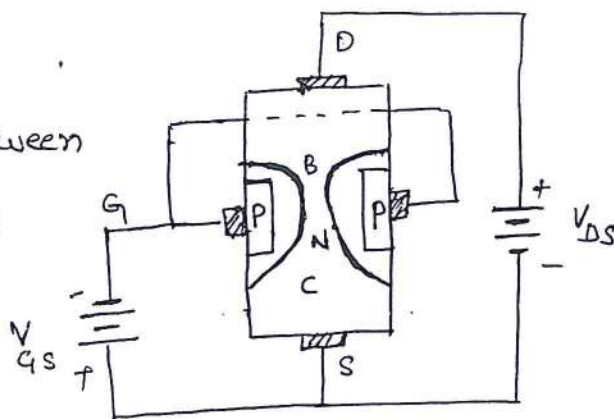


fig (b) JFET of N-channel under applied bias.

2) When $V_{DS} = 0$ and V_{GS} is decreased from zero (i.e. when $V_{DS} = 0$ as V_{GS} is negative) :

In this case, the PN junctions are reverse biased and hence the thickness of the depletion regions increases. As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased and hence the depletion regions become more thick, at a particular voltage of V_{GS} the depletion regions may contact with each other. In this condition, the channel is said to be in cutoff condition. The value of V_{GS} at which the cutoff condition is observed in the channel is called as cutoff voltage V_c .

3) When $V_{GS} = 0$ and V_{DS} is increased from zero : In this case the drain is positive with respect to source with $V_{GS} = 0$.

Now the majority carriers (electrons) flow through the N-channel from source to drain. Therefore the conventional current flows through the channel from drain to source. The magnitude of the drain current depends on the following factors.

- * The number of majority charge carriers available in the channel. i.e. the conductivity of the channel
- * The length 'L' of the channel.

- * The cross sectional area of the channel (denoted by A)
- * The magnitude of the applied voltage V_{DS} .

Hence there exists some resistance in the channel known as channel resistance denoted by R , given by

$$R = \frac{PL}{A}$$

$$I_D = \frac{V_{DS}}{R} = \frac{V_{DS}}{\left(\frac{PL}{A}\right)} = \frac{AV_{DS}}{PL}$$

* where ' ρ ' is the resistivity of the channel. Due to the existence of this channel resistance, there exists some voltage drop along the channel from drain to source. This voltage drop in the channel reverse biases the PN junctions and hence the thickness of the depletion regions also increases.

* As V_{DS} is increased the cross sectional area of the channel will be reduced. At a certain value of V_{DS} the cross sectional area at 'B' becomes minimum. At this voltage the channel is said to be pinched off and the respective value of V_{DS} is known as pinch off voltage denoted by ' V_p '. Any further increase in V_{DS} does not increase the drain current I_D .

* Hence pinch off voltage can also be defined as the voltage of V_{DS} at which the current I_D reaches to its constant saturation level.

* If V_{DS} is increased beyond pinch off voltage, at a certain voltage drain current suddenly increases that may cause break down in the JFET. The voltage of V_{DS} at which the break down occurs is known as break down voltage of JFET denoted by BV_{DSO} .

* The region from $V_{DS}=0$ to $V_{DS}=V_p$ is called ohmic region where the JFET can be used as a voltage variable resistor. The region from $V_{DS}=V_p$ to $V_{DS}=BV_{DSO}$ is called Pinch off region (or) saturation region.

4) when V_{GS} is negative and V_{DS} is increased :

when a negative value of voltage is applied to V_{GS} the PN junctions become more reverse biased. Hence for a negative value of V_{GS} the curve of I_D versus V_{DS} is similar to that of $V_{GS} = 0$, but the pinch off voltage V_p and breakdown voltage BV_{DGO} for this case are lower than + case of $V_{GS} = 0$.

The experimental setup to determine the JFET characteristics is as shown in below figure.

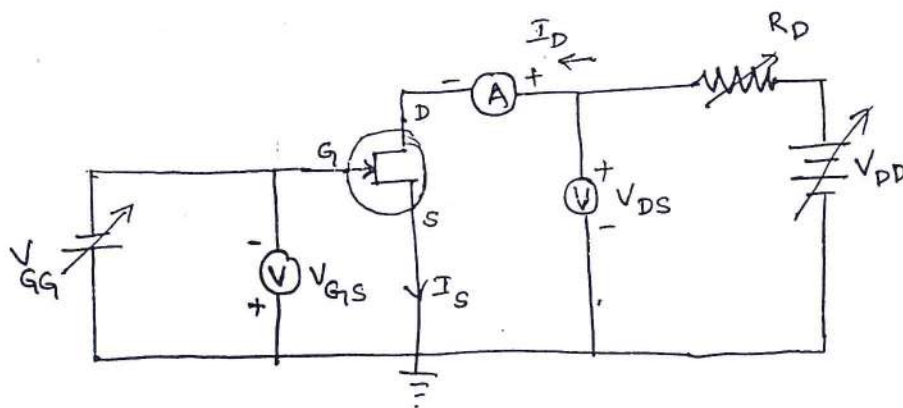


fig:- circuit to determine the characteristics of JFET of n-channel

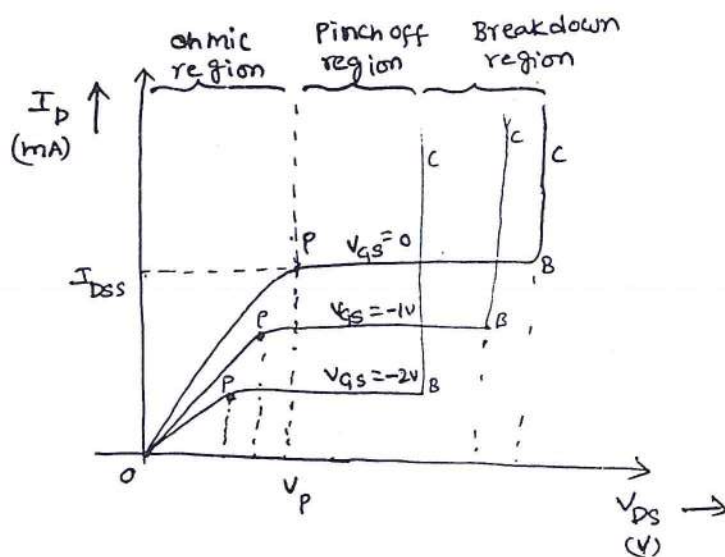


fig:- Drain characteristics of an N-channel JFET.

NOTE: From the drain characteristics of n-channel JFET it is clear that drain current I_D for different curves at a particular value of V_{DS} , is varied by varying the value of V_{GS} . Hence a JFET can be said to be a voltage controlled device.

Transfer Characteristics of an n-channel JFET:

For transfer characteristics V_{DS} is maintained constant at a suitable value greater than pinch off voltage ' V_p '. The Gate to Source Voltage V_{GS} is decreased from zero till drain current I_D is reduced to zero. The shape of the transfer characteristics is very nearly a parabola as shown below which is drawn between V_{GS} and I_D . This relationship between V_{GS} and I_D is defined by Shockley's equation.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

where I_D = Drain saturation current

and I_{DSS} = value of I_D when $V_{GS} = 0$.

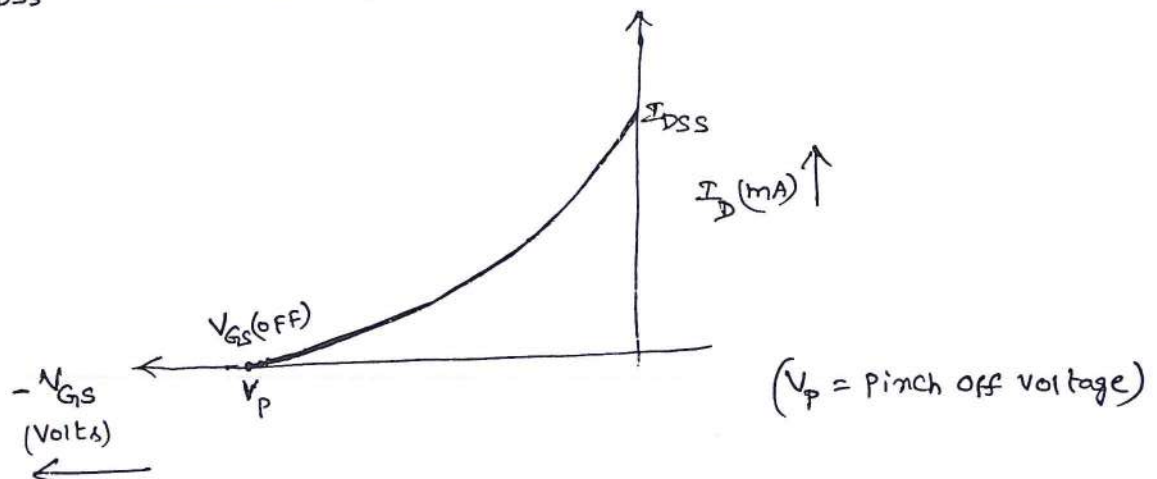


Fig:- Transfer characteristics of JFET.

The drain current $I_D = 0$, when $V_{GS} = V_{GS\text{OFF}}$, where $V_{GS\text{OFF}} = V_p$.

characteristic parameters of the JFET :

1) Mutual Conductance (or) Trans Conductance (g_m) :

* It is defined as the ratio of a small change in the drain current to the corresponding small change in the gate to source voltage at a constant drain to source voltage.

$$\text{Trans conductance } g_m = \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS} = \text{constant}} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} \text{ const}$$

* The units for transconductance is mhos.

2) Drain Resistance : (r_d)

* It is defined as the ratio of a small change in the drain to source voltage (V_{DS}) to the corresponding small change in the drain current, at a constant gate to source voltage (V_{GS}).

$$\text{Drain resistance } (r_d) = \left(\frac{\partial V_{DS}}{\partial I_D} \right)_{V_{GS} = \text{constant}} = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} \text{ const}$$

* The units for drain resistance is ohms

* The drain resistance at $V_{GS} = 0$ is called as drain source ON resistance.

3) Amplification factor (μ) :

It is defined as the ratio of a small change in the drain to source voltage ^{to the} corresponding small change in the gate to source voltage at a constant drain current.

$$\text{Amplification factor } (\mu) = - \left(\frac{\partial V_{DS}}{\partial V_{GS}} \right)_{I_D \text{ constant}} = - \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at } I_D \text{ constant}$$

Here - sign indicates that V_{DS} decreases when V_{GS} is increased

4) Relationship among FET Parameters (g_m , r_d and μ):

The amplification factor ' μ ' is equal to the product of the transconductance (g_m) and drain resistance (r_d).

$$\boxed{\mu = g_m \cdot r_d}$$

5) Power dissipation (P_D):

The power dissipation in FET is denoted by ' P_D ' and is equal to the product of V_{DS} and I_D

$$\boxed{P_D = V_{DS} \cdot I_D}$$

Q) Derive the relationship among g_m , r_d and μ

Ans) If there is a small change in V_{DS} from V_{DS} to $V_{DS} + \Delta V_{DS}$ and a small change in V_{GS} from V_{GS} to $V_{GS} + \Delta V_{GS}$, then the corresponding change in I_D may be obtained by applying the Taylor's theorem with neglecting higher order terms. Thus the small change in drain current ΔI_D is

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS} \text{ constant}} \cdot \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS} \text{ constant}} \Delta V_{GS}$$

dividing both sides by ΔV_{GS} we get

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \cdot \frac{\Delta V_{DS}}{\Delta V_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} \frac{\Delta V_{GS}}{\Delta V_{GS}}$$

If I_D is constant then $\frac{\Delta I_D}{\Delta V_{GS}} = 0$

$$\Rightarrow 0 = \left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \cdot \frac{\Delta V_{DS}}{\Delta V_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}}$$

$$\Rightarrow 0 = \frac{1}{n_d} \cdot (-\mu) + g_m$$

$$\Rightarrow \frac{\mu}{n_d} = g_m$$

$$\therefore \boxed{\mu = g_m n_d}$$

problems:

- ① when a reverse gate voltage of 12V is applied to JFET, the gate current is 1mA. Determine the resistance between gate and source.

sol

$$V_{GS} = 12V, I_G = 10^{-9} A.$$

$$\text{Gate to source resistance} = \frac{V_{GS}}{I_G} = \frac{12}{10^{-9}} = 12000 M\Omega$$

- ② when the reverse gate voltage of JFET changes from 4 to 3V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

sol

$$\Delta V_{GS} = \text{the change in gate voltage} = 4 - 3.9 = 0.1V.$$

$$\Delta I_D = \text{the change in drain current} = 1.6 \text{ mA} - 1.3 \text{ mA} = 0.3 \text{ mA}.$$

$$\text{Transconductance } g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \times 10^{-3}}{0.1} = 3 \text{ mS}$$

- ③ A FET has a drain current of 4 mA. If $I_{DSS} = 8 \text{ mA}$ and $V_{GS(off)} = -6V$, find the values of V_{GS} and V_P .

sol

$$\text{We know that } I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$$

$$\Rightarrow 4 \times 10^{-3} = 8 \times 10^{-3} \left[1 - \frac{V_{GS}}{(-6)} \right]^2$$

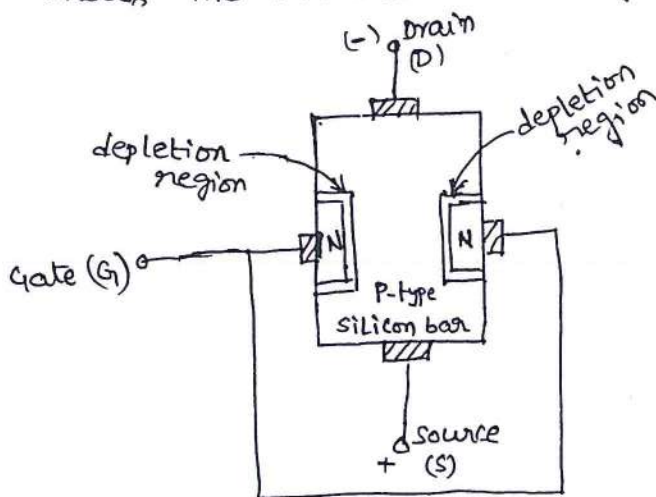
$$\Rightarrow \left(1 + \frac{V_{GS}}{6} \right)^2 = \frac{1}{2} \Rightarrow V_{GS} = -1.76V$$

$$V_P = V_{GS(off)} = -6V$$

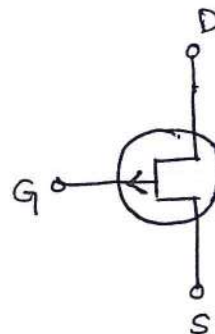
P-channel JFET :

Construction of P-channel JFET :

- * It consists of a P-type silicon bar to which the ohmic contacts are made at the two ends of the bar to take the terminals out called source and drain.
- * on both sides of the P-type Silicon bar, heavily doped n-type silicon is diffused by which PN junctions are formed. These layers are joined together to form the gate (G) terminal.
- * The source is a terminal which is connected to the positive pole of the battery and the drain is connected to the negative pole of the battery.
- * source is the terminal through which the majority carriers in P-type bar enter into the bar and they leave the bar through drain terminal.
- * The region of P-type silicon bar between the depletion regions of two PN junctions is called the channel. The following figures show the structure and symbol of the P-channel JFET.



fig(a) structure of a P-channel JFET



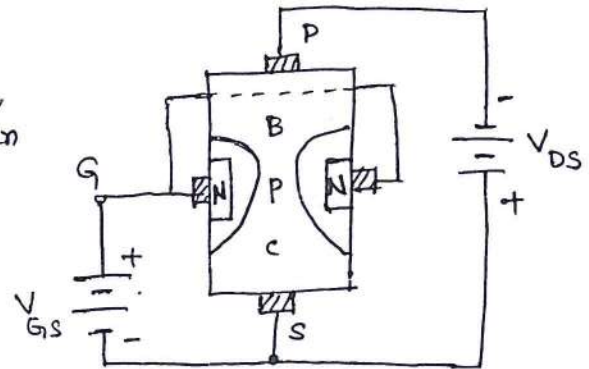
fig(b) symbol of a P-channel JFET

operation of a P-channel JFET (or) Drain characteristics of a

P-channel JFET :

1) when $V_{GS}=0$ and $V_{DS}=0$:

When no voltage is applied between drain and source, gate and source (i.e. $V_{GS}=0$, $V_{DS}=0$), then the thickness of the depletion regions around the PN junctions is uniform as shown in fig(a).



fig(c): JFET of P-channel under applied bias.

2) when $V_{DS}=0$ and V_{GS} is increased from zero (i.e. $V_{GS}>0$) :

In this case both the PN junctions are reverse biased and hence the thickness of the depletion region increases. As V_{GS} is increased from zero, the reverse voltage across the PN junctions will increase and hence the depletion regions become more thick. At a particular voltage of V_{GS} the depletion regions may contact with each other. In this condition the channel is said to be in Cutoff Condition. The value of V_{GS} at which the cut-off condition is observed, is called as cut-off voltage.

3) when $V_{GS}=0$ and V_{DS} is decreased from zero (i.e. $V_{DS}<0$)

When $V_{GS}=0$ and $V_{DS}<0$, the drain is negative with respect to source, due to which the majority carriers (holes) flow through the P-channel from source to drain that constitute the drain current I_D flows from source to drain. The magnitude of the drain current depends on the following factors.

- * The number of majority carriers available in the channel
- * The length of the channel i.e. 'L'.

* The cross section area of the channel (i.e. A)

* The magnitude of the applied voltage V_{DS} .

Hence there exists some resistance in the channel known as channel resistance denoted by ' R ' given by

$$R = \frac{\rho L}{A}$$

$$I_D = \frac{V_{DS}}{R} = \frac{V_{DS}}{\left(\frac{\rho L}{A}\right)} = \frac{AV_{DS}}{\rho L}$$

* where ρ is the resistivity of the channel. Due to the existence of channel resistance, there exists some voltage drop along the channel from source to drain which reverse biases the PN junctions and hence the thickness of the depletion regions is increased.

* As V_{DS} decreases the drain current I_D also increases and the cross sectional area of the channel gets reduced. At a certain value of V_{DS} the drain current I_D reaches to a constant value; and the cross sectional area becomes minimum. At this voltage the channel is said to be pinch off and the respective value of ' V_{DS} ' is called as pinch off voltage denoted by V_p . Any further decrease in V_{DS} does not increase the drain current I_D .

* If V_{DS} is decreased beyond pinch off voltage (V_p), at a certain voltage of V_{DS} , the drain current increases suddenly that may cause a breakdown in the JFET. The voltage at which the breakdown occurs is known as breakdown voltage of JFET, denoted by BV_{DS0} .

* The region from $V_{DS} = 0$ to $V_{DS} = V_p$ is called as the ohmic region where the JFET can be used as a voltage variable resistor. The region from $V_{DS} = V_p$ to $V_{DS} = BV_{DS0}$ is saturation (or) Pinch off region.

4) When V_{GS} is increased from zero ($V_{GS} > 0$) and V_{DS} is decreased from zero ($V_{DS} < 0$) :

When a positive value of voltage is applied to V_{GS} , the PN junctions become more reverse biased. Hence for a positive value of V_{GS} , the curve of I_D versus V_{DS} is similar to that of $V_{GS} = 0$ but the pinch off voltage V_p and breakdown voltage BV_{DS0} for this case are lower than the case of $V_{GS} = 0$.

The experimental setup to determine the JFET characteristics are as shown in below figure.

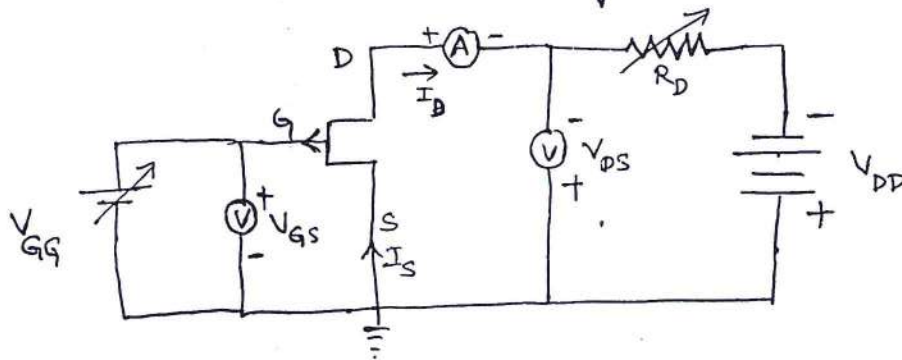


fig: circuit to determine the characteristics of P-channel JFET.

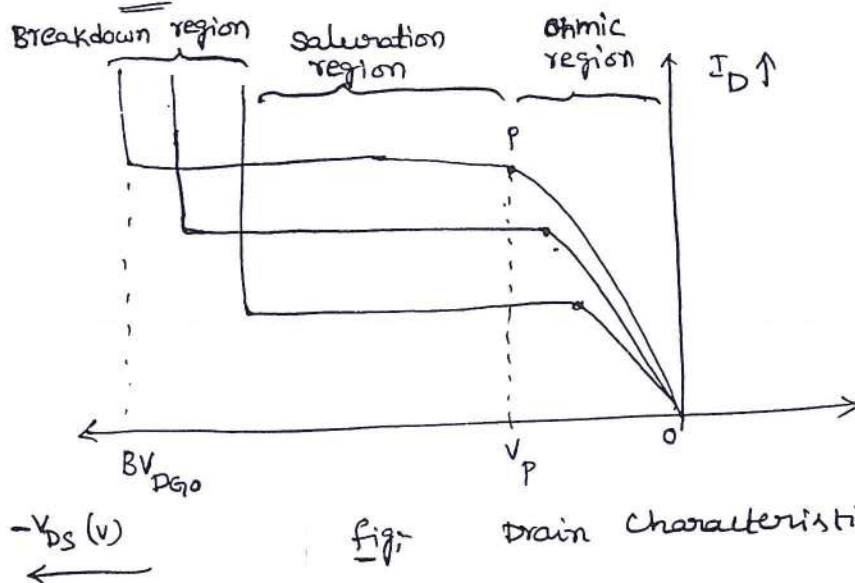


fig: Drain characteristics of P-channel JFET.

Transfer characteristics of a P-channel JFET:

For transfer characteristics V_{DS} is maintained constant at a suitable value greater than pinch off voltage ' V_p ', the gate to source voltage V_{GS} is increased from zero till drain current I_D is reduced to zero. The shape of the transfer characteristics is very nearly a parabola as shown below which is drawn between V_{GS} and I_D .

This relationship between V_{GS} and I_D is defined by Shockley's equation

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

where I_D = drain current

I_{DSS} = value of I_D at $V_{GS} = 0$.

The drain current $I_D = 0$ when $V_{GS} = V_{GS\ OFF} = V_p$.

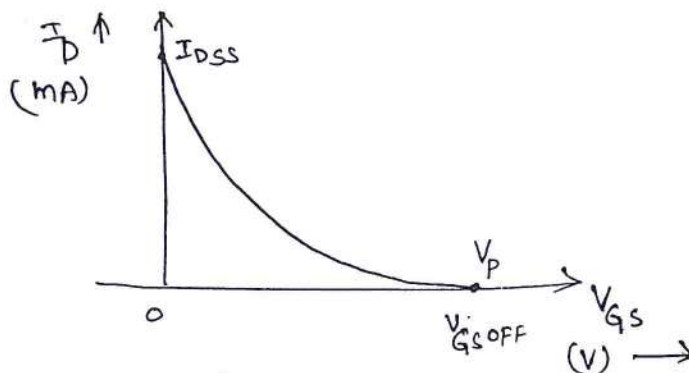


fig:- Transfer characteristics of a P-channel JFET.

Relationship between g_m , V_{GS} , I_{DSS} and V_p :

We know that $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2 \rightarrow (1)$

Differentiating the above equation with respect to V_{GS}

we get

$$\frac{dI_D}{dV_{GS}} = I_{DSS} \cdot 2 \left(-\frac{1}{V_p} \right) \left[1 - \frac{V_{GS}}{V_p} \right]$$

$$\frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_p} \left[1 - \frac{V_{GS}}{V_p} \right] \rightarrow (2)$$

We know that $\frac{dI_D}{dV_{GS}} = \frac{\Delta I_D}{\Delta V_{GS}} = g_m$

$$\therefore g_m = \frac{-2I_{DSS}}{V_p} \left[1 - \frac{V_{GS}}{V_p} \right] \text{ --- (3)}$$

From equation ① $1 - \frac{V_{GS}}{V_p} = \sqrt{\frac{I_D}{I_{DSS}}} \text{ --- (4)}$

$\therefore$ substituting equation ④ in equation ③

we get $g_m = \frac{-2I_{DSS}}{V_p} \sqrt{\frac{I_D}{I_{DSS}}}$

$$g_m = \frac{-2 \sqrt{I_D I_{DSS}}}{V_p}$$

Let $g_m = g_{m_0}$ when $V_{GS} = 0$

$\therefore$ From equation ③ when $V_{GS} = 0$

$$g_{m_0} = \frac{-2I_{DSS}}{V_p} \text{ --- (5)}$$

substituting equation ⑤ in equation ③ we get

$$g_m = g_{m_0} \left[1 - \frac{V_{GS}}{V_p} \right]$$

Applications of JFET:

- 1) FETs are used in RF (radio frequency) amplifiers in communication equipment and in FM tuners.
- 2) FET can be used as a buffer in measuring instruments, receiver since it has high input impedance and low output impedance.
- 3) Since FET is a voltage controlled device it can be used as a voltage variable resistor in some applications.
- 4) FETs are used in mixer circuits in FM and TV receivers.

- 5) FETs are used in digital circuits such as computers and memory circuits because of its small size.
- 6) FET can be used in oscillator circuits.

Comparison of JFET and BJT:

Bipolar Junction Transistor	Field Effect Transistor
1) BJT is a unipolar device	1) FET is Bipolar device.
2) The Current Conduction in BJT depends on both majority charge carriers and minority charge carriers	2) The Current Conduction in FET depends on majority charge carriers only.
3) BJT is a Current Controlled device	3) FET is a Voltage Controlled device.
4) It exhibits low input impedance because input circuit is forward biased. It has high output impedance	4) FET exhibits high input impedance and low output impedance.
5) BJTs are cheaper to produce	5) FETs are costlier when compared to BJT.
6) BJT occupies more space when compared to FET	6) FET occupies less space, hence they are preferred in manufacturing ICs
7) BJT has a positive temperature Coefficient	7) FET has a negative temperature Coefficient.
8) BJTs are not easy to fabricate	8) FET is easier to Fabricate than BJTs.

MOSFET (Metal oxide semiconductor Field Effect Transistor)

A MOSFET can also be called as Insulated Gate Field Effect Transistor (IGFET) or Metal oxide silicon Transistor (MOST)

There are two basic forms of MOSFET. They are

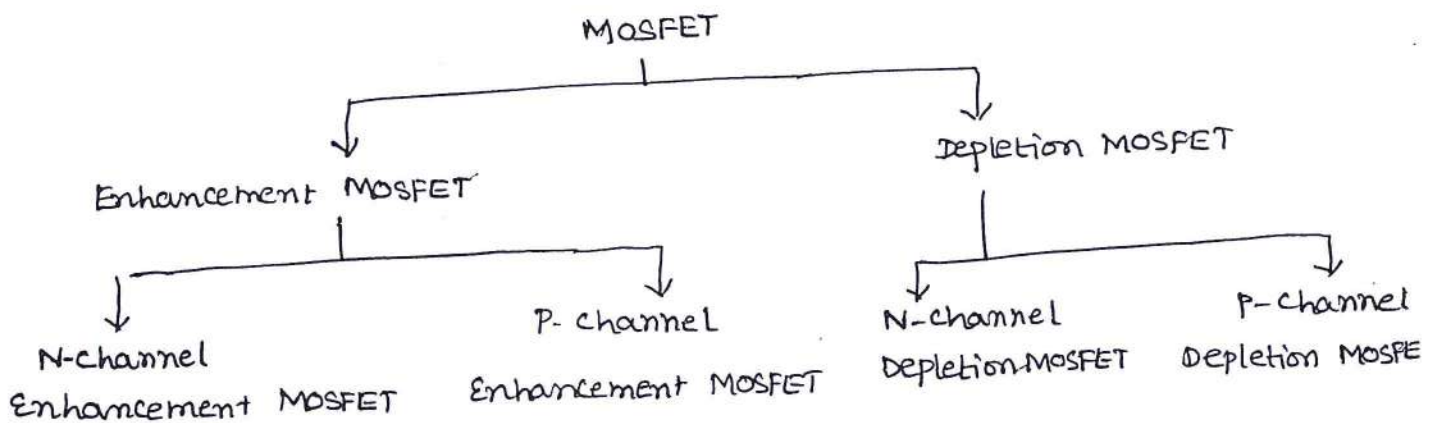
i) Enhancement MOSFET

ii) Depletion MOSFET.

→ The Enhancement MOSFET is again classified into two types.

They are N-channel Enhancement MOSFET and P-channel Enhancement MOSFET.

→ Similarly depletion MOSFET is classified into two types. They are N-channel depletion MOSFET and P-channel depletion MOSFET.



N-channel Enhancement MOSFET:

Construction of N-channel Enhancement MOSFET:

* Two highly doped N regions are diffused in a lightly doped P-type silicon substrate. one of these regions is called as source and the other one is called drain. They are separated by 10^{-3} inch.

* A thin layer of SiO_2 is grown over the surface of the p-substrate i.e. on the surface of the p-substrate between two n-regions.

* A thin layer of aluminium is formed over the layer of SiO_2 .

that forms the Gate terminal 'G'.

* The metal contacts are made with source region and drain region to extract the source and drain terminals.

* The metal area of gate in conjunction with the SiO_2 layer and the semiconductor channel forms a parallel plate capacitor. Here SiO_2 layer acts as a dielectric material, because SiO_2 is an insulating material. Because of this insulating layer of SiO_2 , MOSFET is also called as Insulated Gate Field Effect Transistor.

The symbol and structure of an N-channel enhancement MOSFET is as shown in below figure.

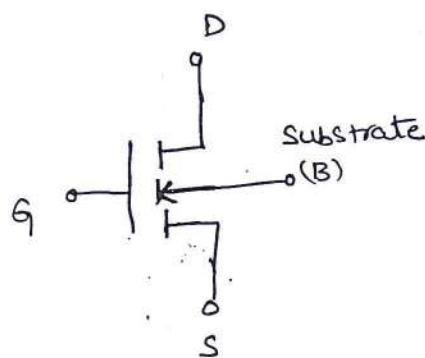
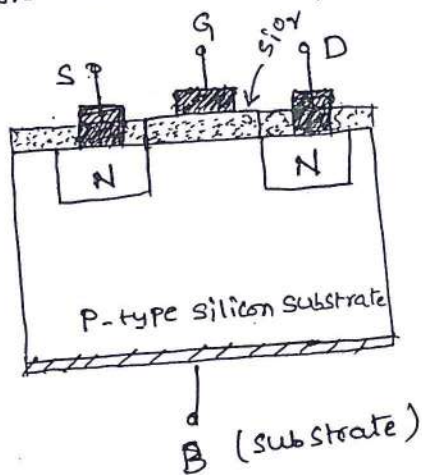


fig. 1 symbol of N channel enhancement MOSFET.

* In enhancement MOSFET the channel is not diffused, but it is induced when positive gate voltage is applied (for N-channel enhancement MOSFET).

operation of an N-channel Enhancement MOSFET :

* Generally the substrate terminal is grounded for a MOSFET.

* If the gate is applied with positive voltage V_{GS} , then the negative charge carriers within the P-type substrate (i.e. minority charge carriers) attract to the positive gate and accumulate between the source and drain regions. These negative charge carriers which are minority carriers in P-type substrate form an inversion layer. This induces a channel between the source and drain regions.

As the positive voltage on gate increases, the induced negative charge increases. Hence the conductivity increases and current flows from drain to source through the induced channel. Hence the drain current is enhanced by the positive gate voltage.

The minimum gate voltage V_{GS} that is required to form the inversion layer is known as the "threshold voltage" (V_t).

The operation of the Enhancement MOSFET is better understood from the following conditions.

i) when $V_{GS} < V_t$ and $V_{DS} = 0$:

When gate to source voltage V_{GS} is less than the threshold voltage V_t then there is no inversion layer is formed. Hence no channel is present between drain and source to cause the drain current. So the drain current $I_D \approx 0$ in this case. This mode of operation is called cut-off region.

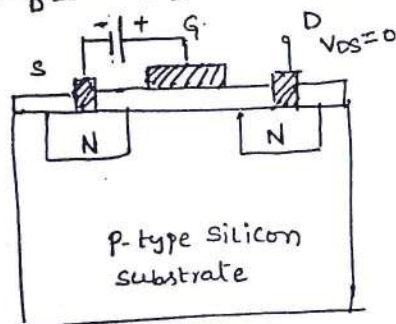


fig:- when $V_{GS} < V_t$ and $V_{DS} = 0$, no channel is induced so $I_D = 0$

ii) when $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$

When the gate to source voltage is greater than the threshold voltage, hence a channel gets induced between the drain and source. During this if V_{DS} is such that $V_{DS} < V_{GS} - V_t$ the charge carriers from source region move towards the drain region through the channel and establish drain current I_D that flows from drain to source.

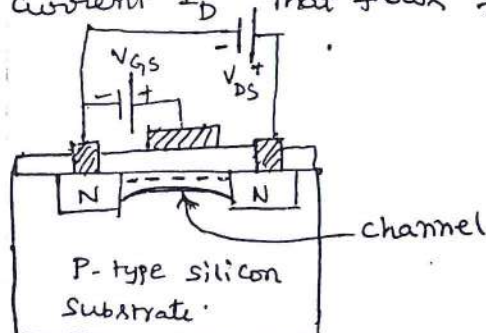


fig:- when $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$, channel is induced, so the drain current is flown.

This mode of operation is known as ohmic region (or) active region (or) non saturated region.

iii) when $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$:

when $V_{GS} > V_t$, a channel is induced between drain and source. Now if V_{DS} is such that $V_{DS} \geq V_{GS} - V_t$, the channel gets depleted. The channel is depleted more at drain than that of source. At a particular point $V_{DS} = V_{GS} - V_t$, the channel becomes pinched off due to which the drain current becomes saturated i.e. I_D becomes constant. This mode of operation is known as saturation region.

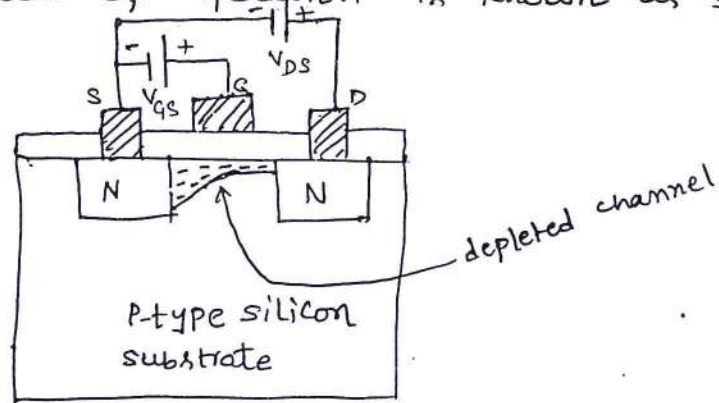


fig:- when $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$ the channel gets pinched-off, hence I_D becomes constant.

The drain characteristics of an n-channel enhancement MOSFET is as shown in below figure.

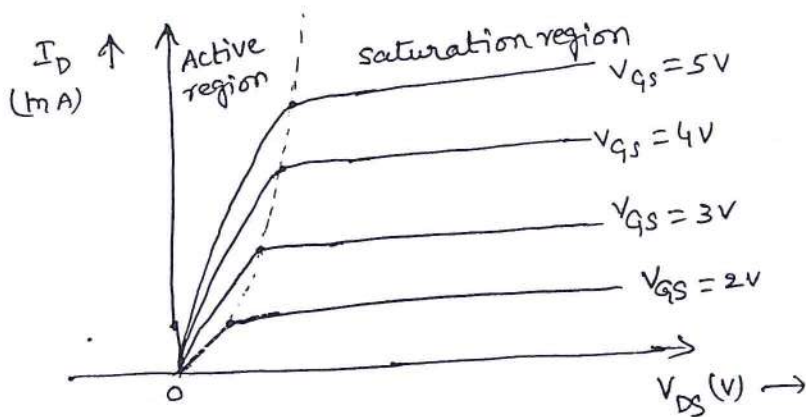


fig: drain characteristics of N-channel enhancement MOSFET.

The transfer characteristics of n-channel enhancement MOSFET is as shown in below. In this case the relationship between I_D and V_{GS} is given as $I_D = K(V_{GS} - V_t)^2$ which is known as square law relation. Here K is a constant

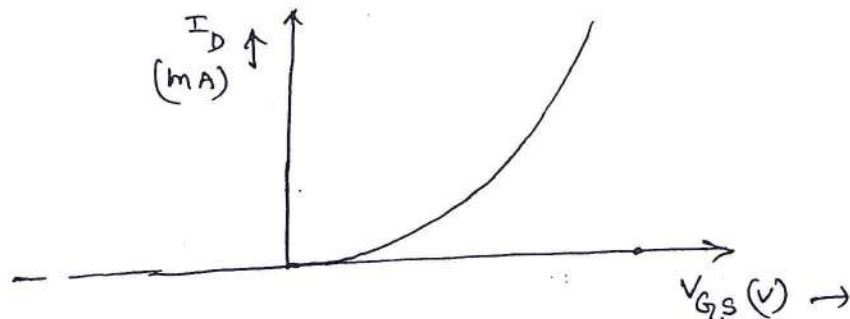


fig :- Transfer characteristics of n-channel enhancement MOSFET

P-channel Enhancement MOSFET:

Construction: * Two highly doped P-regions are diffused in a lightly doped n-type silicon substrate. One of these regions is called as source and the other one is called drain. They are separated by 10^{-3} inch.

* A thin layer of SiO_2 is grown over the surface of the P-substrate and holes are cut into SiO_2 layer allowing contacts with source and drain using aluminium metal contact.

* A thin metal layer is deposited over the layer of SiO_2 , between the two P-regions above the surface, to form the gate terminal.

* The metal area of gate in conjunction with the SiO_2 layer and the semiconductor channel forms a parallel plate capacitor. Here SiO_2 layer acts as a dielectric material, because SiO_2 is an insulating material. Because of this layer of SiO_2 , MOSFET is also called as insulated Gate Field Effect transistor.

The structure and symbol of a p-channel enhancement MOSFET is as shown in below figure.

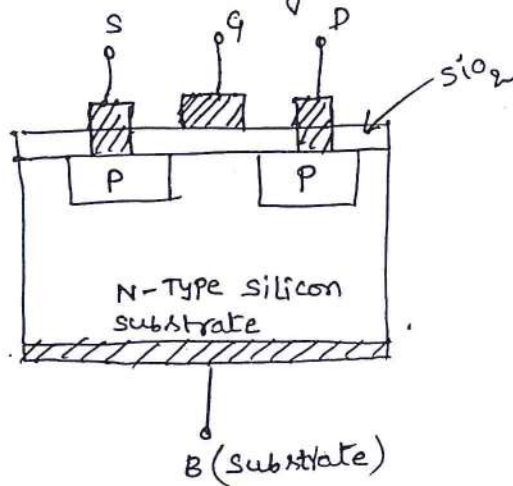


fig: Structure of p-channel enhancement MOSFET.

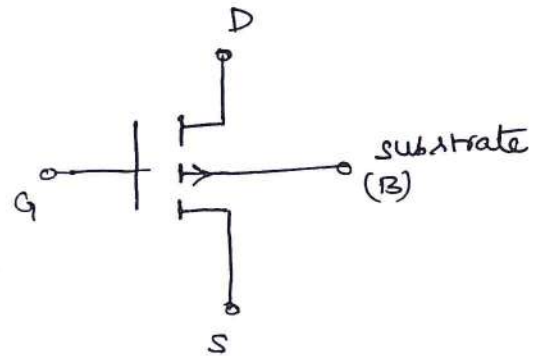


fig: Symbol of p-channel enhancement MOSFET

* For p-channel enhancement MOSFET the channel gets induced when negative gate voltage (V_{GS}) is applied.

operation of p-channel enhancement MOSFET :

- * The substrate terminal is generally grounded in a MOSFET.
- * If the gate is applied with negative voltage V_{GS} , then the positive charge carriers in N-type substrate (i.e. minority charge carriers) attract to the negative gate and accumulate between the source and drain regions. These positive carriers form an inversion layer. This induces a channel between the source and drain regions.
- * As negative gate voltage on gate increases, the induced positive charge carriers also increases. Hence the conductivity increases and the current flows from source to drain through the induced channel. Hence the drain current I_D is enhanced by negative gate voltage (V_{GS})

The minimum gate voltage V_{GS} , that is required to form the

inversion layer is known as the "threshold voltage" V_t .

The operation of the P-channel enhancement MOSFET under different conditions is explained below.

i) When $V_{GS} < V_t$ and $V_{DS} = 0$.

When $V_{GS} < V_t$, there is no inversion layer is formed. Hence no channel is present to cause the drain current. So $I_D \approx 0$. This mode of operation is called cut off region.

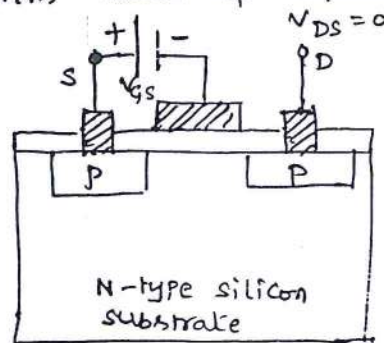


fig:- When $V_{GS} < V_t$ and $V_{DS} = 0$ no channel is induced, so $I_D = 0$.

ii) When $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$.

When $V_{GS} > V_t$, a channel gets induced between source and drain. During this, if V_{DS} is such that $V_{DS} < V_{GS} - V_t$, the charge carriers from source to drain are moved and causing drain current ' I_D ' from source to drain.

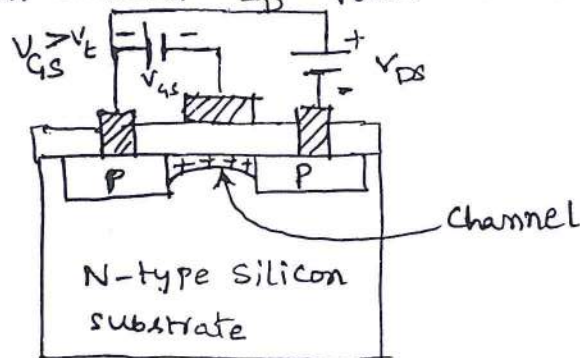


fig:- When $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$, channel is induced, so the drain current is constituted.

This mode of operation is known as ohmic region (or) active-region (or) non saturated region.

(31)

iii) when $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$:

When $V_{GS} > V_t$ and $V_{DS} \geq V_t$ a channel that has been induced due to $V_{GS} > V_t$, gets depleted. The channel is depleted more at drain than that of source. At $V_{DS} = V_{GS} - V_t$ the channel becomes pinched off due to which the drain current becomes constant. i.e. I_D is saturated. This mode of operation is known as saturation region.

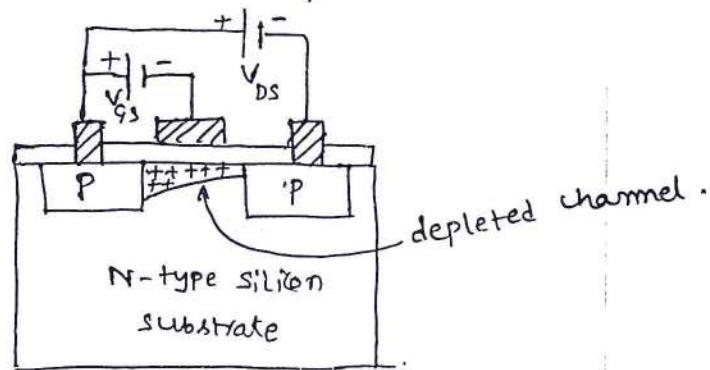


fig:- when $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$ the channel gets pinched off, hence I_D becomes constant.

* The drain characteristics of a P-channel enhancement MOSFET is as shown in below figure.

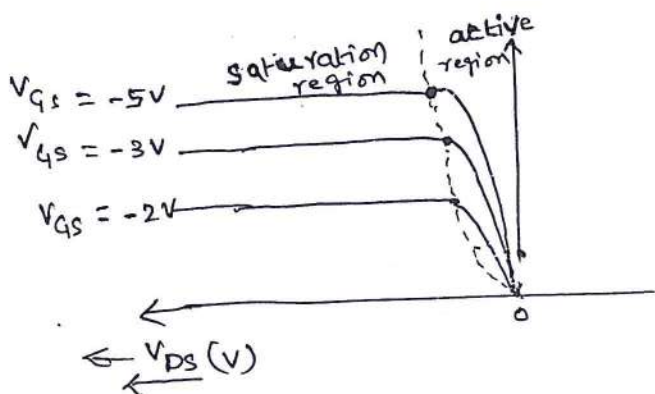


fig:- Drain characteristics of a P-channel enhancement MOSFET.

* The transfer characteristics of a P-channel enhancement MOSFET is as shown in below figure. The relationship between V_{GS} and I_D is given by $I_D = K(V_{GS} - V_t)^2$. where K is a constant.

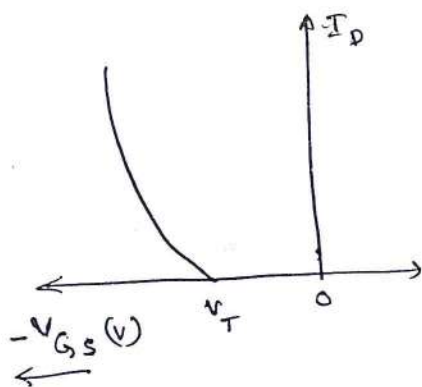


Fig. Transfer Characteristics of a P-channel enhancement MOSFET.

Depletion MOSFETs:

N-channel depletion MOSFET:

Construction:

- * Two highly doped N regions are diffused into a lightly doped P-type silicon substrate. one of these regions is called as source and the other one is called drain.
- * A channel is diffused between the source and drain regions.
- * A thin layer of SiO_2 is deposited over the surface of the P-type substrate and holes are cut into SiO_2 layer allowing contacts with source and drain using aluminium metal contact.
- * A thin metal layer is deposited over the layer of SiO_2 between the two N-regions to form gate terminal.
- * The metal area of gate in conjunction with the SiO_2 layer and the semiconductor channel forms a parallel plate capacitor.

operation of N-channel depletion mode MOSFET:

* When $V_{GS} = 0$ and the drain with respect to source is positive then the (majority carriers) electrons flow through the N-channel from source 's' to drain 'd'. Therefore the current I_D flows through the channel from drain to source.

* Now if V_{GS} is increased i.e. $V_{GS} > 0$, the channel

width is increased due to which the drain current I_D increases.

* If V_{GS} is decreased from '0', i.e. $V_{GS} < 0$, the diffused channel between drain and source will get depleted, as the majority charge carriers of P-substrate are attracted towards the negative gate terminal since $V_{GS} < 0$.

* Hence, in the ^{N-channel} depletion mode MOSFET, the channel is enhanced when $V_{GS} > 0$ and the channel is depleted when $V_{GS} < 0$. Hence it can also be called as "dual mode MOSFET".

The structure and symbol of N-channel depletion MOSFET is as shown in below.

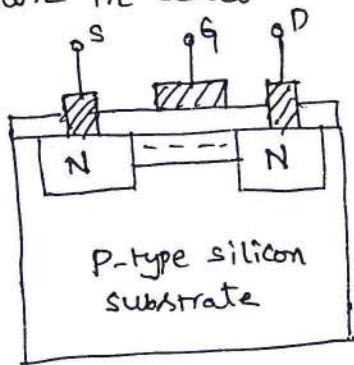


fig: N-channel depletion MOSFET structure

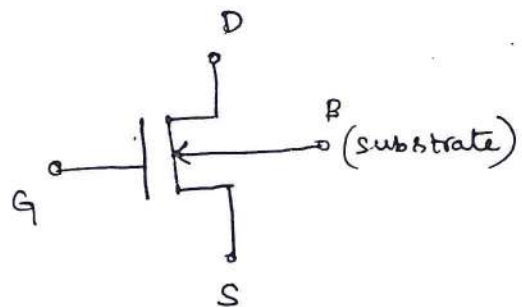


fig: symbol of N-channel depletion MOSFET.

The drain and transfer characteristics are as shown in below figure.

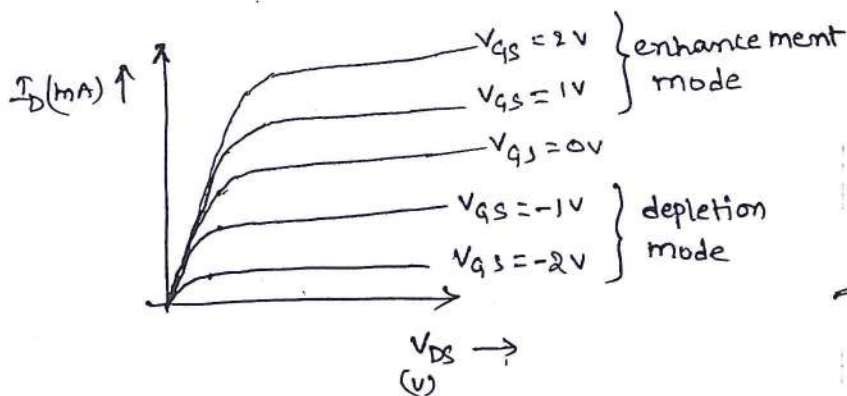


fig: drain characteristics

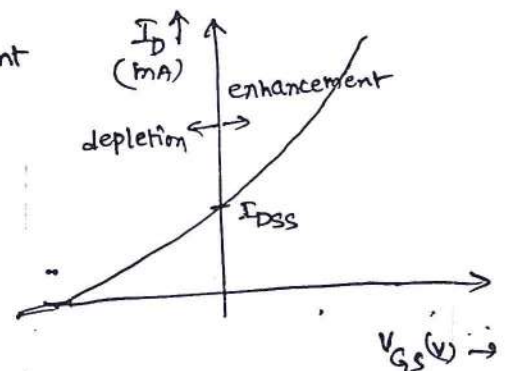


fig: transfer characteristics

The relationship between drain current I_D and V_{GS} for transfer characteristics is given by the equation $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$.

P-channel Depletion MOSFET:

Construction:

- * Two highly doped P-regions are diffused into a lightly doped n-type silicon substrate. one of these regions is called as source and the other one is called drain.
- * A channel is diffused between the source and drain regions.
- * A thin layer of SiO_2 is deposited over the surface of the n-type substrate and holes are cut into SiO_2 layer allowing contacts with source and drain, using aluminium metal contacts.
- * A thin layer of metal is deposited over the SiO_2 layer between the two p-regions to form gate terminal.
- * The metal area of gate in conjunction with the SiO_2 layer and the semiconductor channel forms a parallel plate capacitor.

The construction and symbol of the P-channel depletion MOSFET is as shown in below figure.

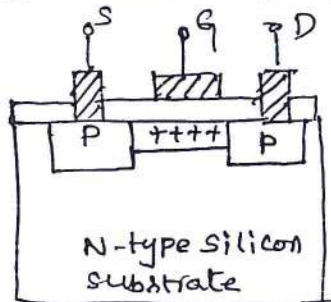


fig:- P-channel depletion-MOSFET structure.

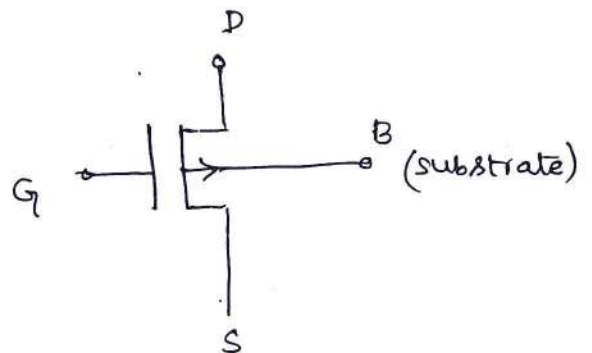


fig:- symbol for P-channel depletion MOSFET.

operation of a p-channel depletion Mode MOSFET:

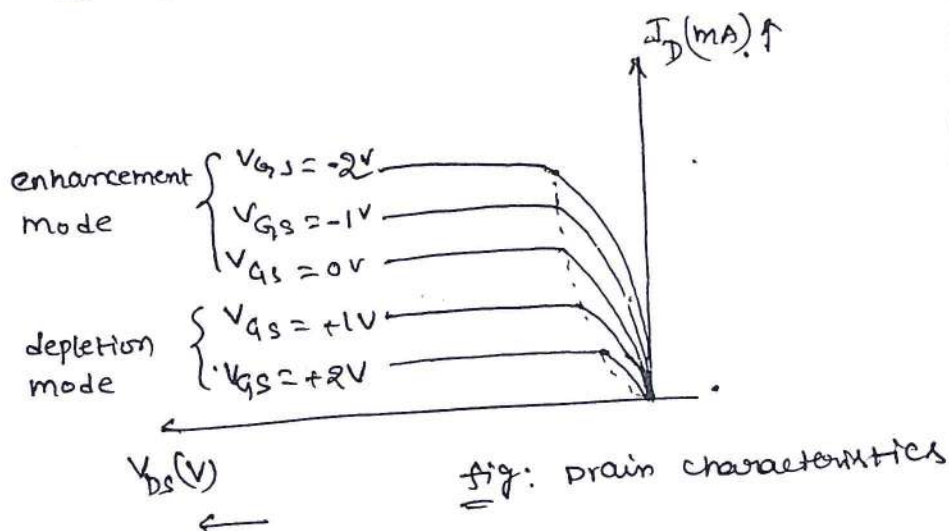
- * when $V_{GS} = 0$ and the drain with respect to source is negative then the holes (majority carriers) flow through the P-channel from source 'S' to drain 'D'. Therefore the current I_D flows from source to drain.
- * Now if V_{GS} is less than zero, the channel width

is increased due to which the drain current I_D increases. (33)

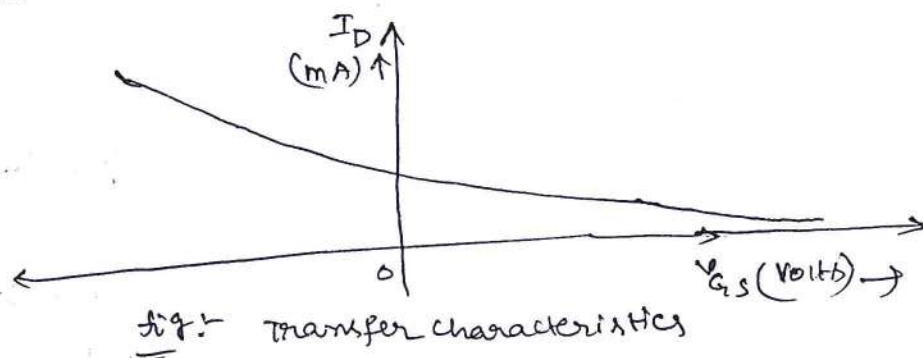
* If V_{GS} is greater than zero, the majority carriers of n-type substrate (i.e. electrons) are attracted towards the positive gate, into the channel hence the channel between the drain and source gets depleted.

* Hence, in the P-channel depletion mode MOSFET the channel is enhanced if $V_{GS} < 0$ and gets depleted if $V_{GS} > 0$. Therefore a depletion MOSFET of p-channel can also be called as "dual mode MOSFET",

The drain characteristics of P-channel depletion MOSFET is as shown below.

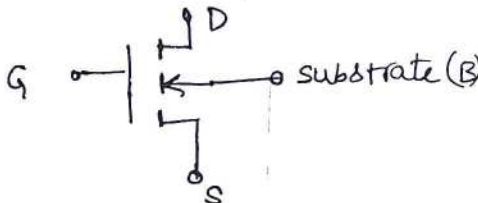
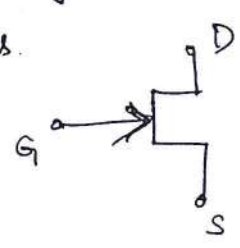


The transfer characteristics of P-channel depletion MOSFET is as shown in below



The relationship between drain current I_D and V_{GS} for transfer characteristics is given by the equation $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$

Comparison of MOSFET with JFET:

MOSFET	JFET
1> MOSFETs are easy to fabricate 2> The depletion MOSFETs are operated in both enhancement mode as well as depletion mode 3> Input impedance is high ($> 10,000 \text{ M}\Omega$) 4> Gate is insulated from channel by a layer of SiO_2 5> channel exists permanently in depletion MOSFET, but not in enhancement MOSFET 6> The symbol for enhancement n-channel MOSFET is 	1> Compare to MOSFET JFET is difficult to fabricate. 2> JFETs are operated in only depletion mode. 3> Input impedance is very high ($> 10 \text{ M}\Omega$) 4> Gate is not insulated from the channel. 5> channel exists permanently 6> The symbol for n-channel JFET is 

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UNIT IV

Junction Field Effect Transistor (FET)

Field Effect Transistor (FET) :

→ The FET is a unipolar device, as the current conduction is only due to majority charge carriers.

→ FET is a voltage controlled device.

→ Like BJT, FET is also a 3 terminal device.

→ Based on the construction, the FET can be classified into

two types. They are

1. Junction Field Effect Transistor (JFET)

2. Metal oxide semiconductor Field Effect Transistor (MOSFET)

→ The MOSFET some times called as Insulated Gate Field-Effect Transistor (IGFET) or Metal oxide silicon Transistor (MOST).

→ Depending on the majority charge carriers JFET has been

classified into two types. They are

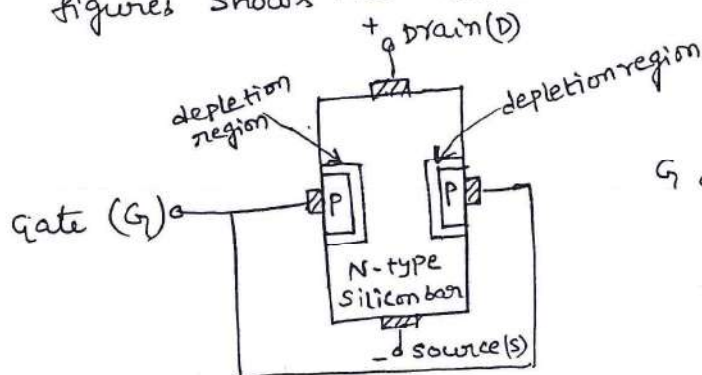
(20)

- 1) N-channel JFET with electrons as majority carriers.
- 2) P-channel JFET with holes as majority carriers.

N-channel JFET:

Construction of N-channel JFET:

- * It consists of an N-type silicon bar to which the ohmic contacts are made at the two ends of the bar to take the terminals out, called source and drain.
- * On either sides of the N-type silicon bar, heavily doped P-type silicon is diffused, by which PN junctions are formed. These layers are joined together and called as gate (G).
- * The source is a terminal which is connected to the negative pole of the battery. The electrons which are the majority charge carriers in N-type bar enter the bar through this terminal.
- * The drain is a terminal which is connected to the positive pole of the battery. The majority charge carriers leave the bar through this terminal.
- * The region of N-type silicon bar between the depletion regions of the two PN junctions is called as the channel. The below figures show the structure of n-channel JFET and its symbol.



fig(a) Structure of an N-channel JFET

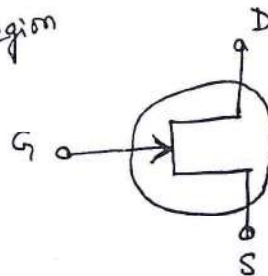


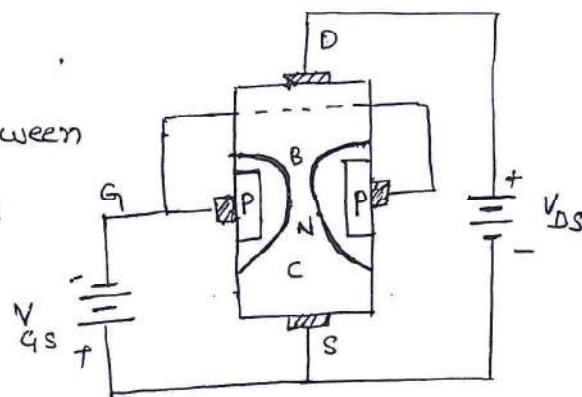
fig: symbol of an N-channel JFET.

** Operation of N-channel JFET (2) (Drain Characteristics of N-channel JFET)

1) When $V_{GS} = 0$ and $V_{DS} = 0$:

When no voltage is applied between drain and source and gate and source (i.e. when $V_{GS} = 0$, $V_{DS} = 0$),

the thickness of the depletion regions round the PN junctions is uniform, as shown in figure (a)



fig(b) JFET of N-channel under applied bias.

2) When $V_{DS} = 0$ and V_{GS} is decreased from zero (i.e. when $V_{DS} = 0$ or V_{GS} is negative) :

In this case, the PN junctions are reverse biased and hence the thickness of the depletion regions increases. As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased and hence the depletion regions become more thick, at a particular voltage of V_{GS} the depletion regions may contact with each other. In this condition, the channel is said to be in cutoff condition. The value of V_{GS} at which the cutoff condition is observed in the channel is called as cutoff voltage V_C .

3) When $V_{GS} = 0$ and V_{DS} is increased from zero : In this case the drain is positive with respect to source with $V_{GS} = 0$.

Now the majority carriers (electrons) flow through the N-channel from source to drain. Therefore the conventional current flows through the channel from drain to source. The magnitude of the drain current depends on the following factors.

- * The number of majority charge carriers available in the channel. i.e. the conductivity of the channel
- * The length 'L' of the channel.

- * The cross sectional area of the channel (denoted by A)
- * The magnitude of the applied voltage V_{DS} .

Hence there exists some resistance in the channel known as channel resistance denoted by R , given by

$$R = \frac{PL}{A}$$

$$I_D = \frac{V_{DS}}{R} = \frac{V_{DS}}{\left(\frac{PL}{A}\right)} = \frac{AV_{DS}}{PL}$$

* where ' P ' is the resistivity of the channel. Due to the existence of this channel resistance, there exists some voltage drop along the channel from drain to source. This voltage drop in the channel reverse biases the PN junctions and hence the thickness of the depletion regions also increases.

* As V_{DS} is increased the cross sectional area of the channel will be reduced. At a certain value of V_{DS} the cross sectional area at 'B' becomes minimum. At this voltage the channel is said to be pinched off and the respective value of V_{DS} is known as pinch off voltage denoted by ' V_P '. Any further increase in V_{DS} does not increase the drain current I_D .

* Hence pinch off voltage can also be defined as the voltage of V_{DS} at which the current I_D reaches to its constant saturation level.

* If V_{DS} is increased beyond pinch off voltage, at a certain voltage drain current suddenly increases that may cause break down in the JFET. The voltage of V_{DS} at which the break down occurs is known as break down voltage of JFET denoted by BV_{DS0} .

* The region from $V_{DS}=0$ to $V_{DS}=V_P$ is called ohmic region where the JFET can be used as a voltage variable resistor. The region from $V_{DS}=V_P$ to $V_{DS}=BV_{DS0}$ is called Pinch off region (or) saturation region.

4) when V_{GS} is negative and V_{DS} is increased :

when a negative value of voltage is applied to V_{GS} the PN junctions become more reverse biased. Hence for a negative value of V_{GS} the curve of I_D versus V_{DS} is similar to that of $V_{GS} = 0$, but the pinch off voltage V_p and breakdown voltage BV_{DGO} for this case are lower than + case of $V_{GS} = 0$.

The experimental setup to determine the JFET characteristics is as shown in below figure.

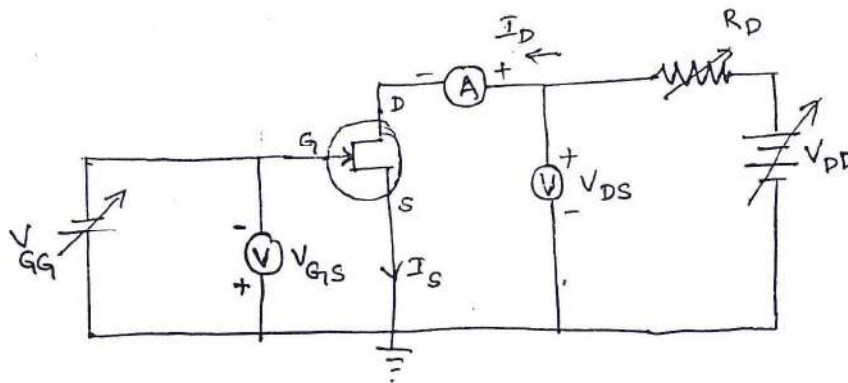


fig:- circuit to determine the characteristics of JFET of n-channel

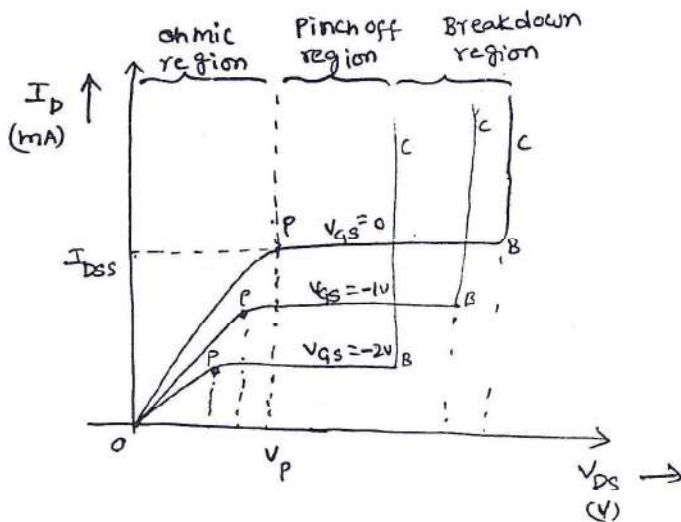


fig:- Drain characteristics of an N-channel JFET.

NOTE: From the drain characteristics of n-channel JFET it is clear that drain current I_D for different curves at a particular value of V_{DS} , is varied by varying the value of V_{GS} . Hence a JFET can be said to be a voltage controlled device.

Transfer Characteristics of an n-channel JFET:

For transfer characteristics V_{DS} is maintained constant at a suitable value greater than pinch off voltage ' V_P '. The Gate to Source voltage V_{GS} is decreased from zero till drain current I_D is reduced to zero. The shape of the transfer characteristics is very nearly a parabola as shown below which is drawn between V_{GS} and I_D . This relationship between V_{GS} and I_D is defined by Shockley's equation.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

where I_D = Drain saturation current

and I_{DSS} = value of I_D when $V_{GS} = 0$.

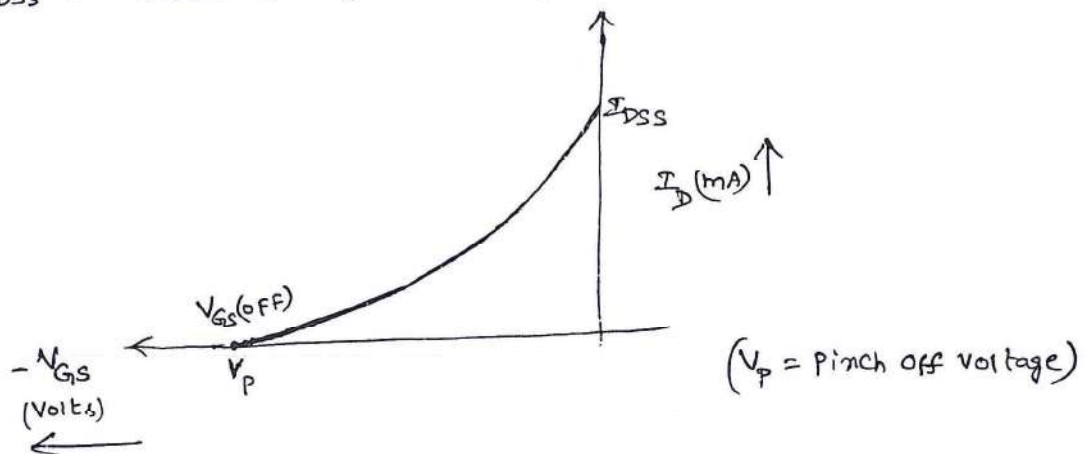


Fig. 1- Transfer characteristics of JFET.

The drain current $I_D = 0$, when $V_{GS} = V_{GS(OFF)}$, where $V_{GS(OFF)} = V_P$.

characteristic parameters of the JFET :

1) Mutual Conductance (or) Trans Conductance (g_m) :

* It is defined as the ratio of a small change in the drain current to the corresponding small change in the gate to source voltage at a constant drain to source voltage.

$$\text{Trans conductance } g_m = \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS} = \text{constant}} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} \text{ const}$$

* The units for transconductance is mhos.

2) Drain Resistance : (r_d)

* It is defined as the ratio of a small change in the drain to source voltage (V_{DS}) to the corresponding small change in the drain current, at a constant gate to source voltage (V_{GS}).

$$\text{Drain resistance } (r_d) = \left(\frac{\partial V_{DS}}{\partial I_D} \right)_{V_{GS} = \text{constant}} = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} \text{ const}$$

* The units for drain resistance is ohms

* The drain resistance at $V_{GS} = 0$ is called as drain source ON resistance.

3) Amplification factor (μ) :

It is defined as the ratio of a small change in the drain to source voltage ^{to the} corresponding small change in the gate to source voltage at a constant drain current.

$$\text{Amplification factor } (\mu) = - \left(\frac{\partial V_{DS}}{\partial V_{GS}} \right)_{I_D \text{ constant}} = - \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at } I_D \text{ constant}$$

Here - sign indicates that V_{DS} decreases when V_{GS} is increased.

4) Relationship among FET parameters (g_m , r_d and μ):

The amplification factor ' μ ' is equal to the product of the transconductance (g_m) and drain resistance (r_d).

$$\mu = g_m \cdot r_d$$

5) Power dissipation (P_D):

The power dissipation in FET is denoted by ' P_D ' and is equal to the product of V_{DS} and I_D .

$$P_D = V_{DS} \cdot I_D$$

Q) Derive the relationship among g_m , r_d and μ

Ans) If there is a small change in V_{DS} from V_{DS} to $V_{DS} + \Delta V_{DS}$ and a small change in V_{GS} from V_{GS} to $V_{GS} + \Delta V_{GS}$, then the corresponding change in I_D may be obtained by applying the Taylor's theorem with neglecting higher order terms. Thus the small change in drain current ΔI_D is

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS} \text{ constant}} \cdot \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS} \text{ constant}} \Delta V_{GS}$$

dividing both sides by ΔV_{GS} we get

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \cdot \frac{\Delta V_{DS}}{\Delta V_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}} \frac{\Delta V_{GS}}{\Delta V_{GS}}$$

If I_D is constant then $\frac{\Delta I_D}{\Delta V_{GS}} = 0$

$$\Rightarrow 0 = \left(\frac{\partial I_D}{\partial V_{DS}} \right)_{V_{GS}} \cdot \frac{\Delta V_{DS}}{\Delta V_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}} \right)_{V_{DS}}$$

$$\Rightarrow 0 = \frac{1}{r_d} \cdot (-\mu) + g_m$$

$$\Rightarrow \frac{\mu}{r_d} = g_m$$

$$\therefore \boxed{\mu = g_m r_d}$$

problems:

- ① when a reverse gate voltage of 12V is applied to JFET, the gate current is 1mA. determine the resistance between gate and source.

sol

$$V_{G_s} = 12V, I_G = 10^{-9} A.$$

$$\text{Gate to source resistance} = \frac{V_{G_s}}{I_G} = \frac{12}{10^{-9}} = 12000 M\Omega$$

- ② when the reverse gate voltage of JFET changes from 4 to 3V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

sol

$$\Delta V_{G_s} = \text{the change in gate voltage} = 4 - 3.9 = 0.1V.$$

$$\Delta I_D = \text{the change in drain current} = 1.6 \text{ mA} - 1.3 \text{ mA} = 0.3 \text{ mA}.$$

$$\text{Transconductance } g_m = \frac{\Delta I_D}{\Delta V_{G_s}} = \frac{0.3 \times 10^{-3}}{0.1} = 3 \text{ mS}$$

- ③ A FET has a drain current of 4 mA. If $I_{DSS} = 8 \text{ mA}$ and $V_{G_s(\text{off})} = -6V$, find the values of V_{G_s} and V_p .

sol

$$\text{We know that } I_D = I_{DSS} \left[1 - \frac{V_{G_s}}{V_p} \right]^2 = I_{DSS} \left[1 - \frac{V_{G_s}}{V_{G_s(\text{off})}} \right]^2$$

$$\Rightarrow 4 \times 10^{-3} = 8 \times 10^{-3} \left[1 - \frac{V_{G_s}}{(-6)} \right]^2$$

$$\Rightarrow \left(1 + \frac{V_{G_s}}{6} \right)^2 = \frac{1}{2} \Rightarrow V_{G_s} = -1.76V$$

$$V_p = V_{G_s(\text{off})} = -6V$$

P-channel JFET:Construction of P-channel JFET:

- * It consists of a P-type silicon bar to which the ohmic contacts are made at the two ends of the bar to take the terminals out called source and drain.
- * on both sides of the P-type silicon bar, heavily doped n-type silicon is diffused by which PN junctions are formed. These layers are joined together to form the gate (G) terminal.
- * The source is a terminal which is connected to the positive pole of the battery and the drain is connected to the negative pole of the battery.
- * source is the terminal through which the majority carriers in P-type bar enter into the bar and they leave the bar through drain terminal.
- * The region of P-type silicon bar between the depletion regions of two PN junctions is called the channel. The following figures show the structure and symbol of the P-channel JFET.

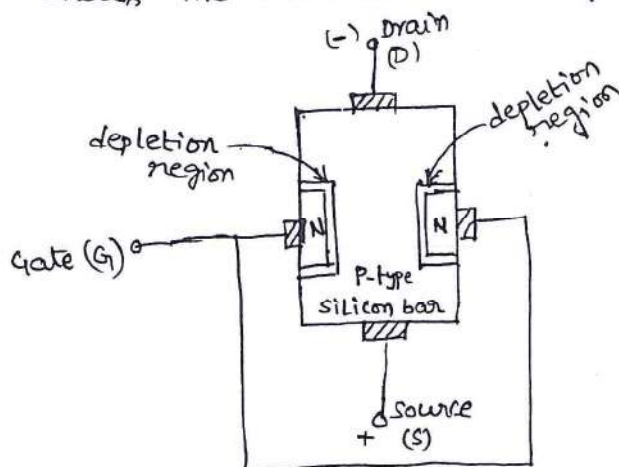


fig a) structure of a P-channel JFET

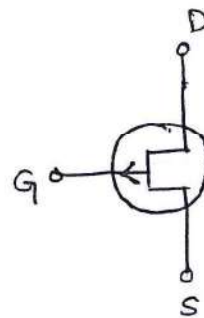


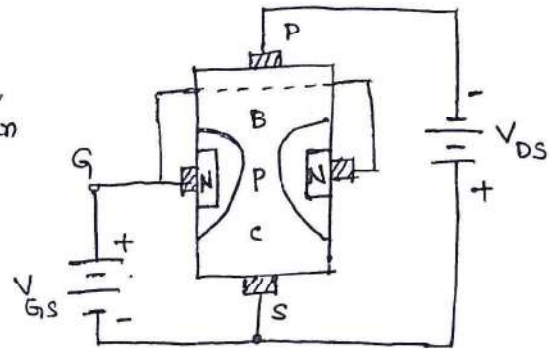
fig b) symbol of a P-channel JFET

operation of a P-channel JFET (or) Drain characteristics of a

P-channel JFET :

1> when $V_{GS}=0$ and $V_{DS}=0$:

When no voltage is applied between drain and source, gate and source (i.e. $V_{GS}=0$, $V_{DS}=0$), then the thickness of the depletion regions around the PN junctions is uniform as shown in fig(a).



fig(c): JFET of P-channel under applied bias.

2> when $V_{DS}=0$ and V_{GS} is increased from zero (i.e. $V_{GS}>0$) :

In this case both the PN junctions are reverse biased and hence the thickness of the depletion region increases. As V_{GS} is increased from zero, the reverse voltage across the PN junctions will increase and hence the depletion regions become more thick. At a particular voltage of V_{GS} the depletion regions may contact with each other. In this condition the channel is said to be in Cut-off Condition. The value of V_{GS} at which the Cut-off Condition is observed, is called as Cut-off voltage.

3> when $V_{GS}=0$ and V_{DS} is decreased from zero (i.e. $V_{DS}<0$)

When $V_{GS}=0$ and $V_{DS}<0$, the drain is negative with respect to source, due to which the majority carriers (holes) flow through the P-channel from source to drain that constitute the drain current I_D flows from source to drain. The magnitude of the drain current depends on the following factors.

- * The number of majority carriers available in the channel
- * The length of the channel i.e. 'L'.

* The cross section area of the channel (i.e. A)

* The magnitude of the applied voltage V_{DS} .

Hence there exists some resistance in the channel known as channel resistance denoted by ' R ' given by

$$R = \frac{\rho L}{A}$$

$$I_D = \frac{V_{DS}}{R} = \frac{V_{DS}}{\left(\frac{\rho L}{A}\right)} = \frac{AV_{DS}}{\rho L}$$

* where ρ is the resistivity of the channel. Due to the existence of channel resistance, there exists some voltage drop along the channel from source to drain which reverse biases the PN junctions and hence the thickness of the depletion regions is increased.

* As V_{DS} decreases the drain current I_D also increases and the cross sectional area of the channel gets reduced. At a certain value of V_{DS} the drain current I_D reaches to a constant value; and the cross sectional area becomes minimum. At this voltage the channel is said to be pinch off and the respective value of ' V_{DS} ' is called as pinch off voltage denoted by V_p . Any further decrease in V_{DS} does not increase the drain current I_D .

* If V_{DS} is decreased beyond pinch off voltage (V_p), at a certain voltage of V_{DS} , the drain current increases suddenly that may cause a breakdown in the JFET. The voltage at which the break down occurs is known as breakdown voltage of JFET, denoted by BV_{DGS} .

* The region from $V_{DS} = 0$ to $V_{DS} = V_p$ is called as the

ohmic region where the JFET can be used as a voltage variable resistor. The region from $V_{DS} = V_p$ to $V_{DS} = BV_{DGS}$ is saturation (or) Pinch off region.

4) When V_{GS} is increased from zero ($V_{GS} > 0$) and V_{DS} is decreased from zero ($V_{DS} < 0$) :

When a positive value of voltage is applied to V_{GS} , the PN junctions become more reverse biased. Hence for a positive value of V_{GS} , the curve of I_D versus V_{DS} is similar to that of $V_{GS} = 0$ but the Pinch off voltage V_p and breakdown voltage BV_{DS0} for this case are lower than the case of $V_{GS} = 0$.

The experimental setup to determine the JFET characteristics are as shown in below figure.

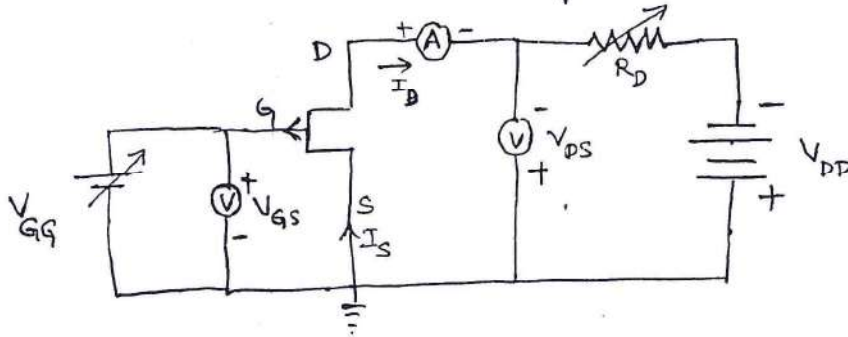


fig: circuit to determine the characteristics of P-channel JFET.

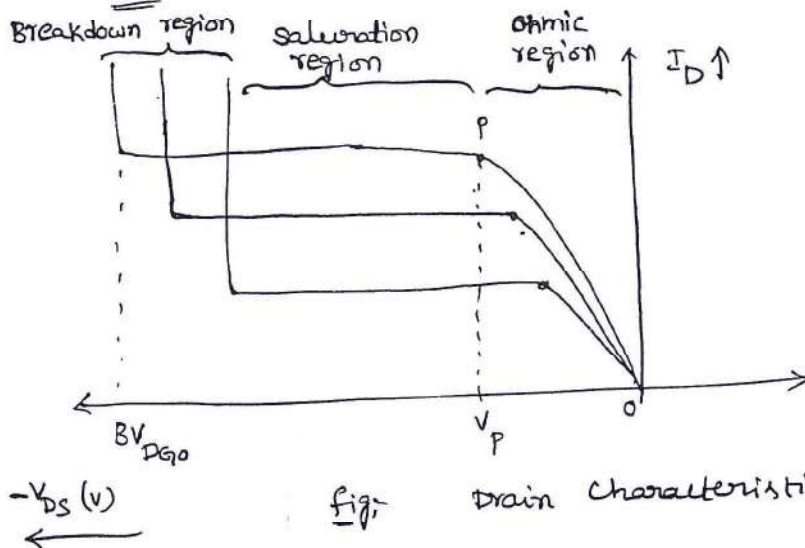


fig: Drain characteristics of P-channel JFET.

Transfer characteristics of a P-channel JFET:

For transfer Characteristics V_{DS} is maintained constant at a suitable value greater than pinch off voltage ' V_p ', the gate to source voltage V_{GS} is increased from zero till drain current I_D is reduced to zero. The shape of the transfer characteristics is very nearly a parabola as shown below which is drawn between V_{GS} and I_D .

This relationship between V_{GS} and I_D is defined by Shockley's equation

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

where I_D = drain current

I_{DSS} = value of I_D at $V_{GS} = 0$.

The drain current $I_D = 0$ when $V_{GS} = V_{GS\text{OFF}} = V_p$.

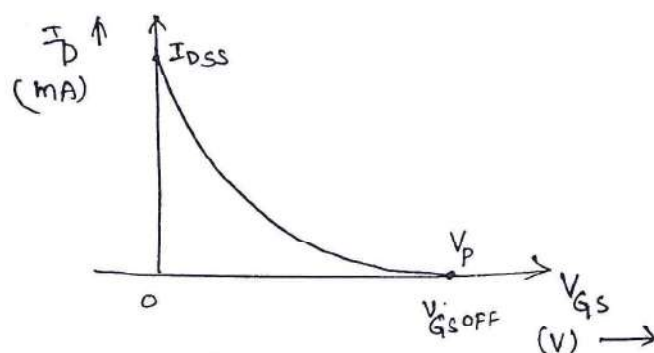


fig: Transfer characteristics of a P-channel JFET.

Relationship between g_m , V_{GS} , I_{DSS} and V_p :

We know that $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2 \rightarrow (1)$

Differentiating the above equation with respect to V_{GS}

we get

$$\frac{dI_D}{dV_{GS}} = I_{DSS} \cdot 2 \left(-\frac{1}{V_p} \right) \left[1 - \frac{V_{GS}}{V_p} \right]$$

$$\frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_p} \left[1 - \frac{V_{GS}}{V_p} \right] \rightarrow (2)$$

We know that $\frac{dI_D}{dV_{GS}} = \frac{\Delta I_D}{\Delta V_{GS}} = g_m$

$$\therefore g_m = -\frac{2I_{DSS}}{V_p} \left[1 - \frac{V_{GS}}{V_p} \right] \quad \text{--- (3)}$$

From equation (1) $1 - \frac{V_{GS}}{V_p} = \sqrt{\frac{I_D}{I_{DSS}}} \quad \text{--- (4)}$

$\therefore$ substituting equation (4) in equation (3)

we get
$$g_m = -\frac{2I_{DSS}}{V_p} \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = -\frac{2\sqrt{I_D I_{DSS}}}{V_p}$$

Let $g_m = g_{m_0}$ when $V_{GS} = 0$

$\therefore$ From equation (3) when $V_{GS} = 0$

$$g_{m_0} = -\frac{2I_{DSS}}{V_p} \quad \text{--- (5)}$$

substituting equation (5) in equation (3) we get

$$\boxed{g_m = g_{m_0} \left[1 - \frac{V_{GS}}{V_p} \right]}$$

Applications of JFET:

- 1) FETs are used in RF (radio frequency) amplifiers in communication equipment and in FM tuners.
- 2) FET can be used as a buffer in measuring instruments, receiver since it has high input impedance and low output impedance.
- 3) Since FET is a voltage controlled device it can be used as a voltage variable resistor in some applications.
- 4) FETs are used in mixer circuits in FM and TV receivers.

- 5) FETs are used in digital circuits such as Computers and memory circuits because of its small size.
- 6) FET can be used in oscillator circuits.

Comparison of JFET and BJT:

Bipolar Junction Transistor	Field Effect Transistor
1) BJT is a unipolar device	1) FET is Bipolar device.
2) The Current Conduction in BJT depends on both majority charge carriers and minority charge carriers	2) The Current Conduction in FET depends on majority charge carriers only.
3) BJT is a Current Controlled device	3) FET is a Voltage Controlled device.
4) It exhibits low input impedance because input circuit is forward biased. It has high output impedance	4) FET exhibits high input impedance and low output impedance.
5) BJTs are cheaper to produce	5) FETs are costlier when compared to BJT.
6) BJT occupies more space when compared to FET	6) FET occupies less space, hence they are preferred in manufacturing ICs
7) BJT has a positive temperature Coefficient	7) FET has a negative temperature Coefficient.
8) BJTs are not easy to fabricate	8) FET is easier to Fabricate than BJTs.

MOSFET (Metal oxide semiconductor Field effect Transistor)

A MOSFET can also be called as Insulated Gate Field Effect Transistor (IGFET) or Metal oxide silicon Transistor (MOST)

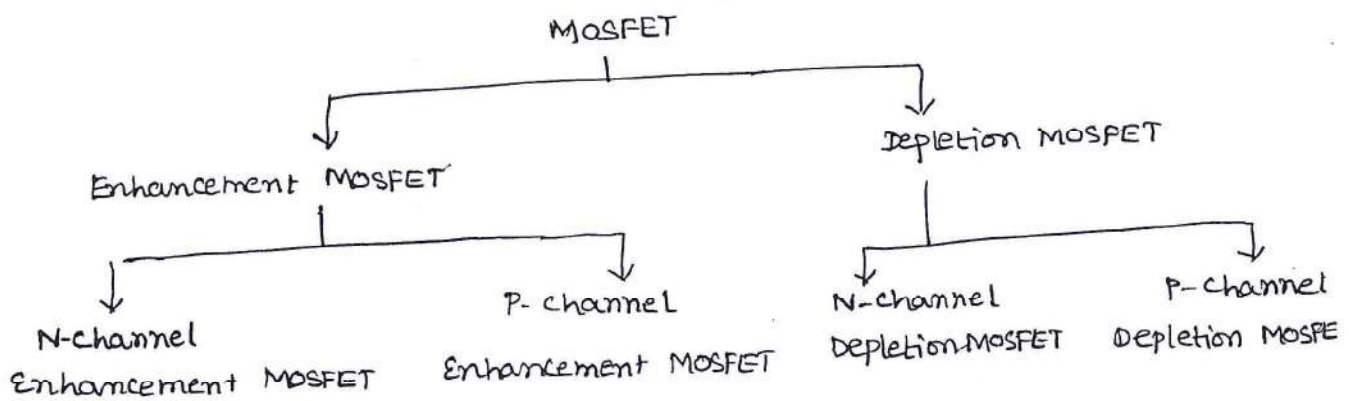
There are two basic forms of MOSFET. They are

i) Enhancement MOSFET

ii) Depletion MOSFET.

→ The Enhancement MOSFET is again classified into two types. They are N-channel Enhancement MOSFET and P-channel enhancement MOSFET.

→ Similarly depletion MOSFET is classified into two types. They are N-channel depletion MOSFET and P-channel depletion MOSFET.



N-channel Enhancement MOSFET:

Construction of N-channel Enhancement MOSFET:

* Two highly doped N regions are diffused in a lightly doped P-type silicon substrate. One of these regions is called as source and the other one is called drain. They are separated by 10^{-3} inch.

* A thin layer of SiO_2 is grown over the surface of the p-substrate i.e. on the surface of the p-substrate between two n-regions.

* A thin layer of aluminium is formed over the layer of SiO_2 .

that forms the Gate terminal 'G'.

* The metal contacts are made with source region and drain region to extract the source and drain terminals.

* The metal area of gate in conjunction with the SiO_2 layer and the semiconductor channel forms a parallel plate capacitor. Here SiO_2 layer acts as a dielectric material, because SiO_2 is an insulating material. Because of this insulating layer of SiO_2 , MOSFET is also called as Insulated Gate Field effect Transistor.

The symbol and structure of an N-channel enhancement MOSFET is as shown in below figure.

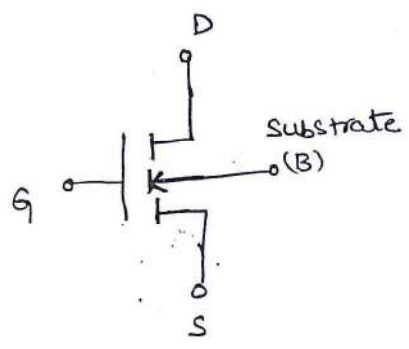
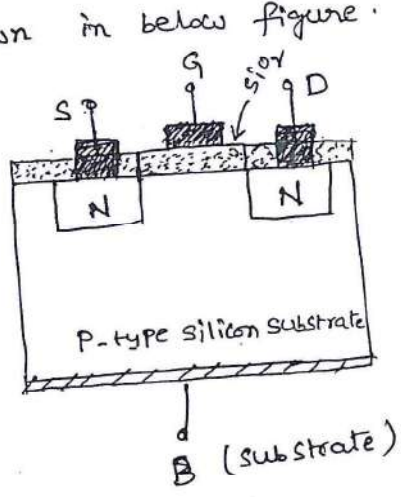


fig. 1 symbol of N channel enhancement MOSFET.

* In enhancement MOSFET the channel is not diffused, but it is induced when positive gate voltage is applied (for N-channel enhancement MOSFET).

operation of an N-channel Enhancement MOSFET :

* Generally the substrate terminal is grounded for a MOSFET.

* If the gate is applied with positive voltage V_{GS} , then the negative charge carriers within the P-type substrate (i.e. minority charge carriers) attract to the positive gate and accumulate between the source and drain regions. These negative charge carriers which are minority carriers in P-type substrate form an inversion layer. This induces a channel between the source and drain regions.

As the Positive voltage on gate increases, the induced negative charge increases. Hence the conductivity increases and current flows from drain to source through the induced channel. Hence the drain current is enhanced by the positive gate voltage.

The minimum gate voltage V_{GS} that is required to form the inversion layer is known as the "threshold voltage" (V_t).

The operation of the Enhancement MOSFET is better understood from the following conditions.

i) when $V_{GS} < V_t$ and $V_{DS} = 0$:

when gate to source voltage V_{GS} is less than the threshold voltage V_t then there is no inversion layer is formed. Hence no channel is present between drain and source to cause the drain current. So the drain current $I_D \approx 0$ in this case. This mode of operation is called cut-off region.

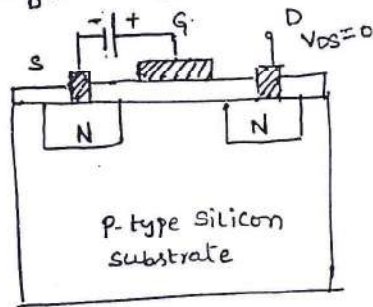


fig:- when $V_{GS} < V_t$ and $V_{DS} = 0$, no channel is induced so $I_D = 0$

ii) when $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$

when the gate to source voltage is greater than the threshold voltage, hence a channel gets induced between the drain and source. During this if V_{DS} is such that $V_{DS} < V_{GS} - V_t$ the charge carriers from source region move towards the drain region through the channel and establish drain current I_D that flows from drain to source.

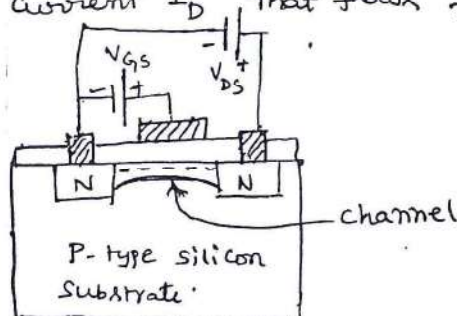


fig:- when $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$, channel is induced, so the drain current is flown.

This mode of operation is known as ohmic region (or) active region (or) non saturated region.

iii) when $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$:

when $V_{GS} > V_t$, a channel is induced between drain and source. Now if V_{DS} is such that $V_{DS} \geq V_{GS} - V_t$, the channel gets depleted. The channel is depleted more at drain than that of source. At a particular point $V_{DS} = V_{GS} - V_t$, the channel becomes pinched off due to which the drain current becomes saturated i.e. I_D becomes constant. This mode of operation is known as saturation region.

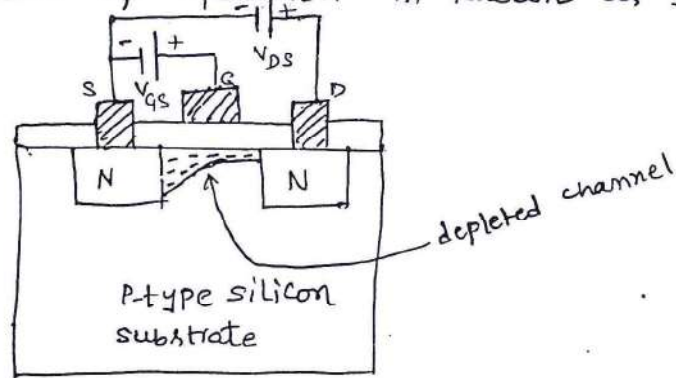


fig: when $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$ the channel gets pinched-off, hence I_D becomes constant.

The drain characteristics of an n-channel enhancement MOSFET is as shown in below figure.

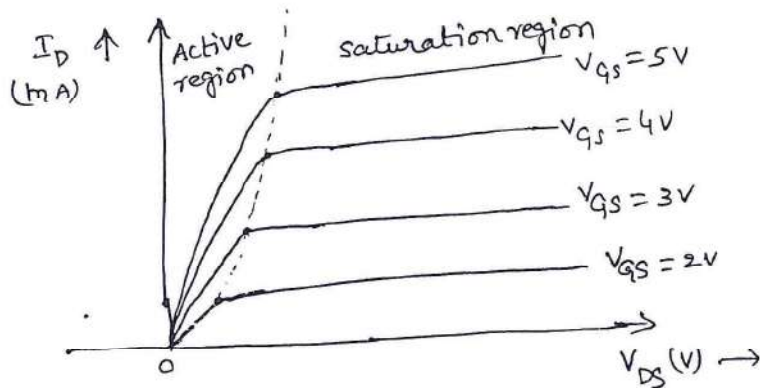


fig: drain characteristics of n-channel enhancement MOSFET.

The transfer characteristics of n-channel enhancement MOSFET is as shown in below. In this case the relationship between I_D and V_{GS} is given as $I_D = K(V_{GS} - V_t)^2$ which is known as square law relation. Here K is a constant

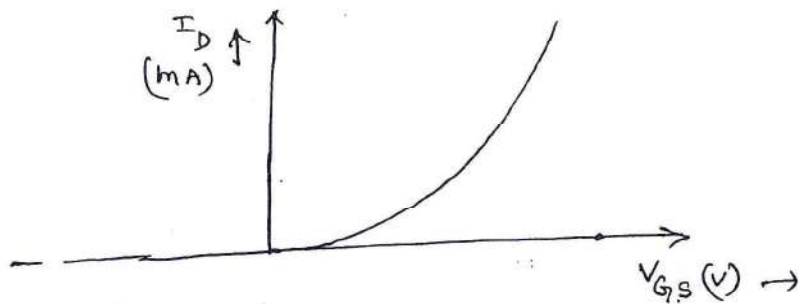


Fig :- Transfer characteristics of n-channel enhancement MOSFET

P-channel Enhancement MOSFET:

Construction: * Two highly doped p-regions are diffused in a lightly doped n-type silicon substrate. One of these regions is called as source and the other one is called drain. They are separated by 10^{-3} inch.

* A thin layer of SiO_2 is grown over the surface of the p-substrate and holes are cut into SiO_2 layer allowing contacts with source and drain using aluminium metal contact.

* A thin metal layer is deposited over the layer of SiO_2 , between the two p-regions above the surface, to form the gate terminal.

* The metal area of gate in conjunction with the SiO_2 layer and the semiconductor channel forms a parallel plate capacitor. Here SiO_2 layer acts as a dielectric material, because SiO_2 is an insulating material. Because of this layer of SiO_2 , MOSFET is also called as insulated Gate Field Effect transistor.

The structure and symbol of a P-channel enhancement MOSFET is as shown in below figure.

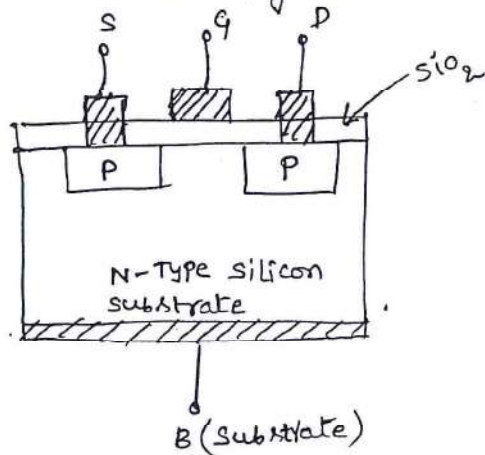


fig: structure of P-channel enhancement MOSFET.

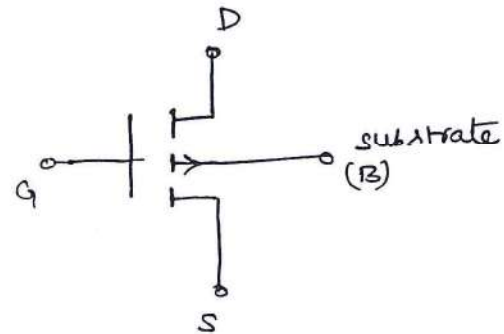


fig: symbol of P-channel enhancement MOSFET

* For P-channel enhancement MOSFET the channel gets induced when negative gate voltage (V_{GS}) is applied.

operation of P-channel enhancement MOSFET:

- * The substrate terminal is generally grounded in a MOSFET.
- * If the gate is applied with negative voltage V_{GS} , then the positive charge carriers in N-type substrate (i.e. minority charge carriers) attract to the negative gate and accumulate between the source and drain regions. These positive carriers form an inversion layer. This induces a channel between the source and drain regions.
- * As negative gate voltage on gate increases, the induced positive charge carriers also increases. Hence the conductivity increases and the current flows from source to drain through the induced channel. Hence the drain current I_D is enhanced by negative gate voltage (V_{GS}).

The minimum gate voltage V_{GS} , that is required to form the

inversion layer is known as the "threshold voltage" V_t .

The operation of the P-channel enhancement MOSFET under different conditions is explained below.

i) When $V_{GS} < V_t$ and $V_{DS} = 0$.

When $V_{GS} < V_t$, there is no inversion layer formed. Hence no channel is present to cause the drain current. So $I_D \approx 0$. This mode of operation is called cut off region.

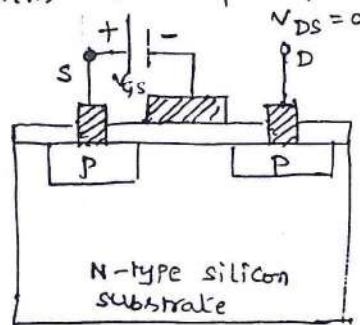


fig:- When $V_{GS} < V_t$ and $V_{DS} = 0$ no channel is induced, so $I_D = 0$.

ii) When $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$:

When $V_{GS} > V_t$, a channel gets induced between source and drain. During this, if V_{DS} is such that $V_{DS} < V_{GS} - V_t$, the charge carriers from source to drain are moved and causing drain current I_D from source to drain.

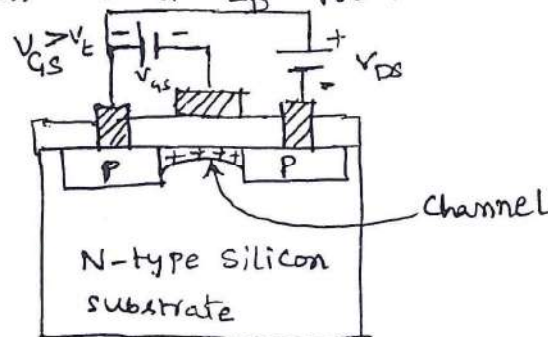


fig:- When $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$, channel is induced, so the drain current is constituted.

This mode of operation is known as ohmic region (or) active-region (or) non saturated region.

(31)

iii) when $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$:

When $V_{GS} > V_t$ and $V_{DS} \geq V_t$ a channel that has been induced due to $V_{GS} > V_t$, gets depleted. The channel is depleted more at drain than that of source. At $V_{DS} = V_{GS} - V_t$ the channel becomes pinched off due to which the drain current becomes constant. i.e. I_D is saturated. This mode of operation is known as saturation region.

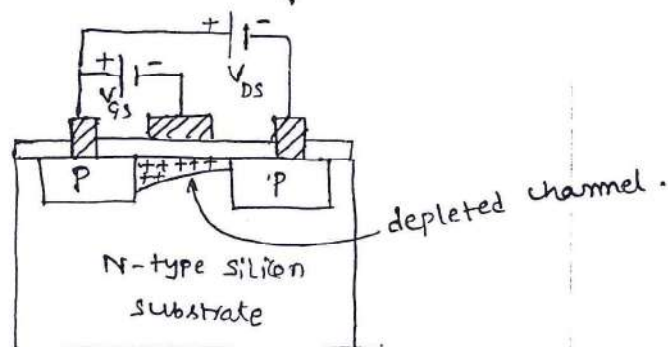


fig:- when $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$ the channel gets pinched off, hence I_D becomes constant.

* The drain characteristics of a P-channel enhancement MOSFET is as shown in below figure.

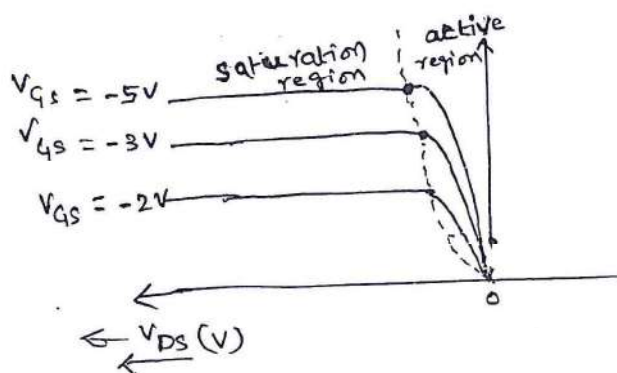


fig:- drain characteristics of a P-channel enhancement MOSFET.

* The transfer characteristics of a P-channel enhancement MOSFET is as shown in below figure. The relationship between V_{GS} and I_D is given by $I_D = k(V_{GS} - V_t)^2$. where k is a constant.

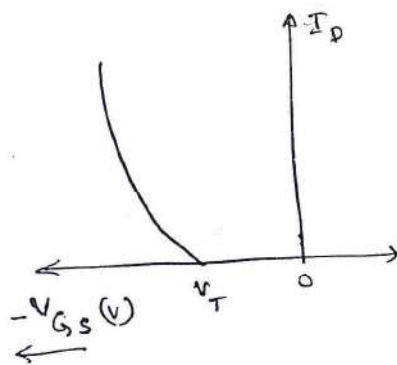


fig. Transfer characteristics of a P-channel enhancement MOSFET.

Depletion MOSFETs:

N-channel depletion MOSFET:

Construction:

- * Two highly doped N regions are diffused into a lightly doped P-type silicon substrate. one of these regions is called as source and the other one is called drain.
- * A channel is diffused between the source and drain regions.
- * A thin layer of SiO_2 is deposited over the surface of the P-type substrate and holes are cut into SiO_2 layer allowing contacts with source and drain using aluminium metal contact.
- * A thin metal layer is deposited over the layer of SiO_2 between the two N-regions to form gate terminal.
- * The metal area of gate in conjunction with the SiO_2 layer and the semiconductor channel forms a parallel plate capacitor.

operation of N-channel depletion mode MOSFET:

- * When $V_{GS} = 0$ and the drain with respect to source is positive then the (majority carriers) electrons flow through the N-channel from source 's' to drain 'd'. Therefore the current I_D flows through the channel from drain to source.

- * Now if V_{GS} is increased i.e. $V_{GS} > 0$, the channel

width is increased due to which the drain current I_D increases.

* If V_{GS} is decreased from '0', i.e. $V_{GS} < 0$, the diffused channel between drain and source will get depleted, as the majority charge carriers of P-substrate are attracted towards the negative gate terminal since $V_{GS} < 0$.

* Hence, in the ^{N-channel} depletion mode MOSFET, the channel is enhanced when $V_{GS} > 0$ and the channel is depleted when $V_{GS} < 0$. Hence it can also be called as "dual mode MOSFET".

The structure and symbol of N-channel depletion MOSFET is as shown in below.

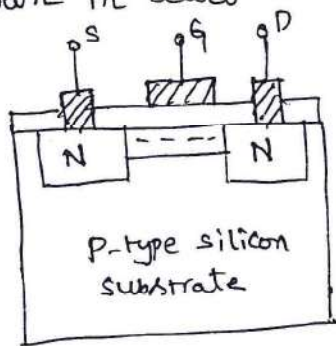


fig: N-channel depletion MOSFET structure

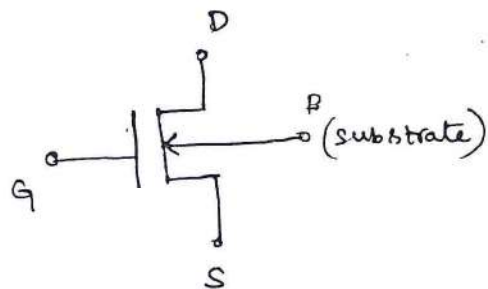


fig: symbol of N-channel depletion MOSFET.

The drain and transfer characteristics are as shown in below figure.

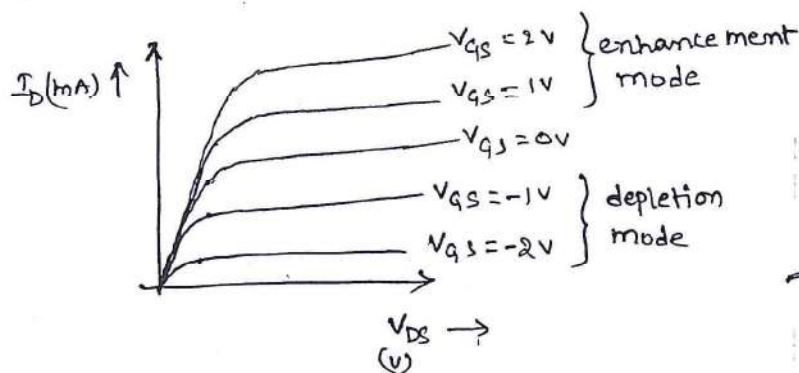


fig: drain characteristics

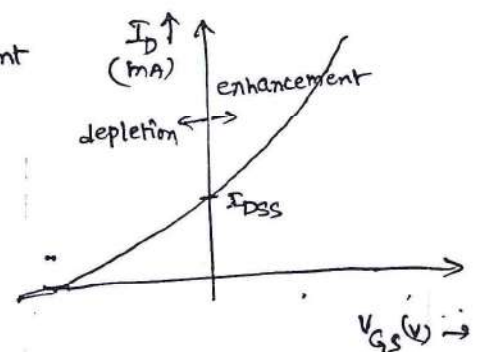


fig: transfer characteristics

The relationship between drain current I_D and V_{GS} for transfer characteristics is given by the equation $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$

P-channel depletion MOSFET:

Construction:

- * Two highly doped P-regions are diffused into a lightly doped n-type silicon substrate. one of these regions is called as source and the other one is called drain.
- * A channel is diffused between the source and drain regions.
- * A thin layer of SiO_2 is deposited over the surface of the n-type substrate and holes are cut into SiO_2 layer allowing contacts with source and drain, using aluminium metal contacts.
- * A thin layer of metal is deposited over the SiO_2 layer between the two p-regions to form gate terminal.
- * The metal area of gate in conjunction with the SiO_2 layer and the semiconductor channel forms a parallel plate capacitor.

The construction and symbol of the P-channel depletion MOSFET is as shown in below figure.

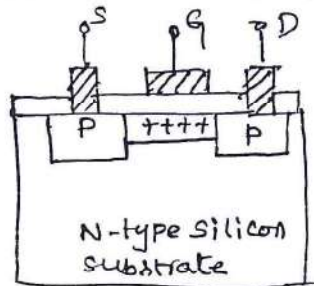


fig:- P-channel depletion-
- MOSFET structure.

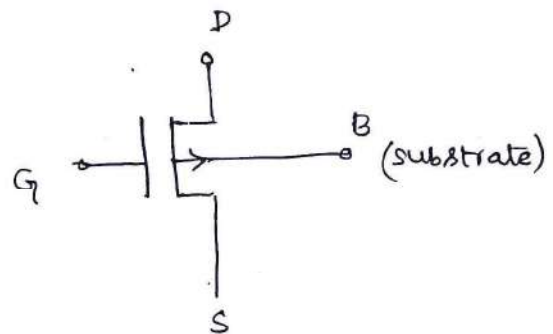


fig:- symbol for P-channel
depletion MOSFET.

operation of a p-channel depletion Mode MOSFET:

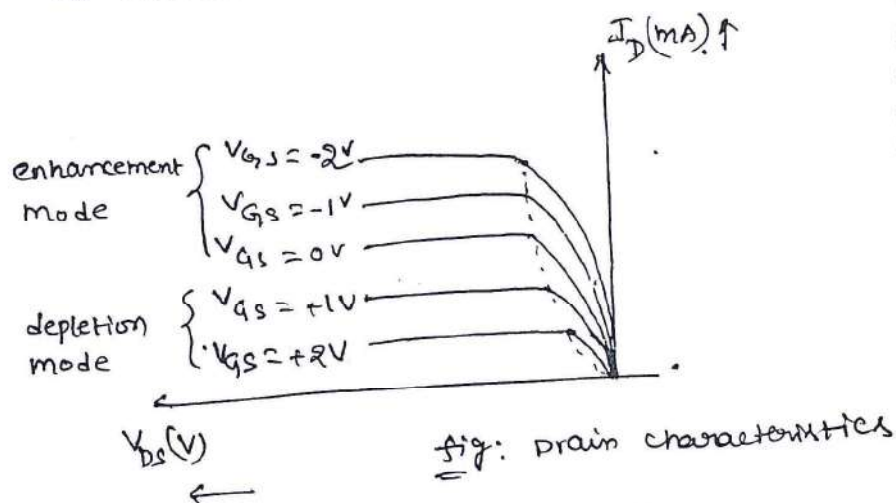
- * when $V_{GS} = 0$ and the drain with respect to source is negative then the holes (majority carriers) flow through the P-channel from source 'S' to drain 'D'. Therefore the current I_D flows from source to drain.
- * Now if V_{GS} is less than zero, the channel width

is increased due to which the drain current I_D increases. (29)

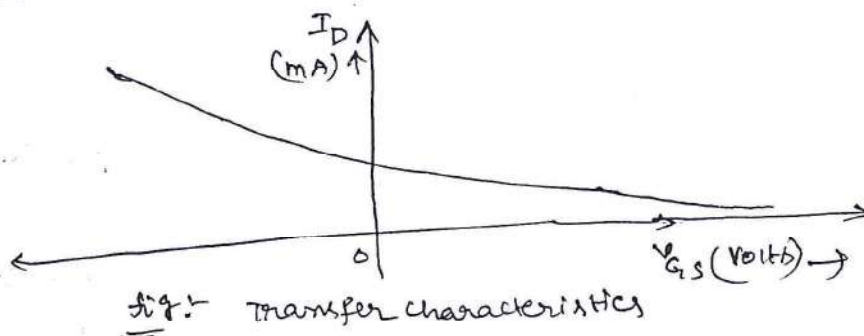
* If V_{GS} is greater than zero, the majority carriers of n-type substrate (i.e. electrons) are attracted towards the positive gate, into the channel hence the channel between the drain and source gets depleted.

* Hence in the P-channel depletion mode MOSFET the channel is enhanced if $V_{GS} < 0$ and gets depleted if $V_{GS} > 0$. Therefore a depletion MOSFET of P-channel can also be called as "dual mode MOSFET".

The drain characteristics of P-channel depletion MOSFET is as shown below.

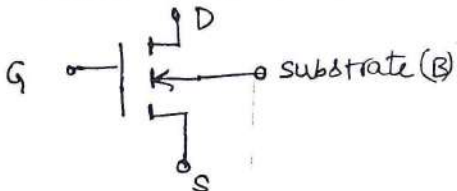
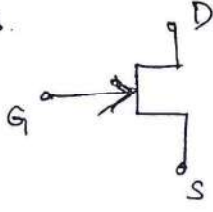


The transfer characteristics of P-channel depletion MOSFET is as shown in below



The relationship between drain current I_D and V_{GS} for transfer characteristics is given by the equation $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$

Comparison of MOSFET with JFET:

MOSFET	JFET
1> MOSFETs are easy to fabricate 2> The depletion MOSFETs are operated in both enhancement mode as well as depletion mode 3> Input impedance is high ($> 10,000 \text{ M}\Omega$) 4> Gate is insulated from channel by a layer of SiO_2 5> channel exists permanently in depletion MOSFET, but not in enhancement MOSFET 6> The symbol for enhancement n-channel MOSFET is 	1> Compared to MOSFET JFET is difficult to fabricate 2> JFETs are operated in only depletion mode 3> Input impedance is very high ($> 10 \text{ M}\Omega$) 4> Gate is not insulated from the channel 5> channel exists permanently 6> The symbol for n-channel JFET is 

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ECE 255, MOSFET Small Signal Analysis

6 March 2018

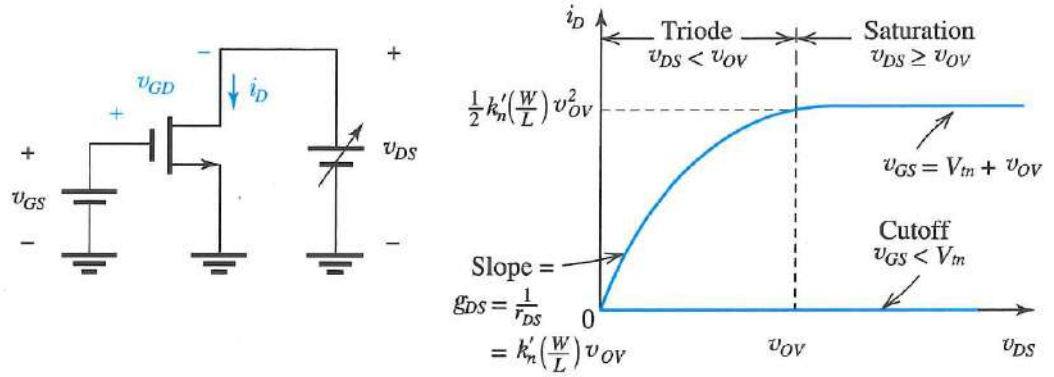
In this lecture, we will introduce small-signal analysis, operation, and models from Section 7.2 of Sedra and Smith. Since the BJT case has been discussed, we will now focus on the MOSFET case. In the small-signal analysis, one assumes that the device is biased at a DC operating point (also called the Q point or the quiescent point), and then, a small signal is super-imposed on the DC biasing point.

1 The DC Bias Point and Linearization—The MOS-FET Case

Before one starts, it will be prudent to refresh our memory on the salient features of the MOSFET from Table 5.1 of Sedra and Smith. Also, Figure 1 is included to remind one of the definition of the relationship between V_{GS} , V_{OV} , V_{GD} , and V_{DS} . When $V_{DS} > V_{OV}$, the channel region is not continuous, and pinching occurs. The device is in the saturation region.

Printed on March 14, 2018 at 10:47: W.C. Chew and S.K. Gupta.

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor



- $v_{GS} < V_{in}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{in} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{in}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k'_n \left(\frac{W}{L} \right) \left[(v_{GS} - V_{in}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$

or equivalently,

$$i_D = k'_n \left(\frac{W}{L} \right) \left(v_{OV} - \frac{1}{2} v_{DS} \right) v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{in}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{in})^2$$

or equivalently,

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{OV}^2$$

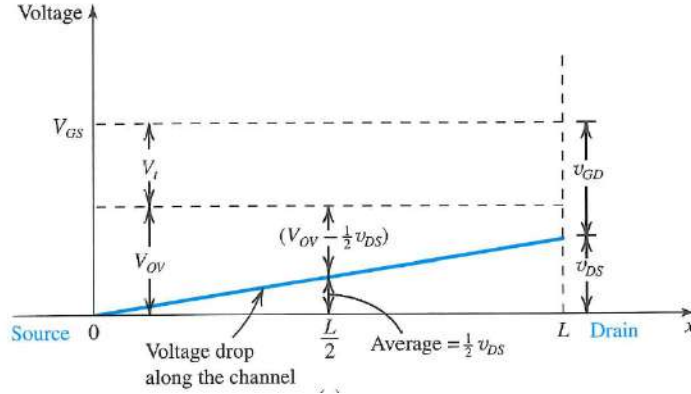


Figure 1: A figure to remind us of the definition of v_{GS} , v_{OV} , v_{DS} , and v_{GD} in the triode region (Courtesy of Sedra and Smith).

Figure 2 illustrates an NMOS operating as an amplifier. It is being biased with a DC voltage, and a small signal is superimposed on top of the DC voltage.

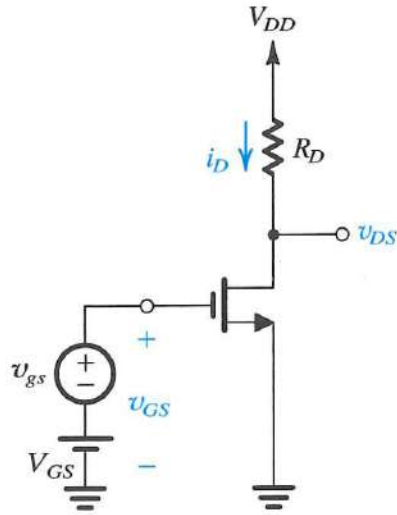


Figure 2: Circuit diagram of a transistor MOSFET (NMOS) amplifier with a small time-varying signal superimposed on top of a DC voltage bias source (Courtesy of Sedra and Smith).

Before proceeding further, one is also reminded of the i - v characteristics of

a MOSFET. Namely, that in the saturation region

$$i_D = \frac{1}{2}k_n(v_{GS} - V_t)^2 = \frac{1}{2}k_nv_{OV}^2 \quad (1.1)$$

where

$$v_{GS} = V_{GS} + v_{gs}, \quad v_{OV} = V_{OV} + v_{ov} \quad (1.2)$$

where $v_{OV} = v_{GS} - V_t$. Again, the notation will be that the total value is denoted by a lower-case letter with upper-case subscript, the DC value or the Q point is denoted by a upper-case letter with upper-case subscript. The small signal is denoted by a lower-case letter with lower-case subscript. However, the threshold voltage, which is a DC value is denoted as V_t in order not to be confused with V_T the thermal voltage.

It is noted that the overdrive voltage v_{OV} is defined as

$$v_{OV} = v_{GS} - V_t = V_{GS} + v_{gs} - V_t \quad (1.3)$$

If we further define that $v_{OV} = V_{OV} + v_{ov}$, equating the time varying and DC parts, one gets

$$V_{OV} = V_{GS} - V_t, \quad v_{ov} = v_{gs} \quad (1.4)$$

If the time-varying signals are turned off, then (1.1), keeping only the DC signals, becomes

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_nV_{OV}^2 \quad (1.5)$$

which is the i - v relation obtained at the Q point, or the operating point.

In (1.1), by letting

$$v_{GS} = V_{GS} + v_{gs} \quad (1.6)$$

then

$$i_D = \frac{1}{2}k_n(V_{GS} + v_{gs} - V_t)^2 = \frac{1}{2}k_n(V_{GS} - V_t)^2 + k_n(V_{GS} - V_t)v_{gs} + \frac{1}{2}k_nv_{gs}^2 \quad (1.7)$$

For small signal analysis, v_{gs} is assumed to be small. Then v_{gs}^2 is even smaller; and hence, the last term can be ignored in the above. By letting the total current here as $i_D = I_D + i_d$, a DC term plus a time-varying term, then from the above, one can see that the time-varying term is approximately given by

$$i_d \approx k_n(V_{GS} - V_t)v_{gs} = g_mv_{gs} \quad (1.8)$$

where quadratic term proportional to v_{gs}^2 has been ignored, and

$$g_m = k_n(V_{GS} - V_t) = k_nV_{OV} = \frac{i_d}{v_{gs}} = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=V_{GS}} \quad (1.9)$$

The above has the unit of conductance, and it is called the **MOSFET transconductance**. The last equality follows from that the transconductance is the ratio

between two incrementally small quantities at the operating point. This incremental relationship is shown in Figure 3.

A more detail analysis by comparing the last two terms on the right-hand side, one can show that the last term in (1.7) can be ignored if

$$v_{gs} \ll 2(V_{GS} - V_t) = 2V_{OV} \quad (1.10)$$

Also, it is seen from the Figure 3 that in order for the small signal analysis to be valid, it is required that $v_{gs} \ll 2V_{OV}$.

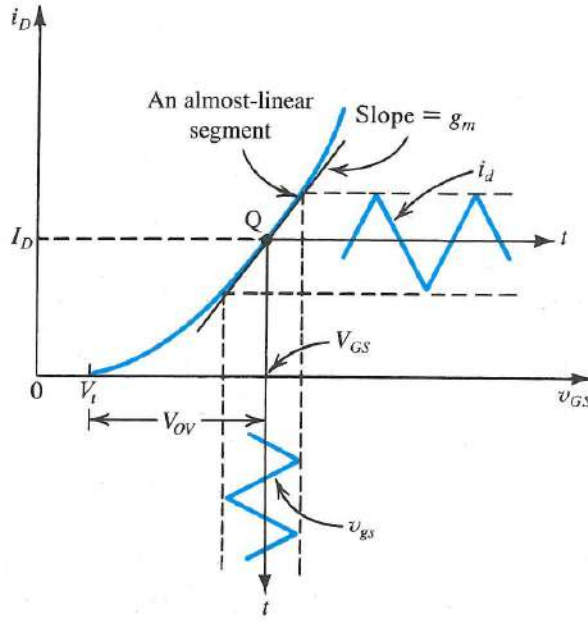


Figure 3: Graphical depiction of the small signal analysis for MOSFET (Courtesy of Sedra and Smith).

Furthermore, it is seen that at the DC operating point, by KVL

$$V_{DS} = V_{DD} - R_D I_D \quad (1.11)$$

If V_{DD} is held fixed, then by KVL again

$$v_{DS} = V_{DD} - R_D i_D = V_{DD} - R_D (I_D + i_d) = V_{DD} - R_D I_D - R_D i_d \quad (1.12)$$

From the above, by first letting $v_{DS} = V_{DS} + v_{ds}$, and then equating the time-varying terms and the DC terms, one concludes that the time varying part of v_{DS} , or v_{ds} , is given by

$$v_{ds} = -i_d R_D = -g_m v_{gs} R_D \quad (1.13)$$

One can define the voltage gain as

$$A_{vo} = \frac{v_{ds}}{v_{gs}} = -g_m R_D \quad (1.14)$$

The negative sign comes about because an increase in v_{gs} causes an increase in i_d , causing the rise in the voltage drop across R_D , and hence, a drop in the voltage v_{ds} . This sign reversal is indicated in Figure 4.

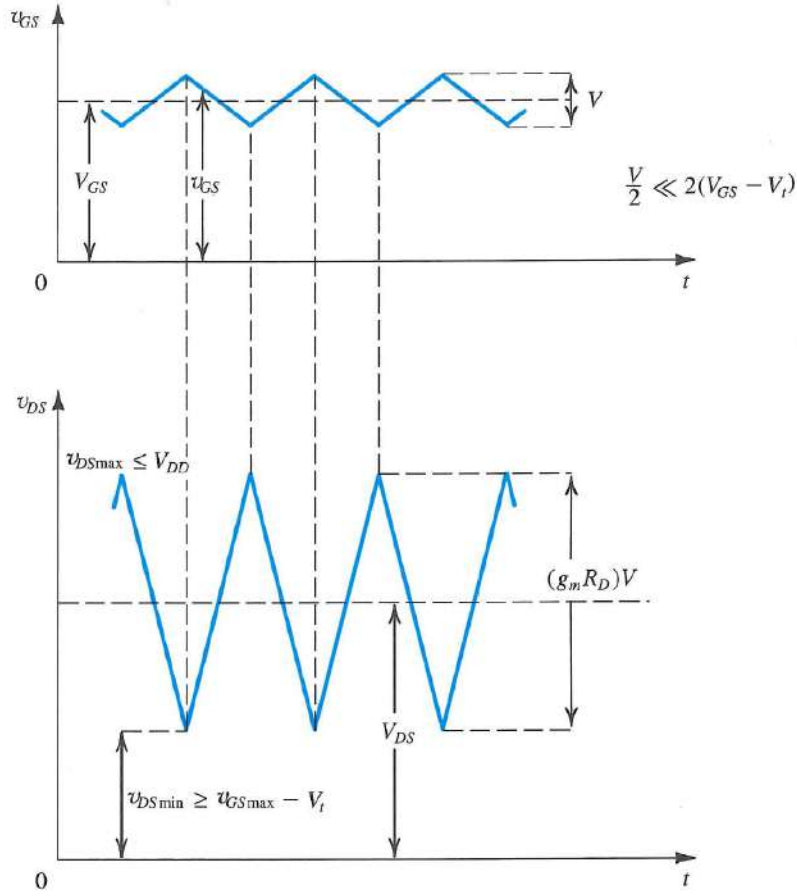


Figure 4: Total instantaneous voltage v_{GS} and v_{DS} for the circuit in Figure 2. Note the sign reversal of the amplified signal (Courtesy of Sedra and Smith).

2 Small Signal Equivalent-Circuit Models

By looking at the i - v characteristic curve of the MOSFET as shown in Table 5.1, it is seen for incremental v_{ds} , the current i_d does not change. This relationship can be modeled by a current source. Moreover, the gate of the MOSFET is essentially an open circuit at DC. Hence, the **small-signal equivalent-circuit model** is presented in Figure 5(a).

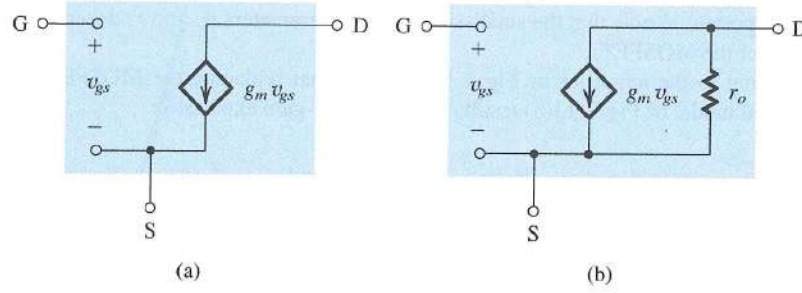


Figure 5: The small-signal model for a MOSFET: (a) no Early effect (channel-length modulation effect); (b) Early effect is included by adding $r_o = |V_A|/I_D$ (Courtesy of Sedra and Smith).

When the Early effect has to be accounted for, an output resistor r_o can be added as shown in Figure 5(b). The value of r_o is given as

$$r_o = \frac{|V_A|}{I_D}, \text{ where } I_D = \frac{1}{2}k_n V_{OV}^2 \quad (2.1)$$

where $V_A = 1/\lambda$, and $-V_A$ is the negative intercept of the i - v curve.

Here, r_o is typically 10 k Ω to 1000 k Ω . When r_o is included, then the voltage gain becomes

$$A_v = \frac{v_{ds}}{v_{gs}} = -g_m(R_D || r_o) \quad (2.2)$$

In other words, the inclusion of r_o reduces the voltage gain.

The above analysis can be used for PMOS by noting for the sign change in PMOS, and by using $|V_{GS}|$, $|V_t|$, $|V_{OV}|$, and $|V_A|$ in the formulas, and replacing k_n with k_p .

3 Transconductance g_m

The transconductance can be looked at with more details by using $k_n = k'_n(W/L)$, giving

$$g_m = k'_n(W/L)(V_{GS} - V_t) = k'_n(W/L)V_{OV} = \mu_n C_{ox}(W/L)V_{OV} \quad (3.1)$$

The transconductance can be increased by increasing the W/L ratio, and also increasing the overdrive voltage V_{OV} . But increasing V_{OV} implies that the operating point for V_{DS} has to increase in order for the MOSFET to be in the saturation region.

Also, by using the fact that

$$I_D = \frac{1}{2}k_n V_{OV}^2 = \frac{1}{2}k'_n(W/L)V_{OV}^2 \quad (3.2)$$

or that $V_{OV} = \sqrt{2I_D/(k'_n(W/L))}$, then g_m in (3.1) can be alternatively rewritten as

$$g_m = \sqrt{2k'_n(W/L)I_D} \quad (3.3)$$

implying that g_m is proportional to the square roots of the drain current I_D , and W/L . At this point, note that

1. The transconductance g_m of a MOSFET is geometry dependent whereas that of the BJT is not.
2. The transconductance of a BJT is much larger than that of a MOSFET.

For example, with biasing point of $I_D = 50$ mA, with $k'_n = 120 \mu\text{A}/\text{V}^2$, with $W/L = 1$, $g_m = 0.35$ mA/V, whereas when $W/L = 100$, $g_m = 3.5$ mA/V. But typically, the $g_m = 20$ mA/V for BJT when $I_C = 0.5$ mA.

Alternatively, by seeing that $I_D = \frac{1}{2}k_n V_{OV}^2$ from (1.5) and that $g_m = k_n V_{OV}$ from (1.9), and by dividing the two equations, it can be shown that

$$g_m = \frac{2I_D}{V_{OV}} \quad (3.4)$$

Since g_m is an incremental relationship, this relationship can be shown graphically as in Figure 6 where the slope is also shown graphically.

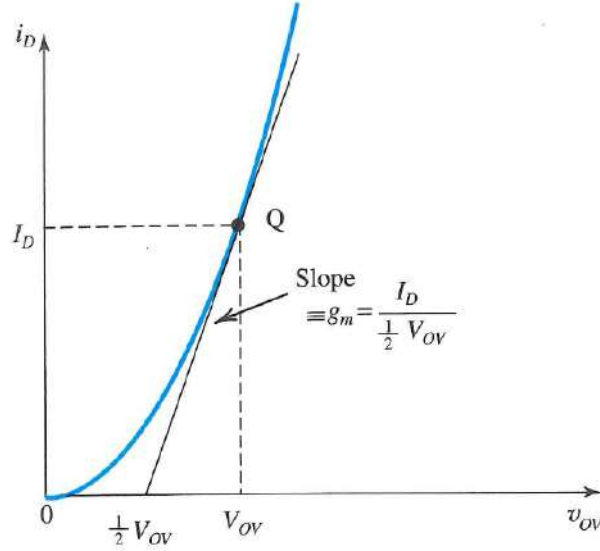


Figure 6: The relationship between I_D , V_{OV} , and g_m as shown in the i_D versus v_{OV} curve (Courtesy of Sedra and Smith).

The above equations indicate that a designer can change g_m by altering W/L , V_{OV} , and I_D .

4 The T Equivalent-Circuit Model

The hybrid- π equivalent-circuit model can be replaced by the T equivalent-circuit model. The morphing of a hybrid- π model to the T model is shown in Figure 7.

1. The current source in the hybrid- π model can be split into two without affecting the branch current. This is seen from the morphing of Figure 7(a) to Figure 7(b).
2. Note that the gate current is zero. The point X can be connected to the gate input, and yet the gate current is zero because of KCL at X. This is indicated in Figure 7(c).
3. But the second voltage-controlled current source is just the voltage and current relation of a resistor whose resistance is $1/g_m$. Hence, it can be replaced by a resistor as shown in Figure 7(d).

Notice that in the T equivalent-circuit model, due to its construction, and KCL, the gate current is always zero, implying that its resistance is infinite.

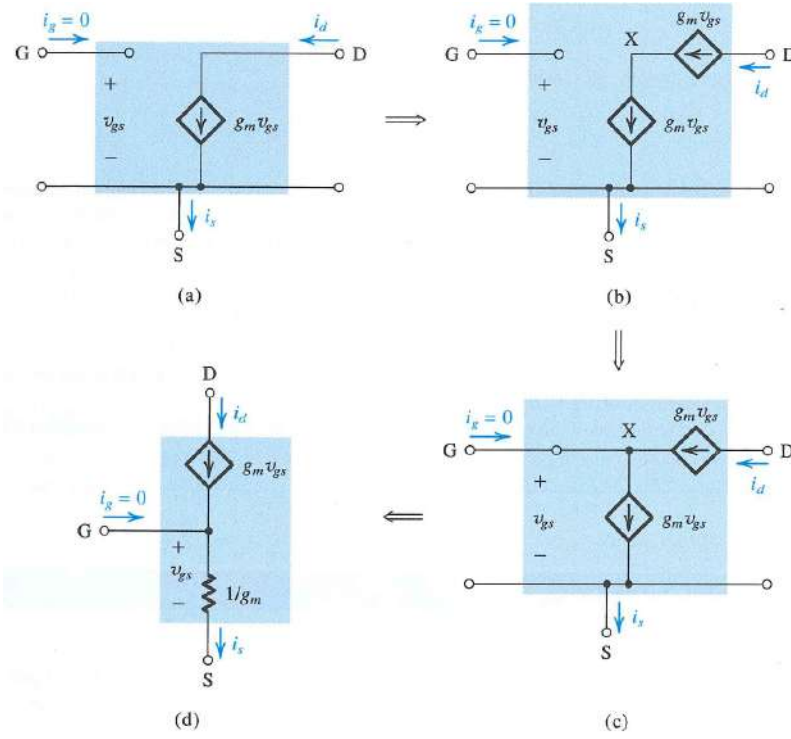


Figure 7: The morphing of the hybrid- π equivalent circuit model in (a) to the T equivalent circuit model in (d) (Courtesy of Sedra and Smith).

Also as the morphing of the hybrid- π equivalent-circuit model to the T equivalent-circuit model is unaffected by connecting a resistor between D and S, an r_o can be thus connected to account for the Early effect or the channel-modulation effect as shown in Figure 8(a). Figure 8(b) is an alternative way of representing the T equivalent-circuit model, so that the gate current is always zero by KCL.

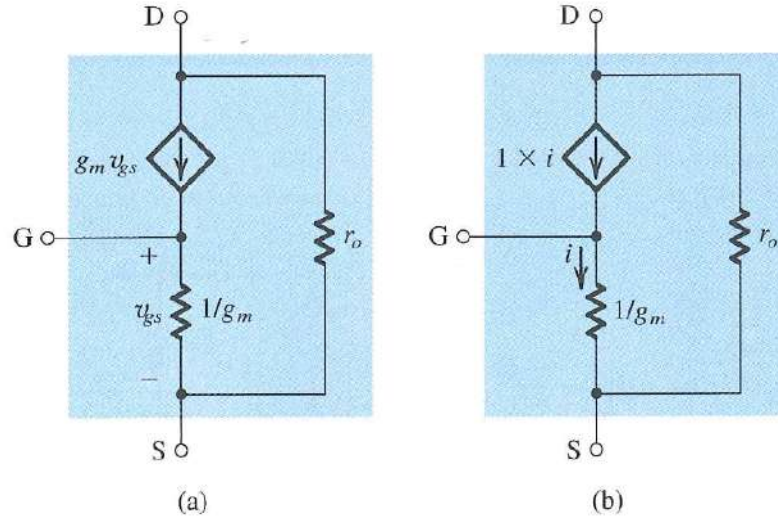


Figure 8: The morphing of the π equivalent-circuit model to the T equivalent circuit model is still valid if a resistor is connected between the drain D and the source S. Hence, in (a), r_o can be connected to account for the Early effect. (b) shows an alternative T model that is equivalent (Courtesy of Sedra and Smith).

Example 7.3

Figure 7.15(a) shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k'_n (W/L) = 0.25$ mA/V², and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

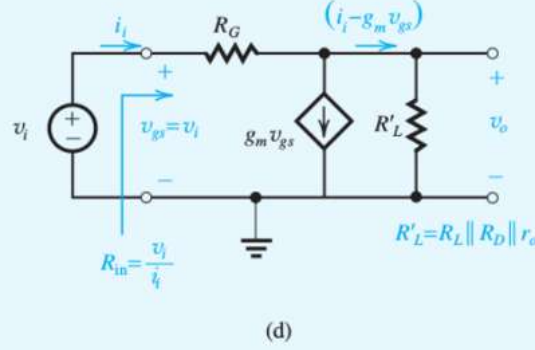


Figure 7.15 continued

Solution

We first determine the dc operating point. For this purpose, we eliminate the input signal v_i , and open-circuit the two coupling capacitors (since they block dc currents). The result is the circuit shown in Fig. 7.14(b). We note that since $I_G = 0$, the dc voltage drop across R_G will be zero, and

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D \quad (7.43)$$

With $V_{DS} = V_{GS}$, the NMOS transistor will be operating in saturation. Thus,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \quad (7.44)$$

where, for simplicity, we have neglected the effect of channel-length modulation on the dc operating point. Substituting $V_{DD} = 15$ V, $R_D = 10$ k Ω , $k_n = 0.25$ mA/V², and $V_t = 1.5$ V in Eqs. (7.43) and (7.44), and substituting for V_{GS} from Eq. (7.43) into Eq. (7.44) results in a quadratic equation in I_D . Solving the latter and discarding the root that is not physically meaningful yields the solution

$$I_D = 1.06 \text{ mA}$$

which corresponds to

$$V_{GS} = V_{DS} = 4.4 \text{ V}$$

and

$$V_{OV} = 4.4 - 1.5 = 2.9 \text{ V}$$

Next we proceed with the small-signal analysis of the amplifier. Toward that end we replace the MOSFET with its small-signal model to obtain the small-signal equivalent circuit of the amplifier, shown in Fig. 7.15(c). Observe that we have replaced the coupling capacitors with short circuits. The dc voltage supply V_{DD} has also been replaced with a short circuit to ground.

Example 7.3 *continued*

The values of the transistor small-signal parameters g_m and r_o can be determined by using the dc bias quantities found above, as follows:

$$\begin{aligned} g_m &= k_n V_{OV} \\ &= 0.25 \times 2.9 = 0.725 \text{ mA/V} \\ r_o &= \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ k}\Omega \end{aligned}$$

Next we use the equivalent circuit of Fig. 7.15(c) to determine the input resistance $R_{in} \equiv v_i/i_i$ and the voltage gain $A_v = v_o/v_i$. Toward that end we simplify the circuit by combining the three parallel resistances r_o , R_D , and R_L in a single resistance R'_L ,

$$\begin{aligned} R'_L &= R_L || R_D || r_o \\ &= 10 || 10 || 47 = 4.52 \text{ k}\Omega \end{aligned}$$

as shown in Fig. 7.15(d). For the latter circuit we can write the two equations

$$v_o = (i_i - g_m v_{gs}) R'_L \quad (7.45)$$

and

$$i_i = \frac{v_{gs} - v_o}{R_G} \quad (7.46)$$

Substituting for i_i from Eq. (7.46) into Eq. (7.45) results in the following expression for the voltage gain $A_v \equiv v_o/v_i = v_o/v_{gs}$:

$$A_v = -g_m R'_L \frac{1 - (1/g_m R_G)}{1 + (R'_L/R_G)}$$

Since R_G is very large, $g_m R_G \gg 1$ and $R'_L/R_G \ll 1$ (the reader can easily verify this), and the gain expression can be approximated as

$$A_v \simeq -g_m R'_L \quad (7.47)$$

Substituting $g_m = 0.725 \text{ mA/V}$ and $R'_L = 4.52 \text{ k}\Omega$ yields

$$A_v = -3.3 \text{ V/V}$$

To obtain the input resistance, we substitute in Eq. (7.46) for $v_o = A_v v_{gs} = -g_m R'_L v_{gs}$, then use $R_{in} \equiv v_i/i_i = v_{gs}/i_i$ to obtain

$$R_{in} = \frac{R_G}{1 + g_m R'_L} \quad (7.48)$$

This is an interesting relationship: The input resistance decreases as the gain ($g_m R'_L$) is increased. The value of R_{in} can now be determined; it is

$$R_{in} = \frac{10 \text{ M}\Omega}{1 + 3.3} = 2.33 \text{ M}\Omega$$

which is still very large.

The largest allowable input signal $\hat{v}_i$ is constrained by the need to keep the transistor in saturation at all times; that is,

$$v_{DS} \geq v_{GS} - V_t$$

Enforcing this condition with equality at the point v_{GS} is maximum and v_{DS} is minimum, we write

$$v_{DS\min} = v_{GS\max} - V_t$$

$$V_{DS} - |A_v| \hat{v}_i = V_{GS} + \hat{v}_i - V_t$$

Since $V_{DS} = V_{GS}$, we obtain

$$\hat{v}_i = \frac{V_t}{|A_v| + 1}$$

This is a general relationship that applies to this circuit irrespective of the component values. Observe that it simply states that the maximum signal swing is determined by the fact that the bias arrangement makes $V_D = V_G$ and thus, to keep the MOSFET out of the triode region, the signal between D and G is constrained to be equal to V_t . For our particular design,

$$\hat{v}_i = \frac{1.5}{3.3 + 1} = 0.35 \text{ V}$$

Since $V_{OV} = 2.9 \text{ V}$, a v_i of 0.35 is indeed much smaller than $2V_{OV} = 5.8 \text{ V}$; thus the assumption of linear operation is justified.

A modification of this circuit that increases the allowable signal swing is investigated in Problem 7.103.

Example 7.4

Figure 7.18(a) shows a MOSFET amplifier biased by a constant-current source I . Assume that the values of I and R_D are such that the MOSFET operates in the saturation region. The input signal v_i is coupled to the source terminal by utilizing a large capacitor C_{C1} . Similarly, the output signal at the drain is taken through a large coupling capacitor C_{C2} . Find the input resistance R_{in} and the voltage gain v_o/v_i . Neglect channel-length modulation.

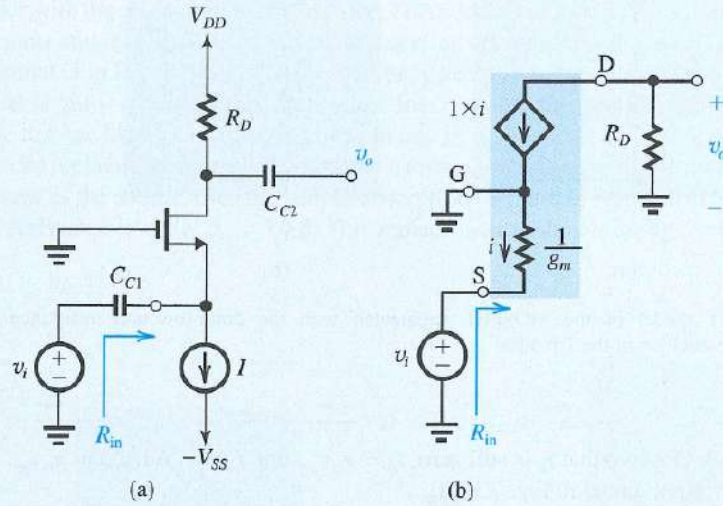


Figure 7.18 (a) Amplifier circuit for Example 7.4. (b) Small-signal equivalent circuit of the amplifier in (a).

Solution

Replacing the MOSFET with its T equivalent-circuit model results in the amplifier equivalent circuit shown in Fig. 7.18(b). Observe that the dc current source I is replaced with an open circuit and the dc voltage source V_{DD} is replaced by a short circuit. The large coupling capacitors have been replaced by short circuits. From the equivalent-circuit model we determine

$$R_{in} = \frac{v_i}{-i} = 1/g_m$$

and

$$v_o = -iR_D = \left(\frac{v_i}{1/g_m} \right) R_D = g_m R_D v_i$$

Thus,

$$A_v \equiv \frac{v_o}{v_i} = g_m R_D$$

We note that this amplifier, known as the common-gate amplifier because the gate at ground potential is common to both the input and output ports, has a low input resistance ($1/g_m$) and a noninverting gain. We shall study this amplifier type in Section 7.3.5.

ELECTRONIC DEVICES AND CIRCUITS
DEPT. OF ELECTRONICS AND COMM. ENGINEERING
IMPORTANT QUESTIONS

PART-A (2 Marks)

1. Differentiate drift and diffusion currents?
2. Define intrinsic semi conductor, write example.
3. Define static and dynamic resistance of P-N diode.
4. Draw PN Junction Diode Characteristics.
5. Explain how P-N junction diode acts as a Rectifier.
6. Write the formula for β in terms of α , and in terms of of a NPN transistor
7. Explain how P-N junction diode acts as a Rectifier.
8. Why BJT is a current controlled Transistor?
9. Common collector is also called as “emitter follower”. Justify it?
10. Write about thermal runaway.
11. Define pinch-off voltage.
12. Define the Stability factors for Fixed Bias Circuit.
13. Explain how transistor works as an amplifier.
14. Define the Stability factors for Fixed Bias Circuit.
15. What is the need of biasing?
16. Draw h-parameter model for CE amplifier
17. What are the parameters in Two port network?
18. Define the transconductance g_m .
19. Draw the structure and symbol of N-Channel JFET.
20. Mention small signal parameters of JFET.
21. Differentiate between BJT and JFET.
22. How FET acts as Voltage Variable Resistor?
23. Write the definition of pinched off Voltage V_p .
24. What is Threshold voltage V_t .
25. Write the Drain current equation for saturation region I_D .

PART-B (10 Marks)

1. Explain the operation of forward biased and reverse biased PN junction Diode and draw its complete V - I Characteristics.
2. Draw the full wave rectifier with π -section filter & explain its operation along with derivation for ripplefactor.
3. What is tunneling phenomena? Explain the principle of operation of tunnel diode with its characteristics.
4. Explain temperature dependence of V-I characteristics in PN junction diode.
5. Explain about Tunnel diode (Esaki) in detail with Construction and operation
6. Explain the Uni-Junction Transistor (UJT) With V-I Characteristics.
7. Draw and explain the input and output characteristics of BJT Connected in common Emitter (CE) configuration.
8. Explain input and output characteristics of transistor in CB configuration with neat diagram.

9. Explain the collector to base bias method along with circuit diagram and derive the stability factor's for it.
10. Draw the circuit diagram of a voltage divider bias and derive expression for Stability factor.
11. Explain the transconductance and input resistance at the base in BJT Small Signal Operation and Models.
12. Derive the operating point using AC and DC load lines.
13. Draw and explain the BJT Small Signal Operation and its equivalent Models for Common-Base (CB) amplifier.
14. Explain the working of an N channel JFET, draw explain the V-I characteristics of the different regions.
15. Describe the construction and working principle of Enhancement mode and depletion mode MOSFET and draw its characteristics.
16. Draw and explain the construction , operation of Enhancement P-Channel MOSFET and explain the three regions of operation of a MOSFET.
17. Draw the small-signal model of common drain MOSFET amplifier. Derive expressions for the transconductance.
18. Explain the common source (CS) amplifier without and with source resistance for small-signal model and Derive expressions for voltage gain and Input and output Impedance.
19. Draw and explain construction and operation of Enhancement mode MOSFET with its characteristics.

Subject Code: 23HPC0403ANNAMACHARYA INSTITUTE OF TECHNOLOGY AND SCIENCES::KADAPA
(AUTONOMOUS)

B.Tech II Year I Semester (HM23) Regular Examinations, November 2024

ELECTRONIC DEVICES AND CIRCUITS
(Electronics & Communication Engineering)

Time: 3 hours

Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)2. In Part-A, each question carries **two marks**.3. Answer **ALL** the questions in **Part-A** and **Part-B****PART-A**
(Compulsory Question)

1. Answer all the following short answer questions (10 X 2 = 20M)		CO	Blooms Level
a)	Draw symbol for PN Diode and LED	CO1	L1
b)	Compare half wave rectifier and full wave rectifier	CO1	L2
c)	Define current amplification factor	CO2	L1
d)	What is the need of biasing?	CO2	L1
e)	Draw h-parameter model for CE amplifier	CO3	L2
f)	What is emitter follower? Draw the circuit diagram of CC configuration	CO3	L1
g)	Why the input impedance of FET is higher than BJT	CO4	L1
h)	Explain how FET acts as a voltage regulator	CO4	L2
i)	Discuss the gain and frequency response characteristics of MOSFET amplifier	CO5	L2
j)	Sketch the drain and transfer characteristics of MOSFET in enhancement mode	CO5	L2

PART-BAnswer **five** questions by choosing one question from each unit (5 x 10 = 50 Marks)

			Marks	CO	Blooms Level
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UNIT-I

Q.2.	Define the following: i. forward static and dynamic resistances of diode. ii. diffusion capacitance iii. transition capacitance.	10	CO1	L2
OR				
Q.3.	A 230V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together has a resistance of 100Ω, determine i) dc voltage across the load ii) dc current flowing through the load iii) dc power delivered to the load iv) PIV across each diode	10	CO1	L3

UNIT-II

Q.4.	a	Explain the working of PNP transistor.	5	CO2	L2
	b	Compare between CB, CE, and CC Amplifier Configurations	5	CO2	L5

Subject Code: 23HPC0403

		OR			
Q.5.		Explain how self biasing can be done in a BJT with relevant sketches and waveforms.	10	CO2	L2

UNIT-III

Q.6.		Draw the circuit diagram and low frequency equivalent circuit of common emitter amplifier and derive an expression for its voltage gain.	10	CO3	L4
		OR			
Q.7.		Derive all components in the Hybrid- π model in terms of h parameters in CE configuration.	10	CO3	L6

UNIT-IV

Q.8.		With the help of neat diagram, explain about operation of an N-channel JFET	10	CO4	L4
		OR			
Q.9.	a	An n-channel JFET has $I_{DSS} = 10\text{mA}$ and $V_P = -2\text{V}$. Determine the drain source resistance r_{ds} for (i) $V_{GS} = 0\text{V}$. (ii) $V_{GS} = -0.5\text{V}$.	5	CO4	L3
	b	Why we call FET as a Voltage Controlled Device	5	CO4	L2

UNIT-V

Q.10.		Draw the low frequency model for Common Drain FET amplifier and derive the equation for its voltage gain.	10	CO5	L6
		OR			
Q.11.		Draw and explain drain and transfer characteristics of depletion type MOSFET	10	CO5	L4

*** End ***