



ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES

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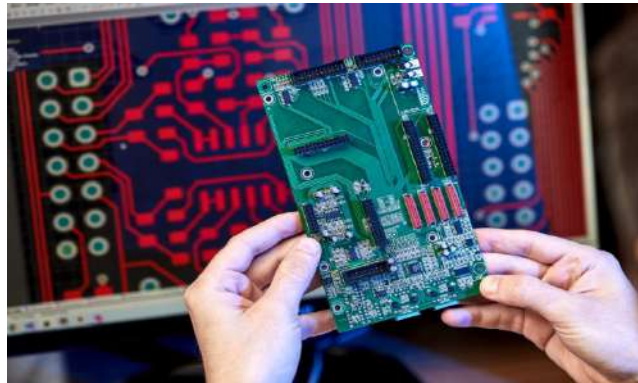
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ELECTRONIC CIRCUITS ANALYSIS (23HPC0408)



LECTURE NOTES II-B.TECH & I-SEM

Prepared by

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SCIENCES, KADAPA
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Web Site: <https://aitskadapa.ac.in>

II Year B.Tech. – II Semester

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(23HPC0408) ELECTRONIC CIRCUITS ANALYSIS**Course Objectives:**

- Understand the characteristics of Differential amplifiers, feedback and power amplifiers.
- Analyze the response of tuned amplifiers
- Categorize different oscillator circuits based on the application
- Design the electronic circuits for the given specifications and for a given application.

Course Outcomes:

- Understand the characteristics of differential amplifiers, feedback and power amplifiers. (L2)
- Examine the frequency response of multistage and differential amplifier circuits using BJT & MOSFETs at low and high frequencies. (L3)
- Investigate different feedback and power amplifier circuits based on the application. (L4)
- Derive the expressions for frequency of oscillation and condition for oscillation of RC and LC oscillator circuits. (L4)
- Evaluate the performance of different tuned amplifiers (L5)
- Design analog circuits for the given specifications and application. (L6)

UNIT I

Multistage & Differential Amplifiers: Introduction, Classification of Amplifiers, Distortion in amplifiers, Coupling Schemes, RC Coupled Amplifier using BJT, Cascaded RC Coupled BJT Amplifiers, Cascode amplifier, Darlington pair, introduction to the MOS Differential Pair, Small-Signal Operation of the MOS Differential Pair, and The BJT Differential Pair, and other Non ideal Characteristics of the Differential Amplifier.

UNIT II

Frequency Response: Low-Frequency Response of the CS and CE Amplifiers, Internal Capacitive Effects and the High-Frequency Model of the MOSFET and the BJT, High-Frequency Response of the CE, Emitter follower, CS, CD, f_{β} , f_T and gain bandwidth product.

UNIT III

Feedback Amplifiers: Introduction, The General Feedback Structure, Some Properties of Negative Feedback, The Four Basic Feedback Topologies, Series—Shunt, Series—Series, Shunt—Shunt, Shunt—Series.

Oscillators: General Considerations, Phase Shift Oscillator, Wien-Bridge Oscillator, LC Oscillators, Crystal Oscillators, Illustrative Problems.

UNIT IV

Power Amplifiers: Introduction, Class A amplifiers (Series fed, Transformer coupled, Push pull), Second Harmonic distortion, Class B amplifiers (Push pull, Complementary symmetry), Crossover distortion and Class AB operation, Class C amplifiers, Power BJTs.

UNIT V

Tuned Amplifiers: Introduction, single Tuned Amplifiers – Q-factor, frequency response, Double Tuned Amplifiers – Q-factor, frequency response, Concept of stagger tuning and synchronous tuning.

Multivibrators: Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using Transistors.

Textbooks:

1. Adel.S.SedraandKennethC.Smith,“MicroElectronicCircuits,”6th Edition, Oxford University Press, 2011.
2. J.Millman,H.TaubandMothikiS.PrakashRao-Pulse,Digital and Switching Waveforms –2nd Ed., TMH, 2008.
3. Millman, CChalkias,“Integrated Electronics”,4th Edition, McGraw Hill Education (India) Private Ltd., 2015.

References:

1. Behzad Razavi,“Fundamentals of Micro Electronics”,Wiley, 2010.
2. Donald A Neamen, “Electronic Circuits –AnalysisandDesign,”3rdEdition, McGraw Hill (India), 2019.
3. Robert L. Boylestad and Louis Nashelsky, “Electronic Devices and Circuits Theory”, 9th Edition, Pearson/Prentice Hall, 2006.

Unit - I

Multistage & Differential Amplifiers

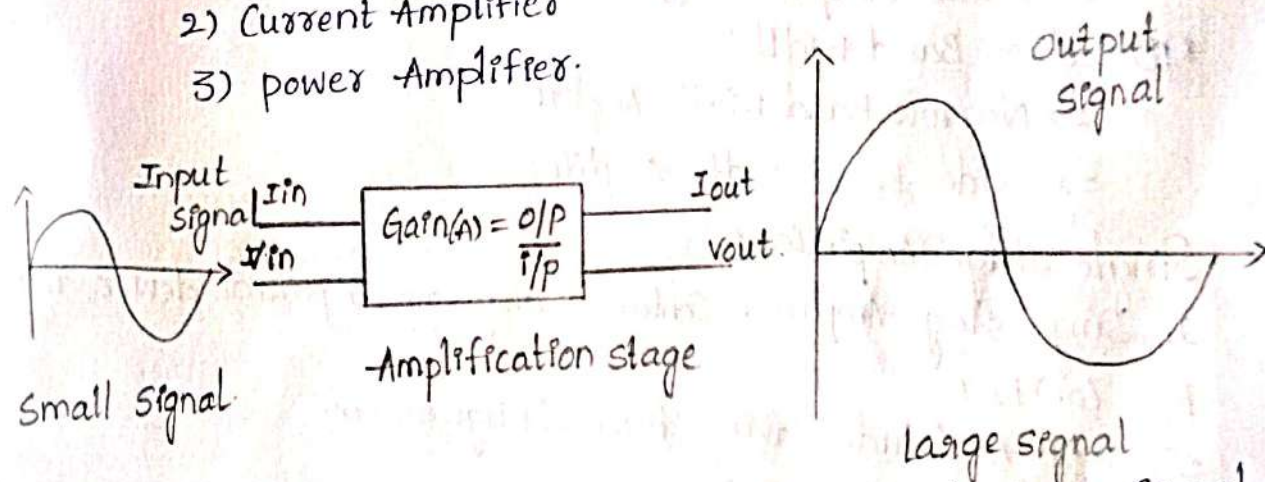
Introduction about Amplifier:

An Amplifier is an electronic device that increases the strength of the signal in terms of voltage, power, current or frequency signals.

* It is used in equipment, electronic devices, such as Television and Radio Receivers, audio equipment and Computers, for the increase the Amplitude of the signal.

* These are classified into three signal

- 1) Voltage Amplifier
- 2) Current Amplifier
- 3) power Amplifier.



A Small signal is fed to Amplitude we can get the large signal at the output.

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Classification of Amplifiers:

Depending upon the nature and level of Amplification and impedance Matching the Amplifiers are classified

* Based upon Transistor Configuration.

- ⇒ Common Base Configuration (CB)
- ⇒ Common Emitter Configuration (CE)
- ⇒ Common Collector Configuration (CC)

* Based on the devices

- ⇒ BJT Amplifier
- ⇒ FET Amplifier

* Based on Q point

- $\Rightarrow$ class A Amplifier
- $\Rightarrow$ class B Amplifier
- $\Rightarrow$ class C Amplifier
- $\Rightarrow$ class AB Amplifier.

* Based on stages

- $\Rightarrow$ Single stage Amplifier
- $\Rightarrow$ Multistage Amplifier

* Based on frequency Response

- $\Rightarrow$ Audio frequency (AF)
- $\Rightarrow$ Intermediate frequency (IF)
- $\Rightarrow$ Radio frequency (RF)

* Based on Band width.

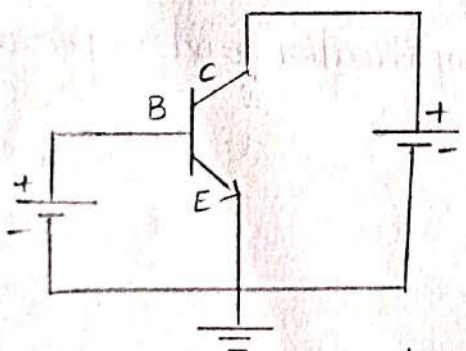
- $\Rightarrow$ Narrow Band width Amplifier
- $\Rightarrow$ Wide Band width Amplifier.

Single stage Amplifier:

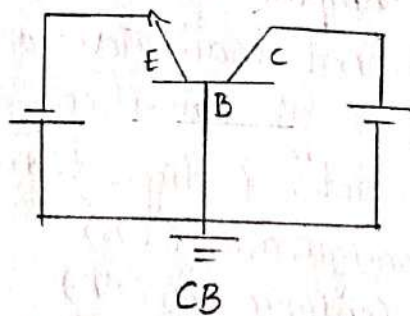
In Single stage Amplifier Containing only one Amplitude device that is BJT (or) FET

• In BJT Amplifier having three Configurations

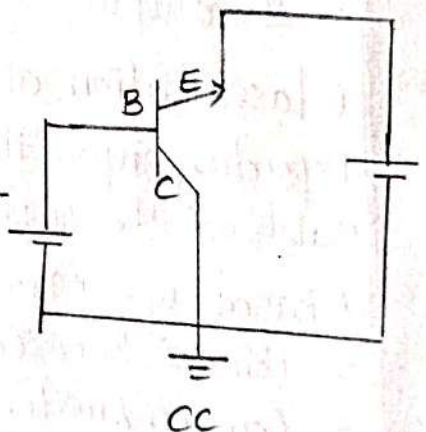
- 1) Common Emitter (CE)
- 2) Common Base (CB)
- 3) Common collector (CC) as shown in below.



CE Configuration.



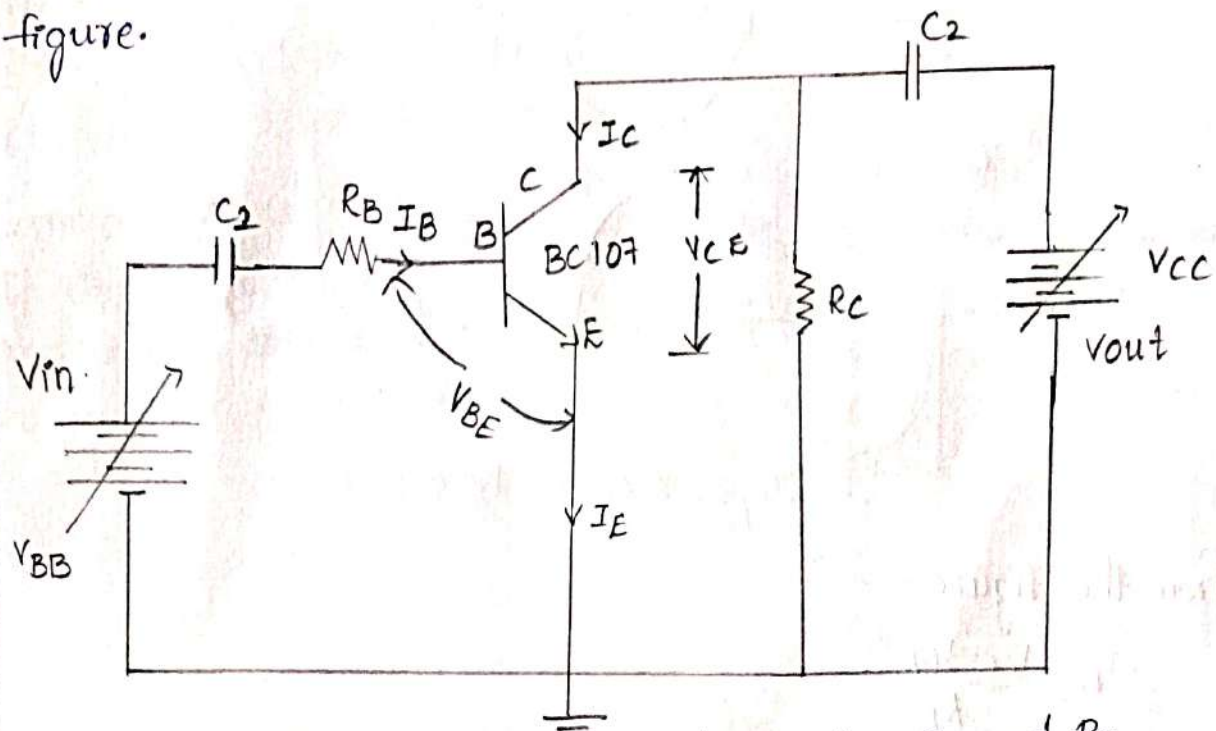
CB



CC

Common Emitter Configuration Amplifier:

In Common Emitter Amplifier emitter junction is Forward bias and Collector base junction is Reverse bias by the power supply V_{BB} & V_{CC} . So transistor is in service in active region as shown in below figure.



The operating Q point is determined by V_{CC} , R_B and R_C .
 The input Signal is applied to the base terminal and the amplifier Output Signal taken by the Collector terminal in the above circuit C_1 and C_2 Capacitors act as Coupling Capacitors

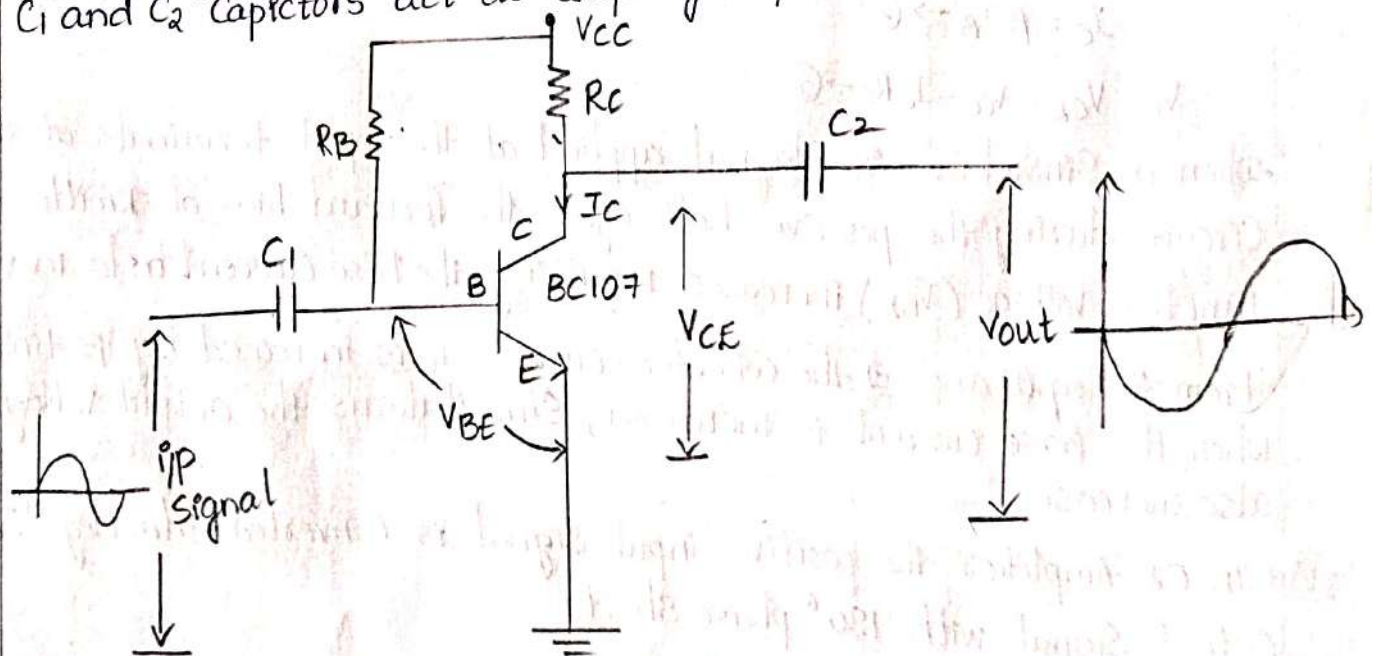
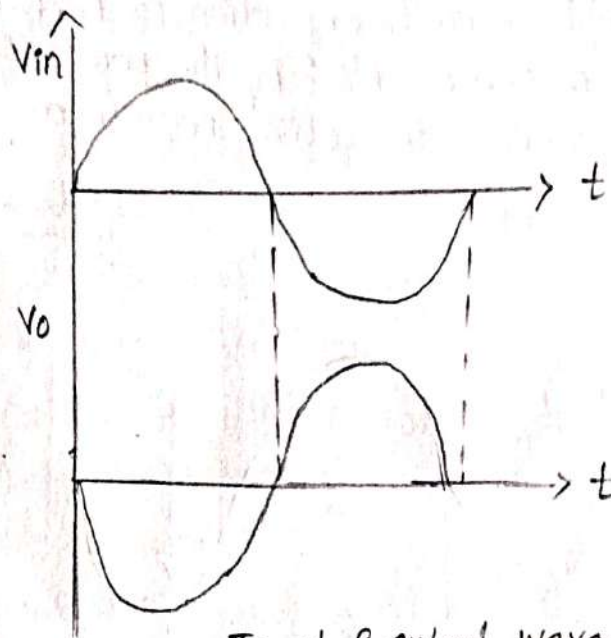


fig: CE Amplifier with Single power Supply



Input & output wave forms.

from the figure

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

if $V_{BE} \approx 0$ then

$$I_B \approx \frac{V_{CC}}{R_B} \rightarrow (1)$$

and

$$I_C = \beta I_B \rightarrow (2)$$

$$V_O = V_{CE} = V_{CC} - I_C R_C \rightarrow (3)$$

• When a sinusoidal AC signal is applied at the input terminals of the circuit during the positive half cycle, the forward bias of emitter-base junction voltage (V_{BE}) increases, resulting in the base current also increasing.

• From the eq (2) and (3), the collector current I_C is increased by β times when the base current is increased, simultaneously the output voltage also increases.

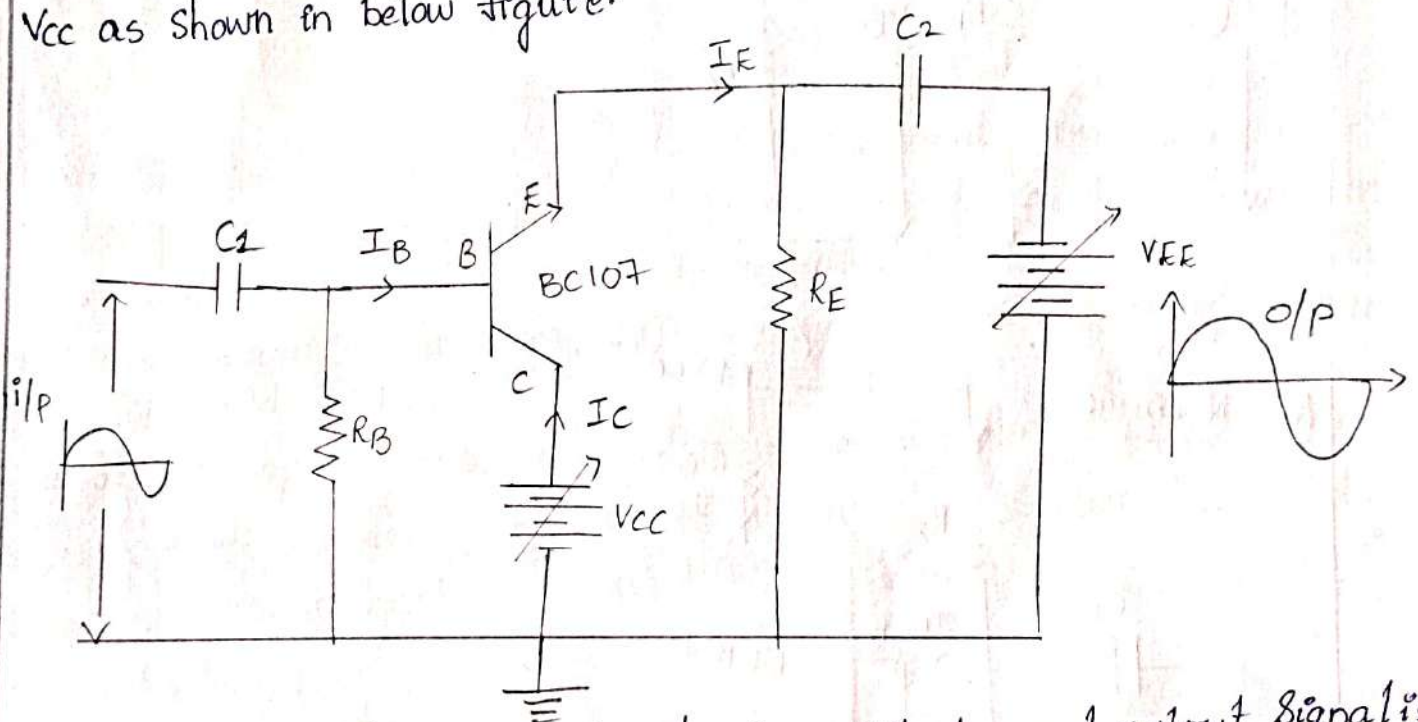
2M * In CE Amplifier, the positive input signal is converted into a negative output signal with 180° phase shift.

Characteristics of CE Amplifier:

- 1) Large current gain: (A_I)
- 2) Large Voltage gain: (A_V)
- 3) Large power gain: (A_P) $A_P = A_V \times A_I$
- 4) Voltage phase shift with 180° degrees
- 5) Modulate Input Impedance
- 6) Modulate Output Impedance.

Common Collector Amplifier:

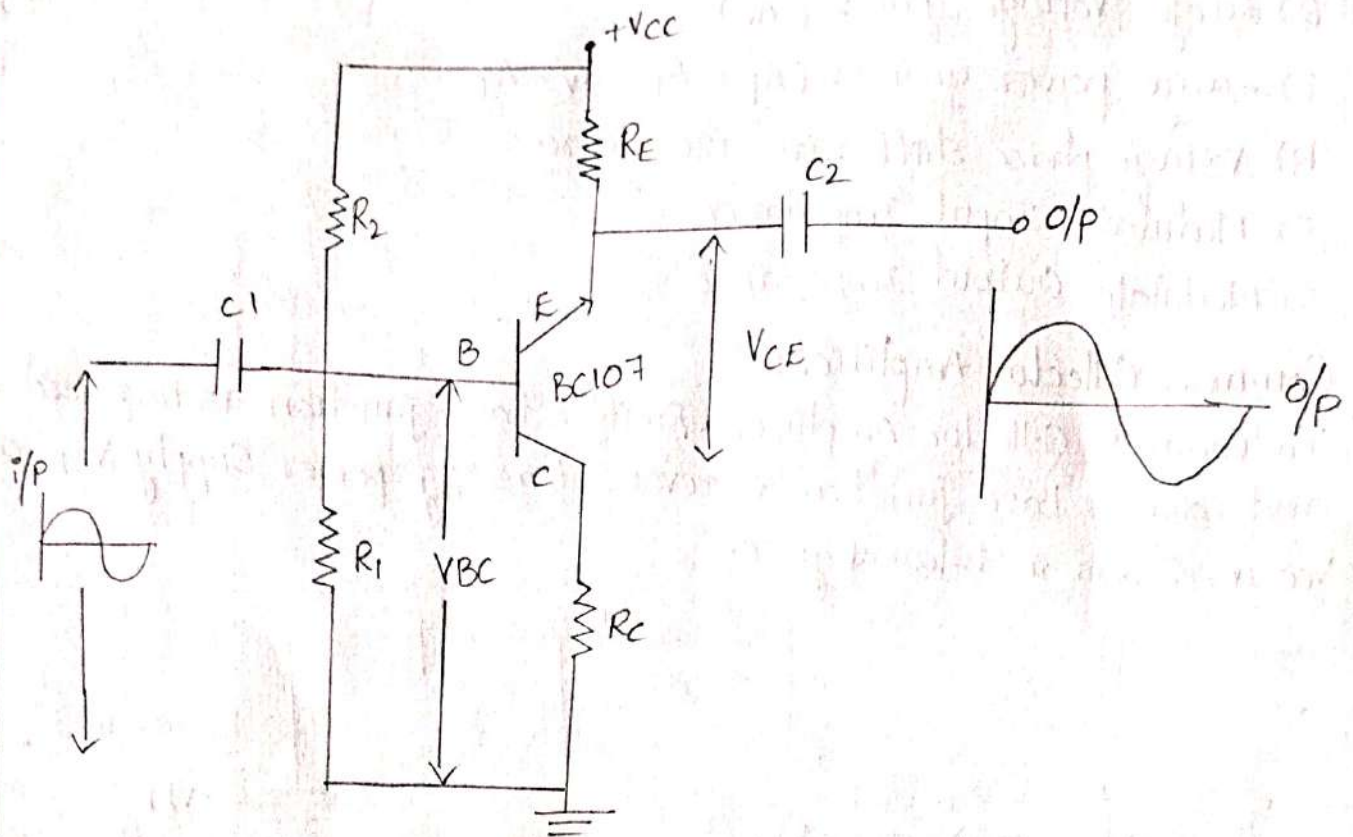
In Common Collector Amplifier Emitter base junction is Forward bias and Collector base junction is reverse bias by power Supply V_{EE} and V_{CC} as shown in below figure.



Here input Signal is given to the base Collector and output Signal is taken from Emitter collector.

*The Capacitors C_1 and C_2 act as Coupling Capacitors for isolation instead of using two power supplies the required bias Condition in a CC Amplifier with Single power Supply (V_{CC}) as shown in below figure.

Theoretical Circuit:



Partial circuit:

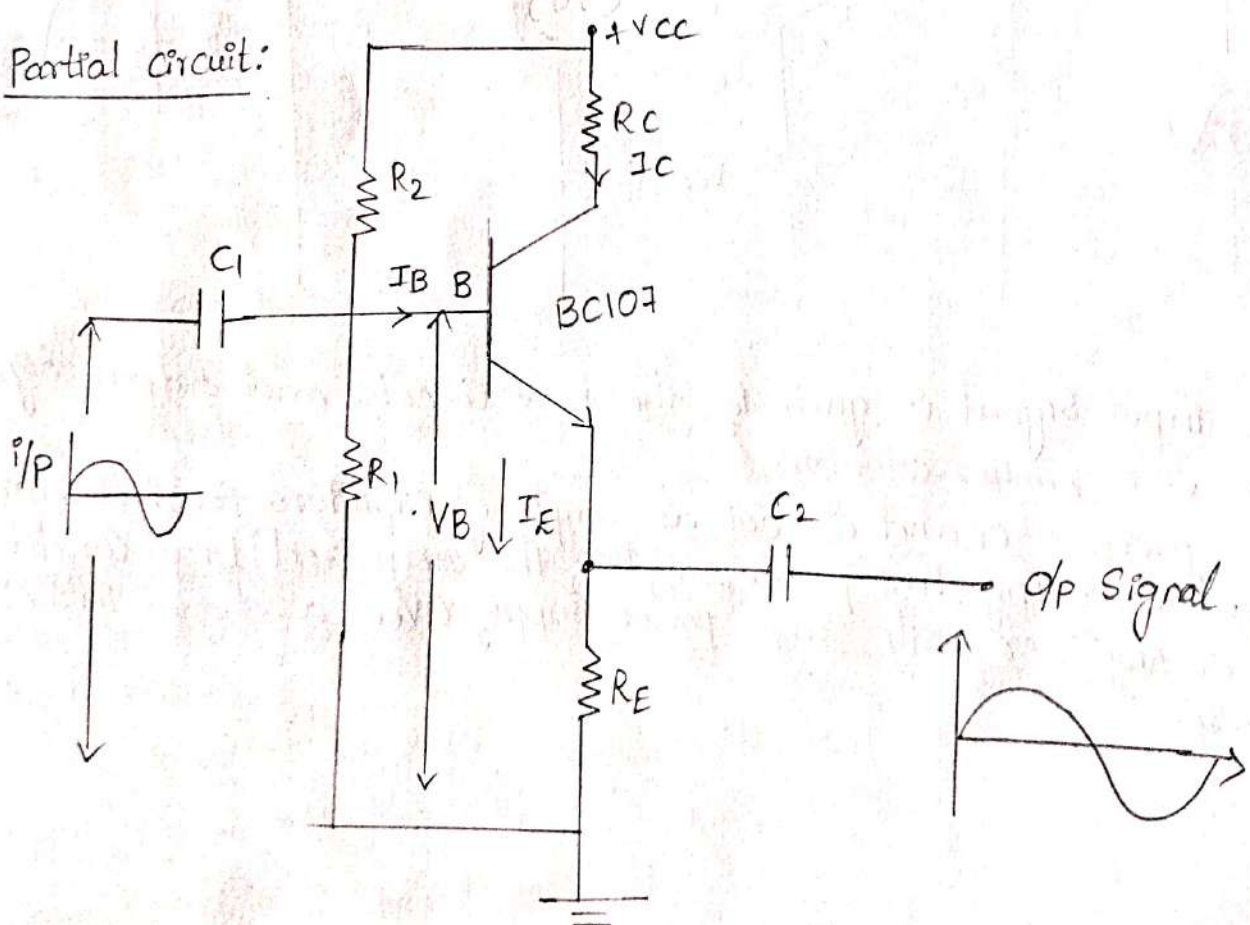
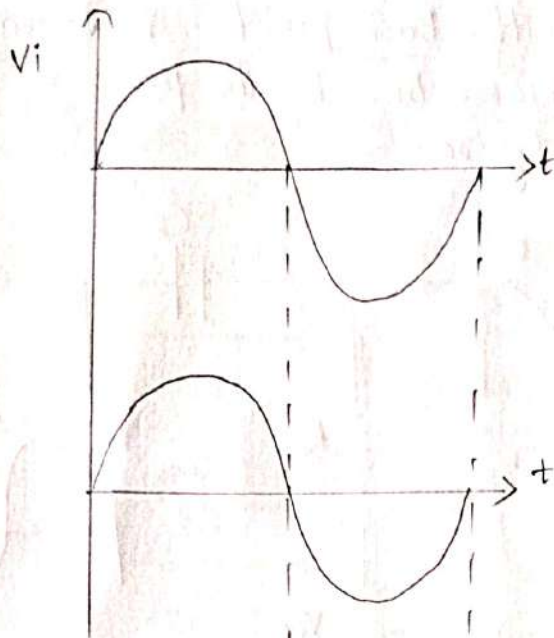


fig: CC Amplifier with Single power Supply

Input output Waveforms:



from fig

$$V_0 = I_E R_E \rightarrow (1)$$

$$V_0 = \beta I_B R_E \rightarrow (2)$$

* When Sinusoidal AC Signal is applied at the input terminal of the Circuit during the positive half cycle is forward bias then the Emitter Bias junction voltage is increased resultant the base Current is also increased. from the equations (1) and (2) the Emitter Current ' I_E ' also increased with ' β ' times

* Hence CC Amplifier input and output waveforms are in phase (same angle)

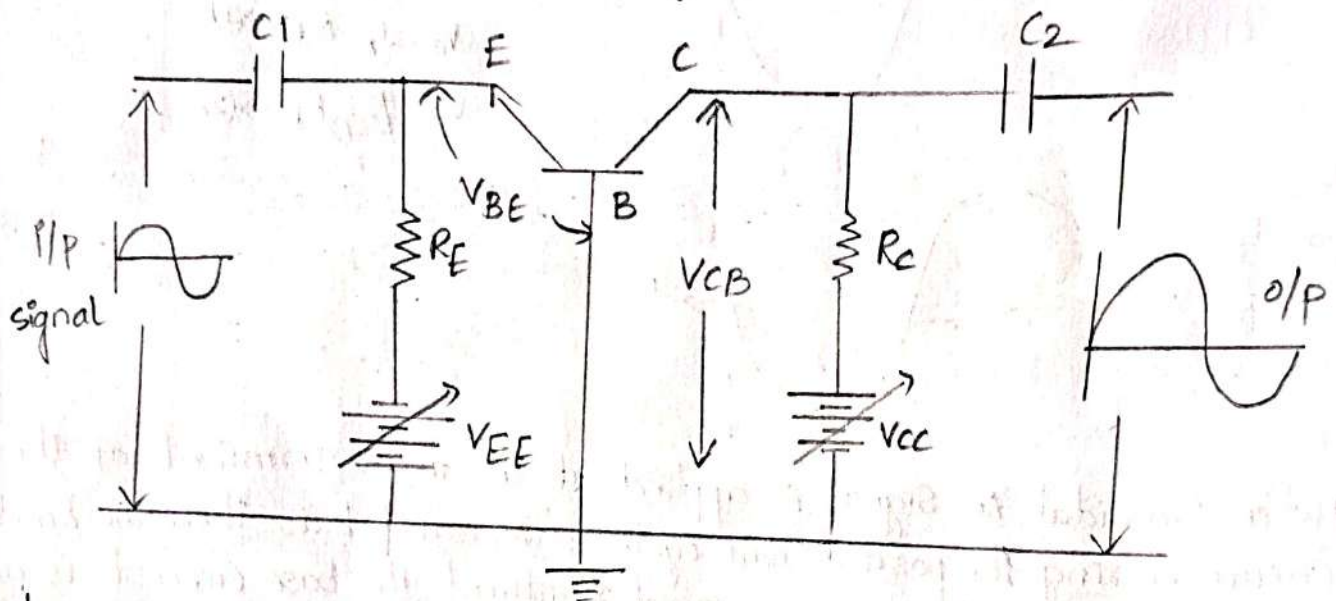
2M * In CC Amplifier the output Signal is taken at Emitter terminal by follows the input signal So CC Amplifier is called as "Emitter follower".

Characteristics :

- 1) High Current gain
- 2) Voltage Current gain approximately equal to 1
- 3) power gain approximately equals to 1
- 4) large input Impedance
- 5) Small Output Impedance.

Common Base Amplifier:

In Common Base Amplifier Emitter Base junction is forward bias and Collector base Junction is Reverse base by the power Supplies V_{EE} and V_{CC} as shown in below figure.



In Common Base amplifier input signal is applied to Emitter Base Output is taken from Collector Base

- * The output voltage $V_o = V_{CC} - I_C R_C$
- * When a sinusoidal waveform applied at the input during positive half cycle of the forward bias resultant the base current is decreased

Characteristics:

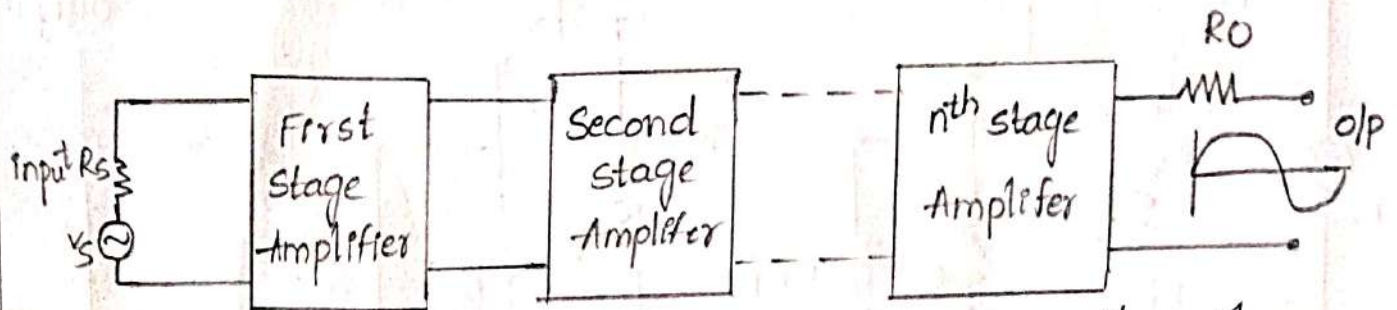
- 1) Current gain is less than 1
- 2) High Voltage gain
- 3) power gain is approximately equals to voltage gain
- 4) Small input impedance
- 5) large output impedance.

Multistage Amplifiers: (or) Cascading

The gain of the single stage amplifier is insufficient for some applications like T.V Receivers, Communication Receivers etc it requires Number of amplification stages may be two (or) more. to

- * To increase the gain by the output of each amplifier stage is coupled into the input of the next stage.

2M * A Amplifier circuit Containing more than the one stage of Mult Amplification is known as Multistage Amplifier it is also called as Cascading Amplifier. In Multistage Amplifier, Single stage Amplifiers are Connected in Cascade Arrangement.



In Multistage Amplifier one stage is Connected to another stage by the Coupling devices^{Ex:} Resistors, Capacitors and Transformers.

* Multistage Amplifier are can be classified into two types

- 1) Cascade Multistage Amplifier
- 2) Cascode Multistage Amplifier.

2M * which Multistage Amplifier ~~is~~ having Same Configuration (CE) in each stage is called as Cascade Amplifier (or) Two or more stages of Common Emitter Amplifier is called as Cascade Amplifier.

2M * A Cascode Amplifier is two stage Amplifier that Amplifier, Common Emitter followed by the Common Base Amplifier.

1) Cascade Multistage Amplifier: (or) Two stage RC-coupled Amplifier:

In two stage RC Coupled Amplifier. having two Single stage Amplifiers, these amplifiers are coupled by the Capacitor and Resistor. Since coupling from one stage to another stage is achieved by Coupling Capacitor along with shunt resistor that why these amplifier is called RC Coupled Amplifier. In general the input impedance of first stage must be high and output impedance of last stage must be low the below figure shows the two stage RC Coupled Amplifier.

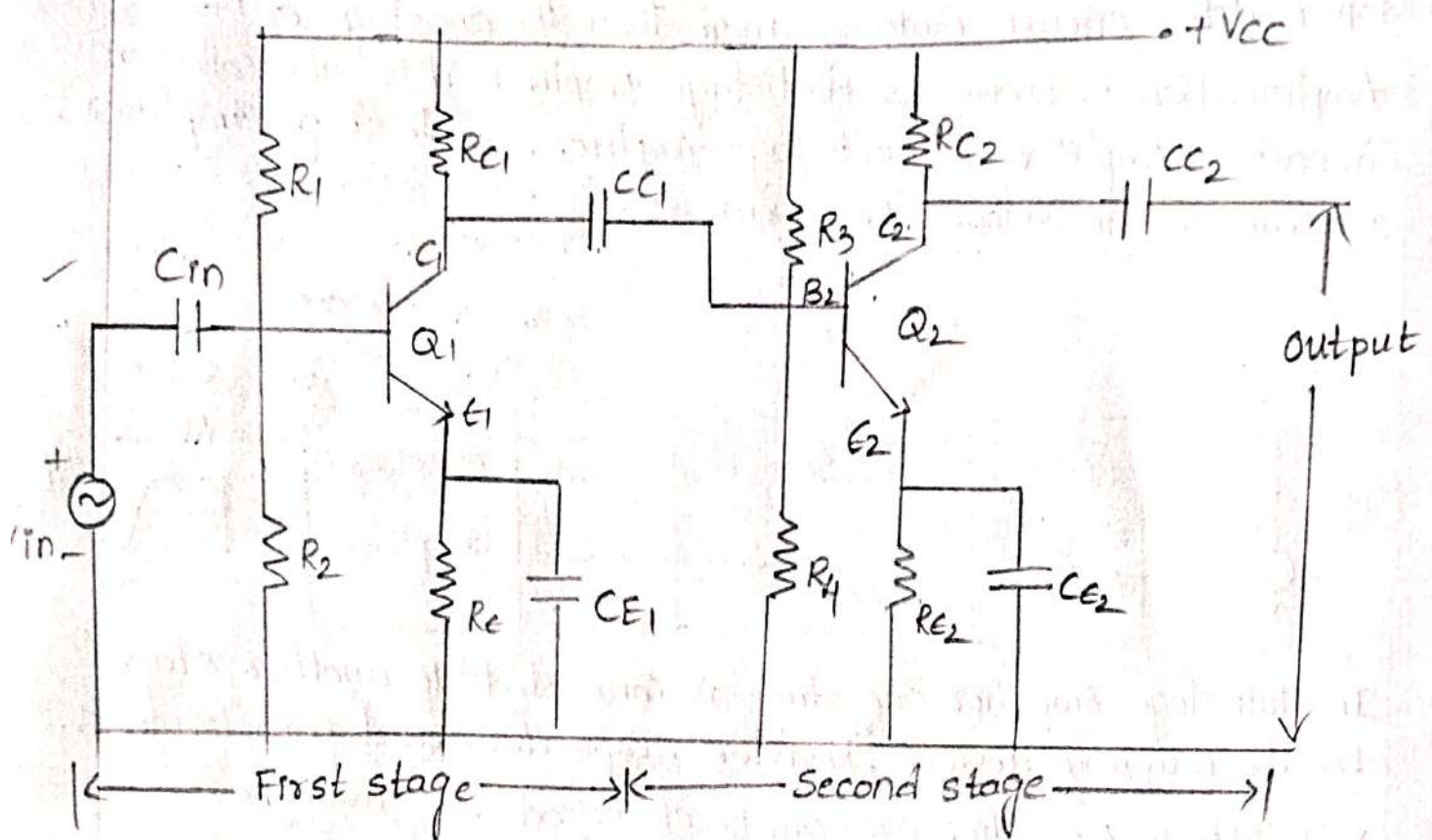


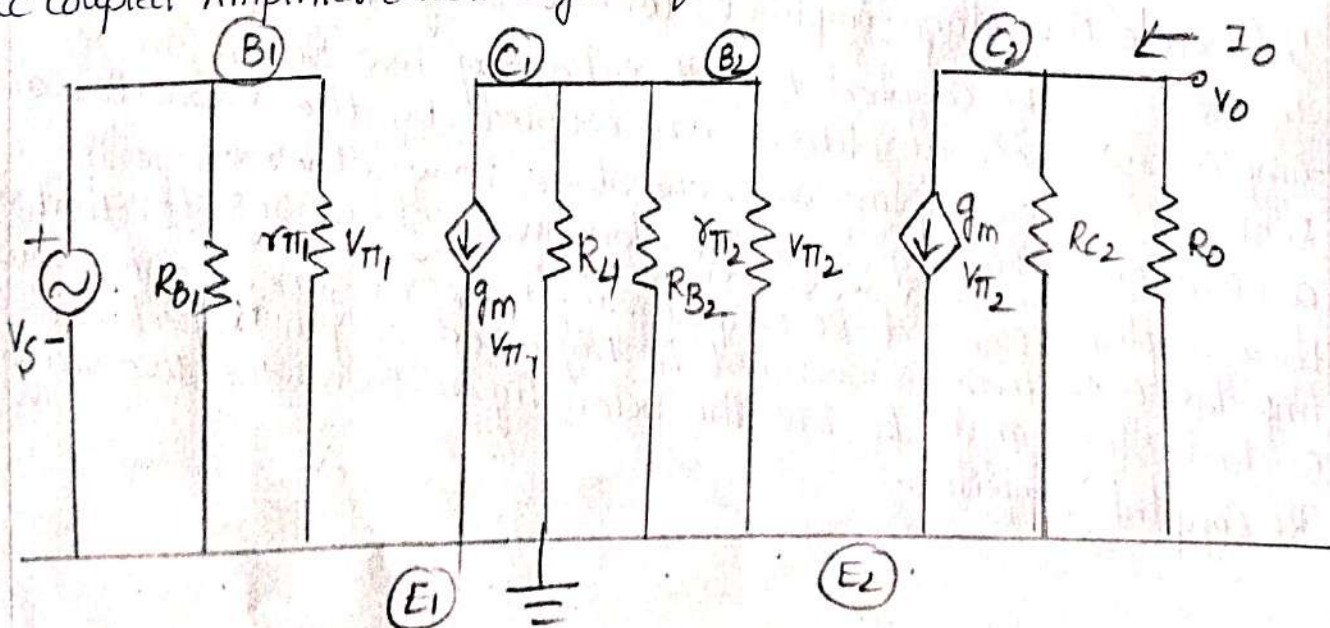
Fig: Two stage RC Coupled Amplifier

* The R_E Resistor R_1 and R_2 form the self bias and R_E from stabilization Resistor

Network

* The Emitter bypass Capacitor (C_E) offers low reactant path to the Signal.

* The below figure shows the equivalent circuit diagram for two stage RC Coupled Amplifier (Small Signal equivalent circuit)

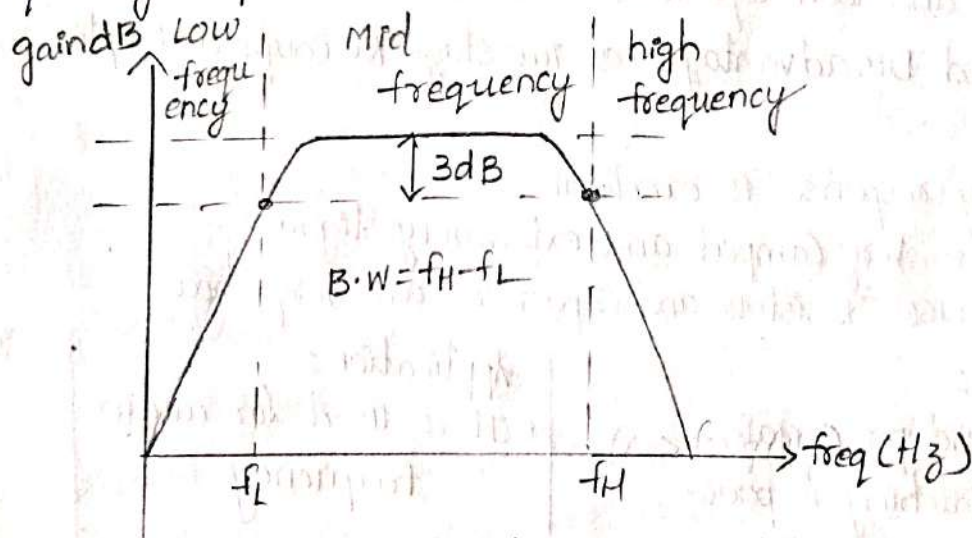


- When the input voltage V_i applied to the base terminal of first transistor through C_{in} , it appears in the amplified form across its collector load R_C
- The output of first stage is given to the base of the next stage through Coupling Capacitor C_C
- The output of Second stage taken out to the Coupling Capacitor through C_{C2}
- The Overall gain of Amplification is equals to the product of the individual stage gains.

$$\boxed{\text{Total gain} = \text{first stage gain} \times \text{Second stage gain}}$$

✓ The below figure shows the frequency Response of two stage RC Coupled Amplifier.

- The graph between gain in dB and frequency in Hz is called as frequency Response



- The frequency Response has three Regions

- $\Rightarrow$ low frequency Range ($< 50 \text{ Hz}$)
- $\Rightarrow$ Med frequency Range ($50 \text{ Hz} - 20 \text{ KHz}$)
- $\Rightarrow$ high frequency Range [$> 20 \text{ KHz}$]

Low frequency Range: ($< 50 \text{ Hz}$)

The frequency is inversely proportional to the Capacitance and Reactance

$$\text{i.e. } X_C = \frac{1}{2\pi f R_C}$$

- In these frequency Range the Circuit behaves like an Simple bypass Circuit which allows only high low frequency.

In these region coupling and bias capacitors must be included in the equivalent circuit.

2) Mid frequency Range (50Hz - 20kHz):

In these Range of frequencies, voltage gain of Amplifier is Constant

* These is due to the reactants of the Coupling Capacitor will be very Small that it can neglected

* In these range transistor and Capacitors are treated as open circuit.

3) High Frequency Range ($> 20\text{kHz}$):

Above the Mid frequency Range is called as High frequency Range.

• As the frequency of input signal increases the gain of the Amplifier is decreases.

• In this region coupling and bypass capacitors treated as short circuits

• The Transistor and load Capacitance Must be included in equivalent circuit.

Advantages and Disadvantages of Two stage RC Coupled Amplifier:

Advantages:

* The frequency response is excellent

* These circuit is very compact and extremely light

* low Cost Because Resistors and Capacitors are very cheap

Disadvantages:

* low voltage and power gain

* Impedance Matching is poor.

Application:

* It is used for audio frequency

Coupling Schemes in Amplifier:

When Amplifiers are cascaded is necessary to use a Coupling Networks between the Output of one Amplifier and input of following Amplifier.

• Basically the Coupling Network follows the two purposes

i) It transfers AC output of one stage to the input of Next stage

ii) It isolates the DC condition of one stage to Next stage

The following Coupling Schemes are commonly used in Multistage Amplifier

⇒

⇒ RC Coupling

⇒ Transformer Coupling

⇒ Direct Coupling.

Transformer Coupling:

Due to Some disadvantages in RC Coupled Amplifier that is low voltage and power gain and poor impedance Matching. these drawbacks are overcome by using transformer Coupled Amplifier. The Below figure shows the two stage transformer Coupled Amplifier.

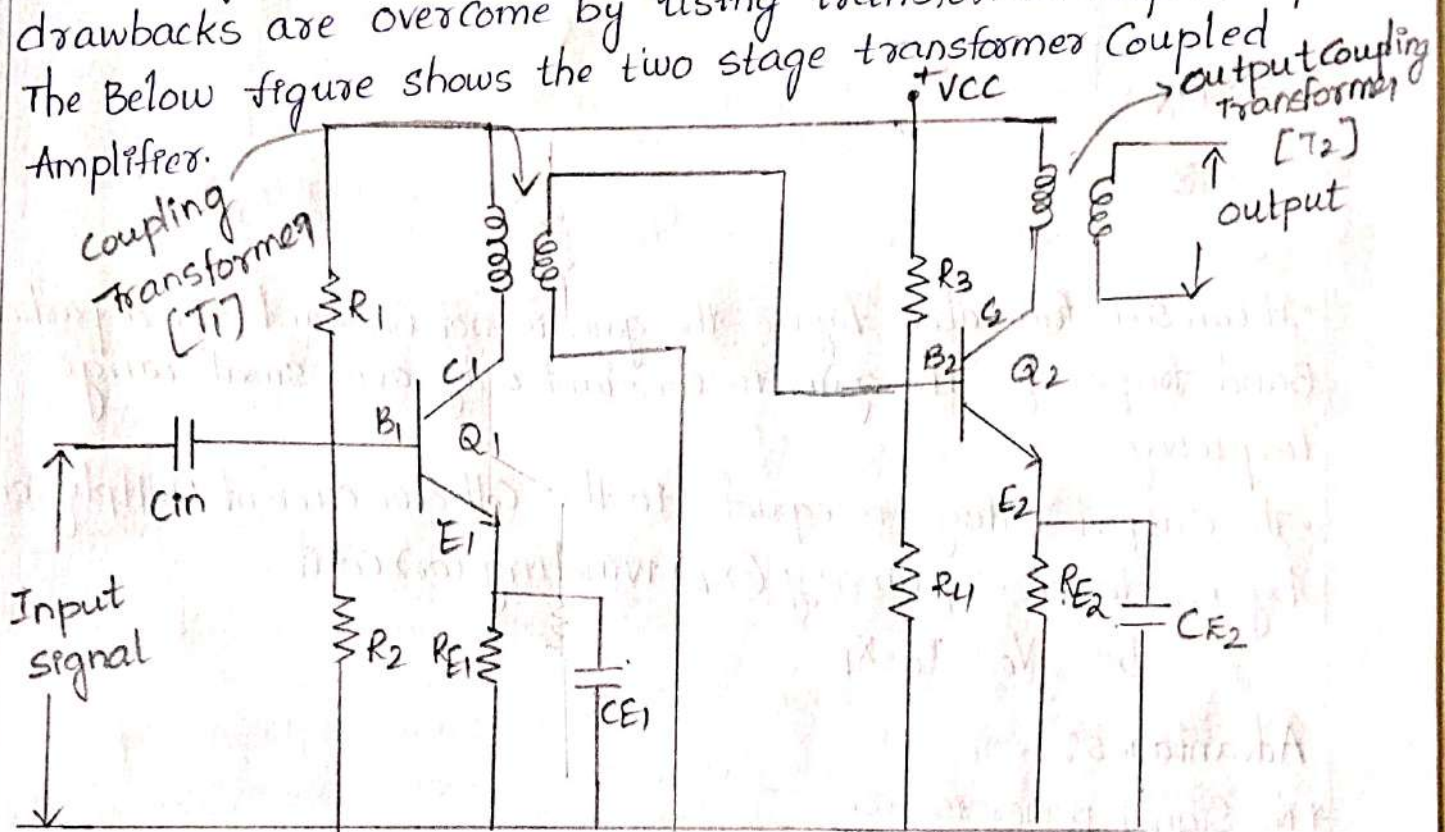
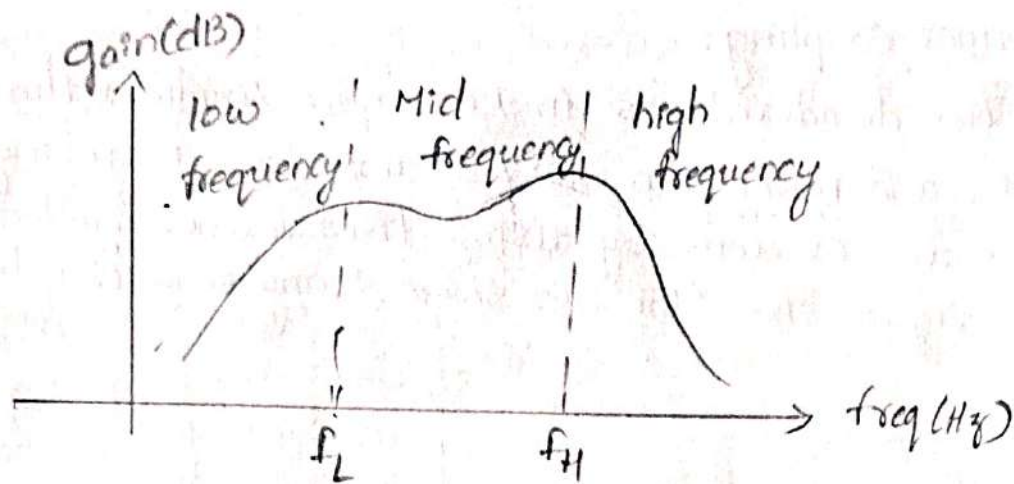


fig: Transformer Coupling Amplifier

- In these Circuit the primary of transformer is placed instead of R_C the Secondary of transformer replaces a wire between the Voltage divider Network and base of the Second stage
- The purpose the input Capacitor C_{in} is couple the AC input Signal to the Base of the first stage and also it blocks the DC Signals.
- The transformer is efficient in providing the DC isolation the biasing of Second stage not disturbed.
- In these methode the primary binding of transformer act as (used as) to collect the Output from Collector terminal and Secondary winding of transformer directly Connected to the Next stage of the base terminal
- In a transformer Coupled Amplifier of the Overall gain of the two Stage transformer Coupled Amplifier is increased the below figure Shows the frequency Response of two stage transformer Coupled Amplifier.



• It can be seen from the above figure that the gain is not constant for a particular band frequency. The gain is constant only over a small range of frequency.

• The output voltage is equal to the collector current multiplied by the reactance of the primary (X_L) winding (or) coil.
i.e. $V_o = I_c \cdot X_L$

Advantages:

- * No signal power is lost
- * Excellent impedance matching
- * Transformer coupling provides higher gain
- * It provides DC isolation between the first stage and the second stage

Disadvantages:

- * It has poor frequency response
- * Cost is also more

Application:

These are mostly used for impedance matching amplifiers.

Direct Coupled Amplifier:

In a direct coupled amplifier, it is suitable for low frequency applications.

• The two-stage direct coupled amplifier is used to amplify less than 10 Hz signals.

• The below figure shows the two-stage direct coupled amplifier.

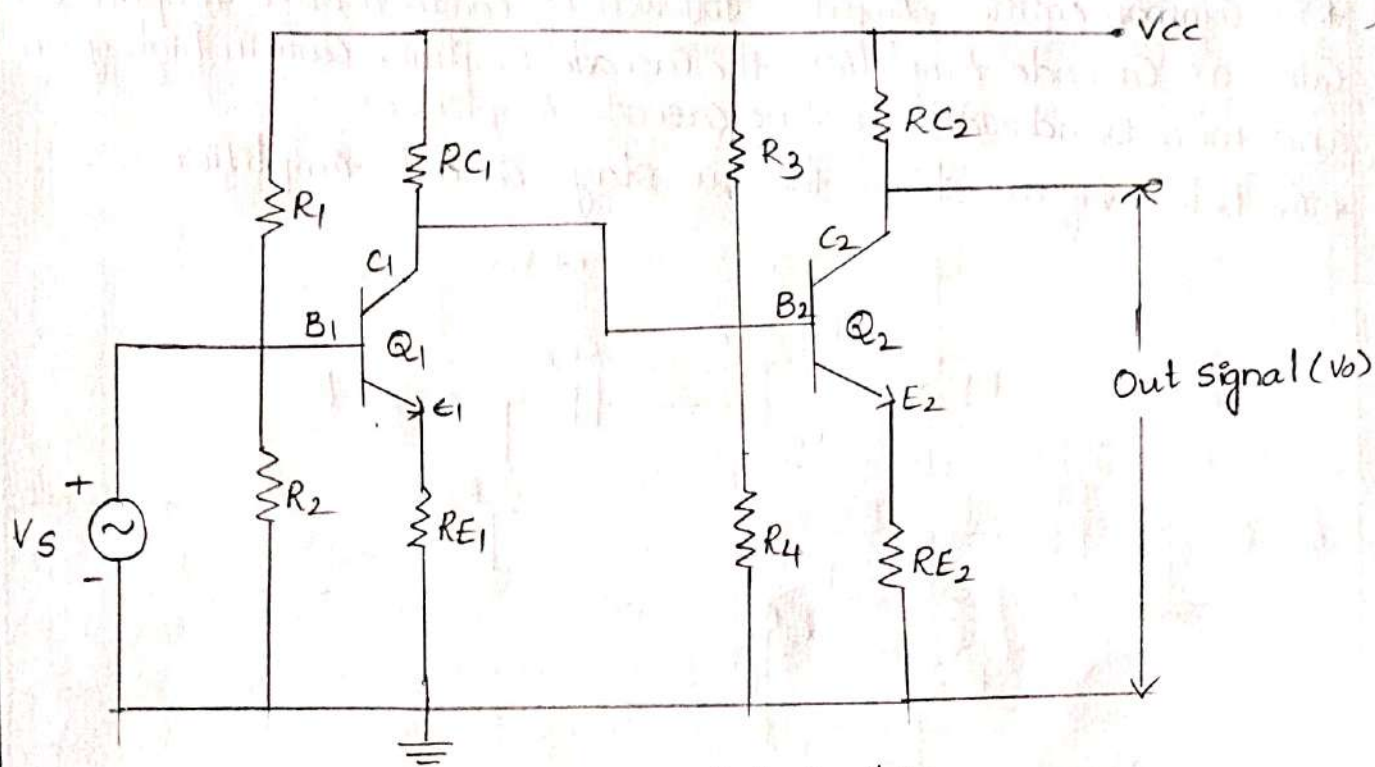


fig: Two-stage Direct Coupled Amplifier.

The main input is connected to first stage of the base terminal without capacitance (low frequency) and output of first stage taken from collector terminal and it is directly connected to the two stage of the base terminal without coupling capacitance.

• Finally the Output is collected from second stage transistor of collector terminal in this way direct coupled amplifier raises the strength of weak signal.

Advantages:

- * The circuit arrangement is simple of minimum use of transistors.
- * The circuit has low cost.

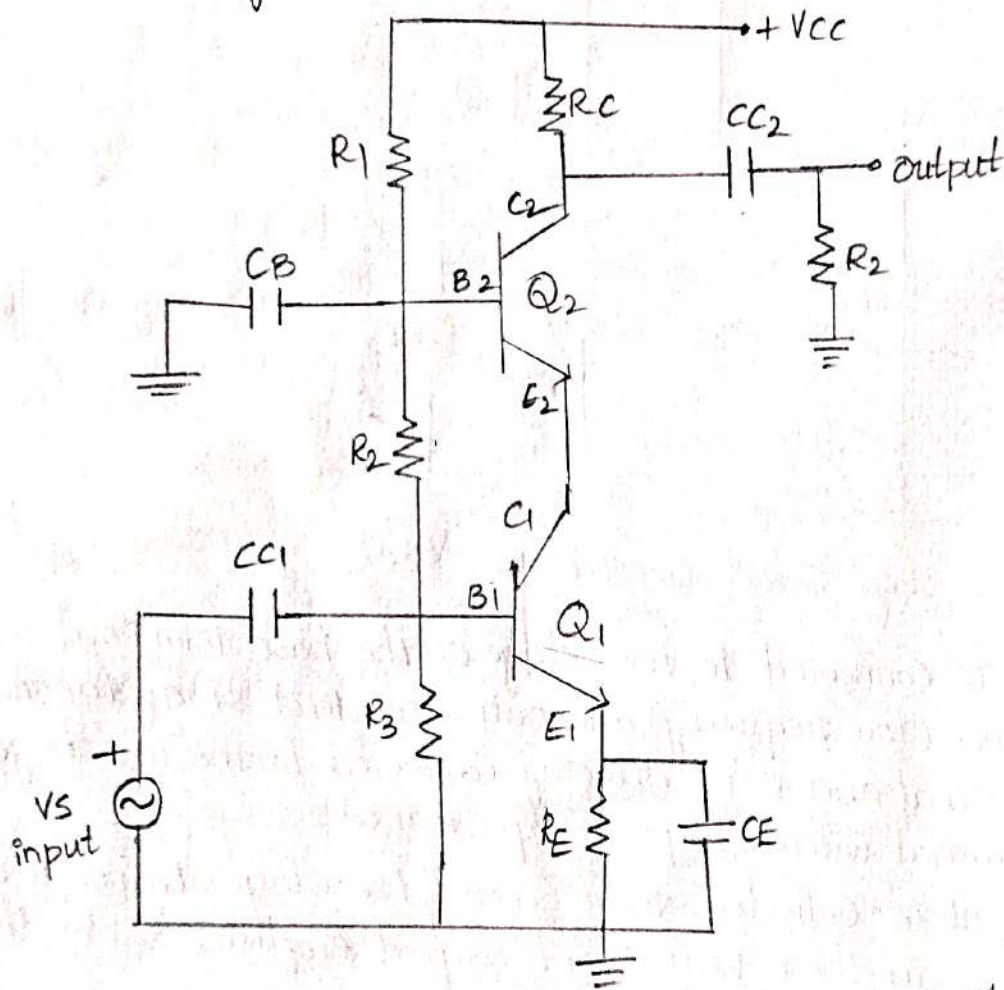
Disadvantages:

- * It can not be used for amplifying high frequency.
- * The operating point is shifted due to temperature variation.

Cascode Amplifier:

Cascode Amplifier is one of the multistage amplifiers and it is a composite amplifier, used for large bandwidth that is radio frequency and video amplifier application.

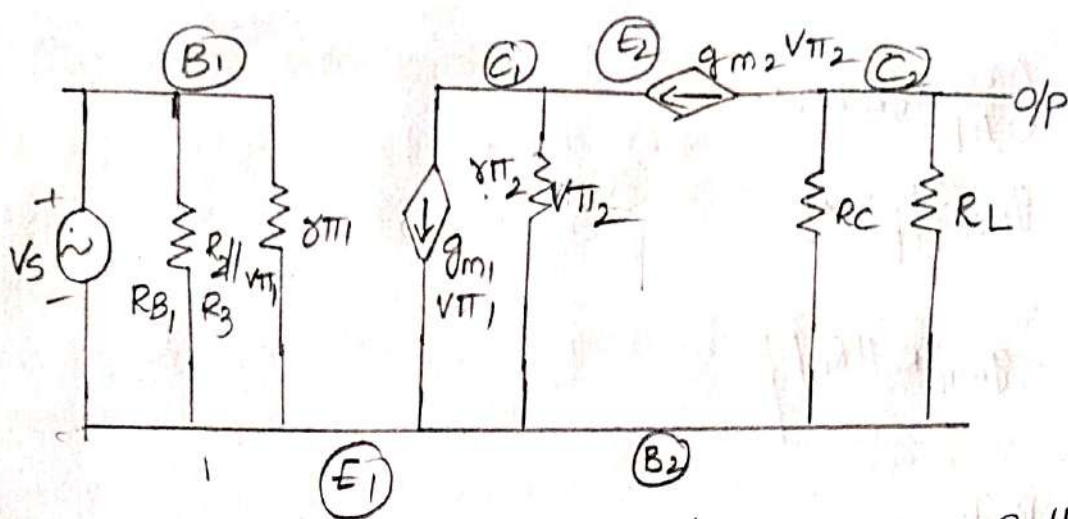
- 2M * The Common emitter Amplifier followed by Common base Amplifier is called as Cascode Amplifier. the Cascode Amplifier contain high gain and more bandwidth (Define Cascode Amplifier)
- * The below figure shows the two stage Cascode Amplifier



In Cascode Amplifier the main input is Connected to CE Amplifier (first stage) of Base terminal Here Emitter is Connected ground and output is taken from Collector terminal.

* The first stage of the output is Connected to CB Amplifier (second stage) of Emitter terminal here Base terminal is Connected to ground final output is taken from Collector terminal

* The below figure shows the small signal equivalent circuit diagram for Cascode Amplifier.



- The Base Bias Resistance of Amplifier is $R_{B1} = R_2 \parallel R_3$
- The input Resistance of Amplifier is $R_i = R_{B1} \parallel \beta \pi_1$
- The output Resistance of Amplifier is $R_o = R_c$
- The voltage gain of Amplifier is $A_v = \frac{V_o}{V_s} \rightarrow (1)$
- The Current gain of Amplifier is $A_i = \frac{I_o}{I_s} \rightarrow (2)$

Voltage gain:

from the fig the output voltage.

$$V_o = -g_{m2} V_{\pi 2} [R_c \parallel R_L] \rightarrow (3)$$

Apply KCL equation at (E_2)

$$g_{m1} V_{\pi 1} = \frac{V_{\pi 2}}{\beta \pi_2} + g_{m2} V_{\pi 2} \quad (\text{here } V_{\pi 1} = V_s)$$

then

$$V_{\pi 2} = g_{m1} V_{\pi 1} \beta \pi_2 - g_{m2} V_{\pi 2} \beta \pi_2$$

$$V_{\pi 2} + g_{m2} V_{\pi 2} \beta \pi_2 = g_{m1} V_{\pi 1} \beta \pi_2$$

$$V_{\pi 2} [1 + g_{m2} \beta \pi_2] = g_{m1} V_{\pi 1} \beta \pi_2$$

$$V_{\pi 2} = \frac{g_{m1} V_{\pi 1} \beta \pi_2}{1 + g_{m2} \beta \pi_2}$$

$$\text{here } \boxed{V_{\pi 1} = V_s} \quad \& \quad \boxed{g_{m2} \beta \pi_2 = \beta_2}$$

then

$$V_{\pi 2} = \left(\frac{\beta \pi_2}{1 + \beta_2} \right) g_{m1} V_s \rightarrow (4)$$

Sub Eq (4) in eq (3) we get

$$V_o = -g_{m1} g_{m2} \left[\frac{\beta \pi_2}{1 + \beta_2} \right] V_s (R_c \parallel R_L)$$

$$\frac{V_o}{V_s} = -g_{m1} g_{m2} \left(\frac{v_{\pi 2}}{1+\beta} \right) (R_c \parallel R_L)$$

here the term $g_{m2} \left(\frac{v_{\pi 2}}{1+\beta} \right) \approx 1$

then

$$\boxed{A_v = \frac{V_o}{V_s} = -g_{m1} [R_c \parallel R_L]}$$

Current gain $[A_I]$:

The output current

$$I_o = -g_{m2} v_{\pi 2} \left[\frac{R_c}{R_c + R_L} \right] \rightarrow (5)$$

W.K.T

$$v_{\pi 2} = \frac{v_{\pi 2}}{1+\beta_2} g_{m1} V_s \rightarrow (6)$$

Sub eq (6) in eq (5)

then

$$I_o = -g_m \left[\frac{R_c}{R_c + R_L} \right] \left[\frac{v_{\pi 2}}{1+\beta_2} \right] g_{m1} V_s \rightarrow (7)$$

actually

$$V_s = I_s R_i \rightarrow (8)$$

Sub eq (8) in eq (7)

then

$$I_o = -g_{m2} \left[\frac{R_c}{R_c + R_L} \right] \left(\frac{v_{\pi 2}}{1+\beta_2} \right) g_{m1} I_s R_i$$

from the above equation

$$\frac{I_o}{I_s} = -g_{m2} \left[\frac{R_c}{R_c + R_L} \right] \left[\frac{v_{\pi 2}}{1+\beta_2} \right] g_{m1} R_i$$

here the term $g_{m2} \left[\frac{v_{\pi 2}}{1+\beta_2} \right] \approx 1$

then

$$A_I = \frac{I_o}{I_s} = -g_{m1} \left[\frac{R_c}{R_c + R_L} \right] R_i$$

IMP Darlington pair Amplifier: Part - B

Darlington pair Amplifier Consists of two individual bipolar NPN and PNP transistor Connected together which acts like a Single transistor

- * A Darling pair Amplifier invented at "BELL" by the engineer "DARLINGTON" in 1953
- * In these two transistors, the emitter follower output is Connected to input of the next emitter follower
- * The main Advantage of Darlington pair is Composite transistor act as a Single transistor with high current gain.
- * The below figure shows the darlington pair Amplifier.

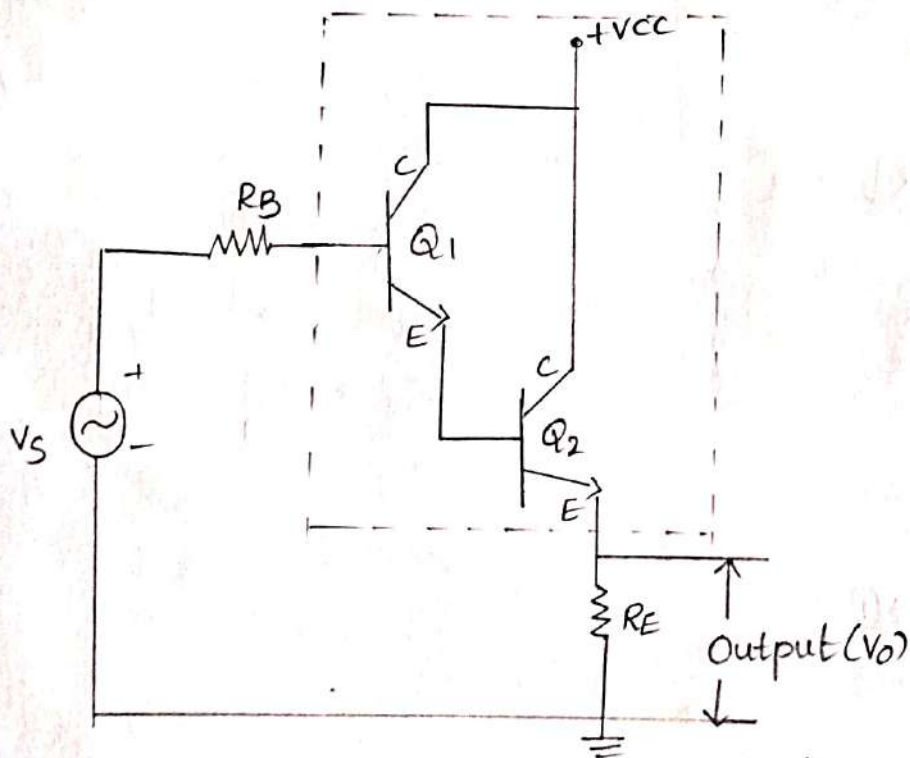


fig: Darlington pair Amplifier

- * The Darlington pair made up with two transistors of current gain β_1 & β_2
- * A very popular Connection two BJTs for operation as One Super-Beta Beta transistor
- * The darlington pair provides the product of individual current gains (β_1, β_2)

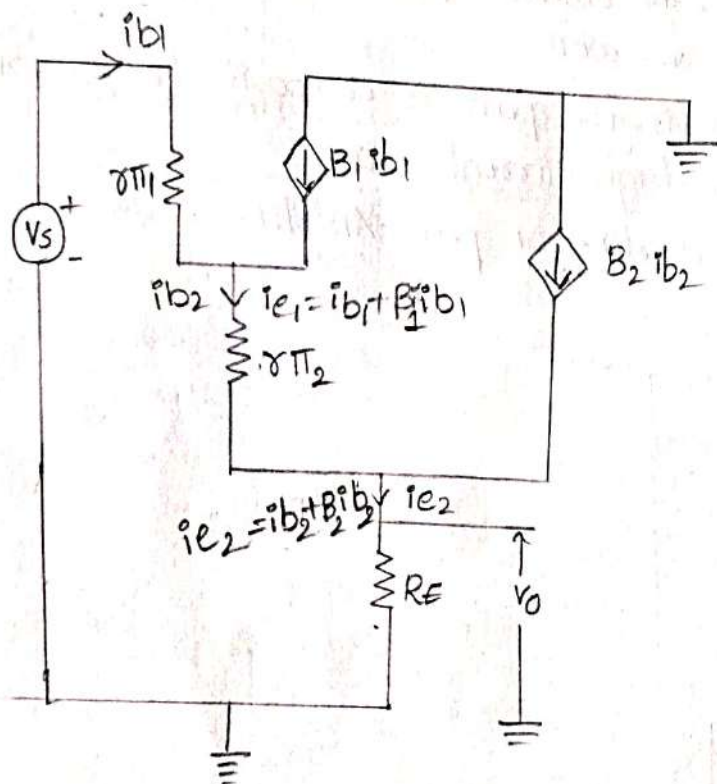
$$i.e \beta_D = \beta_1 \cdot \beta_2$$

if the transistors are matched such that $\beta_1 = \beta_2 = \beta$ then $\beta_D = \beta^2$

The Collectors of both transistors are Connected together

Power Supply $+V_{CC}$

The below figure shows the small signal equivalent model for Darlington pair Amplifier.



$$i_{e1} = i_{b2} = i_{b1} + \beta_1 i_{b1}$$

$$i_{e1} = i_{b2} = i_{b1} [1 + \beta_1] \rightarrow (1)$$

and

$$i_{e2} = i_{b2} + \beta_2 i_{b2}$$

$$i_{e2} = i_{b2} [1 + \beta_2] \rightarrow (2)$$

Substitute eq (1) in eq (2), we get

$$i_{e2} = i_{b1} [1 + \beta_1] [1 + \beta_2] \rightarrow (3)$$

the Current Gain

$$A_I = \frac{i_{e2}}{i_{b1}} = \frac{i_{b1} [1 + \beta_1] [1 + \beta_2]}{i_{b1}}$$

$$A_I = (1 + \beta_1) (1 + \beta_2)$$

here the gain $\beta_1, \beta_2 \gg 1$

$$A_I = \beta_1 \cdot \beta_2$$

if the transistors are identical then $\beta_1 = \beta_2 = \beta$

$$A_I = \beta_1^2 = \beta_2^2 = \beta^2$$

$$\boxed{A_I = \beta^2}$$

Voltage gain:

$$A_V = \frac{V_o}{V_s} = \frac{i_{e2} R_E}{V_s}$$

$$= \frac{i_{b1} [1 + \beta_1] [1 + \beta_2] R_E}{V_s} \rightarrow (4)$$

Apply KVL at input loop

$$V_s = i_{b1} r_{\pi 1} + i_{b2} r_{\pi 2} + i_{e2} R_E \rightarrow (5)$$

Substitute eq's (1), (2) & (3) in eq (5)

$$V_s = i_{b1} r_{\pi 1} + i_{b1} [1 + \beta_1] r_{\pi 2} + i_{b1} [1 + \beta_1] [1 + \beta_2] R_E$$

$$V_s = i_{b1} [r_{\pi 1} + [1 + \beta_1] r_{\pi 2} + [1 + \beta_1] [1 + \beta_2] R_E]$$

here $\beta_1, \beta_2 \gg 1$

$$V_s = i_{b1} [r_{\pi 1} + \beta_1 r_{\pi 2} + \beta_1 \beta_2 R_E]$$

here $r_{\pi 1} \ll \beta_1 r_{\pi 2}$

$$\text{and } r_{\pi 2} = \frac{\beta_2}{g_m}$$

then

$$V_s = i_{b1} \left[\beta_1 \frac{\beta_2}{g_m} + \beta_1 \beta_2 R_E \right]$$

$$= i_b \left[\frac{\beta_D}{g_m} + \beta_D R_E \right]$$

$$V_s = i_b \beta_D \left[\frac{1}{g_m} + R_E \right] \rightarrow (6)$$

Sub eq (6) in eq (4)

$$A_V = \frac{i_{b1} [1 + \beta_1] [1 + \beta_2] R_E}{i_{b1} \beta_D \left[\frac{1}{g_m} + R_E \right]}$$

$$= \frac{\beta_1 \beta_2 R_e}{\beta_D \left[\frac{1}{g_m} + R_e \right]}$$

$$= \frac{\beta_D R_e}{\beta_D \left[\frac{1}{g_m} + R_e \right]}$$

$$= \frac{R_e}{\frac{1}{g_m} + R_e}$$

$$A_V = \frac{R_e}{R_e} \quad A_V \approx 1$$

$$\frac{1}{g_m} \ll R_e$$

Input impedance: (z_i)

$$z_i = \frac{V_s}{i_{b1}} = \frac{i_{b1} \beta_D \left[\frac{1}{g_m} + R_e \right]}{i_{b1}}$$

$$z_i = \beta_D \left[\frac{1}{g_m} + R_e \right]$$

Output Impedance: (z_o)

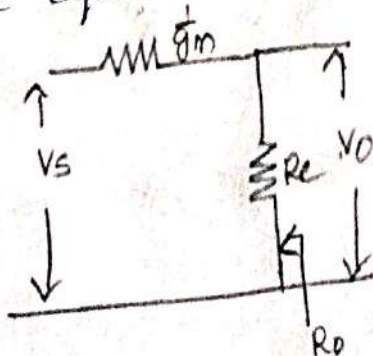
W.K.T

$$A_V = \frac{V_o}{V_s} = \frac{R_e}{\left(\frac{1}{g_m} + R_e \right)}$$

then

$$V_o = \frac{R_e V_s}{\frac{1}{g_m} + R_e}$$

above equation Convert into Circuit.



$$z_o = \frac{1}{g_m} \parallel R_e$$

511 Distortion in Amplifiers:

- The input signal applied to the amplifier is alternating in nature the basic features of any alternating signal are amplitude, frequency and phase.
- The amplifier output should be reproduced faithfully that is there should not be distortion in the amplitude, frequency and phase of the signal.
- Hence these distortions are called as
 - ⇒ Amplitude distortion (Non-linear Distortion)
 - ⇒ phase distortion (delay Distortion)
 - ⇒ frequency Distortion

Non-linear Distortion:

- In the earlier discussion it is assumed that the transistor is linear device.
- The dynamic characteristics transistor is a straight line over the operating range frequency.
- But in partial circuits the dynamic characteristics is not perfectly linear due to such non-linearity in the dynamic characteristics the wave form of the output voltage differs from that of input signal.
- Such Distortion is called as Non-linear Distortion (or) Amplitude (or)

Harmonic Distortion:

Phase Distortion:

- We have seen that delay distortion is a phase shift distortion it results due to unequal phase shifts of signals of different frequencies.

Frequency Distortion:

- These type of distortion raised when the signal components of different frequency are amplified differently.
- These distortions may be caused by the internal ^{device} capacitor or it may be arise because the associated circuit is reactive.
- The graph between the gain and frequency is called frequency response, if these plot is not a horizontal straight line over the range of frequency, then that circuit is said to be exhibits frequency distortion over these range.

IMP Differential pair Amplifier : (or)

BJT Differential Amplifier :

The Differential pair Amplifier is the most widely used building block in Analog integrated Circuit design

- The BJT Differential Amplifier is the basis of Very high Speed logic Circuit family like Emitter Coupled Logic
- The differential Amplifier output voltage is directly proportional to the input voltage i.e. $V_o = A_v[V_1 - V_2]$
- The below figure shows the BJT Differential pair Amplifier with Dual input Balanced output.

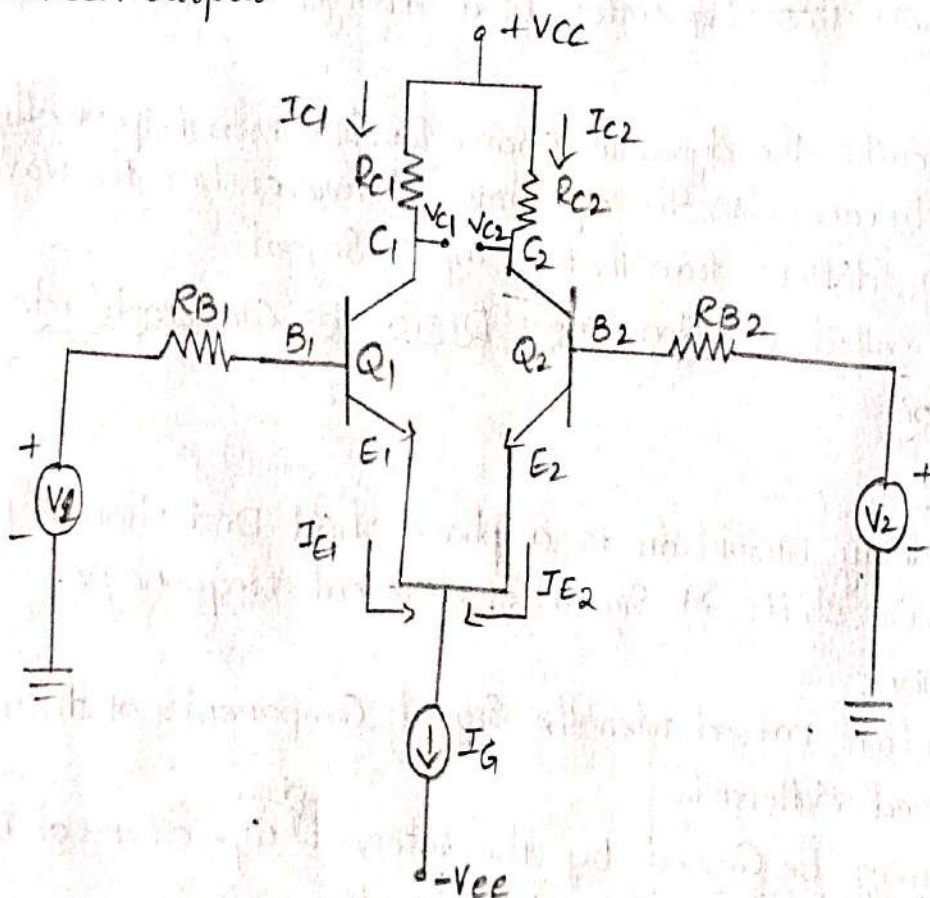


fig : General BJT Differential pair Amplifier

- The above BJT Differential pair Amplifier Consists of two identical transistor i.e. Q_1 and Q_2
- whose Emitters are joined together and biased by a Constant Current Source I_C
- The Collectors are Connected with V_{cc} through R_c
- The BJT Differential pair Amplifier follows the two Cases.

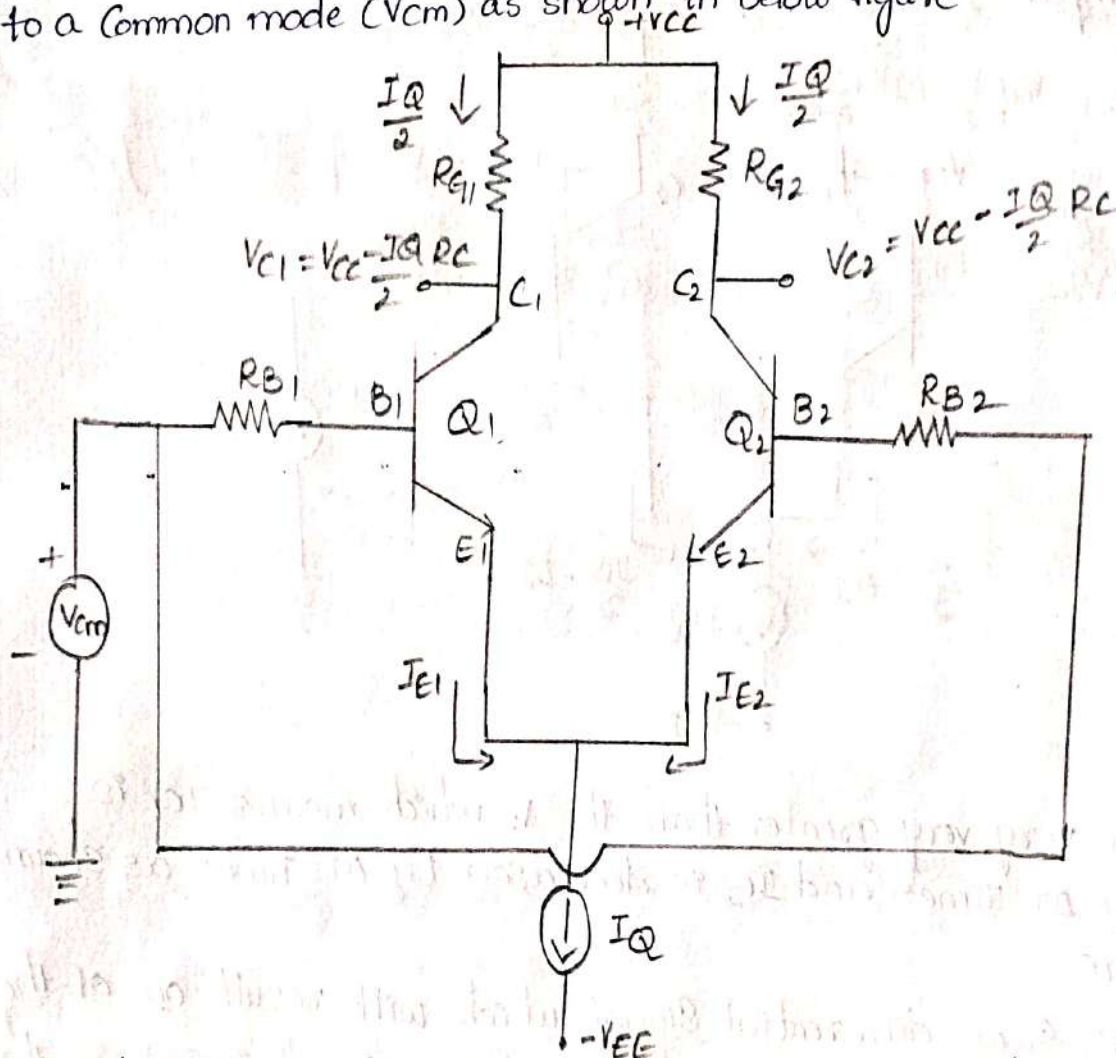
Case i: Common Mode Input Voltage

Case ii: Differential Mode Input Voltage.

Case i: Common Mode Input Voltage:

In Common mode input voltage V_{CM} is average of the individual input Voltages i.e. $V_{CM} = \frac{V_1 + V_2}{2}$

• Let us Consider in these mode the two input Joint together and Connected to a Common mode (V_{CM}) as shown in below figure



• Here the two transistors are matched transistors So the Current I will be divided equally for two transistors i.e. $I_{E1} = I_{E2} = \frac{I_Q}{2}$

and $V_{C1} = V_{C2} = V_{CC} - \frac{I_Q}{2} R_C$

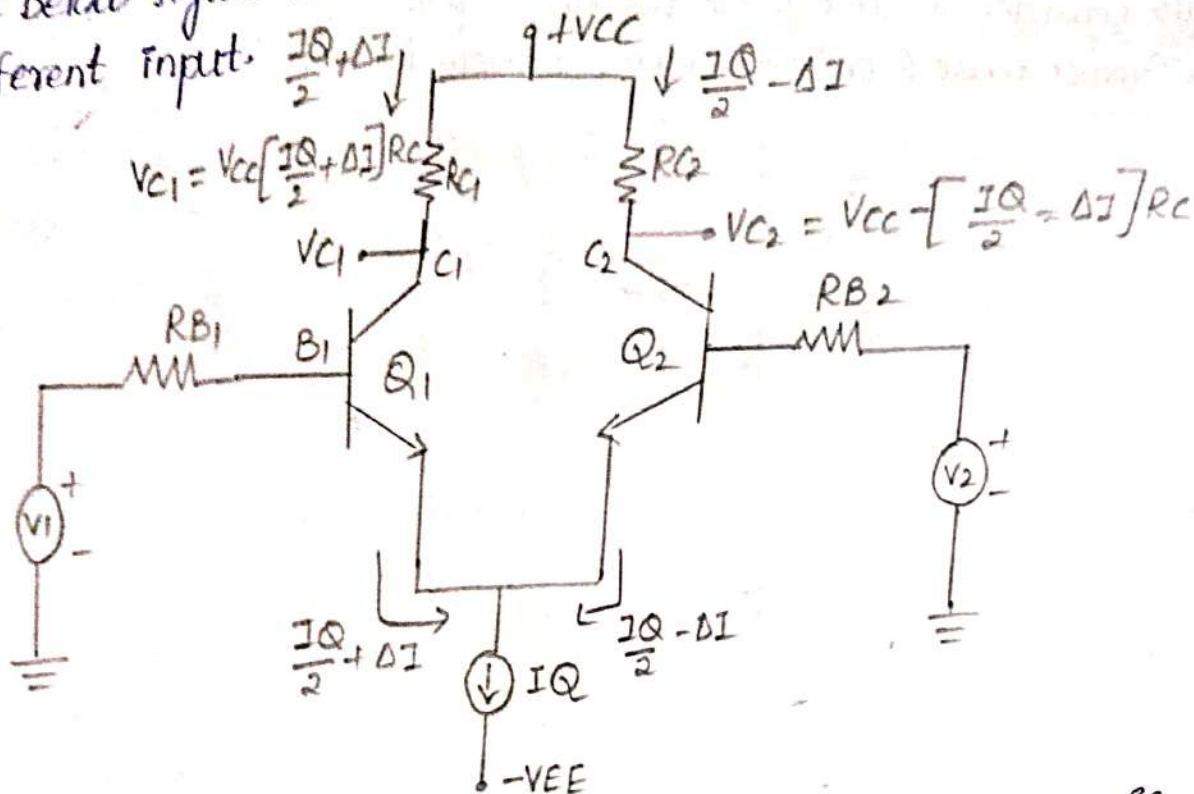
• And the Output voltage $V_O = V_{C1} - V_{C2}$
i.e. $V_O = 0$

• The difference in voltages between the two collectors will be zero
So the differential pair does not respond to (Rejected) the Common mode Input Voltage.

Case (ii) Differential mode input voltage:

In differential mode input voltage the two inputs are different values i.e. V_1 & V_2 like if V_1 increased by ΔI volts and V_2 decreased by same amount.

The below figure shows the differential pair Amplifier with different input.



Here V_1 is very very greater than the V_2 which means I_{C1} is increased by ΔI times and I_{C2} is decreased by ΔI times as shown in above figure.

Apply a very small differential signal which will result one of the transistor conducting a current $(\frac{I_Q}{2} + \Delta I)$ and another side of the transistor conducting a current $(\frac{I_Q}{2} - \Delta I)$.

$$\text{So } V_O = V_{C2} - V_{C1}$$

$$= [V_{CC} - [\frac{I_Q}{2} - \Delta I]RC] - [V_{CC} - [\frac{I_Q}{2} + \Delta I]RC]$$

$$= [-\frac{I_Q}{2} + \Delta I]RC + [\frac{I_Q}{2} + \Delta I]RC$$

$$= -\frac{I_Q}{2}RC + \Delta IRC + \frac{I_Q}{2}RC + \Delta IRC$$

$$V_O = 2\Delta IRC$$

The voltage difference is correlated between V_{C1} and V_{C2} when a differential mode is i/p applied

If the change of the (ΔI) current write in terms of transconductance g_m

$$\Delta I = g_m \left(\frac{V_d}{2} \right)$$

The magnitude of small signal collector current in each transistor is $\frac{g_m V_d}{2}$ then

$$V_o = V_2 - V_1$$

$$= \left[V_{CC} - \left[\frac{I_Q}{2} - g_m \frac{V_d}{2} \right] R_C \right] - \left[V_{CC} - \left[\frac{I_Q}{2} + g_m \frac{V_d}{2} \right] R_C \right]$$

$$= -\frac{I_Q}{2} R_C + g_m \frac{V_d}{2} R_C + \frac{I_Q}{2} R_C + g_m \frac{V_d}{2} R_C$$

$$= 2 g_m \frac{V_d R_C}{2}$$

$$V_o = g_m V_d R_C$$

$$\frac{V_o}{V_d} = g_m R_C$$

$$A_d = g_m R_C$$

V_d = difference of (V_2 and V_1) between i/p voltages

A_d = difference voltage gain

In some cases the output voltage is taken from only one collector which is called as one sided output (or) unbalanced output.

Small Signal Analysis of BJT differential pair Amplifiers.

Let us assume that the transistors are identical

So,

$$\beta_{\pi 1} = \beta_{\pi 2} = \beta_{\pi}$$

and

$$g_{m1} = g_{m2} = g_m$$

Apply KCL at node V_E .

Fig: General differential pair BJT Amplifier

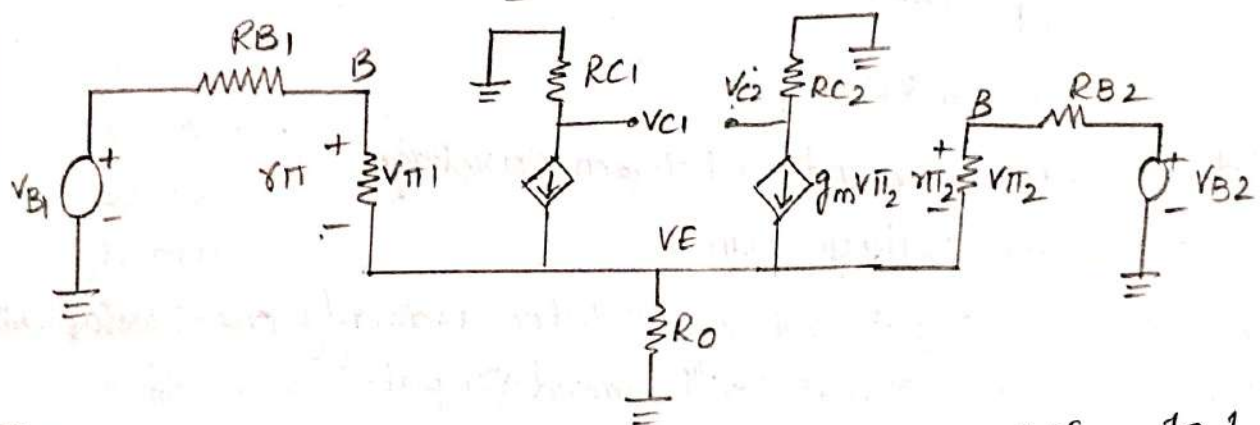
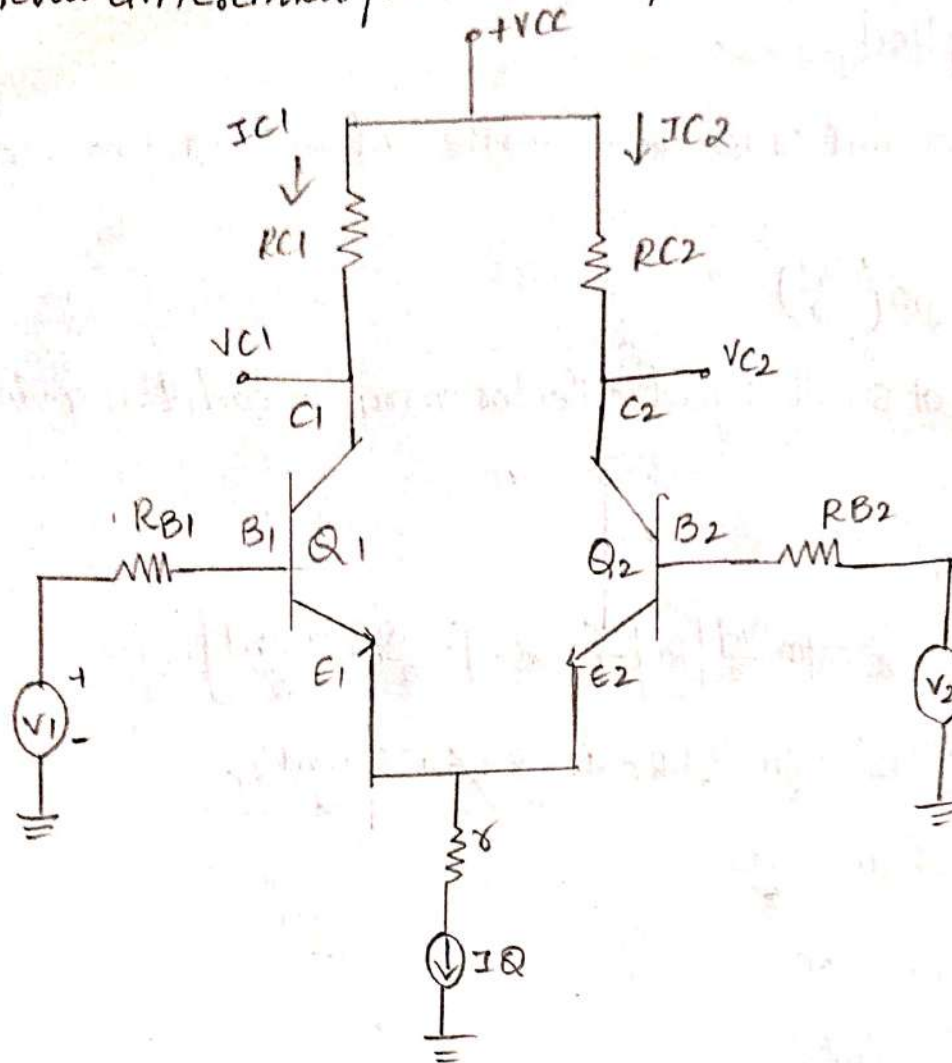


Fig: Small signal equivalent circuit diagram for BJT differential Amplifier.

Let us assuming the transistor are identical so,

$$r_{\pi 1} = r_{\pi 2} = r_{\pi} \text{ and}$$

$$g_{m1} = g_{m2} = g_m$$

Apply KCL at node V_E

$$\frac{V_{\pi 1}}{r_{\pi}} + g_m V_{\pi 1} + g_m V_{\pi 2} + \frac{V_{\pi 2}}{r_{\pi}} = \frac{V_E}{R_E} \rightarrow (1)$$

$$V_{\pi 1} \left[\frac{1}{r_{\pi}} + g_m \right] + V_{\pi 2} \left[g_m + \frac{1}{r_{\pi}} \right] = \frac{V_e}{R_o} \quad (g_m r_{\pi} = \beta)$$

$$V_{\pi 1} \left[\frac{1 + g_m r_{\pi}}{r_{\pi}} \right] + V_{\pi 2} \left[\frac{1 + g_m r_{\pi}}{r_{\pi}} \right] = \frac{V_e}{R_o}$$

$$V_{\pi 1} \left[\frac{1 + \beta}{r_{\pi}} \right] + V_{\pi 2} \left[\frac{1 + \beta}{r_{\pi}} \right] = \frac{V_e}{R_o} \rightarrow (2)$$

from the circuit

$$\boxed{\frac{V_{\pi 1}}{r_{\pi}} = \frac{V_{b1} - V_e}{r_{\pi} + R_B}} \quad \& \quad \boxed{\frac{V_{\pi 2}}{r_{\pi 2}} = \frac{V_{b2} - V_e}{r_{\pi} + R_B}}$$

$$V_{\pi 1} = r_{\pi} \left[\frac{V_{b1} - V_e}{r_{\pi} + R_B} \right] \quad \& \quad V_{\pi 2} = r_{\pi} \left[\frac{V_{b2} - V_e}{r_{\pi} + R_B} \right]$$

Substitute $V_{\pi 1}$ & $V_{\pi 2}$ in eq (2)

$$r_{\pi} \left[\frac{V_{b1} - V_e}{r_{\pi} + R_B} \right] \left[\frac{1 + \beta}{r_{\pi}} \right] + r_{\pi} \left[\frac{V_{b2} - V_e}{r_{\pi} + R_B} \right] \left[\frac{1 + \beta}{r_{\pi}} \right] = \frac{V_e}{R_o}$$

$$\left[\frac{1 + \beta}{r_{\pi} + R_B} \right] \cdot [V_{b1} + V_{b2} - 2V_e] = \frac{V_e}{R_o}$$

$$V_{b1} + V_{b2} - 2V_e = \frac{V_e}{R_o} \left[\frac{r_{\pi} + R_B}{1 + \beta} \right]$$

$$V_{b1} + V_{b2} = \frac{V_e}{R_o} \left[\frac{r_{\pi} + R_B}{1 + \beta} \right] + 2V_e$$

$$V_{b1} + V_{b2} = V_e \left[\frac{r_{\pi} + R_B}{R_o [1 + \beta]} + 2 \right]$$

$$\boxed{V_e = \frac{V_{b1} + V_{b2}}{\left[\frac{r_{\pi} + R_B}{R_o [1 + \beta]} + 2 \right]}} \rightarrow (3)$$

If we consider a one sided o/p at the collector of " Q_2 " then

$$V_o = V_{c2} = -g_m V_{\pi 2} R_c$$

$$= -\beta r_{b2} R_c$$

$$= -\beta R_c \left[\frac{V_{b2} - V_e}{r_{\pi} + R_B} \right] \rightarrow (4)$$

$$\text{here } g_m V_{\pi} = I_c = \beta I_b \quad I_{b2} = \left[\frac{V_{b2} - V_e}{r_{\pi} + R_B} \right]$$

Subeq (3) ineq (4)

$$V_o = \frac{-\beta R_c}{(r_{\pi} + R_B)} \left[V_{b2} - \frac{V_{b1} + V_{b2}}{\left(\frac{r_{\pi} + R_B}{(1 + \beta) R_o} \right) + 2} \right]$$

$$= \frac{-\beta R_C}{(\gamma \pi + R_B)} \left[\frac{2V_{b2} + V_{b2} \left(\frac{\gamma \pi + R_B}{(1+\beta)R_O} \right) - V_{b1} - V_{b2}}{\left(\frac{\gamma \pi + R_B}{(1+\beta)R_O} + 2 \right)} \right]$$

$$V_O = \frac{-\beta R_C}{(\gamma \pi + R_B)} \left[\frac{V_{b2} \left[\frac{\gamma \pi + R_B}{(1+\beta)R_O} + 1 \right] - V_{b1}}{\left(\frac{\gamma \pi + R_B}{(1+\beta)R_O} + 2 \right)} \right] \rightarrow (5)$$

In a identical transistor the current source of the output resistance is equals to infinity i.e. $R_O = \infty$ then the above equation reduces to

$$V_O = \frac{-\beta R_C [V_{b2} - V_{b1}]}{2(\gamma \pi + R_B)}$$

The Differential mode input voltage $V_d = V_{b2} - V_{b1}$

then

$$V_O = \frac{-\beta R_C V_d}{2[\gamma \pi + R_B]}$$

$$\frac{V_O}{V_d} = \frac{-\beta R_C}{2[\gamma \pi + R_B]}$$

$$A_d = \frac{-\beta R_C}{2(\gamma \pi + R_B)}$$

Differential Amplifier for Common Input Mode:

The two input signal can be written as some of differential mode input signal component and common mode input signal component. The V_{B1} and V_{B2} write of terms of V_{cm} and V_d

$$V_{b1} = V_{cm} + \frac{V_d}{2}$$

$$V_{b2} = V_{cm} - \frac{V_d}{2}$$

Substitute V_{B1} and V_{B2} in eq (5) then

$$\begin{aligned}
 V_o &= \frac{-\beta R_C}{r_{\pi} + R_B} \left[\frac{\left(V_{cm} - \frac{V_d}{2} \right) \left[\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 1 \right] - \left[V_{cm} + \frac{V_d}{2} \right]}{\left[\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 2 \right]} \right] \\
 &= \frac{-\beta R_C}{r_{\pi} + R_B} \left[\frac{V_{cm} \left[\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 1 \right] - \frac{V_d}{2} \left[\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 2 \right]}{\left[\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 2 \right]} \right] \\
 &= \frac{-\beta R_C}{r_{\pi} + R_B} \left[\frac{V_{cm} \left[\frac{r_{\pi} + R_B}{(1+\beta)R_o} \right]}{\left[\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 2 \right]} - \frac{V_d}{2} \left[\frac{\left(\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 2 \right)}{\left(\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 2 \right)} \right] \right]
 \end{aligned}$$

$$V_o = \frac{-\beta R_C}{r_{\pi} + R_B} \cdot \frac{V_{cm} \left(\frac{r_{\pi} + R_B}{(1+\beta)R_o} \right)}{\frac{r_{\pi} + R_B}{(1+\beta)R_o} + 2} + \frac{\beta R_C}{r_{\pi} + R_B} \frac{V_d}{2}$$

$$V_o = \frac{-\beta R_C}{r_{\pi} + R_B} \times \frac{V_{cm} \left[\frac{r_{\pi} + R_B}{(1+\beta)R_o} \right]}{\frac{r_{\pi} + R_B + 2[R_o(1+\beta)]}{(1+\beta)R_o}} + \frac{\beta R_C}{r_{\pi} + R_B} \frac{V_d}{2}$$

$$= \frac{-\beta R_C}{r_{\pi} + R_B + 2[R_o(1+\beta)]} V_{cm} + \frac{\beta R_C}{(r_{\pi} + R_B)2} V_d \rightarrow \textcircled{A}$$

The general form of output voltage is $V_o = A_{cm} V_{cm} + A_d V_d \rightarrow \textcircled{B}$
 Compare the above equations $\textcircled{A}$ & $\textcircled{B}$ then

$$A_{cm} = \frac{-\beta R_C}{r_{\pi} + R_B + 2[R_o(1+\beta)]}$$

$$A_d = \frac{\beta R_C}{(r_{\pi} + R_B)2}$$

In an ideal Constant Current Source the output Resistance R_o is infinity that is $R_o = \infty$

then

$$A_{cm} = 0$$

2M (or) 5M

IMP Common Mode Rejection Ratio (CMRR):

The ability of an differential Amplifier to Reject a Common mode Signal is described in terms of the Common mode Rejection Ratio. The CMRR is a figure of Merit for a differential Amplifier and it is defined as ratio of different mode gain (A_d) and Common mode gain (A_{cm}).

$$\text{i.e. } CMRR = \frac{A_d}{A_{cm}}$$

The CMRR expressed in decibels as follow

$$CMRR = 20 \log \left[\frac{A_d}{A_{cm}} \right] \text{ in dB}$$

- For an ideal differential Amplifier, $A_{cm} = 0$ then $CMRR = \infty$
- In general the CMRR expressed as

$$CMRR = \frac{A_d}{A_{cm}}$$

$$= \frac{\beta R_C}{\dots}$$

$$\frac{(\gamma \pi + R_B)^2}{\dots}$$

$$- \beta R_C$$

$$(\gamma \pi + R_B) + 2(1 + \beta) R_O$$

$$= -\frac{1}{2} \left[\frac{\gamma \pi + R_B + 2(1 + \beta) R_O}{(\gamma \pi + R_B)} \right]$$

$$CMRR = -\frac{1}{2} \left[1 + \frac{2(1 + \beta) R_O}{(\gamma \pi + R_B)} \right]$$

Problems:

- 1) Determine the differential and Common mode gains and CMRR of a differential pair amplifier $I_Q = 0.8 \text{ mA}$, $R_C = 12 \text{ k}\Omega$ and transistor parameter β is 100, output Resistance $R_O = 25 \text{ k}\Omega$ assume $R_B = 0$ and use one-sided output at V_{C2} here $V_T = 0.026$

Sol Given data

$$I_Q = 0.8 \text{ mA}$$

$$R_C = 12 \text{ k}\Omega$$

$$\beta = 100$$

$$R_O = 25 \text{ k}\Omega$$

$$R_B = 0$$

$$V_T = 0.026$$

We know that the differential gain A_d is

$$A_d = g_m R_C$$

But here we are collecting the output from one side the differential gain is half of the A_d

$$\text{i.e. } A_d = \frac{g_m R_C}{2}$$

$$= \frac{I_C R_C}{2 V_T}$$

$$\text{here } I_C = \frac{I_Q}{2}$$

$$= \frac{\frac{I_Q}{2} \cdot R_C}{2 V_T}$$

$$= \frac{I_Q R_C}{4 V_T}$$

$$= \frac{(0.8) \times 10^{-3} \times 12 \times 10^3}{4 \times 0.026}$$

$$= 92.3077$$

$$A_{cm} = \frac{-\beta R_C}{(r_{\pi} + R_B) + 2 R_O (1 + \beta)}$$

$$= \frac{-100 \times (12 \times 10^3)}{(r_{\pi} + 0) + 2 \times 25 \times 10^3 [1 + 100]}$$

$$(r_{\pi} + 0) + 2 \times 25 \times 10^3 [1 + 100]$$

$$\text{here } r_{\pi} = \beta / g_m$$

$$= \frac{\beta}{\frac{I_C}{V_T}} = \frac{V_T \beta}{I_C} = \frac{0.026 \times 100}{\frac{I_Q}{2}} = \frac{2 \times 0.026 \times 100}{0.8} = 6.5$$

then

$$A_{cm} = \frac{-100 \lambda (12 \times 10^3)}{(6.5) + 2 \times 25 \times 10^3 (101)}$$

$$A_{cm} = -0.237$$

$$CMRR = \left| \frac{A_d}{A_{cm}} \right|$$

$$= \left| \frac{92.3}{-0.237} \right|$$

$$CMRR = 389$$

$$CMRR_{dB} = 20 \log \left| \frac{A_d}{A_{cm}} \right| \text{ in dB}$$

$$= 20 \log (389)$$

$$CMRR_{dB} = 51.8$$

Mos differential Amplifier:

- The below figure shows the basic mos differential pair configuration
- It can consist of two matched transistor Q_1 and Q_2 whose source joined together and biased by current source I here that assume that the current source is ideal and that has infinite output resistance and drains are connected to positive supply (V_{DD}) to a resistance R_D

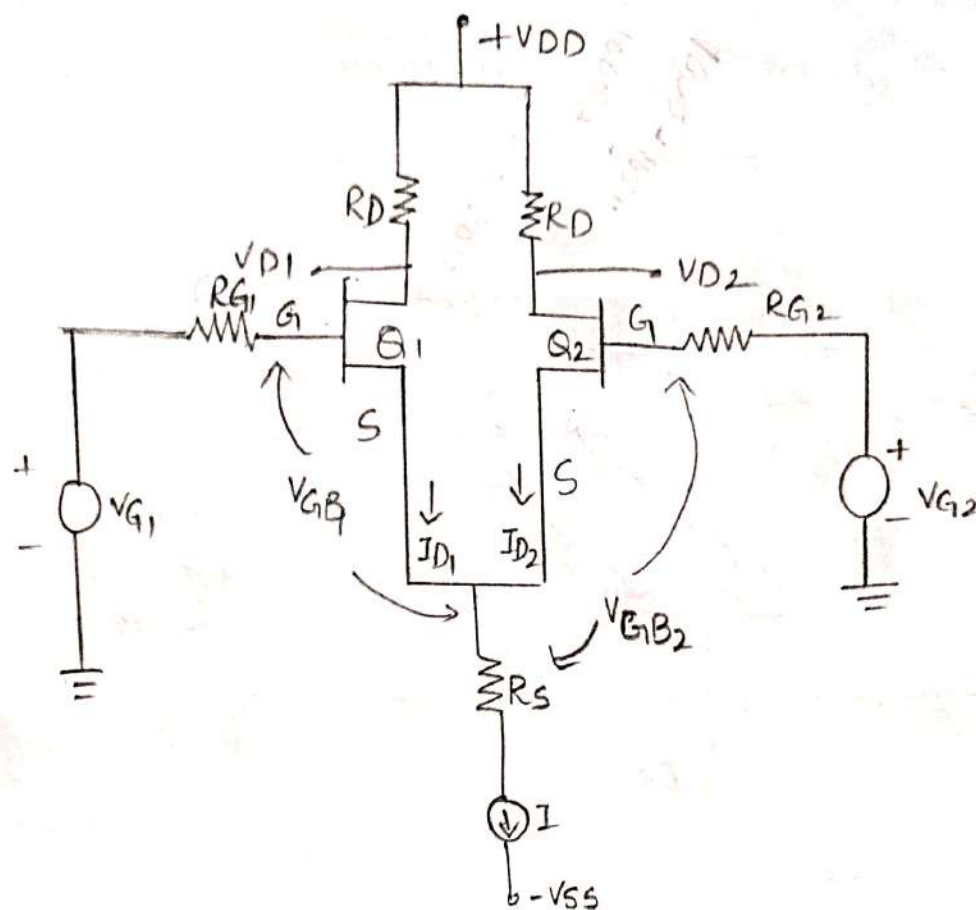


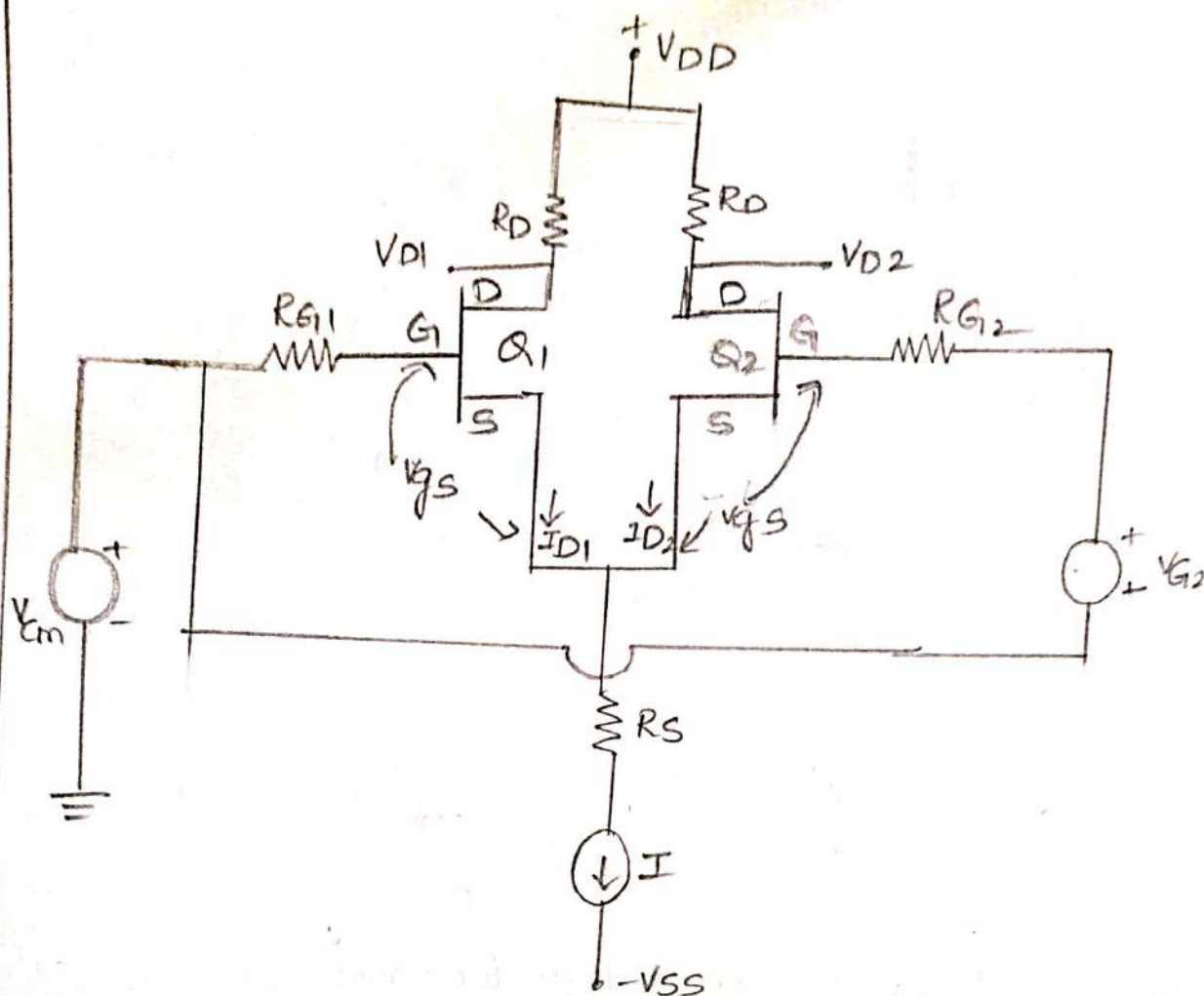
fig: General mass differential Amplifier

MOS differential Amplifier operated in two cases.

1. Common mode input voltage.
2. Differential mode input voltage

Case(i) Common mode input voltage:

In Common mode differential Amplifier the gate terminals are joined together and Connected to V_{cm} here. $V_{G1} = V_{G2} = V_{cm}$
 the below figure shows the Common mode input voltage differential Amplifier.



Since the two transistors are matched and its Current flows from drain to Source, the Current is equally divided between the two transistors i.e. $I_{D1} = I_{D2} = \frac{I}{2}$.

• The voltage Source $V_S = V_{cm} - V_{GS}$ then the Output Voltage.

$$V_{D1} = V_{D2} = V_{DD} - \frac{I}{2} R_D$$

• We know the drain Current $I_D = \frac{1}{2} K \frac{W}{L} [v_{gs} - V_t]^2$ here the term " $(v_{gs} - V_t)$ " called as overdrive voltage and it is represented by V_{ov}

then

$$I_{D1} = \frac{I}{2} = \frac{1}{2} K \frac{W}{L} [V_{ov}]^2$$

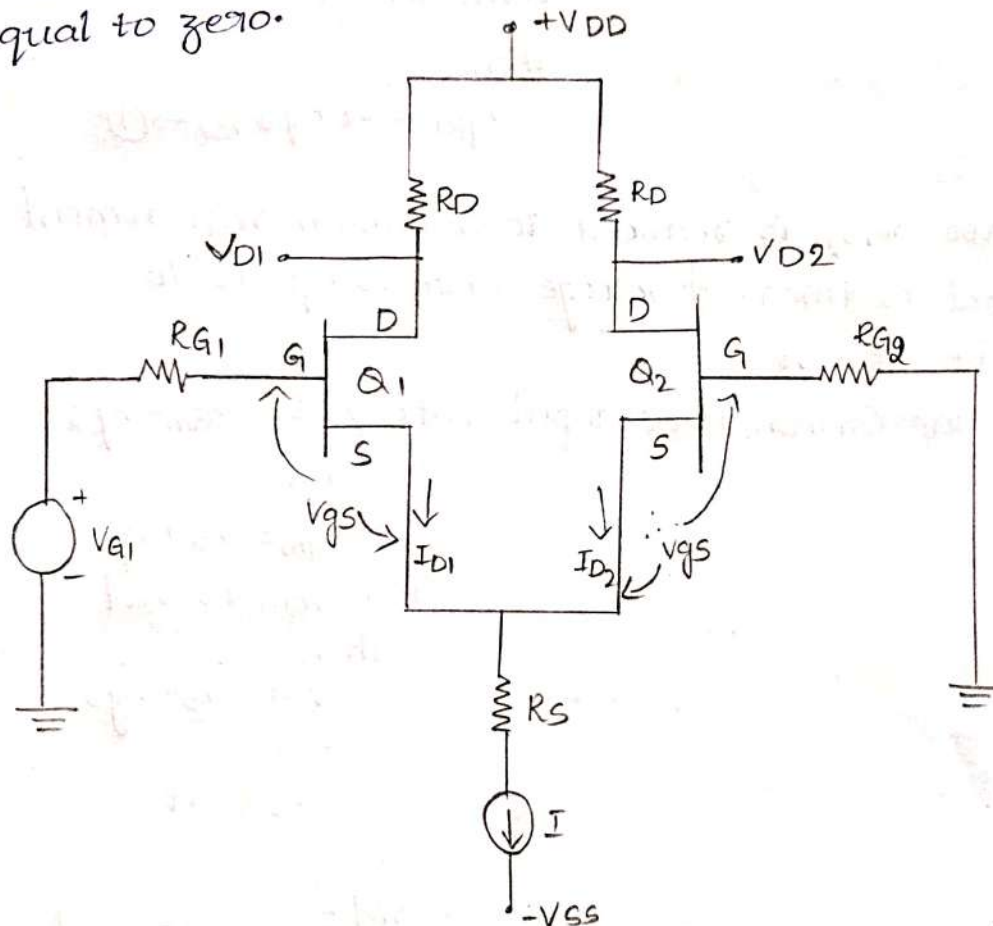
$$I = K \frac{W}{L} (V_{ov})^2$$

$$V_{ov} = \sqrt{\frac{I}{K \left(\frac{W}{L}\right)}}$$

Finally the difference in voltages between two drains will be zero
i.e. $V_{out} = V_{D1} - V_{D2} = 0$

Case(ii) Differential mode input Voltage:

In differential mode input voltage we are applying the two different voltages for differential amplifier that is V_{G1} and V_{G2} .
• Comparing with Common mode input we have to increase the V_{cm} times voltage for one side and another side we have to decrease the same (V_{cm}) voltage that is one side of the voltage is equal to zero.



• In these conditions the second input voltage is connected to ground, i.e. $V_{G2} = 0$ and apply a single first input voltage is called as differential input voltage (V_{ID})

$$\text{i.e. } V_{id} = V_{G1} - V_{G2}$$

• here

$$V_{G2} = 0$$

$$V_{id} = V_{G1}$$

• If V_{id} is positive, V_{GS1} will be greater than V_{GS2} and hence I_{D1} will be greater than I_{D2} and difference output voltage " $(V_{d1} - V_{d2})$ " will be positive.

We know the Current equation $I = \frac{1}{2} k \frac{W}{L} [V_{GS} - V_t]^2$

from the above equation

$$V_{GS1} = V_t + \sqrt{\frac{2I}{k(\frac{W}{L})}}$$

ther form $\sqrt{\frac{I}{k(\frac{W}{L})}}$ is called as over drive voltage

then

$$V_{GS1} = V_t + \sqrt{2} V_{ov} \rightarrow (1)$$

In this case V_{GS2} is reduced to minimum requirement of voltage that is threshold voltage which is equals to
i.e $V_S = -V_t$

• We know the Common mode input voltage $V_S = V_{GM} - V_{GS}$
then

$$V_{GM} = V_S + V_{GS}$$

here V_{CM} is V_{id}

then

$$V_{id} = V_S + V_{GS}$$

W.K.T

$$V_S = -V_t$$

then

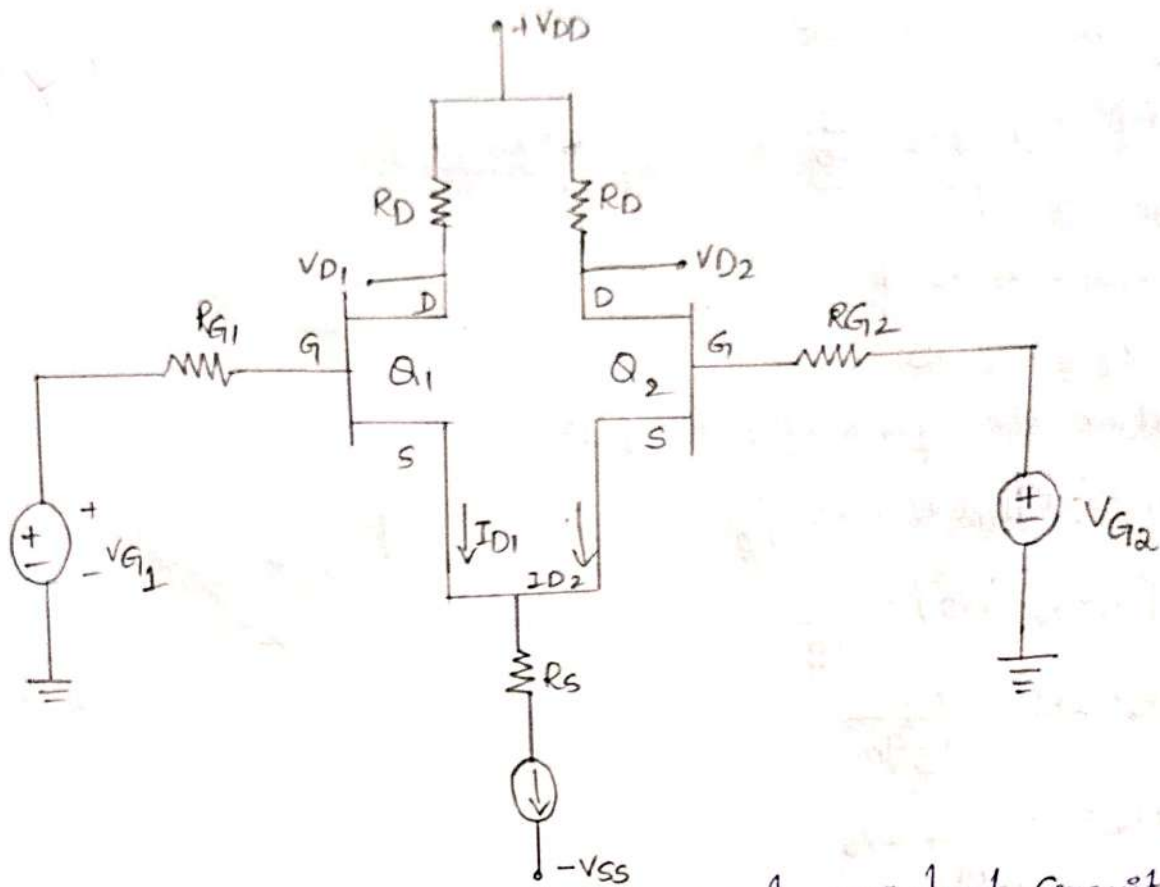
$$V_{id} = V_{GS} - V_t \rightarrow (2)$$

Substitute eq (2) in eq (1)

$$V_{id} = V_t + \sqrt{2} V_{ov} - V_t$$

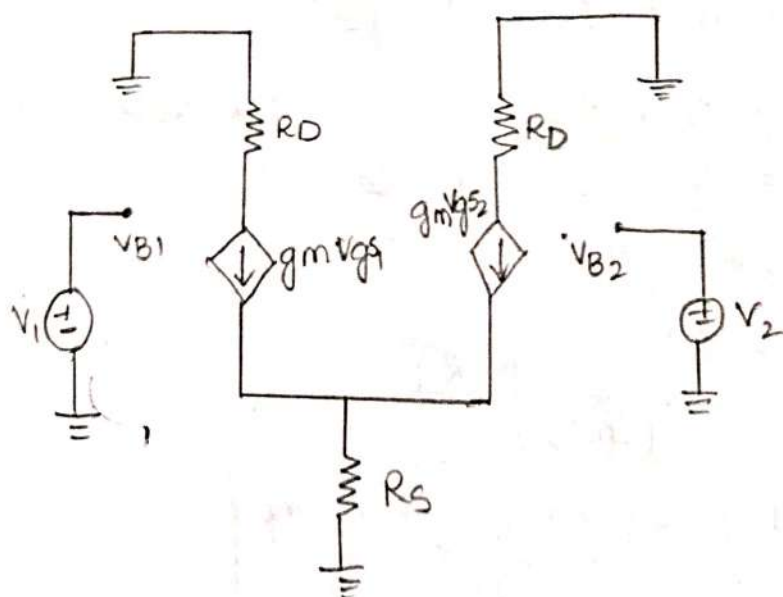
Small Signal operation of (MOS) Differential pair Amplifier :

The below figure shows the basic MOS differential pair Amplifier



The below figure shows the Small signal equivalent circuit diagram for MOS differential pair Amplifier.

In these circuit $+V_{DD}$ and $-V_{SS}$ (positive and negative terminals) treated as grounded.



In the above circuit the transistors are identical then

$$g_{m1} = g_{m2} = g_m$$

Apply the KCL at node S.

$$g_m V_{gs1} + g_m V_{gs2} = \frac{V_S}{R_o} \quad \text{--- (1)} \quad \frac{V_S}{R_S} = R_o = R_S$$

from the circuit

$$V_{gs1} = V_1 - V_S$$

$$V_{gs2} = V_2 - V_S$$

Substitute the V_{gs1} & V_{gs2} in eq (1)

$$g_m (V_1 - V_S) + g_m (V_2 - V_S) = \frac{V_S}{R_o}$$

$$g_m [V_1 + V_2 - 2V_S] = \frac{V_S}{R_o}$$

$$V_1 + V_2 - 2V_S = \frac{V_S}{R_o g_m}$$

$$V_1 + V_2 = \frac{V_S}{R_o g_m} + 2V_S$$

$$V_1 + V_2 = V_S \left[\frac{1}{g_m R_o} + 2 \right]$$

$$V_S = \left[\frac{V_1 + V_2}{\left(\frac{1}{g_m R_o} + 2 \right)} \right] \rightarrow \text{--- (2)}$$

For a one sided output at the Drain of " Q_2 "

$$V_o = V_{d2} = -g_m V_{gs2} R_D$$

$$V_{gs2} = V_2 - V_S$$

$$V_o = V_{d2} = -g_m [V_2 - V_S] R_D \rightarrow \text{--- (3)}$$

Sub eq (2) in eq (3)

$$V_o = V_{d2} = -g_m \left[V_2 - \frac{V_1 + V_2}{2 + \left[\frac{1}{g_m R_o} \right]} \right] R_D$$

$$= -g_m R_D \left[\frac{V_2 \left[2 + \frac{1}{g_m R_o} \right] - V_1 - V_2}{2 + \frac{1}{g_m R_o}} \right]$$

$$= -g_m R_d \left[\frac{v_2 \left[2 + \frac{1}{g_m R_o} \right] - v_1}{2 + \frac{1}{g_m R_o}} \right]$$

$$= -g_m R_d \left[\frac{v_2 \left(1 + \frac{1}{g_m R_o} \right) - v_1}{2 + \frac{1}{g_m R_o}} \right] \rightarrow (4)$$

v_1 & v_2 in terms of v_d & v_{cm}

$$v_1 = v_{cm} + \frac{v_d}{2}, \quad v_2 = v_{cm} - \frac{v_d}{2}$$

Substitute v_1 & v_2 in eq (4)

$$v_o = -g_m R_d \left[\frac{(v_{cm} - \frac{v_d}{2}) \left(1 + \frac{1}{g_m R_o} \right) - (v_{cm} + \frac{v_d}{2})}{2 + \frac{1}{g_m R_o}} \right]$$

$$= -g_m R_d \left[\frac{v_{cm} \left(1 + \frac{1}{g_m R_o} \right) - \frac{v_d}{2} \left(1 + \frac{1}{g_m R_o} + 1 \right)}{2 + \frac{1}{g_m R_o}} \right]$$

$$v_o = -g_m R_d \left[\frac{v_{cm} \left(\frac{1}{g_m R_o} \right) - \frac{v_d}{2} \left(2 + \frac{1}{g_m R_o} \right)}{2 + \frac{1}{g_m R_o}} \right]$$

$$= -g_m R_d \left[\frac{\frac{1}{2g_m R_o + 1}}{\frac{1}{g_m R_o}} \right] v_{cm} + \frac{g_m R_d}{2} \left[\frac{2 + \frac{1}{g_m R_o}}{2 + \frac{1}{g_m R_o}} \right] v_d$$

$$\boxed{v_o = -g_m R_d \left[\frac{1}{2g_m R_o + 1} \right] v_{cm} + \frac{g_m R_d}{2} v_d} \rightarrow (5)$$

The general form of output voltage.

$$\boxed{v_o = A_{cm} v_{cm} + A_d v_d} \rightarrow (6)$$

Compare eq (5) & eq (6)

then $\boxed{A_{cm} = \frac{-g_m R_d}{2g_m R_o + 1}}$

$$\boxed{A_d = \frac{g_m R_d}{2}}$$

The transconductances " g_m " of the "MOSFET" is

$$g_m = 2\sqrt{k I_{DQ}}$$

$W \cdot k \cdot T$

$$I_{DQ} = \frac{I_Q}{2}$$

then

$$g_m = 2\sqrt{k \frac{I_Q}{2}}$$

$$g_m = \sqrt{2 \times 2 \times k \frac{I_Q}{2}}$$
$$= \sqrt{2k I_Q}$$

then

$$A_d = \frac{g_m R_d}{2}$$

$$A_d = \sqrt{2k I_Q} \times \frac{R_d}{2}$$

$$= \sqrt{\frac{2k I_Q}{2 \times 2}} \times R_d$$

$$A_d = \sqrt{\frac{k I_Q}{2}} \cdot R_d$$

and

$$A_{cm} = \frac{-g_m R_d}{2g_m R_o + 1}$$

$$A_{cm} = \frac{-\sqrt{2k I_Q} \times R_d}{2\sqrt{2k I_Q} \times R_o + 1}$$

CMRR:

$$CMRR = \left| \frac{A_d}{A_{cm}} \right|$$

$$= \frac{\sqrt{\frac{k I_Q}{2}} \cdot R_d}{\frac{-\sqrt{2k I_Q} \cdot R_d}{2\sqrt{2k I_Q} \times R_o + 1}}$$

$$= \frac{1}{2} \times \frac{\sqrt{2k I_Q} \cdot R_d \times (1 + 2\sqrt{2k I_Q} \cdot R_o)}{\sqrt{2k I_Q} \cdot R_d}$$

$$CMRR = \frac{1}{2} [1 + 2\sqrt{2kTQ R_O}]$$

Non ideal characteristics of the differential pair Amplifier:

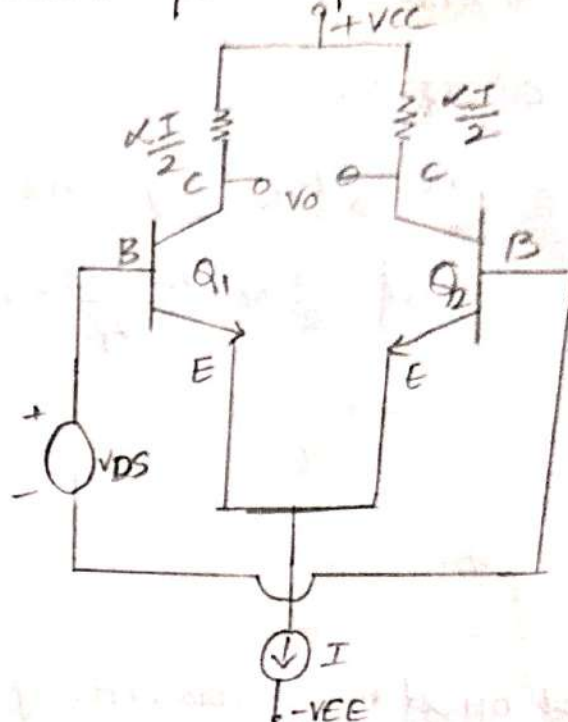
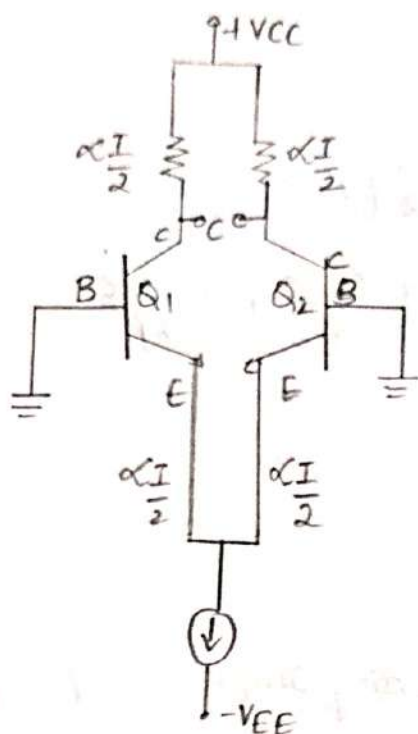


fig: Both ifp are grounded Differential Amplifier

fig: Differential Amplifier with VOS

- Consider the basic MOS differential Amplifier with both inputs are grounded as shown in figure (1)
- If the two transistors are perfectly Matched then the Current I will be Splitted equally between two transistors and output voltage should be zero.
- If the Output voltage is not equal to zero due to non-ideal characteristics of BJT
- There are two factors are Considerable to the DC off set voltage
 - 1) Mismatched in load Resistance (R_C)
 - 2) Scale Current (I_S)
- Let us Consider the first Case of two transistors Q_1 and Q_2 are perfectly matched and load resistance is mismatched.

$$R_{C1} = R_C + \frac{\Delta R_C}{2}$$

$$R_{C2} = R_C - \frac{\Delta R_C}{2}$$

then the output voltage

$$V_{C1} = V_{CC} - \frac{\alpha I}{2} (R_C + \frac{\Delta R_C}{2})$$

$$V_{C2} = V_{CC} - \frac{\alpha I}{2} \left(R_C - \frac{\Delta R_C}{2} \right)$$

• The differential between two output voltages

$$V_0 = V_{C2} - V_{C1}$$

$$= V_{CC} - \frac{\alpha I}{2} \left(R_C - \frac{\Delta R_C}{2} \right) - V_{CC} - \frac{\alpha I}{2} \left(R_C + \frac{\Delta R_C}{2} \right)$$

$$= \cancel{V_{CC}} - \frac{\alpha I}{2} R_C + \frac{\alpha I \Delta R_C}{2} - \cancel{V_{CC}} + \frac{\alpha I R_C}{2} + \frac{\alpha I \Delta R_C}{2}$$

$$= \frac{2 \alpha I \Delta R_C}{2}$$

$$\boxed{V_0 = \frac{\alpha I \Delta R_C}{2}}$$

• Input offset voltage obtained, by dividing output voltage by gain

$$i.e. V_{OS} = \frac{V_0}{A_d}$$

W.K.T

$$A_d = g_m R_C$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{\alpha I}{2 V_T}$$

then

$$V_{OS} = \frac{V_0}{A_d}$$

$$= \frac{\alpha I \Delta R_C}{2}$$

$$\frac{\alpha I}{2 V_T} \cdot R_C$$

$$\boxed{V_{OS} = V_T \frac{\Delta R_C}{R_C}}$$

Similarly due to mismatched in Scale Current (I_S) then $V_{OS} =$

$$\boxed{V_{OS} = V_T \frac{\Delta I_S}{I_S}}$$

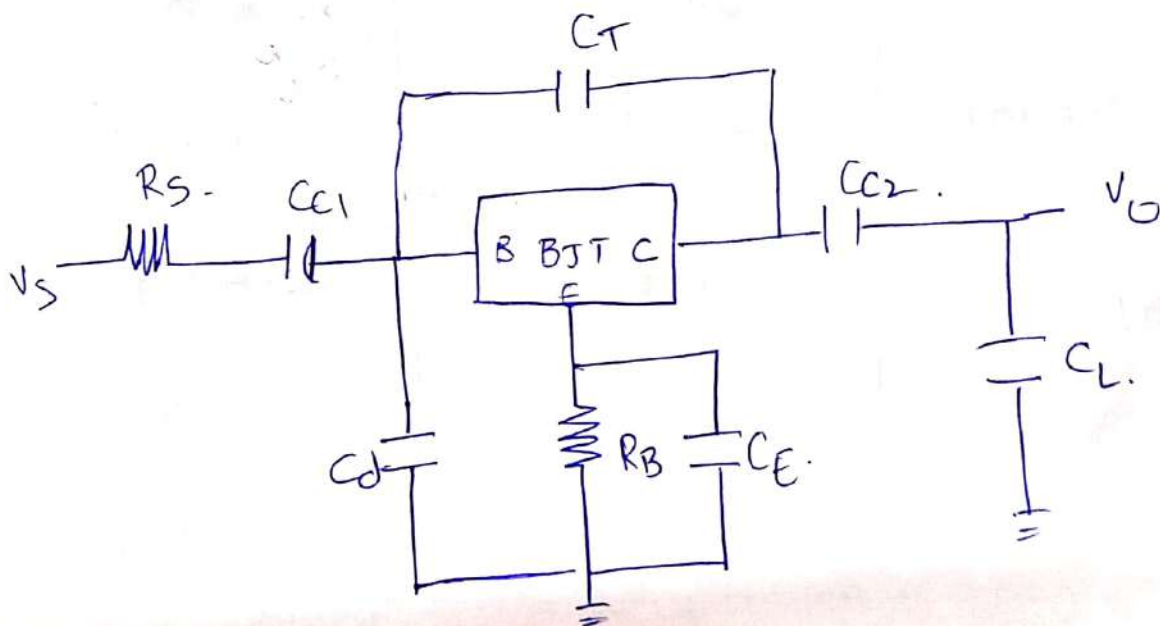
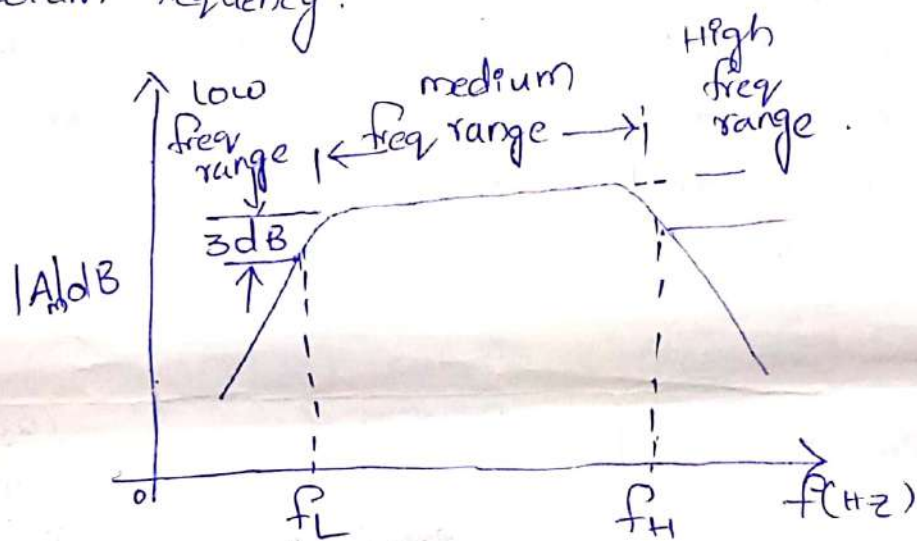
UNIT - 2
Frequency Response

M. Sairam
Asst. Professor

→ The Curve drawn between frequency Vs Gain is called frequency response curve.

→ The frequency ranges are divided as.

- 1) Low frequency ($f < f_L$).
- 2) High frequency ($f > f_H$).
- 3) Medium frequency.



The above amplifier consists of coupling capacitors C_{C1}, C_{C2} ; by-pass capacitor C_E , parasitic capacitance C_D, C_T and load capacitance C_L . (C_D = diffusion capacitance, C_T = transition capacitance).

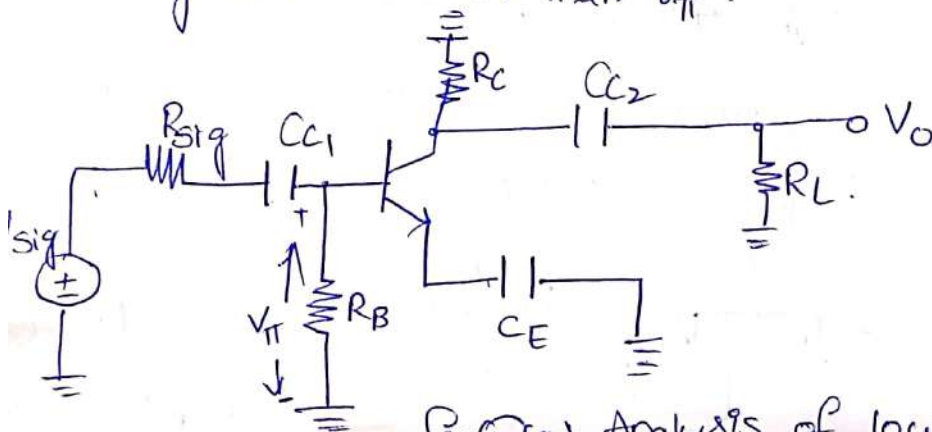
Based on the frequency range we consider the required capacitance i.e; for low frequency range we consider the coupling and by-pass capacitors, the load & parasitic capacitance are open circuited.

For mid-band frequency range the coupling & by-pass capacitors are short circuited and load & parasitic capacitors are open circuited. Similarly for high frequency we consider the load & parasitic capacitors and short circuited the coupling & by-pass capacitors.

freq range	Coupling & by-pass cap	load & Parasitic cap
LF	Consider	open
mid-band	short	open.
HF	short	consider.

② Low frequency response of CE Amplifier:-

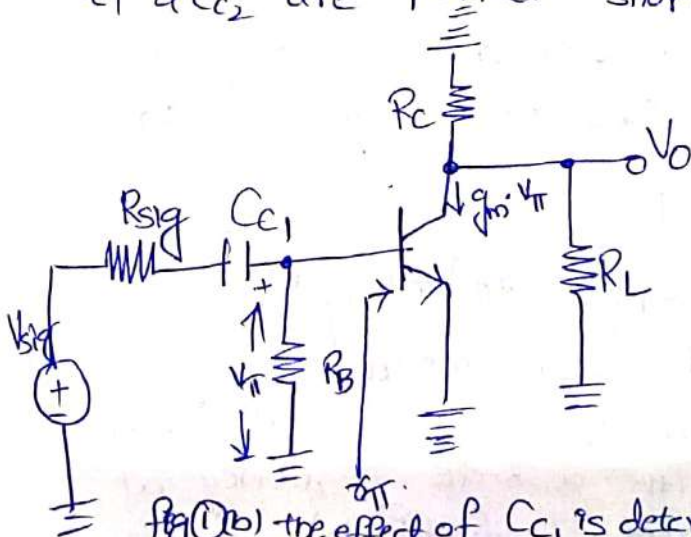
To determine the low-frequency gain of the CE amplifier circuit shown in fig(1a) the circuit with the dc sources eliminated ~~is that~~ we shall perform the Small-signal analysis directly on this circuit shown in fig(1b). Here we will neglect r_o . The reader can verify through SPICE simulation the effect of r_o which is usually much smaller than r_{π} .



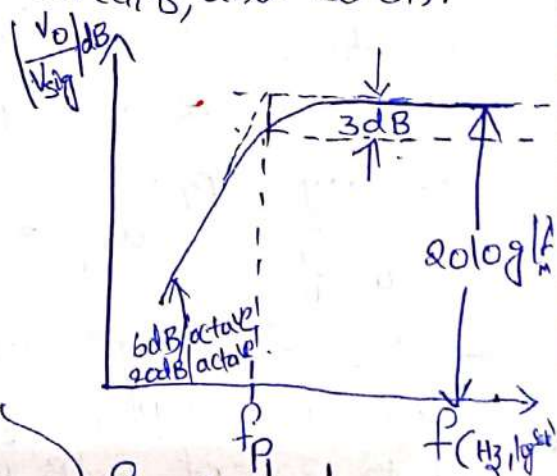
fig(1a) Analysis of low frequency response of the CE amplifier with dc sources removed.

The analysis of the circuit in fig(1a) is to consider the effect of the 3 capacitors. C_{c1} , C_E and C_{c2} one at a time. i.e., when finding the effect of C_{c1} we shall assume that C_E & C_{c2} are acting as perfect short circuits.

Similarly when considering C_E , we assume that C_{c1} & C_{c2} are perfect short circuits, and so on.



fig(1b) the effect of C_{c1} is determined. (with C_E & C_{c2} assumed as short ckt.)



$$f_{P1} = \frac{1}{2\pi R_c} = \frac{1}{2\pi C_{c1} (R_B \parallel r_{\pi} + R_{sig})}$$

First, we consider the effect of C_1 & C_2 on the circuit. Fig (1)(b) shows the circuit with C_1 & C_2 with short circuits. The voltage V_{π} at the base of the transistor can be written as.

$$V_{\pi} = V_{sig} \cdot \frac{R_B \parallel r_{\pi}}{(R_B \parallel r_{\pi}) + R_{sig} + \frac{1}{sC_1}}$$

and the output voltage is obtained as.

$$V_o = -g_m \cdot V_{\pi} (R_C \parallel R_L)$$

These two equations can be combined to obtain the voltage gain $\frac{V_o}{V_{sig}}$ including the effect of C_1 as.

$$V_o = -g_m \cdot \left[V_{sig} \cdot \frac{R_B \parallel r_{\pi}}{(R_B \parallel r_{\pi}) + R_{sig} + \frac{1}{sC_1}} \right] (R_C \parallel R_L)$$

$$\frac{V_o}{V_{sig}} = - \frac{R_B \parallel r_{\pi}}{(R_B \parallel r_{\pi}) + R_{sig}} g_m (R_C \parallel R_L) \left[\frac{s}{s + \frac{1}{C_1 (R_B \parallel r_{\pi}) + R_{sig}}} \right] \quad \text{--- (1)}$$

From which we observe that the effect of C_1 is to introduce the frequency dependent factor between the square brackets on the right-hand side of eq (1). We recognize this factor as a transfer function of a single-time-constant (STC) network of high pass type with a corner frequency ω_{p1} .

$$\left(\because \omega = \frac{1}{RC} \right), \quad \omega_{p1} = \frac{1}{C_1 [(R_B \parallel r_{\pi}) + R_{sig}]} \quad \text{--- (2)}$$

→ The STC high-pass factor introduced by C_1 will cause the amplifier gain to roll-off at low frequencies at the rate of 6dB with a 3-dB frequency at $f_{p1} = \omega_{p1}/2\pi$ as indicated in fig (1)(b).

Next, we consider the effect of C_E . For this purpose we assume that C_1 & C_2 are acting as perfect short circuits and thus obtain the circuit in fig (c).

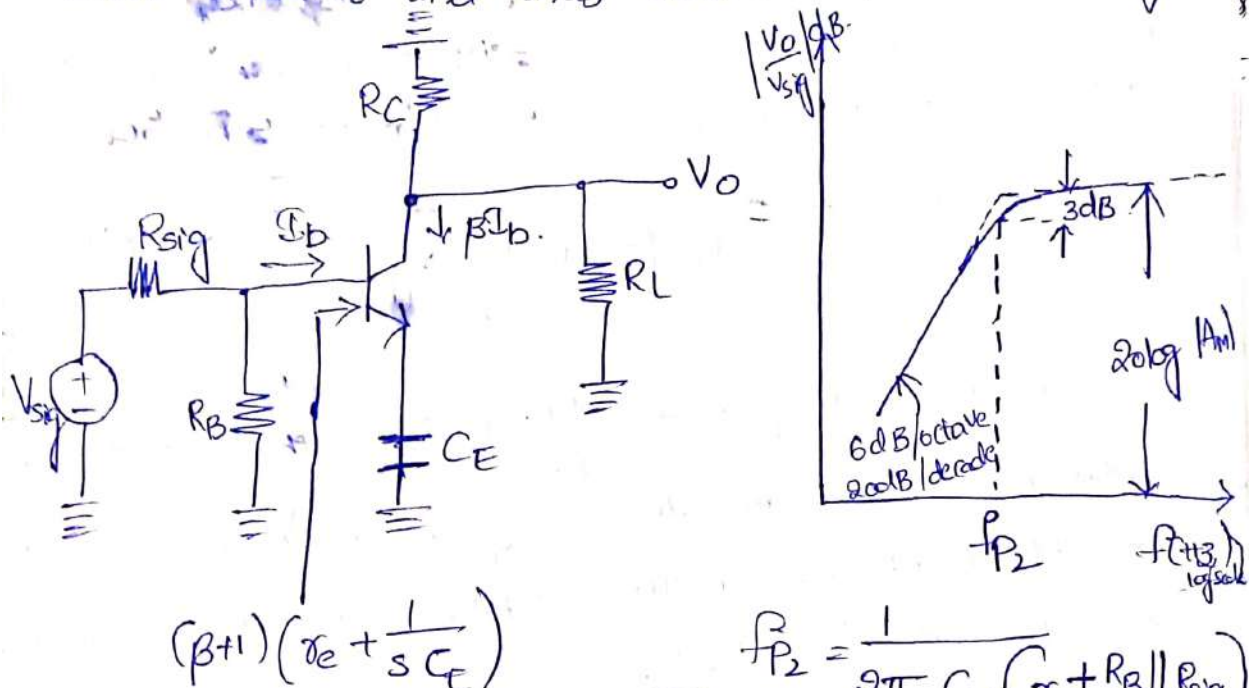


Fig (c) the effect of C_E is

determined with C_1 & C_2 assumed short circuit.

Reflecting r_e & C_E into the base circuit & utilizing Thevenin theorem enables us to obtain the base current as.

$$I_B = V_{sig} \cdot \frac{R_B}{R_B + R_{sig}} \cdot \frac{1}{(R_B \parallel R_{sig}) + (\beta + 1) \left(r_e + \frac{1}{s C_E} \right)}$$

The collector current can then be found as βI_B and the output voltage as.

$$V_O = -\beta I_B (R_C \parallel R_L).$$

$$V_O = - \frac{R_B}{R_B + R_{sig}} \cdot \frac{\beta (R_C \parallel R_L)}{(R_B \parallel R_{sig}) + (\beta + 1) \left(r_e + \frac{1}{s C_E} \right)} \cdot V_{sig}$$

Thus, the voltage gain including the effect of C_E can be expressed as.

$$\frac{V_O}{V_{sig}} = - \frac{R_B}{R_B + R_{sig}} \cdot \frac{\beta (R_C \parallel R_L)}{(R_B \parallel R_{sig}) + (\beta + 1) r_e} \cdot \frac{s}{s + \left[\frac{1}{C_E \left(r_e + \frac{R_B \parallel R_{sig}}{\beta + 1} \right)} \right]} \quad \text{--- (3)}$$

we observe that C_E introduces the STC high-pass factor on the extreme right-hand side. Thus C_E causes the gain to fall off at low frequency at the rate of 6dB/octave with a 3dB frequency equal to the corner frequency of the high-pass STC factor, i.e.,

$$\omega_{P2} = \frac{1}{C_E \left[r_e + \frac{R_B \parallel R_{sig}}{\beta + 1} \right]} \quad (4)$$

Observe that $\left[r_e + \frac{R_B \parallel R_{sig}}{\beta + 1} \right]$ is the resistance seen between the two terminals of C_E when V_{sig} is set to zero. The effect of C_E on the amplifier frequency response is shown in Fig (1Cc).

→ Finally, we consider the effect of ' C_2 ', The circuit with C_1 & C_E assumed to be acting as perfect short circuits is shown Fig (1Cd).

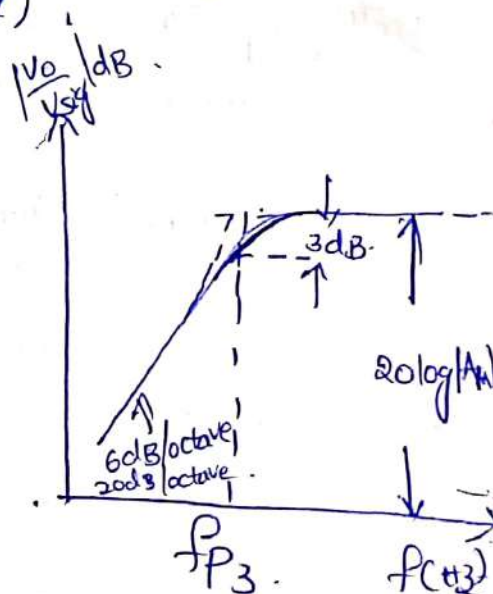
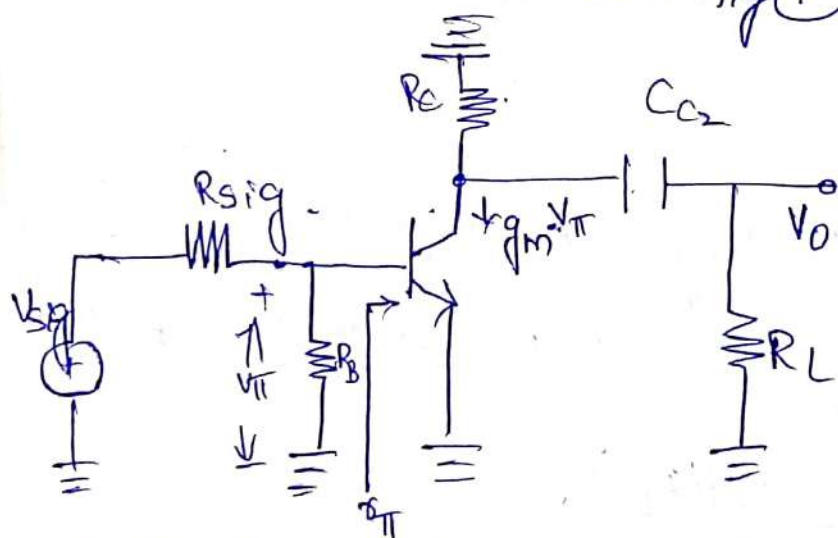


Fig (1Cd) the effect of C_2 is determined with C_1 & C_E assumed to be acting as perfect short circuits.

$$f_{P3} = \frac{1}{2\pi C_2 (R_C + R_L)}$$

From Fig (1cd) for which we can write. (4)

$$V_{\pi} = V_{sig} \cdot \frac{R_B \parallel r_{\pi}}{(R_B \parallel r_{\pi}) + R_{sig}}$$

and

$$V_o = -g_m \cdot V_{\pi} \cdot \frac{R_C}{R_C + \frac{1}{sC_2} + R_L} \cdot R_L$$

These two equations can be combined to obtain the low-frequency gain including the effect of C_2 as

$$\frac{V_o}{V_{sig}} = \frac{-R_B \parallel r_{\pi}}{(R_B \parallel r_{\pi}) + R_{sig}} \cdot g_m (R_C \parallel R_L) \left[\frac{s}{s + \frac{1}{C_2(R_C + R_L)}} \right] \rightarrow (5)$$

We observe that C_2 introduces the frequency-dependent factor between the square brackets, which we recognize as the transfer function of a high-pass STC network with a break frequency ω_{P3} .

$$\omega_{P3} = \frac{1}{C_2 (R_C + R_L)} \rightarrow (6)$$

Here, we note that as expected, $(R_C + R_L)$ is the resistance seen between the terminals of C_2 when V_{sig} is set to zero. Thus capacitor C_2 causes the low-frequency gain of the amplifier to decrease at the rate of -20 dB/octave with a 3-dB frequency at $f_{P3} = \omega_{P3} / 2\pi$, as illustrated in Fig (1cd).

Now, that we have determined the effects of each of C_{c1} , C_c and C_{c2} acting alone the total amplifier low frequency gain can be expressed as,

$$\left[\frac{V_o}{V_{sig}} = -A_m \left(\frac{s}{s + \omega_{p1}} \right) \left(\frac{s}{s + \omega_{p2}} \right) \left(\frac{s}{s + \omega_{p3}} \right) \right] \quad (7)$$

from which we see that it acquires three break frequencies at f_{p1} , f_{p2} & f_{p3} all in the low frequency band.

If '3' frequencies are widely separated, their effects will be distinct as shown in fig (1c)

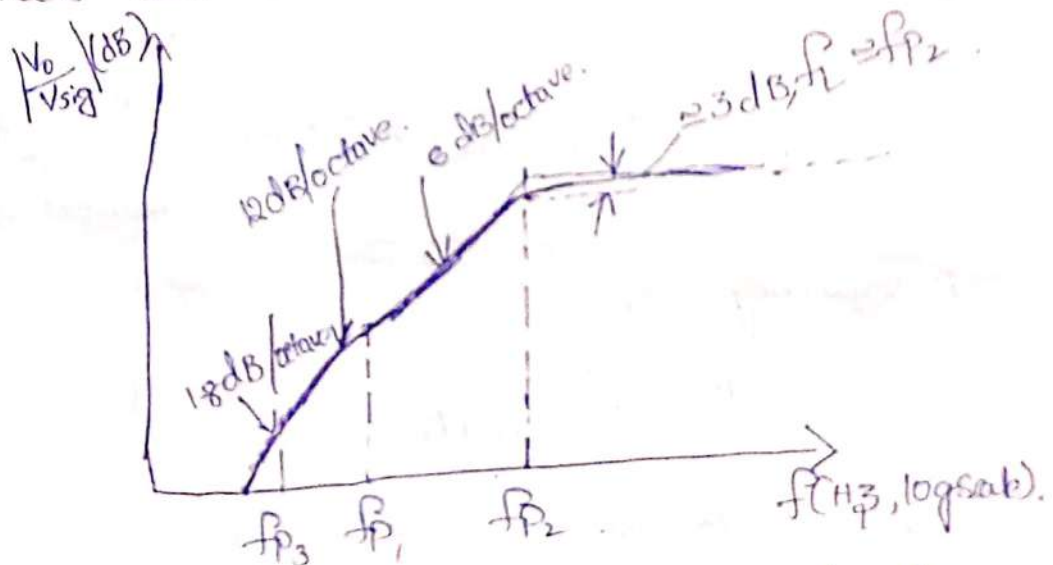


Fig (1c) low frequency gain under the assumptions that C_{c1} , C_c , C_{c2} do not interact and their break frequencies are widely spaced.

The important point to note here is that the 3dB frequency f_L is determined by the highest of the 3 break frequencies.

As an alternative, for hand calculations we can use a reasonably good estimate for f_L using following formula.

$$f_L \approx \frac{1}{2\pi} \left[\frac{1}{C_{c1} R_{c1}} + \frac{1}{C_c R_E} + \frac{1}{C_{c2} R_o} \right] \quad (8)$$

(or) equivalently,

$$f_L = f_{P_1} + f_{P_2} + f_{P_3} \quad \rightarrow (9)$$

where R_A , R_E , & R_C are the resistances seen by C_1 , C_E & C_2 , respectively, when V_{sig} is set to zero and the other two capacitances are replaced with short circuits.

$\Rightarrow$ Selecting values for C_1 , C_E , and C_2 :-

we now address the design issue of selecting appropriate values for C_1 , C_E & C_2 . The design objective is to place the lower 3-dB frequency f_L at a specified location while minimizing the capacitor values.

As mentioned above C_E usually sees the lowest of the three resistances, the total capacitance is minimized by selection C_E so that its contribution to f_L is dominant. i.e; by reference to eq. (8) we may select C_E such that $\frac{1}{C_E R_E}$ is, say 80% of $\omega_L = 2\pi f_L$, leaving each of the other capacitors to contribute 10% to the value of ω_L .

→ The Low-Frequency Response of CS Amplifier:-

To determine the low-frequency gain (or) transfer function of the common-source amplifier, we show in Fig (1a) the circuit with the dc sources eliminated. We shall perform the small-signal analysis directly on this circuit. However, we will ignore v_o . This is done in order to keep the analysis simple and thus focus attention on significant issues.

The effect of v_o on the low-frequency operation of this amplifier is minor, as can be verified by a SPICE simulation.

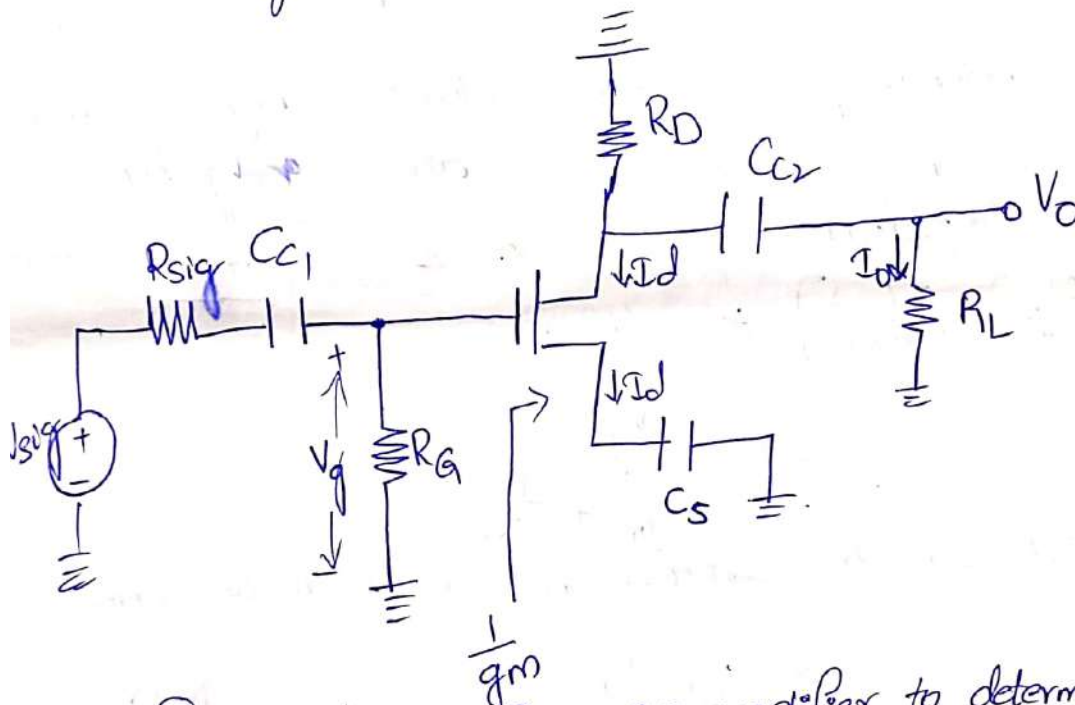


Fig (1a) Analysis of the CS amplifier to determine its low-frequency transfer function.

The analysis begins at the signal generator by finding the fraction of v_{sig} that appears at the transistor gate.

$$V_g = v_{sig} \cdot \frac{R_G}{R_G + \frac{1}{sC_{c1}} + R_{sig}}$$

which can be written in the alternative form,

$$V_g = v_{sig} \cdot \frac{R_G}{R_G + R_{sig}} \cdot \frac{s}{s + \frac{1}{C_{c1}(R_G + R_{sig})}} \quad \rightarrow (1)$$

Thus, we see that the expression for the signal transmission from signal generator to amplifier input has acquired a frequency dependent factor. We recognize this factor as the transfer function of an STC network of the high-pass type with a break (or) corner frequency $\omega_0 = \frac{1}{C_1(R_G + R_{sig})}$. Thus, the effect of the coupling capacitor C_1 is to introduce a high-pass STC response with a break frequency that we shall denote ω_{p1} .

$$\omega_{p1} = \omega_0 = \frac{1}{C_1(R_G + R_{sig})} \quad \text{--- (2)}$$

Continuing with the analysis, we next determine the drain current ' I_d ' by dividing ' V_g ' by the total impedance in the source circuit, which is $\left[\left(\frac{1}{g_m} \right) + \left(\frac{1}{sC_s} \right) \right]$ to obtain.

$$I_d = \frac{V_g}{\frac{1}{g_m} + \frac{1}{sC_s}}$$

which can be written in the alternate form.

$$I_d = g_m \cdot V_g \cdot \frac{s}{s + \frac{g_m}{C_s}} \quad \text{--- (3)}$$

we observe that C_s introduces a frequency-dependent factor, which is also of the STC high pass type. Thus the amplifier acquires another break frequency.

$$\omega_{p2} = \frac{g_m}{C_s} \quad \text{--- (4)}$$

To complete the analysis, we find $\tilde{V}_O$ by first ⁽⁴⁾ using the current divider rule to determine the fraction of $\tilde{I}_D$ that flows through R_L .

$$\tilde{I}_O = -\tilde{I}_D \cdot \frac{R_D}{R_D + \frac{1}{sC_2} + R_L}$$

and then multiplying $\tilde{I}_O$ by R_L to obtain

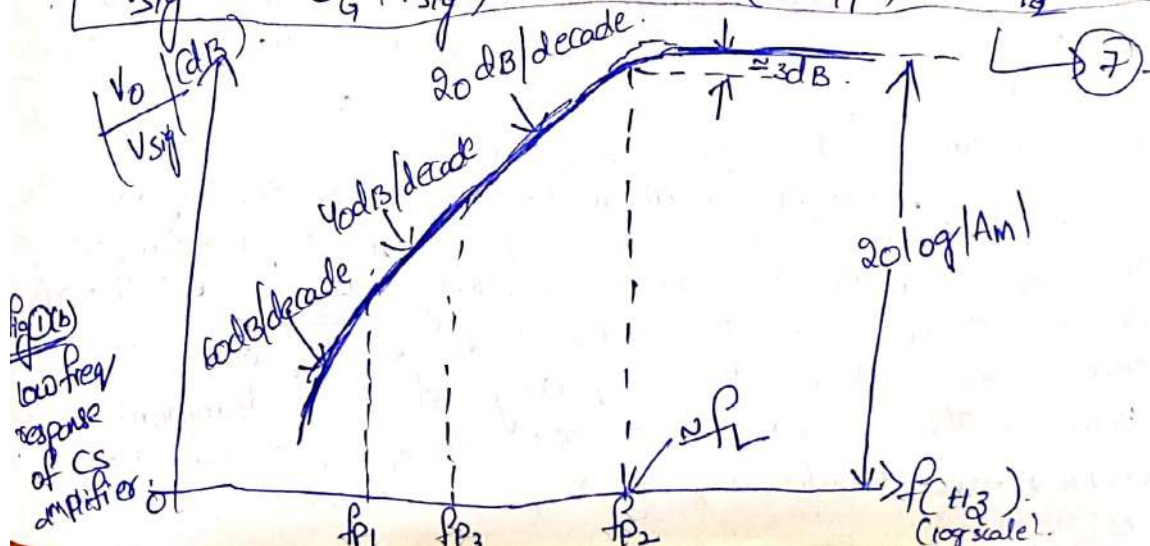
$$\tilde{V}_O = \tilde{I}_O \cdot R_L = -\tilde{I}_D \cdot \frac{R_D \cdot R_L}{R_D + R_L} \cdot \frac{s}{s + \frac{1}{C_2(R_D + R_L)}} \quad \rightarrow (5)$$

from which we see that C_2 introduces a third STC high-pass factor, giving the amplifier a third break frequency at

$$\omega_3 = \frac{1}{C_2(R_D + R_L)} \quad \rightarrow (6)$$

The overall low-frequency transfer function of the amplifier can be found by combining eq ⁽¹⁾ (2) & (5) and replacing the break frequencies by their symbols from eq (3), (4) & (6).

$$\frac{\tilde{V}_O}{\tilde{V}_{sig}} = - \left(\frac{R_G}{R_G + R_{sig}} \right) [g_m(R_D \parallel R_L)] \left(\frac{s}{s + \omega_{P1}} \right) \left(\frac{s}{s + \omega_{P2}} \right) \left(\frac{s}{s + \omega_3} \right)$$



The low-frequency magnitude response can be obtained from eq (1) by replacing ' s ' by $j\omega$ & finding $\frac{|V_o|}{|V_{sig}|}$. In many cases, however, one of the '3' break frequencies can be much higher than the other two, say by a factor greater than 4.

In such a case, it is this highest frequency break point that will determine the lower 3dB frequency f_L , and we do not have for instance, because the expression of ω_{p2} includes g_m , ω_{p2} is usually higher than ω_{p1} & ω_{p3} . If ω_{p2} is sufficiently separated from ω_{p1} & ω_{p3} , then -

$$f_L \approx f_{p2}$$

which means, the bypass capacitor determines the low end of the mid band.

It is important to find the time constant and hence the break frequency associated with each of the 3 capacitors. The procedure is simple:-

- 1) Reduce V_{sig} to zero.
- 2) Consider each capacitor separately, i.e., assume that the other 2 capacitors are acting as perfect short circuits.
- 3) For each capacitor, find the total resistance seen between its terminals. This is the resistance that determines the time constant associated with this capacitor.

⇒ Selecting values for the coupling and Bypass capacitors.

we now address the design issue of selecting appropriate values for C_1 , C_s & C_2 . The design objective is to place the lower 3dB frequency ' f_L ' at a specified value while minimizing the capacitor values.

As mentioned above ' C_s ' results in the highest of the '3' break frequencies, the total capacitance is minimized by selecting ' C_s '. So, that its break frequency $f_{p2} = f_L$. we then decide on the location of the other 2 break frequencies, say 5 to 10 times lower than the frequency of the dominant one f_L . However, the values selected for f_{p1} & f_{p3} should not be too low for that would require larger values for C_1 & C_2 than may be necessary.

→ Internal Capacitances and High Frequency Model of the MOSFET:- (8)

We know that MOSFET has internal capacitances i.e; gate-to-channel capacitance, however we did not account for the finite time required to charge and discharge the various internal capacitances. As a result, the device models we derived, such as the small-signal model, do not include any capacitances. The use of these models would predict constant amplifier gains independent of frequency.

We know, however, that this is not the case. In fact, the gain of every MOSFET amplifier falls off at some high frequency. To be able to predict these results, the MOSFET model must be augmented by including internal capacitances.

1) The gate capacitive effect:- The gate electrode forms a parallel-plate capacitor with the channel, with the oxide layer serving as the capacitor dielectric.

2) The source-body and drain-body depletion-layer capacitances
These are the capacitances of the reverse-biased pn junctions formed by the n^+ source region and the p-type substrate and by the n^+ drain region (the drain, diffusion) and the ^{p-type} substrate.

These two capacitive effects can be modeled by including capacitances in the MOSFET model between its four terminals, G, D, S, & B. There will be five capacitances in total: C_{gs} , C_{gd} , C_{gb} , C_{sb} and C_{db} , where

⇒ The Gate Capacitive Effects:-

The gate capacitive effect can be modeled by the three capacitances C_{gs} , C_{gd} , and C_{gb} . The values of these capacitances can be determined as follows:-

1) When the MOSFET is operating in the triode region at small V_{DS} , the channel will be of uniform depth. The gate-channel capacitance will be $WL C_{ox}$ and can be modeled by dividing it equally between the source and drain ends; thus.

$$C_{gs} = C_{gd} = \frac{1}{2} WL C_{ox} \text{ (triode region)}$$

└───────────> (1)

2) When the MOSFET operates in saturation, the channel has a tapered shape and is pinched off at (or) near the drain end. It can be shown that the gate-to-channel capacitance is approximately $\frac{2}{3} WL C_{ox}$ and can be modeled by assigning this entire amount to C_{gs} and a zero amount to C_{gd} . i.e;

$$\left. \begin{aligned} C_{gs} &= \frac{2}{3} WL C_{ox} \\ C_{gd} &= 0 \end{aligned} \right\} \text{ (saturation region)}$$

└───────────> (2)

3) When the MOSFET is ^{operates in} cut-off, the channel disappears, and thus $C_{gs} = C_{gd} = 0$. However, we can model the gate capacitive effect by assigning a capacitance $WL C_{ox}$ to the gate-body model capacitance, thus,

$$\left. \begin{aligned} C_{gs} &= C_{gd} = 0 \\ C_{gb} &= WL C_{ox} \end{aligned} \right\} \text{ (cut-off)}$$

└───────────> (3)

4). There is an additional small capacitive component that should be added to C_{gs} and C_{gd} in all the preceding formulas. This is the capacitance that results from the fact that the source & drain diffusions extend slightly under the gate oxide. If the overlap length is denoted L_{ov} , we see that the overlap capacitance component is

$$C_{ov} = W L_{ov} C_{ox} \quad \text{--- (4)}$$

Typically, $L_{ov} = 0.05$ to 0.1μ .

→ 2) The Junction Capacitances:-

The depletion-layer capacitances of the two reverse-biased pn junctions formed between each of the source & drain diffusions and the body can be determined by using the formula

$C_{jo} = A \sqrt{\left(\frac{\epsilon_s q}{2}\right) \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \left(\frac{1}{V_0}\right)}$. Thus for the source diffusion, we have the source body capacitance, C_{sb}

$$C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_{SB}}{V_0}}} \quad \text{--- (5)}$$

where; C_{sbo} is the value of C_{sb} at zero body bias

V_{SB} is the magnitude of the R.B voltage,

V_0 is the junction built-in voltage (0.6 to 0.8V)

Similarly, for the drain diffusion, we have the drain-body capacitance C_{db} ,

$$C_{db} = \frac{C_{dbo}}{\sqrt{1 + \frac{V_{DB}}{V_0}}} \quad \text{--- (6)}$$

where C_{dbo} is the capacitance value at zero R.B voltage.
 V_{DB} is the magnitude of this R.B voltage.

⇒ The High-frequency MOSFET Model:-

Below fig (a) shows the small-signal model of the MOSFET, including the four capacitances C_{gs} , C_{gd} , C_{sb} and C_{db} . This model can be used to predict the high-frequency response of MOSFET amplifiers. It is, however, quite complex for manual analysis, and its use is

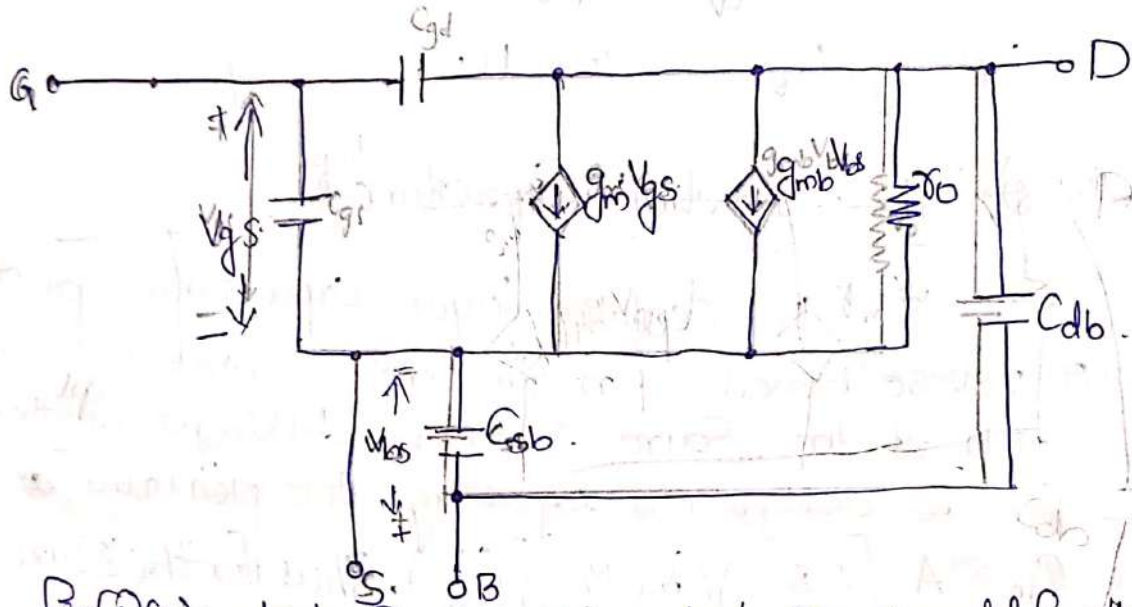


Fig 1(a):- high frequency equivalent circuit model for the MOSFET

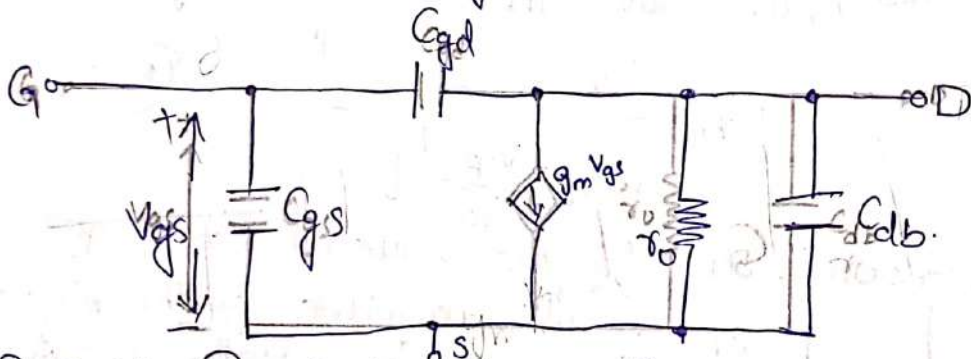


Fig 1(b):- The equivalent circuit for the case in which the source is connected to the substrate (body).

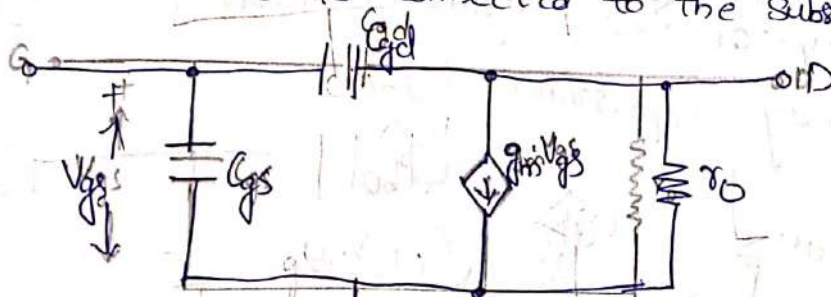


Fig 1(c):- The equivalent circuit model of Fig 1(b) with C_{db} neglected

High frequency equivalent circuit model for the MOSFET. (a) The equivalent circuit for the case in which the source is connected to the substrate (body). (b) The equivalent circuit model of (a) with C_{ab} neglected (to simplify analysis).

Limited to Computer simulation using, for example, SPICE. Fortunately, for the case when the source is connected to the body, the model simplifies considerably, as shown in Fig: 1(b). In this model, C_{gs} , although small, plays a significant role in determining the high-frequency response of amplifiers and thus must be kept in the model. Capacitance C_{db} , on other hand, can usually be neglected, resulting in significant simplification of manual analysis. The resulting circuit is shown in Fig 1(c).

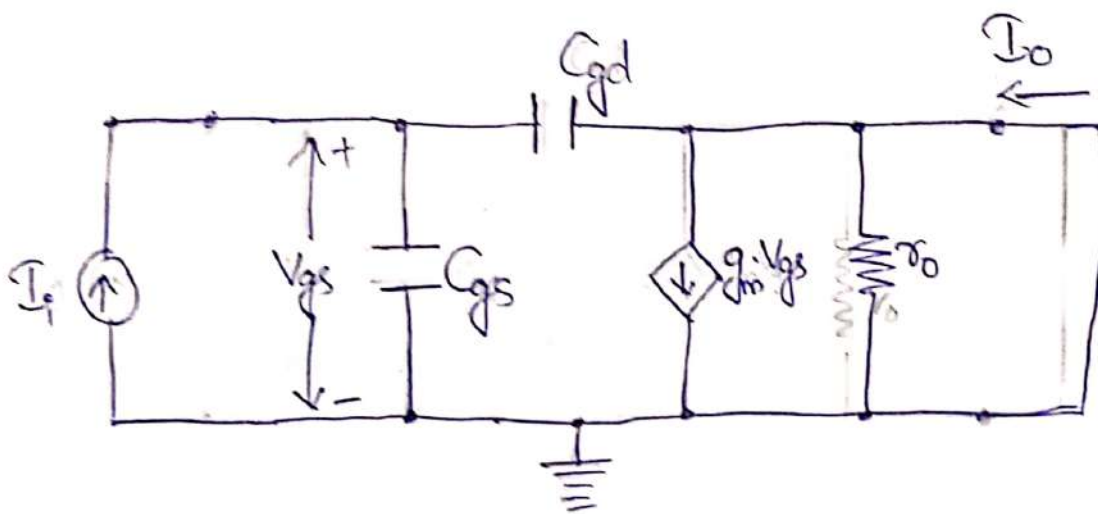


Fig 1(c) Determining the short-circuit current gain $\frac{I_o}{I_i}$.

⇒ Internal Capacitive Effects and the High-Frequency Model of the BJT:-

The transistor models we have developed do not include any elements (i.e., capacitors (or) inductors) that would cause time (or) frequency dependence.

Actual transistors, however, exhibit charge storage phenomena that limit the speed and frequency of their operation.

We have already encountered such effects in our study of the pn junction and learned that they can be modeled using capacitances.

In the following we study the charge-storage effects that take place in the BJT and them into account by adding capacitances to the hybrid- π model.

The resulting augmented BJT model will be able to predict the observed dependence of amplifier gain on frequency and the time delays that transistor switches and logic gates exhibit.

⇒ The Base-charging (or) Diffusion Capacitance C_{de}

When the transistor is operating in the active (or) saturation modes, minority-carrier charge is in the case of an npn transistor operating in the active mode $Q_n = \frac{A_E q W n_i^2}{2 N_A} e^{V_{BE}/V_T}$ using the result in eq (1) together with eq's $i_C = I_S e^{V_{BE}/V_T}$ and $I_S = \frac{A_E q D_n n_i^2}{N_A W}$. we can express Q_n in terms of the collector current i_C as

$$Q_n = \frac{W^2}{2 D_n} i_C = \tau_F i_C \quad \text{--- (2)}$$

where; τ_F is a device constant,

$$\tau_F = \frac{W^2}{2 D_n} \quad \text{--- (3)}$$

with the dimension of time. It is known as the base-transit time and represents the average time a charge carrier (electron) spends in crossing the base. Typically, τ_F is in the range of 10ps to 100ps.

For operation in the reverse active mode, a corresponding constant τ_R applies and is many orders of the magnitude larger than τ_F .

eq (2) applies for large signals, and since Q_n is exponentially related to V_{BE} , Q_n will similarly depend on V_{BE} . Thus this charge-storage mechanism represents a non-linear capacitive effect. However, for small signal diffusion capacitance C_{de} .

$$C_{de} \equiv \frac{dQ_n}{dV_{BE}} \longrightarrow (4)$$

$$= \tau_F \cdot \frac{dI_C}{dV_{BE}}$$

resulting in

$$C_{de} = \tau_F \cdot g_m = \tau_F \cdot \frac{I_C}{V_T} \longrightarrow (5)$$

$\Rightarrow$ The Base-emitter Junction Capacitance C_{je} :

Using the development in Diodes, and in particular eq $A_V = \frac{V_{CC} - V_{CEsat}}{V_T}$, the base-emitter junction (or) depletion-layer capacitance C_{je} can be expressed as

$$C_{je} = \frac{C_{je0}}{\left(1 - \frac{V_{BE}}{V_{oe}}\right)^m} \longrightarrow (6)$$

where, C_{je0} is the value of C_{je} at zero voltage, V_{oe} is the EBJ built-in voltage (0.7V), m is grading co-efficient of the EBJ junction. (Typically, 0.5).

It turns out, however, that because r_{be} is forward biased in the active mode, eq (6) does not provide an accurate prediction of C_{je} . Alternatively, one typically uses an approximate value for C_{je} .

$$C_{je} \cong 2 C_{je0} \quad \rightarrow (7)$$

⇒ The collector-base junction capacitance C_{cb} :

In active-mode operation, the CBJ is reverse biased, and its junction (or) depletion capacitance, usually, denoted ' C_{cb} ', can be found from.

$$C_{cb} = \frac{C_{cb0}}{\left(1 + \frac{V_{cb}}{V_{oc}}\right)^m} \quad \rightarrow (8)$$

where; C_{cb0} is the value of C_{cb} at zero voltage.
 V_{oc} is the CBJ built-in voltage (typically, 0.75V)
 m is its grading coefficient (typically, 0.2-0.5)

⇒ The High-Frequency Hybrid- π model:-

The below Fig (1) shows the hybrid- π model of BJT, including capacitive effects. Specifically, there are two capacitances: the emitter-base capacitance $C_{\pi} = C_{de} + C_{je}$ and the collector-base capacitance C_{cb} .

Typically, C_{π} is in the range of a few picofarads to a few tens of picofarads, and C_{cb} is in the range of a fraction of a picofarad to a few picofarads.

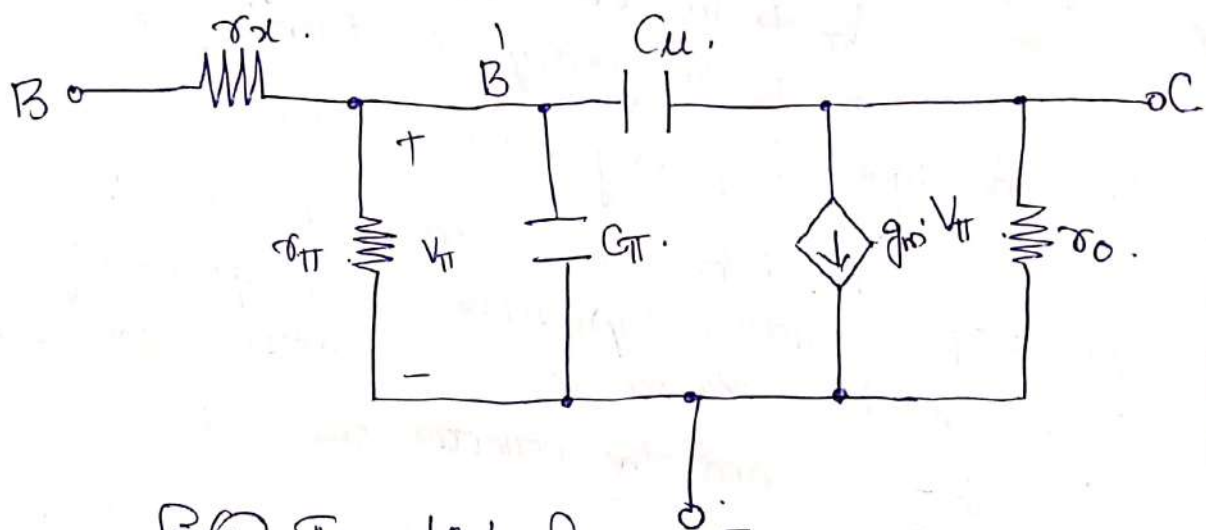
Note that we have also added a resistor r_x to model the resistance of the silicon material of the base region between the base terminal B and a

intrinsic, base terminal B' that is right under the emitter region.

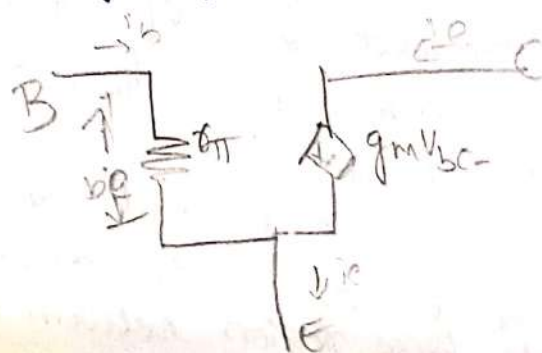
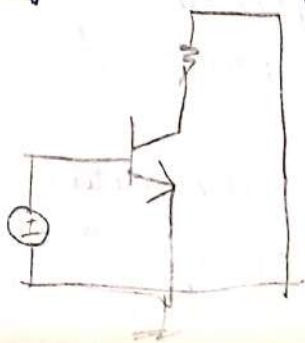
Since $\tau_b \ll \tau_{\pi}$, its effect is negligible at low frequencies.

The values of the hybrid- π equivalent circuit parameters can be determined at a given bias point using the formulas. They can also be found from the terminal measurements specified on the BJT data sheets. For computer simulation, SPICE uses the parameters of the given IC technology to evaluate the BJT model parameters.

A note on notation is in order. Since, we are now dealing with voltages & currents that are functions of frequency, we have reverted to using symbols that are upper case letters (eg: V_{π} , I_C).



Fig(1) The high-frequency hybrid- π model.



⇒ The High-Frequency Response of CE Amplifier: (B)

To determine the gain, (or) the transfer function, of the CE amplifier at high frequencies, and in particular the upper 3dB frequency f_H , we replace the BJT with the high frequency model of BJT. At these frequencies C_1, C_2 & C_E will be behaving as perfect short circuits. The result is the high-frequency amplifier equivalent circuit shown in below Fig (1a).

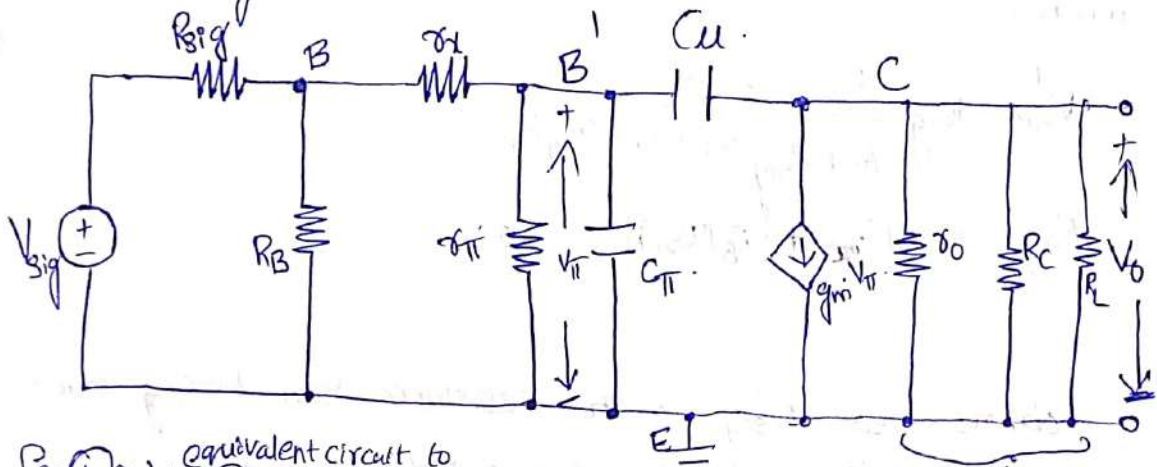
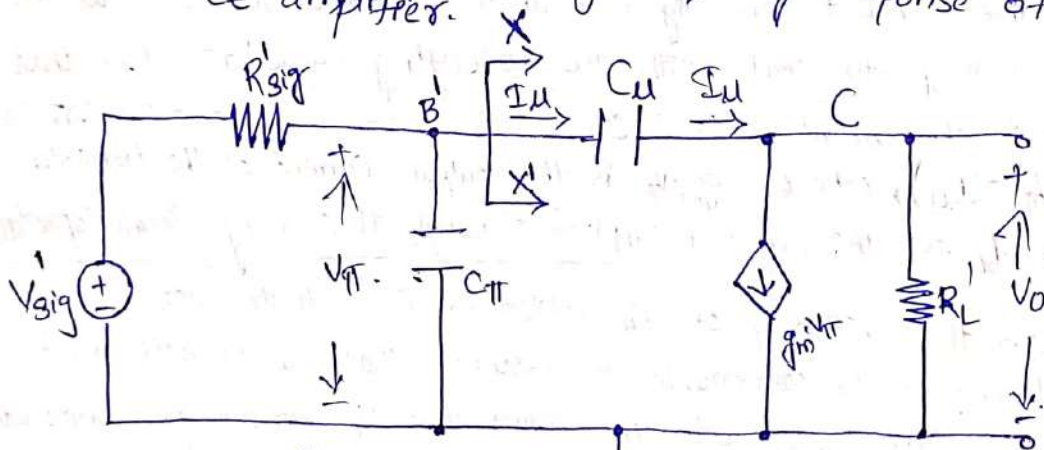


Fig (1a): equivalent circuit to determine the high-frequency response of the CE amplifier.



$$V'sig = Vsig \cdot \frac{R_B}{R_B + Rsig} \cdot \frac{r_{\pi}}{r_{\pi} + r_x + (Rsig \parallel R_B)}$$

$$R'sig = r_{\pi} \parallel [r_x + (R_B \parallel Rsig)]$$

$$R'_L = r_o \parallel R_C \parallel R_L$$

Fig (1b) simplified circuit of (1a) at both input side & the output side.

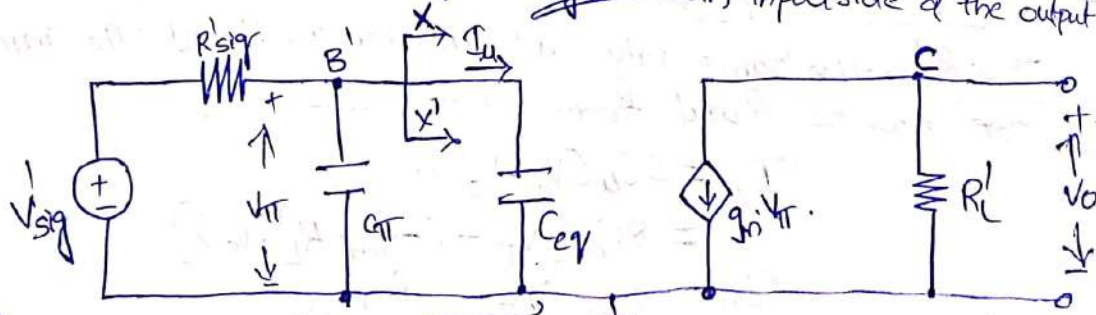


Fig (1c) Equivalent circuit with C_{π} replaced with C_{eq} .

$$C_{in} = C_{\pi} + C_{eq} = C_{\pi} + \frac{C_{\pi} (1 + g_m R'_L)}{1 + g_m R'_L}$$

$$V_o = -g_m R'_L V_{tr}$$

The equivalent circuit of Fig(1a) can be simplified by utilizing Thevenin theorem at the input side and by combining the 3 parallel resistances at the output side. Specifically, the reader should be able to show that applying Thevenin theorem twice simplifies the resistive network at the input side to a signal generator V_{sig} and a resistance R_{sig} .

where;

$$V'_{sig} = V_{sig} \cdot \frac{R_B}{R_B + R_{sig}} \cdot \frac{r_{\pi}}{r_{\pi} + r_x + (R_{sig} \parallel R_{B3})} \quad \text{---> (1)}$$

$$R'_{sig} = r_{\pi} \parallel [r_x + (R_B \parallel R_{sig})] \quad \text{---> (2)}$$

observe that R'_{sig} is the resistance seen looking back into the resistive network between nodes B' and E .

The circuit in Fig(1c) can be simplified further if we can find a way to deal with the bridging capacitance C_u that connects the output node. It can be seen that the load current is $(g_m V_{\pi} - I_u)$, where $g_m V_{\pi}$ is the output current of the transistor and I_u is the current supplied through the very small capacitance.

In the vicinity of f_H , which is close to the edge of the midband, it is reasonable to assume that I_u is still much smaller than $g_m V_{\pi}$, with the result that V_o can be given approximately by $V_o \approx -g_m V_{\pi} R_L' = -g_m R_L' V_{\pi}$ ---> (3)

Since, $V_o = C_u$, eq(3) indicates that the gain from B' to C' is $-g_m R_L'$, the same value as in the midband. The current I_u can now be found from

$$\begin{aligned} I_u &= sC_u(V_{\pi} - V_o) \\ &= sC_u[V_{\pi} - (-g_m R_L' V_{\pi})] \\ I_u &= sC_u(1 + g_m R_L') V_{\pi} \end{aligned}$$

Now, in fig (b), the left hand-side of the circuit at $X'X'$, knows of the existence of C_u only through the current I_u . Therefore, we can replace C_u by an equivalent capacitance C_{eq} between B' and ground as long as C_{eq} draws a current equal to I_u . That is,

$$sC_{eq} V_{\pi} = I_u = sC_u (1 + g_m R_L') V_{\pi}$$

which results in

$$C_{eq} = C_u (1 + g_m R_L') \longrightarrow (4)$$

Using C_{eq} enables us to simplify the equivalent circuit at the input side to that shown in fig (1c), which we recognize as a single-time-constant (STC) network of the low-pass type. There we can express V_{π} in terms of V_{sig}' as

$$V_{\pi} = V_{sig}' \frac{1}{1 + \frac{s}{\omega_0}} \longrightarrow (5)$$

where; ω_0 is the corner frequency of the STC network composed of C_{in} and R_{sig}' .

$$\omega_0 = \frac{1}{C_{in} R_{sig}'} \longrightarrow (6)$$

where; C_{in} is the total input capacitance at B' .

$$C_{in} = C_{\pi} + C_{eq} = C_{\pi} + C_u (1 + g_m R_L') \longrightarrow (7)$$

and R_{sig}' is the effective source resistance, given by eq (2). Combining eq. Am (5) & (6) give the voltage gain in the high-frequency band as

$$\frac{V_o}{V_{sig}} = - \left[\frac{R_B}{R_B + R_{sig}'} \cdot \frac{\tau_{\pi} g_m R_L'}{\tau_{\pi} + \tau_x + (R_{sig}' \parallel R_B)} \right] \left[\frac{1}{1 + \frac{s}{\omega_0}} \right] \times \left[\frac{R_L}{R_L + R_{sig}'} \right]$$

The quantity between the square brackets of eq (8) is the midband gain, and except for the fact that here τ_x is taken into account, this expression is the same as that in A_m . Thus,

$$\frac{V_o}{V_{sig}} = \frac{A_m}{1 + \frac{s}{\omega_0}} \longrightarrow (9)$$

from which we deduce that the upper 3-dB frequency f_H' must be.

$$f_H = \frac{\omega_0}{2\pi} = \frac{1}{2\pi C_{in} R_{sig}'} \rightarrow (9)$$

Thus, we see that the high-frequency response will be that of a low-pass STC network with a 3-dB frequency f_H determined by the time constant $C_{in} R_{sig}'$. Fig (1d) shows a sketch of the magnitude of the high-frequency gain.

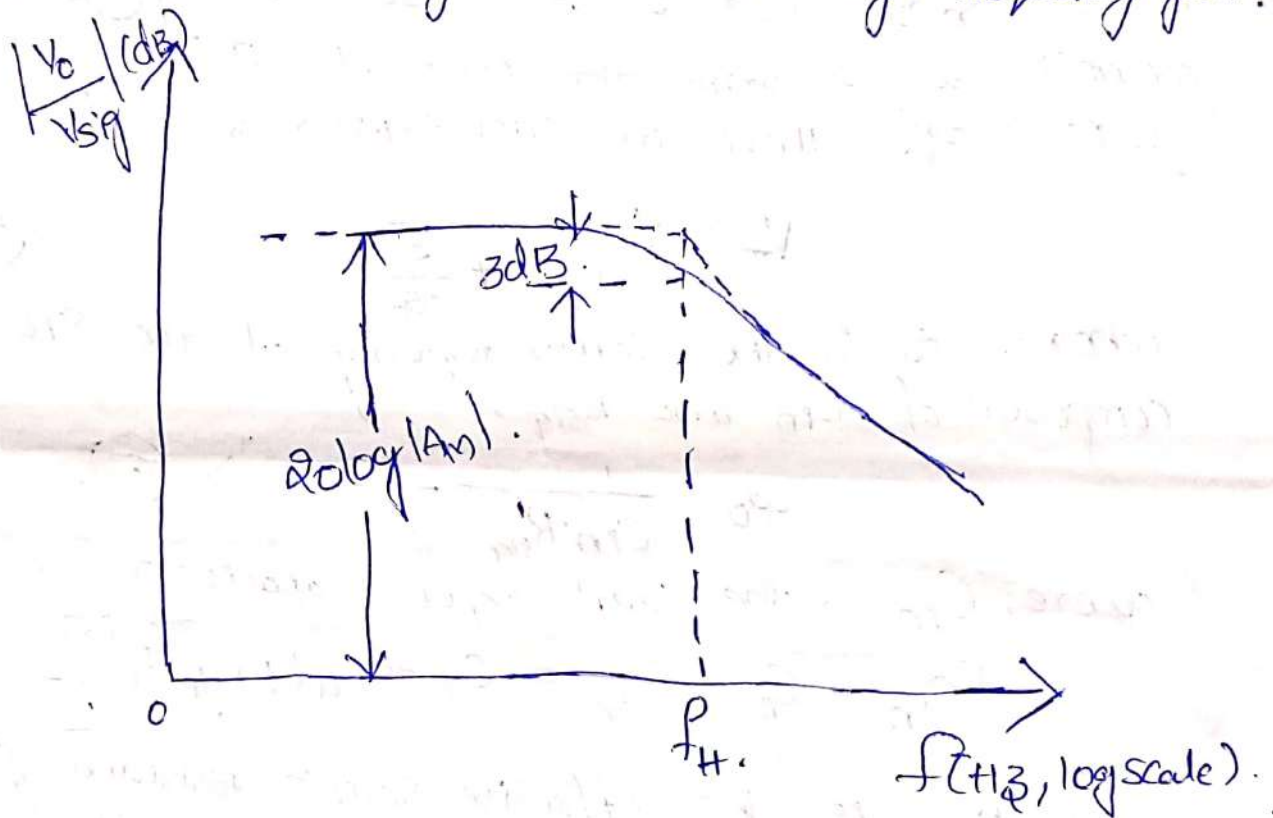


Fig (1d) Sketch of the frequency-response plot, which is that of a low-pass STC circuit.

⇒ The High-Frequency Response of CS Amplifier: ¹⁵

To determine the gain (or) the transfer function, of the amplifier of CS amplifier at high frequencies, and particularly the upper 3-dB frequency f_H , we replace the MOSFET with its high-frequency model. At this frequency C_1, C_2 and C_s will be behaving as perfect short circuits. The result is the high-frequency amplifier equivalent circuit shown in fig (a).

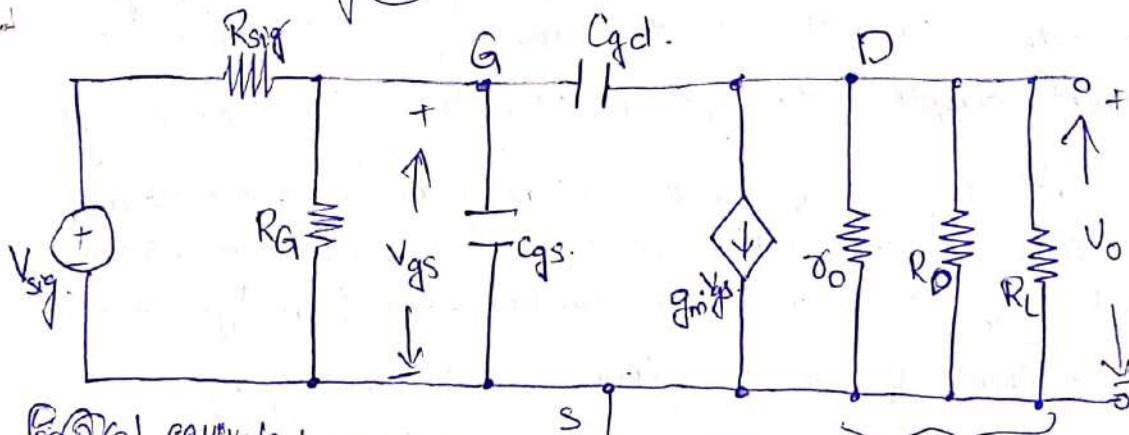


Fig 2(a) equivalent circuit to determine the high-freq. of CS amplifier.

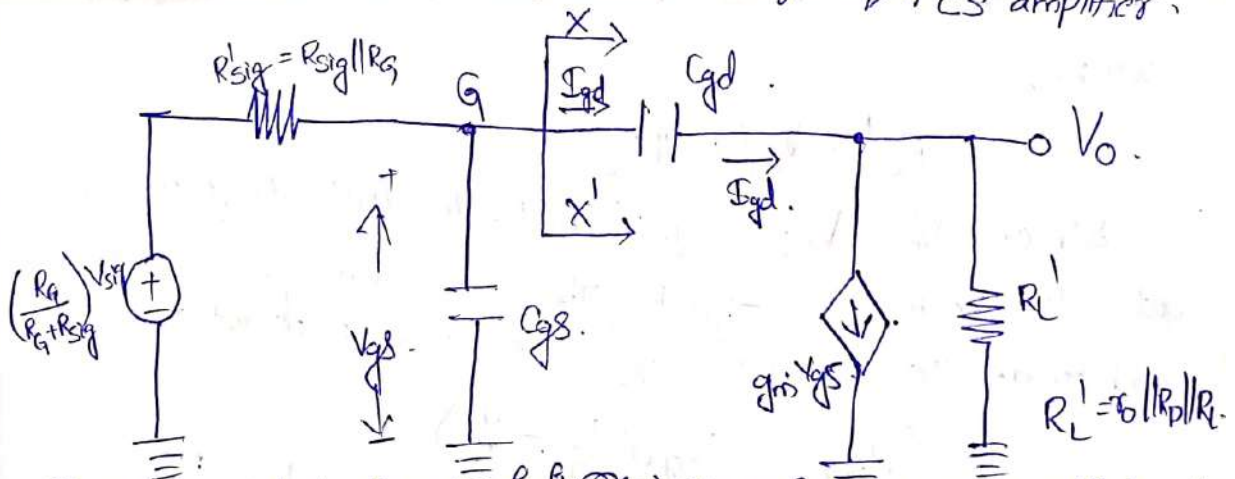


Fig 2(b) equivalent circuit of fig 2(a) simplified at the input & the output

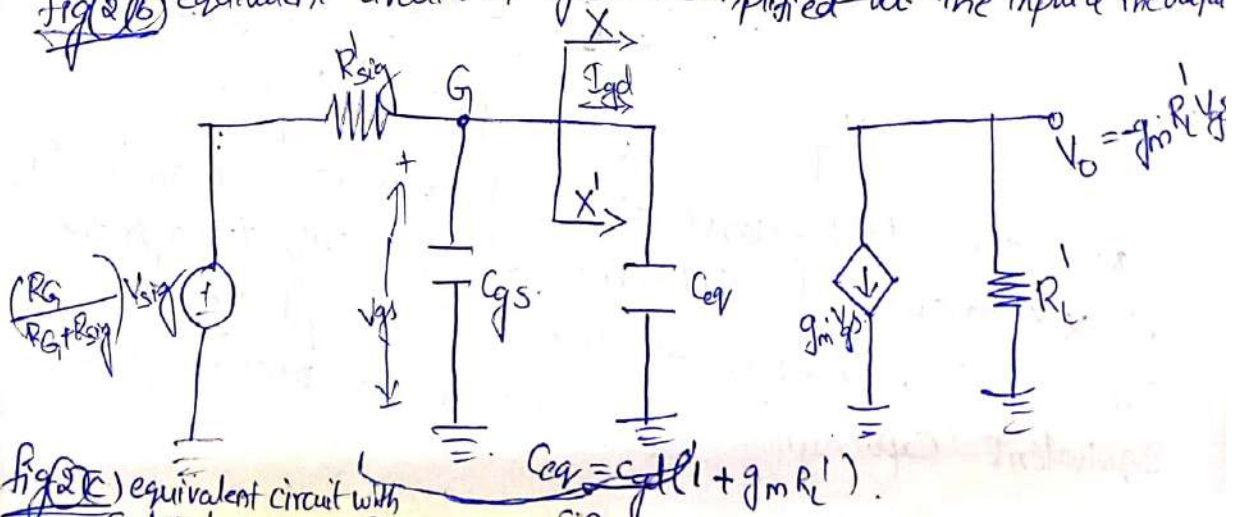


Fig 2(c) equivalent circuit with $C_{eq} = C_{gd}(1 + g_m R_L')$

The equivalent circuit of fig(2a) can be simplified by utilising the Thevenin theorem at the input side and by combining the three parallel resistances at the output side. The resulting simplified circuit is shown in fig(2b).

The circuit can be further simplified if we can find a way to deal with the bridging capacitor C_{gd} that connects the output node to the input side. Toward that end, consider first the output node. It can be seen that the load current is $(g_m V_{gs} - I_{gd})$, where $(g_m V_{gs})$ is the output current of the transistor and I_{gd} is the current supplied through the very small capacitance C_{gd} .

At frequencies in the vicinity of f_{π} , which defines the edge of the mid band, it is reasonable to assume that I_{gd} is still much smaller than $(g_m V_{gs})$. With the result that V_o can be given approximately by

$$V_o \cong (-g_m \cdot V_{gs}) R_L' = -g_m R_L' V_{gs} \quad \text{--- (1)}$$

where;

$$R_L' = r_o \parallel R_D \parallel R_L$$

Since, $V_o = V_{ds}$, eq(1) indicates that the gain from gate to drain is $-g_m R_L'$, the same value as in the mid-band. The current I_{gd} can now be found as

$$\begin{aligned} I_{gd} &= s C_{gd} (V_{gs} - V_o) \\ &= s C_{gd} [V_{gs} - (-g_m R_L' V_{gs})] \end{aligned}$$

$$I_{gd} = s C_{gd} (1 + g_m R_L') V_{gs}$$

Now, the left-hand side of the circuit in fig(2b), at X_X' , knows of existence of C_{gd} only through the current I_{gd} . Therefore, we can replace C_{gd} by an equivalent capacitance C_{eq} between the gate and ground.

as long as C_{eq} draws a current equal to I_{gd} , (16)

That is, $sC_{eq}V_{gs} = sC_{gd}(1+g_m R_L')V_{gs}$.

which results in.

$$C_{eq} = C_{gd}(1+g_m R_L') \rightarrow (2)$$

Using C_{eq} enables us to simplify the equivalent circuit at the input side to that shown in Fig (2)(c). We recognize the circuit of Fig (2)(c) as a single-time-constant (STC) circuit of the low-pass type. We can express the output voltage V_{gs} of the STC circuit in the form

$$V_{gs} = \left(\frac{R_G}{R_G + R_{sig}} V_{sig} \right) \cdot \frac{1}{1 + \frac{s}{\omega_0}} \rightarrow (3)$$

where, ω_0 is the corner frequency (or) the break frequency of the STC circuit,

$$\omega_0 = \frac{1}{C_{in} R_{sig}} \rightarrow (4)$$

with $C_{in} = C_{gs} + C_{eq} = C_{gs} + C_{gd}(1+g_m R_L') \rightarrow (5)$

and $R_{sig}' = R_{sig} \parallel R_G \rightarrow (6)$

Combining eqs (1) and (3) results in the following expression for the high-frequency gain of the CS amplifier,

$$\frac{V_o}{V_{sig}} = - \left[\frac{R_G}{R_G + R_{sig}} \right] (g_m R_L') \cdot \frac{1}{1 + \frac{s}{\omega_0}} \rightarrow (7)$$

which can be expressed in the form

$$\frac{V_o}{V_{sig}} = \frac{A_M}{1 + \frac{s}{\omega_H}} \rightarrow (8)$$

where the mid-band gain A_m is given by eq.
 ω_H is the upper 3dB frequency,

$$\omega_H = \omega_0 = \frac{1}{C_{in} \cdot R_{sig}} \quad \text{--- (9)}$$

and

$$f_H = \frac{\omega_H}{2\pi} = \frac{1}{2\pi C_{in} \cdot R_{sig}} \quad \text{--- (10)}$$

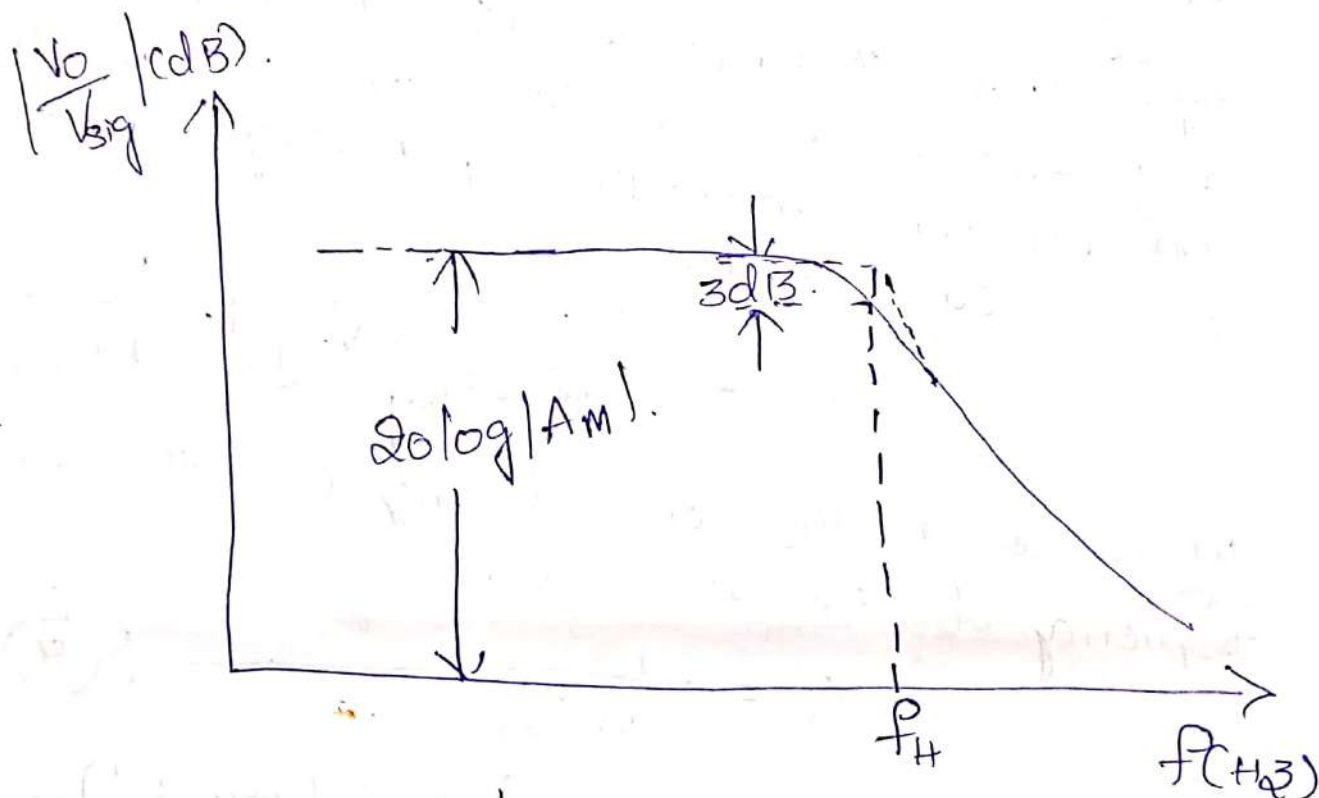


Fig (2)(d) : ^{high} the frequency response plot.

Frequency Response of the MOS Cascode Amplifier

The below fig 1 shows the Cascode amplifier with all transistor internal capacitances indicated. Also included a capacitance C_L at the output node to represent the combination of C_{db2} , the input capacitance of a succeeding amplifier stage, and a load capacitance. Note that C_{db1} & C_{gs2} appear in parallel, and we shall combine them in the following analysis. Similarly, C_L and C_{gd2} appear in parallel and will be combined.

The easiest approach to determining the 3dB frequency f_{3dB} is to employ the open-circuit time-constants method.

- 1) Capacitance C_{gs1} sees a resistance R_{sig} .
- 2) Capacitance C_{gd1} sees a resistance R_{gd1} , which can be obtained by adapting the formula $R_{gd} = R_{sig}(1 + g_m R_D)$ to $R_{gd1} = (1 + g_{m1} R_{D1}) R_{sig} + R_{D1}$ ————— (1)

where, R_{D1} , the total resistance at D_1 .

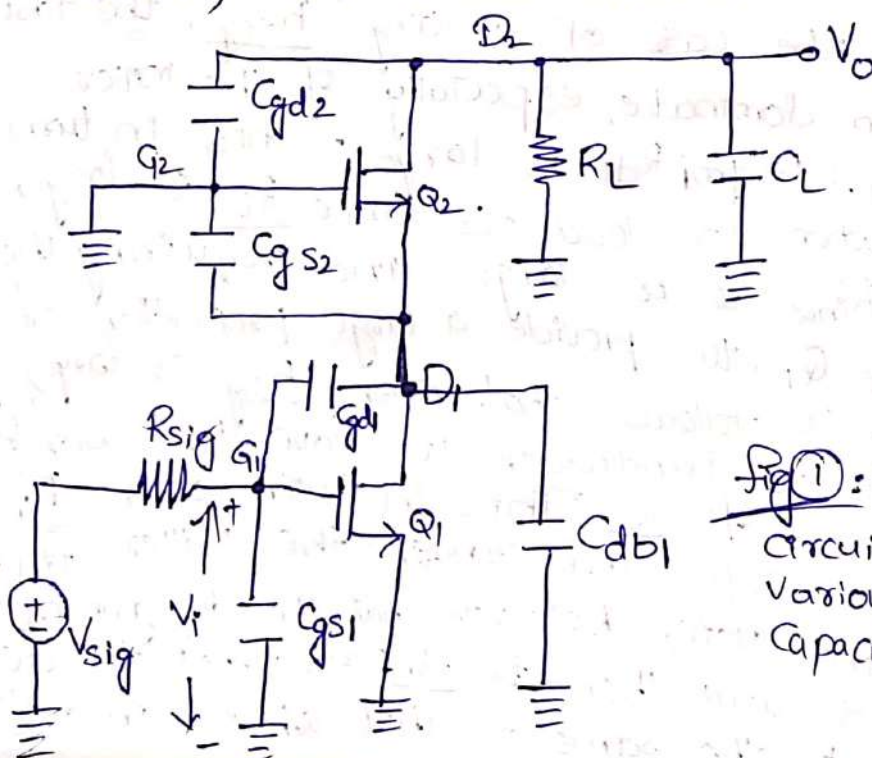


Fig 1: The Cascode circuit with the various transistor capacitances indicated.

- 3) Capacitance $(C_{db1} + C_{gs2})$ sees a resistance $\underline{R_{d1}}$.
 4) Capacitance $(C_L + C_{gd2})$ sees a resistance $(R_L \parallel R_{out})$.
 With the resistances determined, the effective time constant τ_H can be computed as.

$$\tau_H = C_{gs1} R_{sig} + C_{gd1} [(1 + g_{m1} R_{d1}) R_{sig} + R_{d1}] + (C_{db1} + C_{gs2}) R_{d1} + (C_L + C_{gd2}) (R_L \parallel R_{out}).$$

and the 3-dB frequency $\underline{f_H}$ as. (2)

$$f_H \approx \frac{1}{2\pi \tau_H}.$$

To gain insight regarding what limits the high-frequency gain of the MOS cascode amplifier we rewrite eq (2) in the form.

$$\tau_H = R_{sig} [C_{gs1} + C_{gd1} (1 + g_{m1} R_{d1})] + R_{d1} (C_{gd1} + C_{db1} + C_{gs2}) + (R_L \parallel R_{out}) (C_L + C_{gd2})$$
(3)

In the case of a large $\underline{R_{sig}}$, the first term can dominate, especially if the Miller multiplier $(1 + g_{m1} R_{d1})$ is large. This in turn happens when the load resistance $\underline{R_L}$ is large, causing R_{in2} to be large and requiring the first stage, Q_1 , to provide a large proportion of the gain. It follows that when $\underline{R_{sig}}$ is large, to extend the bandwidth we have to lower $\underline{R_L}$ to the order of $\underline{r_o}$. This in turn lowers $\underline{R_{in2}}$ and hence $\underline{R_{d1}}$ and renders the Miller effect insignificant. Note, however, that the dc gain of the cascode will then be $\underline{A_o}$. Thus, while the dc gain will be the same as that achieved in a CS amplifier, the band-width will be greater.

In the case when R_{sig} is small, the Miller effect in Q_1 will not be of concern. A large value of ' R_L ' can then be used to realize the large dc gain possible with a cascode amplifier - that is, a dc gain on the order of A_0^2 . eq (3) indicates that in this case the third term will usually be dominant. To pursue this point a little further, consider the case $R_{sig} = 0$, and assume that the middle term is much smaller than the third term. It follows that.

$$C_{u1} \cong (C_L + C_{gd2})(R_L \parallel R_{out})$$

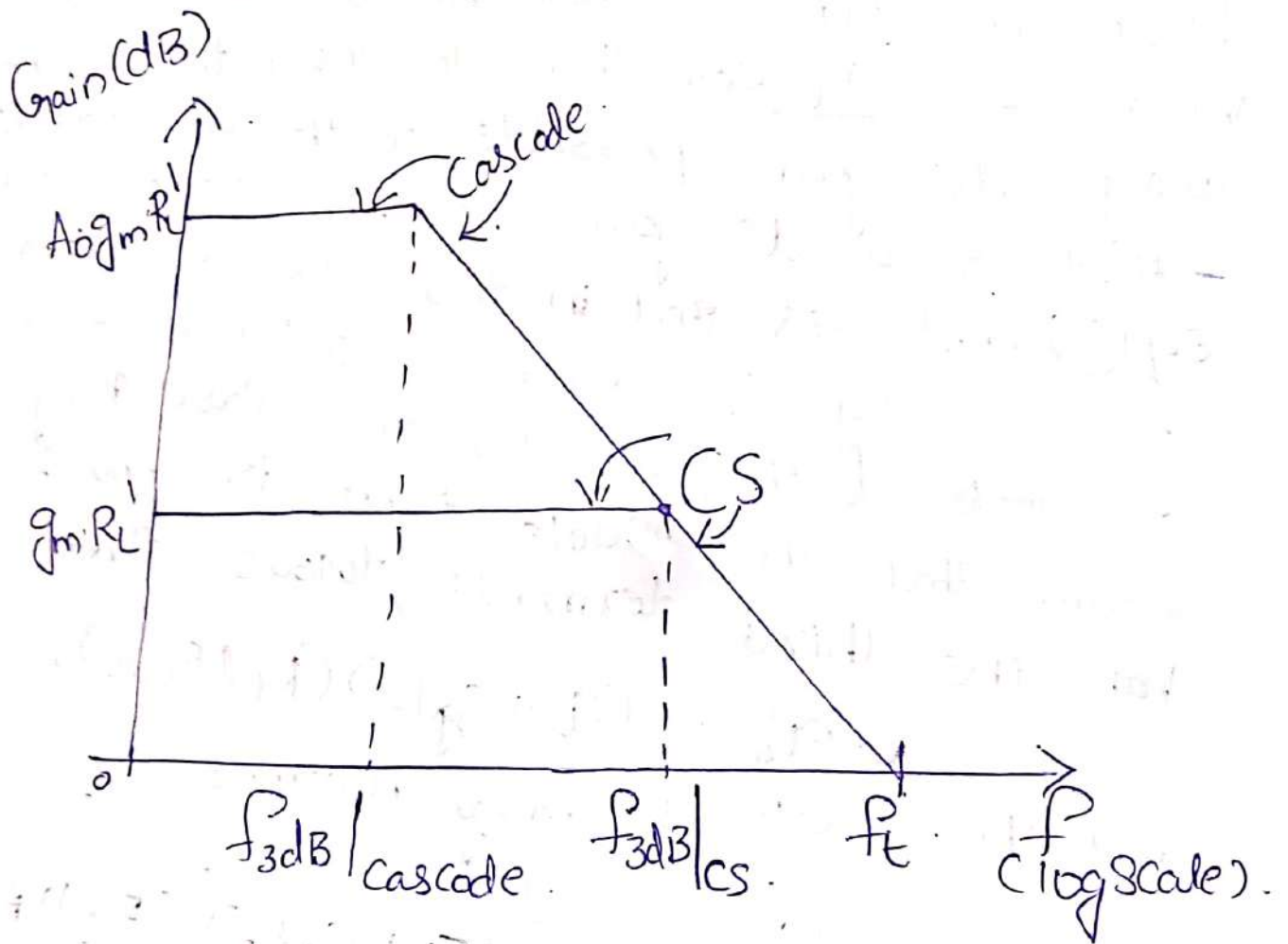
and the 3dB frequency becomes.

$$f_H \cong \frac{1}{2\pi (C_L + C_{gd2})(R_L \parallel R_{out})}$$

which is of the same form as the formula for the CS amplifier with $R_{sig} = 0$. Here, however, $(R_L \parallel R_{out})$ is larger than R_L by a factor of about A_0 . Thus, the f_H of the cascode will be lower than that of the CS amplifier by the same factor A_0 . The below fig (2) shows a sketch of the frequency response of the cascode & of the corresponding common-source amplifier. we observe that in this case, cascoding increases the dc gain by a factor A_0 while keeping the unity-gain frequency unchanged at.

$$f_t \cong \frac{1}{2\pi} \cdot \frac{g_m}{C_L + C_{gd2}}$$

→ (4) = Circuit



Fig(2) Effect of cascoding on gain & B.W
in the case $R_{sig} = 0$.

(19)

Frequency Response of the Source Follower:-

A major advantage of the source follower is its excellent high-frequency response. Because, none of the internal capacitances suffers from the Miller effect. The below fig (1)(a) shows the high-frequency equivalent circuit of a source follower fed with a signal V_{sig} from a source having a resistance R_{sig} . In addition to the MOSFET capacitances C_{gs} & C_{gd} , a capacitance C_L is included between the output node & ground to account for the source-to-body capacitance C_{sb} as well as any actual load capacitance.

(The simplifications performed above on the low frequency equivalent)

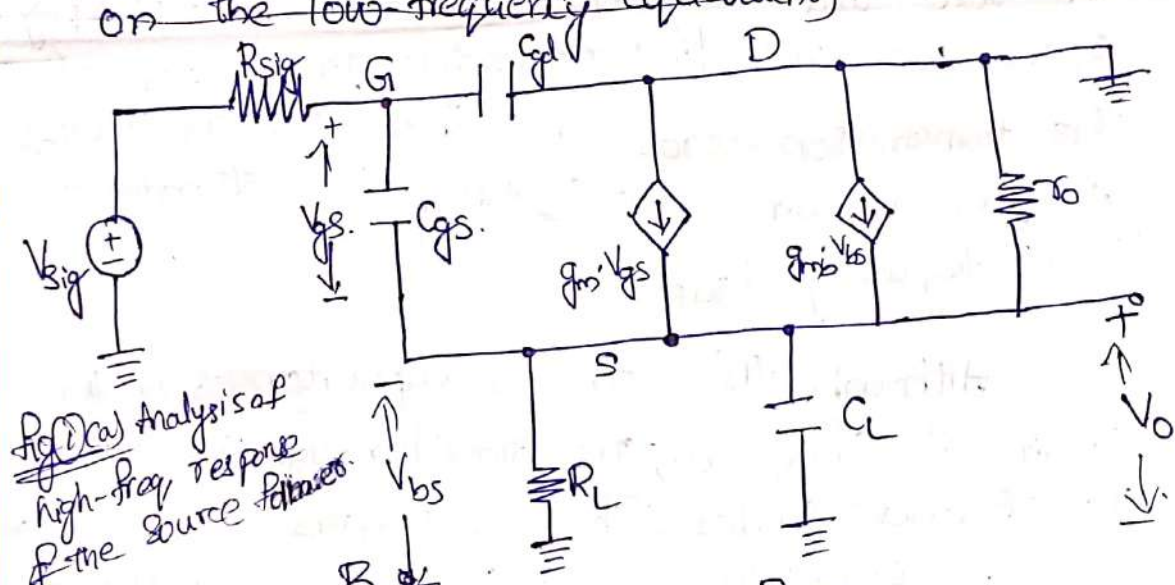


Fig (1)(a) Analysis of high-freq response of the source follower

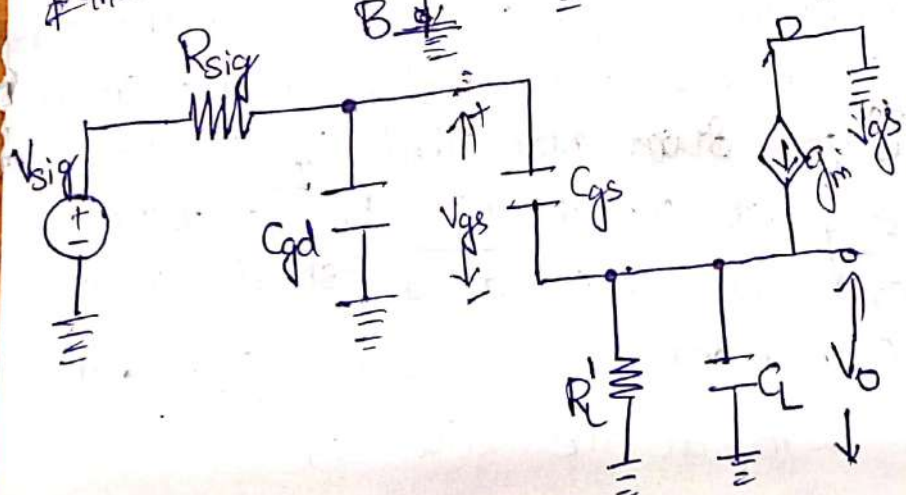
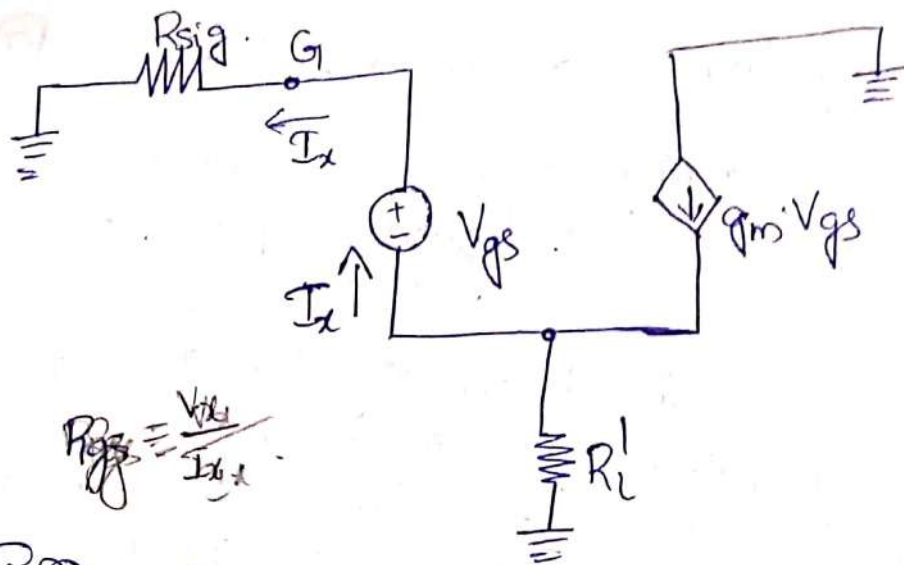


Fig (1)(b) Simplified equivalent circuit



Fig(1c) determining the resistance R_{gs} seen by G_s

The Simplifications performed above on the low-frequency equivalent circuit can be applied to the high-frequency model of Fig(1a). Although one can derive an expression for insight regarding the role that each of the three Capacitances plays. Rather, we shall first determine the location of the transmission zeros and then use the method of open-circuit time constants to estimate the 3-dB frequency, f_{3dB} .

Although there are 3 Capacitances in the circuit of Fig(1b), the transfer function is of the Second order. This is because the 3 Capacitors form a continuous loop. To determine the location of the two transmission zeros, refer to the circuit in Fig(1b), and ~~start~~ note that V_o is zero at the frequency at which C_L has a zero impedance and thus acts as a short circuit across the output, which is ω (or) $s = \infty$. Also, V_o will be zero at the value of 's' that

Causes the Current into the impedance $R_L \parallel C_L$ to be zero. Since this Current is $(g_m + sC_{gs})V_{gs}$, the transmission zero will be at $s = s_z$, where

$$s_z = \frac{-g_m}{C_{gs}} \longrightarrow (1)$$

i.e.; the zero will be on the negative real axis of the s-plane with a frequency.

$$\omega_z = \frac{g_m}{C_{gs}} \longrightarrow (2)$$

Recalling that the MOSFET's $\omega_T = \frac{g_m}{C_{gs} + C_{gd}}$ and that $C_{gd} \ll C_{gs}$, we see that ω_z will be very close to ω_T .

$$f_z \approx f_T \longrightarrow (3)$$

Next, we turn our attention to the poles. Specifically, we will find the resistance seen by each of three capacitances C_{gd} , C_{gs} and C_L and then compute the time constant associated with each. With V_{sig} set to zero and C_{gs} & C_L assumed to be open circuited, we find by inspection that the resistance R_{gd} seen by C_{gd} is given by.

$$R_{gd} = R_{sig} \longrightarrow (4)$$

This is intuitively obvious: Because of the ground at the drain terminal, the input capacitance of the source follower, in the absence of C_{gs} & C_L is equal to C_{gd} . Thus, R_{sig} and C_{gd} form a high-frequency pole.

Next, we consider the effect of C_{gs} . The resistance R_{gs} seen by C_{gs} can be determined by straight forward analysis of the circuit in fig ①(c) to obtain.

$$R_{gs} = \frac{R_{sig} + R_L'}{1 + g_m R_L'} \rightarrow \text{⑥}$$

We note that the factor $(1 + g_m R_L')$ in the denominator will result in reducing the effective resistance with which C_{gs} interacts. In the absence of the two other capacitances, C_{gs} together with R_{gs} introduces a pole with frequency $\frac{1}{2\pi C_{gs} R_{gs}}$.

Finally, it is easy to see from the circuit in fig ①(b) that C_L interacts with $R_L \parallel R_o$;

$$\text{i.e., } R_{CL} = R_L \parallel R_o$$

usually, R_o is low. Thus R_{CL} will be low, and the effect of C_L will be small.

Nevertheless, all three time constants can be added to obtain τ_H and hence f_H . i.e., $\tau_H = C_{gd} R_{sig} + C_{gs} R_{gs} + C_L R_{CL}$

then

$$f_H = \frac{1}{2\pi \tau_H} = \frac{1}{2\pi (C_{gd} R_{sig} + C_{gs} R_{gs} + C_L R_{CL})}$$

⑦

⇒ Frequency Response of Emitter Follower: 21

The below fig (a) shows an emitter follower suitable for IC fabrication. It is biased by a Constant-Current Source I . However, the circuit that sets the dc voltage at the base is not shown. The emitter follower is fed with a signal V_{sig} from a source with resistance R_{sig} . The resistance R_L shown at the output, includes the output resistance of Current Source I as well as any actual load resistance.

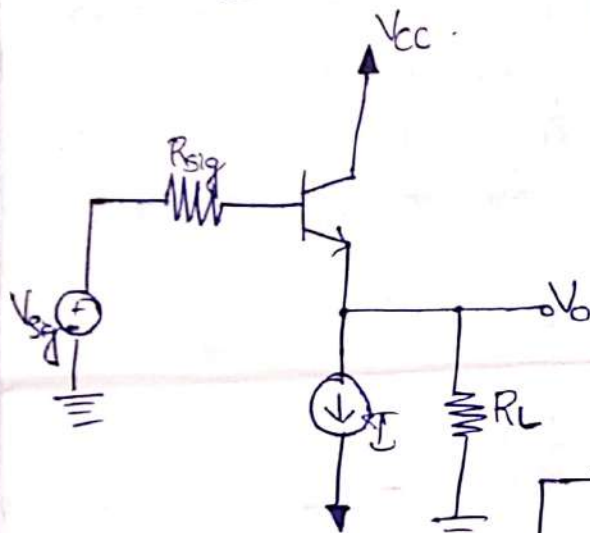


Fig 1(a) emitter follower

Fig 1(b) high-frequency equivalent circuit.

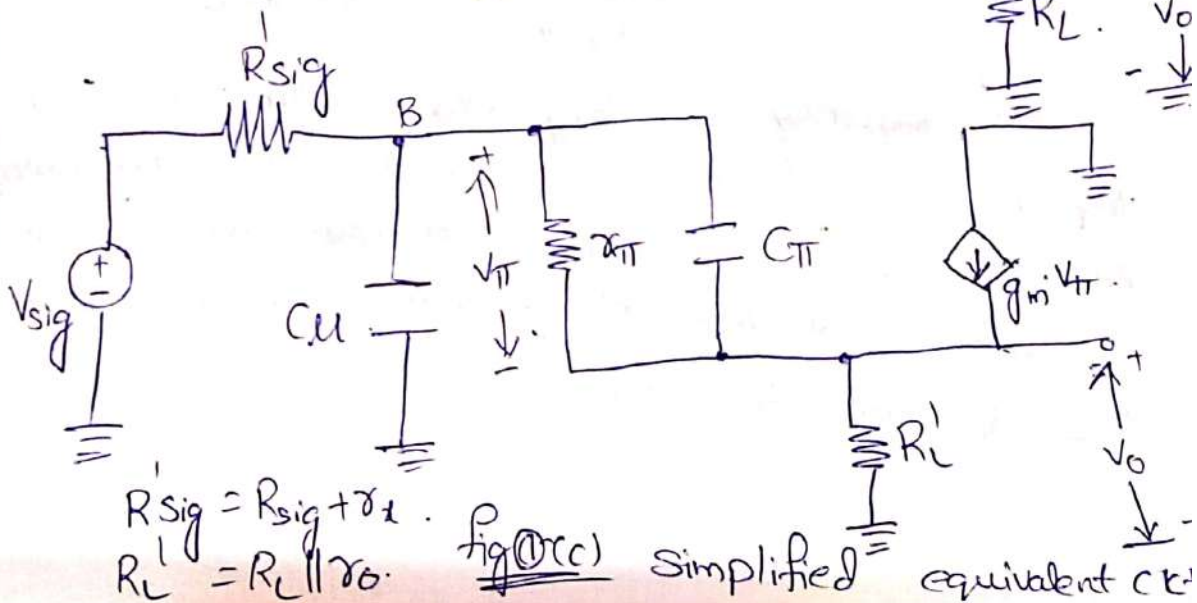
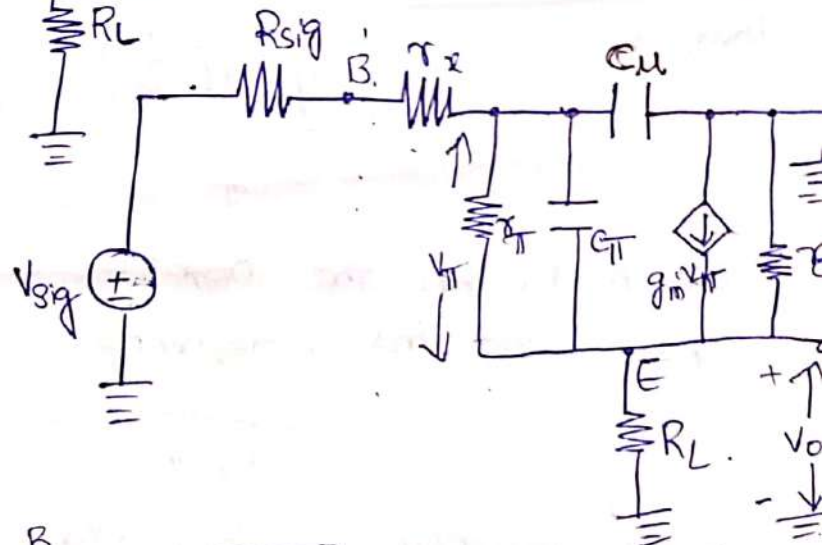


Fig 1(c) simplified equivalent circuit

(Analysis of the emitter follower of Fig 1(a) to determine its low-frequency gain, i/p resistance & o/p resistance r_s & r_o)

Fig 1(b) shows the high-frequency equivalent circuit. Lumping r_o together with R_L & r_e together with R_{sig} & making a slight change in the way the circuit is drawn results in the simplified equivalent circuit shown in Fig 1(c). We will follow a procedure for the analysis of this circuit similar to that used above for the source follower. Specifically, to obtain the location of the transmission zero, note that V_o will be zero at the frequency s_z for which the current fed to R_L is zero:

$$g_m V_{\pi} + \frac{V_{\pi}}{r_{\pi}} + s_z C_{\pi} = 0$$

Thus,

$$s_z = \frac{-g_m + \left(\frac{1}{r_{\pi}}\right)}{C_{\pi}} = \frac{-1}{C_{\pi} r_e} \quad \text{--- } \textcircled{1}$$

which is on the negative real-axis of the s-plane and has a frequency

$$\omega_z = \frac{1}{C_{\pi} r_e} \quad \text{--- } \textcircled{2}$$

This frequency is very close to the unity-gain frequency ω_T of the transistor. The other transmission zero is at $s = \infty$. This is because at this frequency C_{μ} acts as a short circuit, making V_{π} zero, and hence V_o will be zero.

Next, we determine the resistances ⁽⁹²⁾ seen by C_u and G_π . For C_u the reader should be able to show that the resistance it sees, R_u , is the parallel equivalent of R_{sig}' and the input resistance looking into B' , that is.

$$R_u = R_{sig}' \parallel [\alpha_\pi + (\beta + 1)R_L'] \quad \longrightarrow \textcircled{3}$$

eq $\textcircled{3}$ indicates that R_u will be smaller than R_{sig}' , and since C_u is usually very small, the time constant $C_u R_u$ will be correspondingly small.

The resistance R_π seen by G_π can be determined using an analysis similar to that employed for the determination of R_{gs} in the MOSFET case. The result is

$$R_\pi = \frac{R_{sig}' + R_L'}{1 + \frac{R_{sig}'}{r_\pi} + \frac{R_L'}{r_e}} \quad \longrightarrow \textcircled{4}$$

We observe that the term $\frac{R_L'}{r_e}$ will usually make the denominator much greater than unity thus rendering R_π rather low. Thus, the time constant $G_\pi R_\pi$ will be small. The end result is that the 3-dB frequency f_H of the emitter follower,

$$f_H = \frac{1}{2\pi(C_u R_u + C_\pi R_\pi)} \quad \boxed{f_H = \frac{1}{2\pi f_H} = \frac{1}{2\pi(C_u R_u + C_\pi R_\pi)}}$$

will usually be very high. We urge the reader to solve the following exercise to gain familiarity with typical values of various parameters that determine f_H . Exercise 1(c):-
mmom-mx

Q3 ⇒ Frequency Response of the Differential Amplifiers:-

Here, we study the frequency response of the differential amplifier. We will consider the variation with frequency of both the differential gain & the Common-mode gain and hence of the CMRR.

1) Analysis of the Resistively loaded MOS amplifier:-

We begin with the basic, resistively loaded MOS differential pair shown in Fig 1(a). Note that we have explicitly shown the transistor Q_S that supplies the bias current I . Although we are showing a dc bias voltage V_{BIAS} at its gate, usually Q_S is part of a current mirror.

Most importantly, we are interested in the total impedance between node 'S' and ground, Z_{SS} . As we shall shortly see, this impedance plays a significant role in determining the common-mode gain & the CMRR of the differential amplifier. Resistance R_{SS} is simply the o/p resistance of current source Q_S .

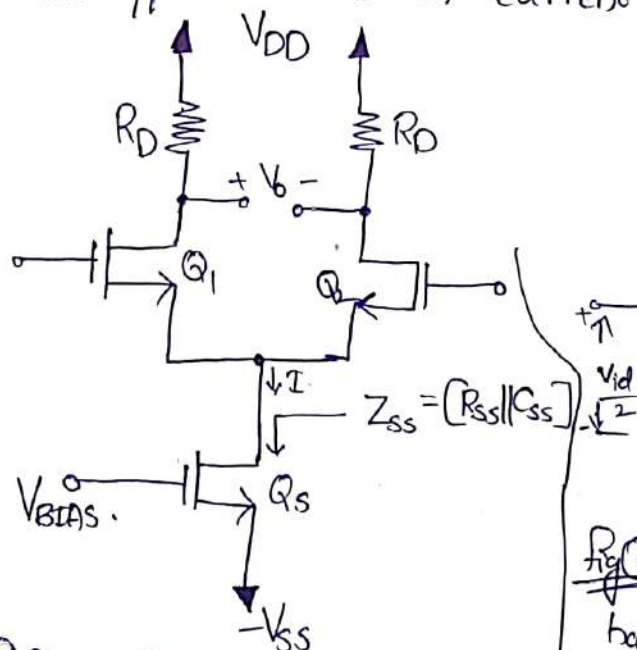


Fig 1(a) A resistively loaded MOS differential pair with the transistor supplying the bias current explicitly shown.

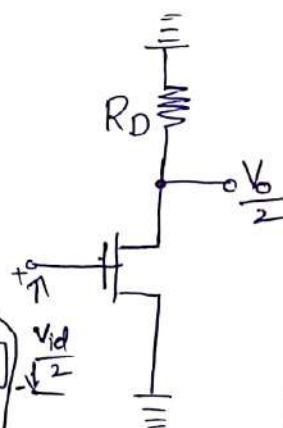


Fig 1(b) :- Differential half-circuit.

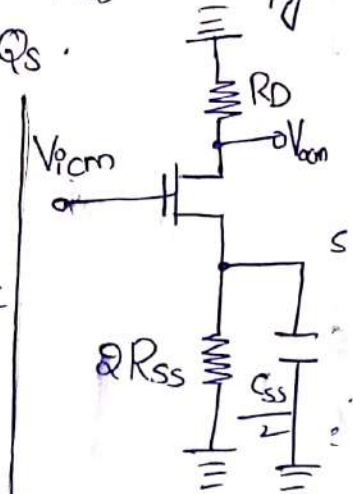


Fig 1(c) :- Common-mode half-circuit.

Capacitance ' C_{ss} ' is the total capacitance between node 'S' and ground and includes C_{db} & C_{gd} of Q_5 , as well as C_{sb1} & C_{sb2} . This capacitance can be significant, especially if wide transistors are used for Q_5 , Q_1 , and Q_2 .

The differential half-circuit shown in Fig (1)(b) can be used to determine the frequency dependence of the differential gain $\frac{V_o}{V_{id}}$. Indeed the gain function $A_d(s)$ of the differential amplifier will be identical to the transfer function of this Common-Source amplifier.

See. The Common-mode half-circuit is shown in Fig (1)(c). Although this circuit has other capacitances, namely C_{gs} , C_{gd} and C_{db} of the transistor in addition to other stray capacitances, we have chosen to show only $\frac{C_{ss}}{2}$. This is because $(\frac{C_{ss}}{2})$ together with (R_{ss}) forms a real-axis zero in the common-mode gain function at a frequency much lower than those of the other poles and zeros of the circuit. This zero then dominates the frequency dependence of A_{cm} and CMRR.

If the output of the differential amplifier is taken single-endedly, then the common-mode gain of interest is $\frac{V_{ocm}}{V_{icm}}$. More typically, the output is taken differentially. Nevertheless, as we have seen $\frac{V_{ocm}}{V_{icm}}$ still plays a major role in determining the common-mode gain. To be specific, consider what happens when the o/p is taken differentially & there is a mismatch ΔR_D between the two drain resistances. The resulting common-mode gain is:

$$A_{cm} = - \left(\frac{R_D}{2R_{ss}} \right) \frac{\Delta R_D}{R_D} \longrightarrow (7)$$

Thus, the frequency dependence of A_{cm} can be obtained by simply replacing R_{ss} by Z_{ss} in this factor. Doing so for the expression in eq (7) gives

$$A_{cm}(s) = -\frac{R_D}{2Z_{ss}} \left(\frac{\Delta R_D}{R_D} \right) \quad (24)$$

$$= -\frac{1}{2} R_D \left(\frac{\Delta R_D}{R_D} \right) Y_{ss}$$

$$= -\frac{1}{2} R_D \left(\frac{\Delta R_D}{R_D} \right) \left(\frac{1}{R_{ss}} + s C_{ss} \right)$$

$$A_{cm}(s) = -\frac{R_D}{2R_{ss}} \left(\frac{\Delta R_D}{R_D} \right) (1 + s C_{ss} R_{ss}) \quad (2)$$

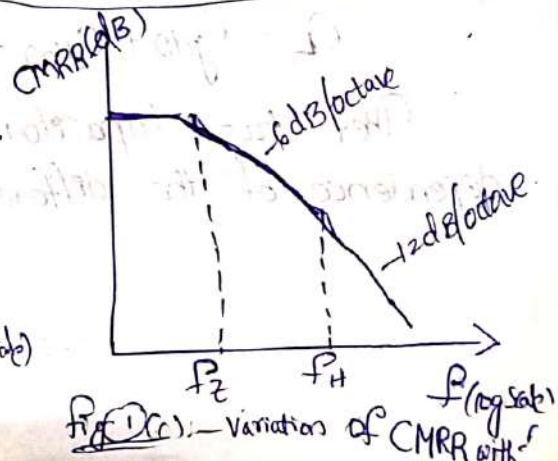
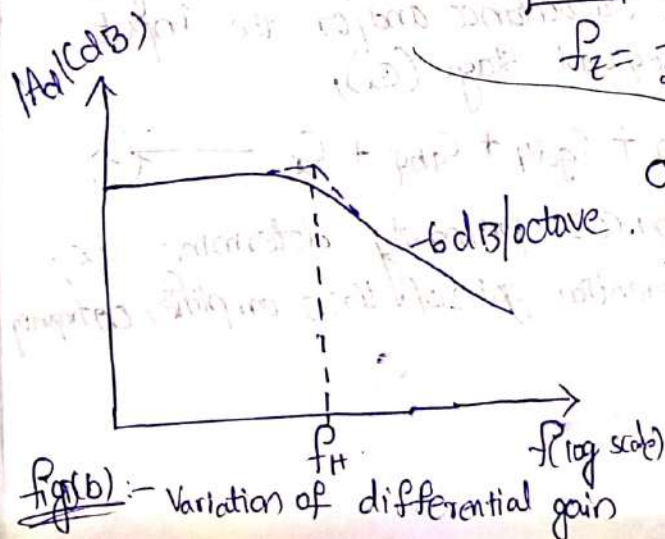
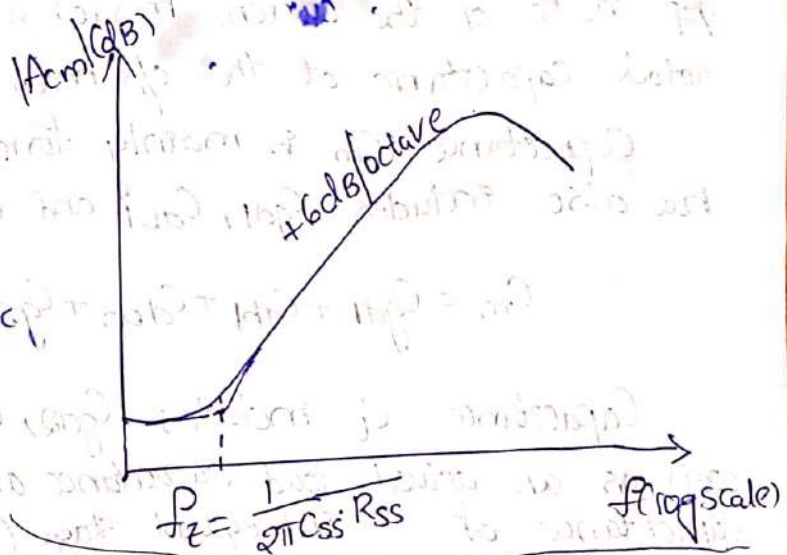
From which we see that A_{cm} acquires a zero on the negative real-axis of the s-plane with frequency ω_z ,

$$\omega_z = \frac{1}{C_{ss} \cdot R_{ss}} \quad \longrightarrow (3)$$

(or) in hertz,

$$f_z = \frac{\omega_z}{2\pi} = \frac{1}{2\pi C_{ss} R_{ss}} \quad \longrightarrow (4)$$

Fig (a) Variation of Common-mode gain



As mentioned above, usually f_E is much lower than the frequencies of the other poles and zeros. As a result, the common-mode gain increases at the rate of $+60\text{dB}/\text{decade}$ (20dB/decade) starting at a relatively low frequency, as indicated in fig(1ca). Of course, A_{cm} drops off at high frequencies because of the other poles of the common-mode half-circuit. It is, however, f_E that is significant, for it is the frequency at which the CMRR of the differential amplifier begins to decrease, as indicated in fig(1cc). Note that if both A_d and A_{cm} are expressed and plotted in dB, then CMRR in dB is simply the difference between A_d and A_{cm} .

Analysis of the Active-loaded MOS Amplifier:-

We next consider the frequency response of the current-mirror-loaded MOS differential-pair circuit. The circuit is shown in fig(2a) with two capacitances indicated: C_m , which is the total capacitance at the ~~ip~~ node of the current mirror, and C_L which is the total capacitance at the op node.

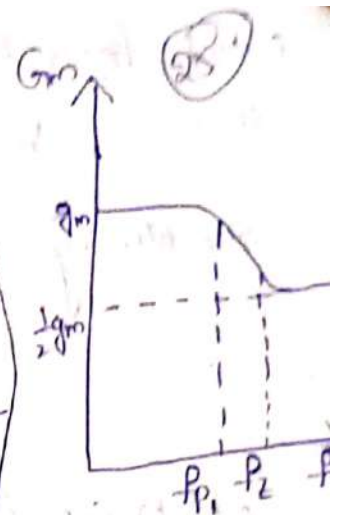
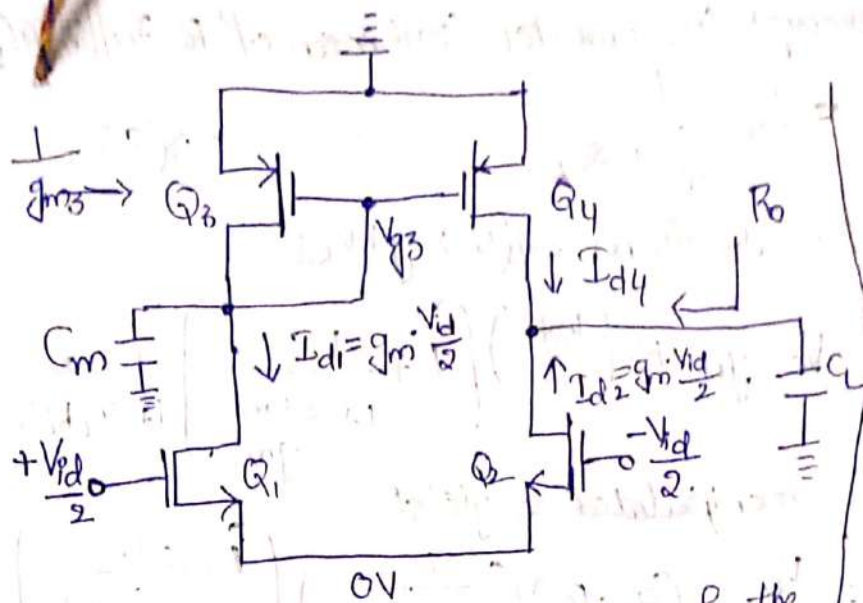
Capacitance C_m is mainly formed by C_{gs3} & C_{gs4} , but also includes C_{gd1} , C_{db1} and C_{db3} .

$$C_m = C_{gd1} + C_{db1} + C_{db3} + C_{gs3} + C_{gs4} \quad \text{--- (1)}$$

Capacitance C_L includes C_{gd2} , C_{db2} , C_{db4} , C_{gd4} as well as an actual load capacitance and/or the input capacitance of a subsequent stage (C_x),

$$C_L = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_x \quad \text{--- (2)}$$

These two capacitances primarily determine the dependence of the differential gain of this amplifier on frequency.



Fig(2a) frequency-response analysis of the active-loaded MOS differential amplifier

Fig(2b) The overall transconductance G_m as a function of frequency.

As indicated in Fig(2a) the i/p differential signal V_d is applied in a balanced fashion. Transistor Q_1 will conduct a drain current signal of $g_{m1} \frac{V_d}{2}$, which flows through the parallel combination of $(\frac{1}{g_{m3}})$ and C_m , where we have neglected the resistance r_{o1} and r_{o3} which are much larger than $(\frac{1}{g_{m3}})$, thus.

$$V_{g3} = - \frac{g_{m1} \frac{V_d}{2}}{g_{m3} + sC_m} \quad \text{--- (3)}$$

In response to V_{g3} , transistor Q_4 conducts a drain current I_{d4} ,

$$I_{d4} = -g_{m4} V_{g3} = \frac{g_{m4} g_{m1} \frac{V_d}{2}}{g_{m3} + sC_m}$$

Since, $g_{m3} = g_{m4}$, this equation reduces to

$$I_{d4} = \frac{g_{m1} \frac{V_d}{2}}{1 + s \frac{C_m}{g_{m3}}} \quad \text{--- (4)}$$

Now, at the o/p node the total o/p current is

$$\begin{aligned} I_o &= I_{d4} + I_{d2} \\ &= \frac{g_{m1} \frac{V_d}{2}}{1 + s \frac{C_m}{g_{m3}}} + g_{m2} \left(\frac{V_d}{2} \right) \quad \text{--- (5)} \end{aligned}$$

which flows through the parallel combination of $R_0 = r_{o1} || r_{o4} || C_L$.

thus

$$V_0 = I_0 \cdot \frac{1}{\frac{1}{R_0} + sC_L} \quad \longrightarrow (6)$$

Substituting for I_0 from eq(5) gives.

$$V_0 = g_m \cdot R_0 \left(\frac{V_{id}}{2} \right) \left[1 + \frac{1}{1 + s \frac{C_m}{g_{m3}}} \right] \frac{1}{1 + sC_L R_0}$$

which can be manipulated to yield.

$$A_d(s) = \frac{V_0}{V_{id}} = (g_m \cdot R_0) \left(\frac{1}{1 + sC_L R_0} \right) \left[\frac{1 + s \frac{C_m}{2g_{m3}}}{1 + s \frac{C_m}{g_{m3}}} \right]$$

we recognize the first factor on the right-hand side as the dc gain of the amplifier. The second factor indicates that C_L & R_0 form a pole with frequency f_{P1} .

$$f_{P1} = \frac{1}{2\pi C_L \cdot R_0} \quad \longrightarrow (8)$$

This, of course, is an entirely expected result, and in fact this d/p pole is often dominant, especially when a large load capacitance is present. The third factor on the right-hand side of eq(7) indicates that the capacitance C_m at the i/p of the current mirror gives rise to a pole with frequency f_{P2} ,

$$f_{P2} = \frac{g_{m3}}{2\pi C_m} \quad \longrightarrow (9)$$

and a zero with frequency f_z ,

$$f_z = \frac{2g_{m3}}{2\pi C_m} \quad \longrightarrow (10)$$

That is, the zero frequency is twice that of the pole. Since C_m is approximately $C_{gs3} + C_{gs4} = 2C_{gs3}$,

$$f_{P2} \cong \frac{g_{m3}}{2\pi (2C_{gs3})} \cong \frac{f_T}{2} \quad \longrightarrow (11)$$

and

$$f_z \cong f_T \quad \longrightarrow (12)$$

where, f_T is the frequency at which the magnitude of the high-frequency current gain of the MOSFET becomes unity. Thus, the mirror pole and zero occur at very high frequencies. Nevertheless, their effect can be significant.

Frequency Response of multistage Amplifiers (28)

For a second transistor stage connected directly to the output of the first stage, there will be significant change in the overall frequency response. There will be additional low frequency cut-off levels due to the second stage that will further reduce the overall gain of the system in this region. For each additional stage, the upper cut-off frequency will be determined primarily by the stage having the lowest high frequency cut-off frequency. The low frequency cut-off is primarily determined by that stage having the highest low frequency cut-off frequency. Hence one poorly designed stage can off set an otherwise well designed cascaded system.

The effect of increasing the number of identical stages, having the same lower and upper cut-off frequencies, can be clearly demonstrated by considering fig. 2.38.

For a single stage the cut-off frequencies are f_1 and f_2 as indicated. For two identical stages in cascade, the drop off rate in the low and high frequency regions has increased to -12dB/octave or -40dB per decade . At f_1 and f_2 therefore, the decibel drop is now -6dB , rather than the defined band frequency gain level of -3dB . The -3dB point has shifted to

f_1' and f_2' as indicated, with a resulting drop in the bandwidth. A -18dB/octave or -60dB/decade slope will result for a three stage system of identical stages, with indicated reduction in bandwidth (f_1'' and f_2'').

Assuming identical stages, an equation for each band frequency as a function of the number of

for stages(n) can be determined in the following manner.
for the low frequency region.

$$A_{vlow(overall)} = A_{v1low} A_{v2low} A_{v3low} \dots A_{vnlow}$$

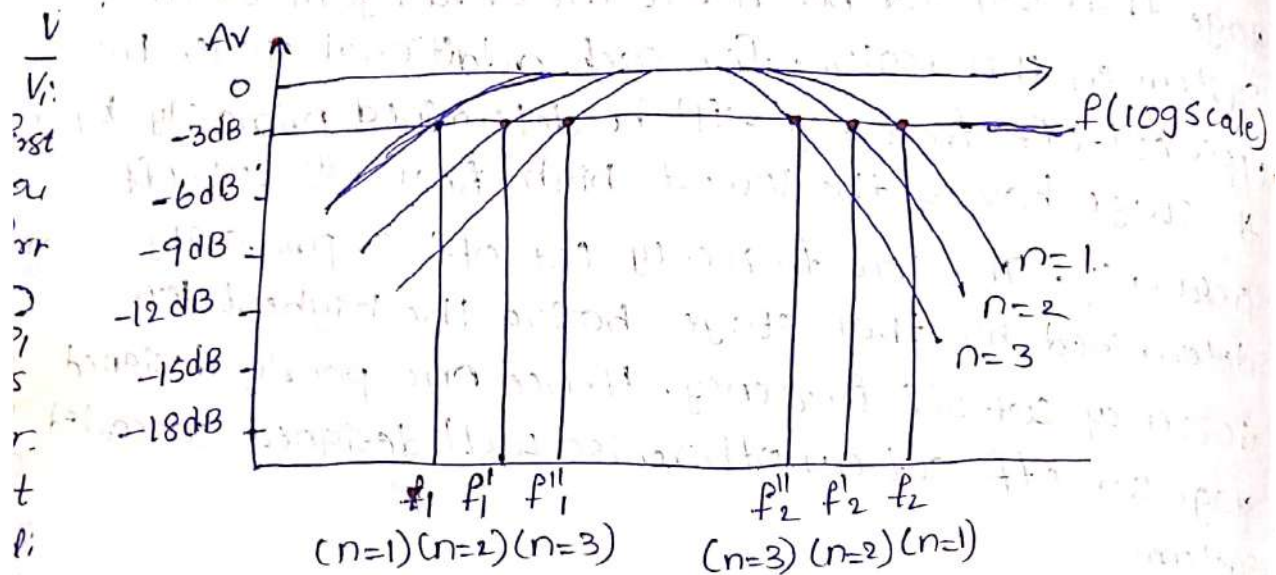


fig. 2.38 Effect of an increased number of stages on the cut off frequencies and bandwidth

As each stage is identical

$$A_{v1low} = A_{v2low} = \dots = A_{vnlow}$$

Therefore,

$$A_{vlow(overall)} = (A_{vlow})^n$$

$$A_{vlow}/A_{vmid(overall)} = (A_{vlow}/A_{vmid})^n$$

$$= 1/[1 + (f_1/f)^2]^n$$

Setting the magnitude of the result equal to $1/\sqrt{2}$ (-3dB level) results in

$$1/\sqrt{[1 + (f_1/f)^2]^n} = 1/\sqrt{2}$$

Rearranging the above we get

$$\{ \sqrt{[1 + (f_1/f)^2]} \}^{-n} = 1/\sqrt{2}$$

$$\{ [1 + (f_1/f)^2]^{1/2} \}^n = (2)^{1/2}$$

$$\left\{ \left[1 + (f_1/f'_1)^2 \right] \right\}^{n/2} = 2$$

(27)

$$1 + (f_1/f'_1)^2 = (2)^{2/n}$$

And hence we get

$$f'_1 = \left[f_1 / \sqrt{(2)^{2/n} - 1} \right]$$

In a similar manner, it can be shown that for the high frequency region,

$$f'_2 = \left[\sqrt{(2)^{2/n} - 1} \right] f_2$$

The presence of $\left[\sqrt{(2)^{2/n} - 1} \right]$ is to be noted in both f'_1 and f'_2 . The magnitude of this factor for various values of n is listed as follow.

n	$\left[\sqrt{(2)^{2/n} - 1} \right]$
2	0.64
3	0.51
4	0.43
5	0.39

For $n=2$, consider the upper cut-off frequency $f'_2 = 0.64 f_2$ or 64% of the value obtained for a single stage, while $f'_1 = (1/0.64) f_1 = 1.56 f_1$.

For $n=3$, consider the upper cut-off frequency $f'_2 = 0.51 f_2$ or approximately half the value of a single stage, while $f'_1 = (1/0.51) f_1 = 1.96 f_1$ or approximately twice the single stage value.

A decrease in bandwidth is not always associated with an increase in the number of stages if the mid band gain can remain fixed and independent of the number of stages.

UNIT-II

FEEDBACK AMPLIFIERS

Introduction:

Feedback plays a very important role in electronic circuits and the parameters such as input impedance, current gain, voltage gain, output impedance and bandwidth may be altered considerably by the use of feedback for a given amplifier.

In large signal amplifiers and electronic measuring instruments the major problem of distortion should be avoided as far as possible. And also the gain must be independent of external factors such as variation in DC supply voltage and the values of the circuit components. All this can be achieved with the help of feedback.

A portion of the output signal is taken from the output of the amplifier and is combined with the normal input signal to accomplish the feedback for an amplifier.

Classification of Basic amplifiers:

The basic amplifiers are classified into four categories as voltage amplifier, current amplifier, transconductance amplifier and trans resistance amplifier based on the magnitudes of input and output resistances of an amplifier with respect to the source and load resistances. These basic amplifiers are used in feedback amplifiers.

Voltage Amplifier:

The figure shows a thevenin's equivalent circuit of a voltage amplifier.

An Ideal voltage amplifier is defined

as an amplifier which provides the output voltage proportional to the input voltage and the proportionality factor does not depend on the magnitude of source and load resistances. An ideal voltage amplifier has

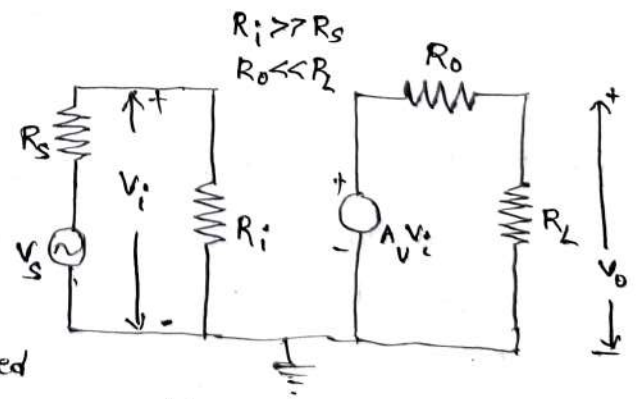


fig: voltage amplifier
 $V_o \approx A_v V_s$

infinite input resistance (R_i) and zero output resistance (R_o). But a practical voltage amplifier has $R_i \gg R_s$ and $R_o \ll R_L$.

The output voltage $V_o \approx A_v V_i \approx A_v V_s$ where A_v is the open circuit voltage gain with $R_L = \infty$.

Current Amplifier:

Figure shows the Norton's equivalent circuit for current amplifier. An ideal current amplifier is defined as an amplifier which provides the output current proportional to the input current and the proportionality factor is independent of R_s and R_L .

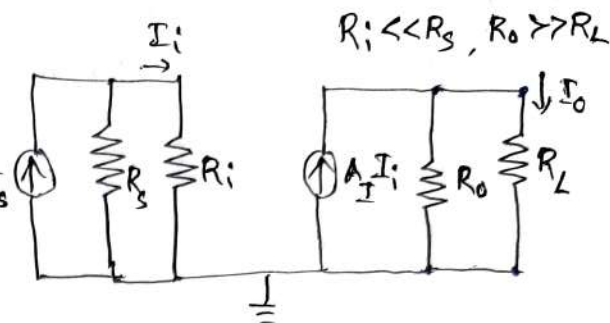


fig: Current amplifier
 $I_o \approx A_I I_s$

An ideal current amplifier has zero input resistance (R_i) and infinite output resistance (R_o). But practical current - amplifier has $R_i \ll R_s$ and $R_o \gg R_L$.

The output current $I_o \approx A_I \cdot I_i$, where A_I is the short circuit current gain with $R_L = 0$.

Transconductance amplifier:

Figure shows the transconductance amplifier in which the input circuit is Thevenin and output circuit is Norton.

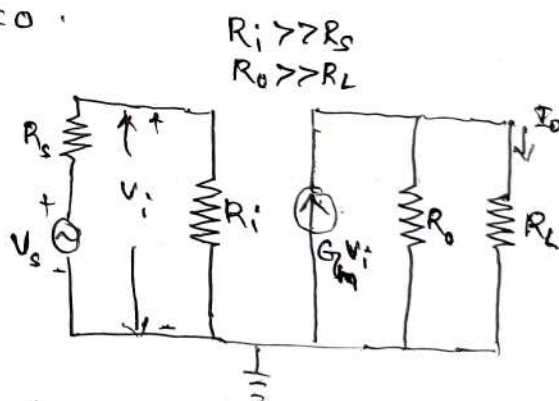


fig: Transconductance Amplifier
 $I_o \approx G_m V_s$

An ideal transconductance amplifier is defined as an amplifier in which the output current is proportional to the input voltage and the proportionality factor is independent of R_s and R_L .

An ideal transconductance amplifier has $R_i = \infty$ and $R_o = \infty$. But practical transconductance amplifier has $R_i \gg R_s$, $R_o \gg R_L$.

The output current $I_o \approx G_m V_i$, where G_m is short circuit transconductance with $R_L = 0$.

Transresistance Amplifier:

Figure shows the transresistance amplifier in which the input is Norton and output is thevenin.

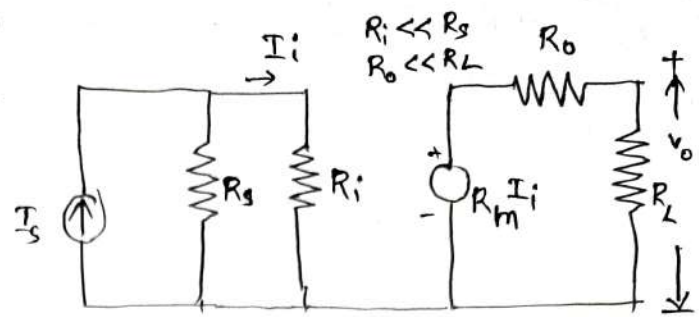


fig: Transresistance amplifier
 $V_o \approx R_m I_s$

An Ideal transresistance amplifier is defined as an amplifier

the output voltage is proportional to the input current and proportionality factor is independent of the values of R_s and R_L .

For an ideal transresistance amplifier $R_i = 0$ and $R_o = 0$.

But in practical transresistance amplifier $R_i \ll R_s$ and $R_o \ll R_L$.

The output voltage $V_o = R_m I_i$ where R_m is open circuit transfer resistance with $R_L = \infty$.

Basic Concept of feedback:

The block diagram of an amplifier with feedback is shown in below figure

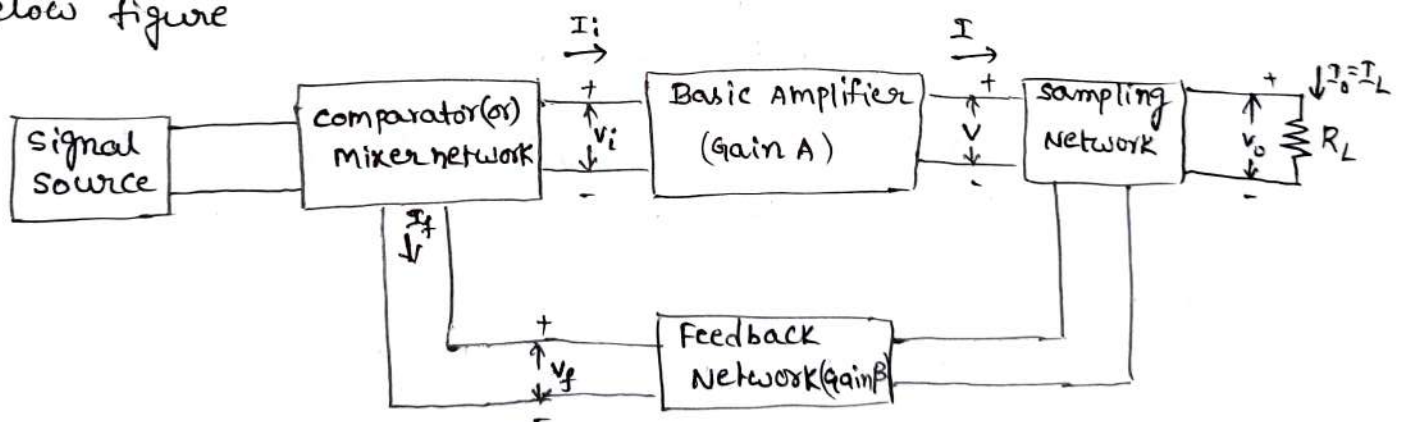


fig: Block diagram of an amplifier with feedback

In a feedback amplifier a basic amplifier is used that can be a voltage amplifier (or) a current amplifier (or) transconductance (or) transresistance amplifier. In each one of these circuits we may sample the output voltage (or) output current by means of a suitable sampling network which is of two types, namely, voltage sampler and current sampler. and apply the sampled signal to the

feedback network. The output of the feedback network is combined with the source signal through a mixer and fed to the basic amplifier.

Mixers are also known as comparators which are of two types Series mixer and shunt mixer.

In the block diagram shown above we have

$$A = \text{gain of the basic amplifier} = \frac{V_o}{V_i}$$

$$\beta = \text{feedback ratio (or) reverse transmission factor} = \frac{V_f}{V_o}$$

$$A_f = \text{gain of the feedback amplifier} = \frac{V_o}{V_s}$$

V_s = signal voltage from the source.

V_f = feedback signal voltage.

The signal source in a feed back amplifier can be either a signal voltage V_s in series with a resistor R_s (or) a signal current I_s in parallel with a resistor R_s .

The feedback network may contain resistors, capacitors and inductors. Most often it is simply a resistive configuration.

If sampling network is a voltage sampler, the output voltage is sampled by connecting the feedback network in shunt across the o/p. If it is a current sampler the output current is sampled by connecting the o/p to feedback network in series.

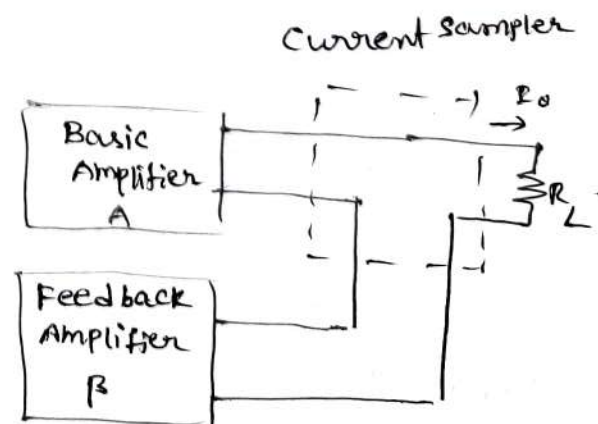
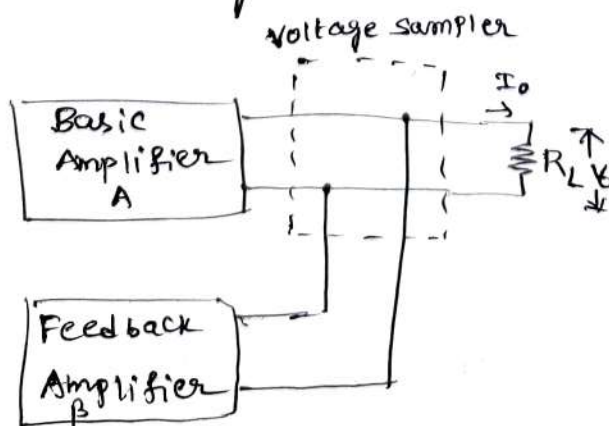


Fig:- Feedback Connections at the o/p of a basic amplifier, sampler o/p.

Mixer (or) comparator network is used for combining the feedback signal with the input signal. There are two types of mixer networks series mixer and shunt mixer as shown in below.

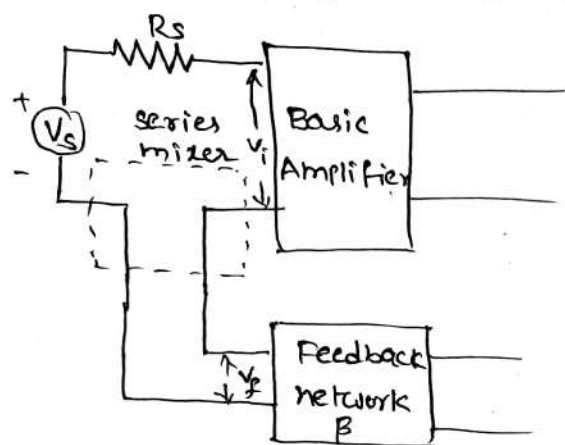


fig (a)

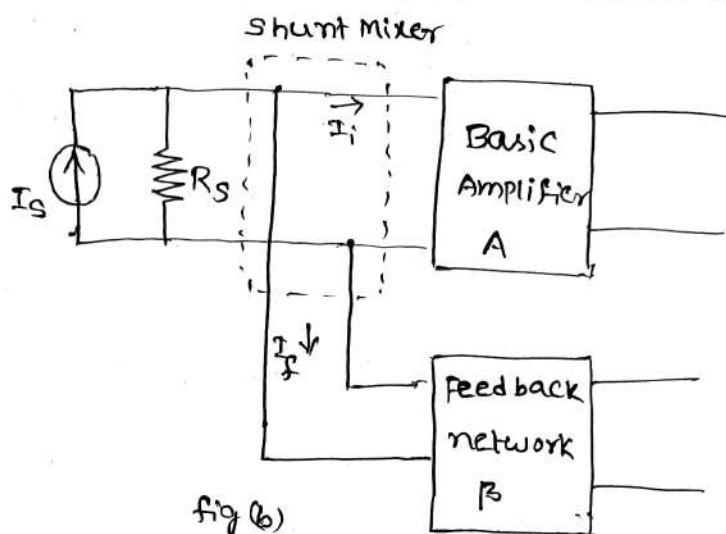


fig (b)

fig: Feedback Connections at the input of the basic amplifier
fig(a) using series mixing fig(b) using shunt mixing

Transfer ratio (or) Gain:

The ratio of the output signal to the input signal of a basic amplifier is called as transfer ratio denoted as A' .

The transfer ratio V_o/V_i is the voltage gain denoted by A_V . Similarly the transfer ratio I_o/I_i is the current gain denoted by A_I .

The transfer ratio I_o/V_i is the trans conductance denoted by G_m and the transfer ratio V_o/I_i is the trans resistance R_m .

Generally each of these four A_V , A_I , G_m and R_m are referred as the transfer gain of the basic amplifier without feedback and we use the symbol A to represent any one of these quantities.

The symbol A_f is defined as the ratio of the output signal to the input signal of the amplifier and is called as transfer gain of the amplifier with feedback. Hence A_f is used to represent any

one of the four ratios $V_o/V_s = A_{Vf}$, $I_o/I_s = A_{If}$, $I_o/V_s = G_{mf}$, $V_o/I_s = R_{mf}$

Schematic representation (or) The general structure of a feedback amplifier:

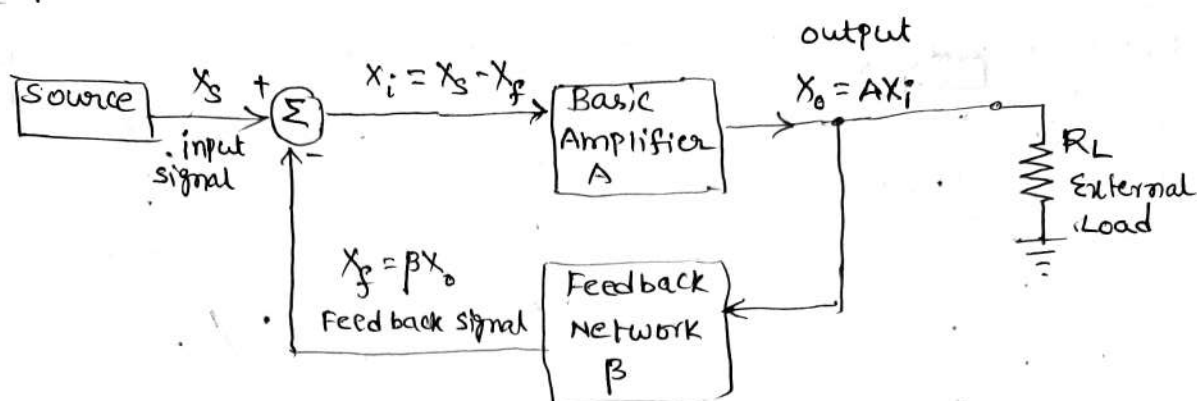


fig: Schematic representation of a single loop feedback amplifier.

The above figure shows the schematic representation of a feedback amplifier. Here X represents either voltage or current signals.

When the feedback signal (X_f) and input signal (X_s) are out of phase that feedback is called negative feedback and if the feedback signal (X_f) and input signal (X_s) are in phase, that feedback is called as positive feedback.

Negative feedback is also called as degenerative feedback where as positive feedback is also called as regenerative feedback.

Positive feedback:

Positive feedback is also known as regenerative feedback.

If the feedback signal (X_f) is in phase with the input signal X_s then that feedback is called as positive feedback. In this case, the positive feedback causes the input of the basic amplifier (X_i) to be increased, which causes the output (X_o) to increase.

The gain of amplifier with positive feedback is

$$A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i - X_f}$$

$$\Rightarrow A_f = \frac{1}{\left(\frac{X_i}{X_o}\right) - \left(\frac{X_f}{X_o}\right)} = \frac{1}{\left(\frac{1}{A}\right) - \beta} = \frac{A}{1 - A\beta}$$

$$\therefore A_f = \frac{A}{1 - A\beta}$$

Here $|A_f| > |A|$. The product of open loop gain and the feedback factor (β), is called as loop gain i.e. loop gain = $A\beta$

If $|AB| = 1$ then $A_f = \infty$. Hence the gain of the amplifier with positive feedback is infinite and the amplifier gives an ac signal without ac input signal. Drawbacks of positive feedback is

• The positive feedback increases the instability of an amplifier, reduces the bandwidth and increases the distortion and noise.

The positive feedback is used in oscillators.

Negative feedback:

If the feedback signal (X_f) is out of phase with the input signal (X_i) then that feedback is called as negative feedback.

The negative feedback causes the input of the basic amplifier (X_i) to be decreased causing the output (X_o) to be decreased.

Negative feedback is also called as degenerative feedback.

The gain of the amplifier with negative feedback is

$$A_f = \frac{X_o}{X_i} = \frac{X_o}{X_i + X_f}$$

$$\Rightarrow A_f = \frac{1}{\frac{X_i}{X_o} + \frac{X_f}{X_o}} = \frac{1}{\frac{1}{A} + \beta} = \frac{A}{1 + AB}$$

$$\therefore A_f = \frac{A}{1 + AB}$$

Here $|A_f|$ is less than $|A|$. If $|AB| \gg 1$ then $A_f = \frac{1}{\beta}$

where β is feedback ratio. Then the gain A_f depends completely on feedback network.

If the feedback network contains only passive elements, the gain of the amplifier with negative feedback will be stable.

Advantages of negative feedback : (characteristics of negative feedback)

The stabilization of the operating point of a transistor amplifier is accomplished by using negative feedback with respect to the changes in dc supply voltage and the operating point is kept constant in the case of change in temperature or a change in h_{fe}

(or) β of a transistor.

Negative feedback is also used to improve the performance of an amplifier i.e. frequency response is improved with negative feedback.

Negative feedback always helps to increase the bandwidth, decrease distortion and noise, modify the input and output resistances as desired.

All the above advantages are derived at an expense of reduction in voltage gain. But the amplifier with negative feedback provides a stabilized voltage gain.

Classification of feedback amplifiers (or) Feedback topologies:

Based on the type of sampling at output side and the type of mixing to the input side, feedback amplifiers are classified into four topologies. They are

- 1) Voltage series feedback (or) series shunt feedback
- 2) Current series feedback (or) series series feedback
- 3) Current shunt feedback (or) shunt series feedback
- 4) Voltage shunt feedback (or) shunt shunt feedback

The feedback amplifier topologies are given below.

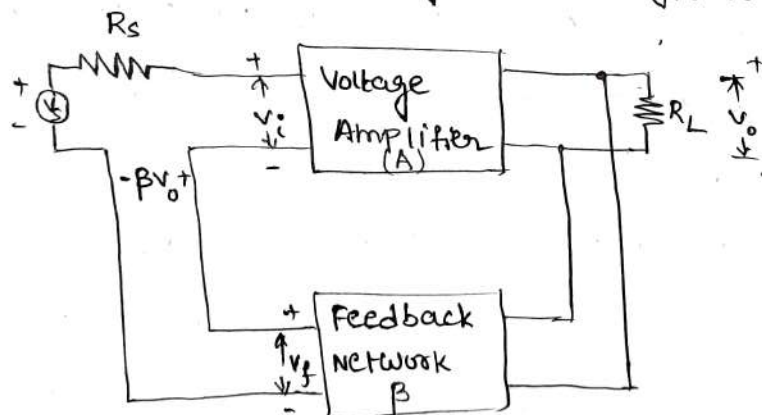


Fig: Voltage series feedback Topology

(or) voltage amplifier with voltage series feedback

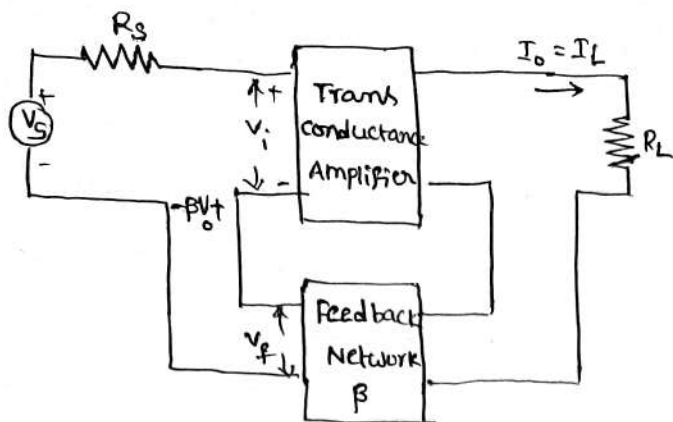


fig: Current series feedback (or)

Transconductance amplifier with current series feed back .

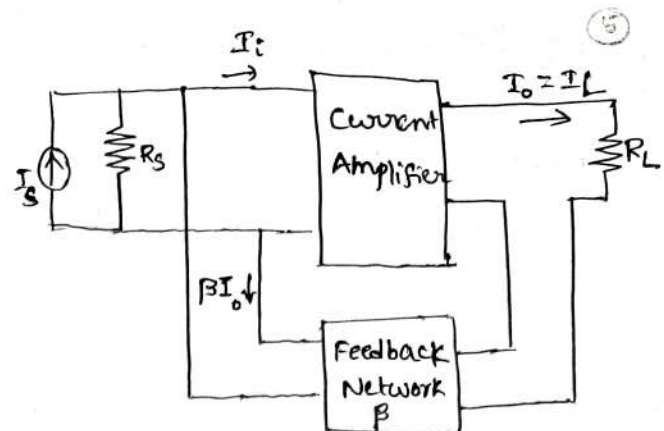


fig: current shunt feedback (or) current amplifier with current shunt - feedback

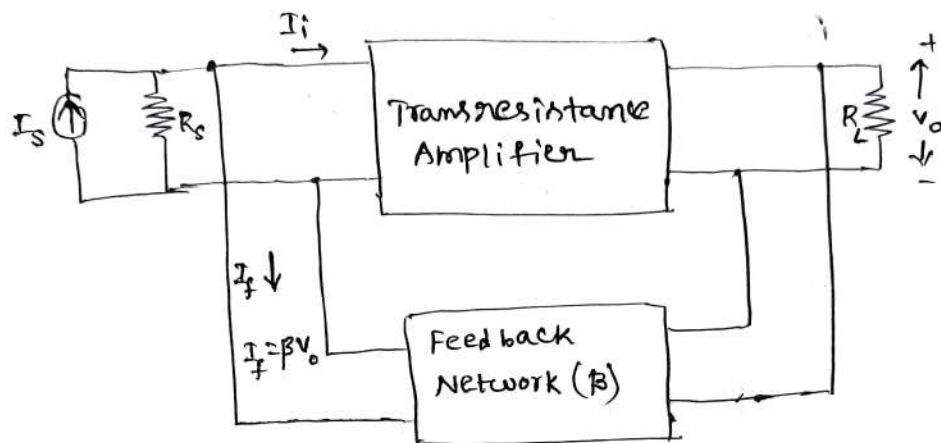


fig: Transresistance amplifier with feedback network i.e Voltage shunt feed back

Let the input signal x_s , the output signal x_o , the feedback signal x_f and the input of the basic amplifier is x_i . These signals and the corresponding ratios A and β are listed below.

Signal (or) ratio	Voltage series feed back	Current series feed back	Current shunt feedback	Voltage shunt feed back
x_o	Voltage	Current	Current	Voltage
x_s, x_f and x_i	Voltage	Voltage	Current	Current
A	A_V	G_m	A_I	R_m
β	$\frac{V_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$	$\frac{I_f}{V_o}$

characteristics of negative feed back amplifiers

1) Stability of gain (or) Desensitization:

The gain of the amplifiers is not constant in general as it depends on the factors such as temperature, ageing of the components and temperature dependent parameters. This lack of stability can be reduced by introducing negative feed back.

we know that the expression for gain with feedback

$$A_f = \frac{A}{1 + A\beta} \quad \rightarrow (1)$$

differentiating A_f with respect to A .

$$\frac{dA_f}{dA} = \frac{(1 + A\beta) \cdot (1) - A \cdot (\beta)}{(1 + A\beta)^2}$$

$$\frac{dA_f}{dA} = \frac{1}{(1 + A\beta)^2}$$

multiplying both sides with $\frac{1}{A_f}$ we get

$$\frac{dA_f}{dA} \cdot \frac{1}{A_f} = \frac{1}{(1 + A\beta)^2} \cdot \frac{1}{A_f}$$

$$\frac{dA_f}{dA} \cdot \frac{1}{A_f} = \frac{1}{(1 + A\beta)^2} \cdot \frac{1}{\frac{A}{(1 + A\beta)}}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \cdot \frac{1}{(1 + A\beta)}$$

$$\Rightarrow \left(\frac{dA_f}{A_f} \right) / \left(\frac{dA}{A} \right) = \frac{1}{1 + A\beta}$$

$$\therefore S = \frac{1}{1 + A\beta} \quad \rightarrow (2)$$

The fractional change in amplification with feedback is divided by the fractional change in amplification with out feedback is called as sensitivity of the transfer gain denoted by S .

The reciprocal of sensitivity is known as desensitivity denoted by D . i.e. $D = \frac{1}{S} = \frac{1}{(1/1+AB)} = 1+AB \rightarrow (3)$

From equation (1) and (2) $A_f = \frac{A}{D}$

In equation (1) if $BA \gg 1$ then $A_f = \frac{A}{1+BA} \approx \frac{A}{BA} = \frac{1}{\beta}$

Thus the gain A_f is made to depend entirely on feedback network. If the feed back network contains only passive elements the improvement in stability is achieved.

Then the voltage gain $A_{vf} \approx 1/\beta$ for voltage series feedback, transconductance $G_{mf} \approx 1/\beta$ for current series feedback, the current gain $A_{if} \approx 1/\beta$ for a current shunt feedback and the trans resistance $R_{mf} \approx 1/\beta$ for a voltage shunt feedback is achieved.

2) Extension of bandwidth :

We know that the gain of the amplifier with negative feedback is given as $A_f = \frac{A}{1+AB} \rightarrow (1)$

Then we can write $A_{fmid} = \frac{A_{mid}}{1+A_{mid}\beta} \rightarrow (2)$

$A_{flow} = \frac{A_{low}}{1+A_{low}\beta} \rightarrow (3)$

$A_{fhigh} = \frac{A_{high}}{1+A_{high}\beta} \rightarrow (4)$

The effect of negative feedback on lower cut-off and upper cut-off frequencies of the amplifier is analyzed here.

Lower cut-off frequency : (f_{Lf})

We know that the relation between the gain at lower cut-off frequency and the gain at midband frequency of an amplifier is given as $A_{low} = (A_{mid}) / \left[1 - j\left(\frac{f_L}{f} \right) \right] \rightarrow (5)$

Substitute equation (5) in equation (3) we get

$$A_{f \text{ low}} = \frac{(A_{\text{mid}}) / (1 - j \frac{f_L}{f})}{1 + \left[A_{\text{mid}} / (1 - j \frac{f_L}{f}) \right] \cdot \beta}$$

$$= \frac{A_{\text{mid}}}{1 - j \frac{f_L}{f} + A_{\text{mid}} \cdot \beta}$$

$$\therefore = \frac{A_{\text{mid}}}{(1 + A_{\text{mid}} \beta) - j \frac{f_L}{f}}$$

Dividing the numerator and the denominator with $\frac{1}{1 + A_{\text{mid}} \beta}$ we get

$$A_{f \text{ low}} = \frac{A_{\text{mid}}}{(1 + A_{\text{mid}} \cdot \beta)} \cdot \frac{1}{1 - j \left(\frac{f_L}{1 + A_{\text{mid}} \beta} \right) \frac{1}{f}}$$

$$A_{f \text{ low}} = \frac{A_{f \text{ mid}}}{1 - j \left(\frac{f_{L_f}}{f} \right)} \quad \left(\begin{array}{l} \text{since } A_{f \text{ mid}} = \frac{A_{\text{mid}}}{1 + A_{\text{mid}} \beta} \\ \text{let } f_{L_f} = \frac{f_L}{1 + A_{\text{mid}} \beta} \end{array} \right)$$

where $f_{L_f} = \frac{f_L}{1 + A_{\text{mid}} \beta}$ is the lower cut off frequency with feed back.

From this equation of f_{L_f} it is clear that the lower cut off frequency of an amplifier with feed back (f_{L_f}) is lesser than that of the lower cut off frequency of an amplifier without feed-back (f_L) by a factor $(1 + A_{\text{mid}} \beta)$. Thus by introducing negative feedback, low frequency response of an amplifier is improved.

Higher cut-off frequency (f_{H_f}):

We know that $A_{\text{high}} = \frac{A_{\text{mid}}}{1 + j \left(\frac{f}{f_H} \right)} \rightarrow (6)$

substituting equation (6) in equation (4) we get

$$A_{f \text{ high}} = \left[\frac{A_{\text{mid}}}{1 + j \left(\frac{f}{f_H} \right)} \right] / \left[1 + \left(\frac{A_{\text{mid}}}{1 + j \left(\frac{f}{f_H} \right)} \right) \cdot \beta \right]$$

$$\Rightarrow A_{f \text{ high}} = \frac{A_{\text{mid}}}{1 + j \frac{f}{f_H} + A_{\text{mid}} B}$$

$$\Rightarrow A_{f \text{ high}} = \frac{A_{\text{mid}}}{(1 + A_{\text{mid}} B) + j \frac{f}{f_H}}$$

Dividing the numerator and denominator of RHS with $1 + A_{\text{mid}} B$

we get
$$A_{f \text{ high}} = \frac{A_{\text{mid}}}{1 + A_{\text{mid}} B} \cdot \frac{1}{1 + j \frac{f}{f_H (1 + A_{\text{mid}} B)}} = \frac{A_{f \text{ mid}}}{1 + j \frac{f}{f_{Hf}}}$$

where $A_{f \text{ mid}} = \frac{A_{\text{mid}}}{1 + A_{\text{mid}} B}$ and $f_{Hf} = f_H (1 + A_{\text{mid}} B)$

f_{Hf} is the higher cut off frequency of an amplifier with feedback.

From the equation of f_{Hf} it is clear that upper cutoff frequency of an amplifier with feedback (f_{Hf}) is greater than the upper cutoff frequency of an amplifier without feedback (f_H) by a factor $1 + A_{\text{mid}} B$. Therefore by introducing negative feedback high frequency response of the amplifier is improved.

The bandwidth of an amplifier without feedback is given as $BW = f_H - f_L$.

The bandwidth of an amplifier with feedback is

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{\text{mid}} B) f_H - \frac{f_L}{(1 + A_{\text{mid}} B)} \quad \text{or}$$

it can also be written as $BW_f = BW (1 + A_{\text{mid}} B)$

It is very clear that $f_{Hf} - f_{Lf} > f_H - f_L$.

so bandwidth of the amplifier with feedback is greater than the bandwidth of amplifier without feedback.

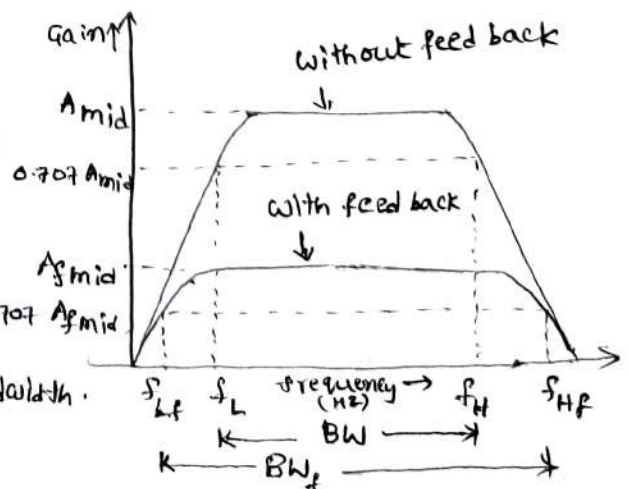


fig: Effect of negative feedback on gain and bandwidth.

Note: As the voltage gain of the feedback amplifier reduces by a factor $1+A\beta$ and its bandwidth increases by $1+A\beta$, the product of gain bandwidth product remains same for with feedback and for without feedback.

$$A_f \times BW_f = \left(\frac{A}{1+A\beta} \right) \times BW (1+A\beta)$$

$$\therefore \boxed{A_f \times BW_f = A \times BW}$$

3) Frequency distortion: (or) Phase distortion reduction

If the feedback network does not contain reactive elements, the gain of the feedback amplifier is not a function of frequency. Under these circumstances the frequency distortion or phase distortion can be reduced.

If feedback factor β is made up of reactive elements, the reactances of those elements will change with frequency, causing β to be changed. As a result feedback amplifier gain will also change with frequency. So feedback network should be made up of passive elements.

4) Reduction in nonlinear distortion:

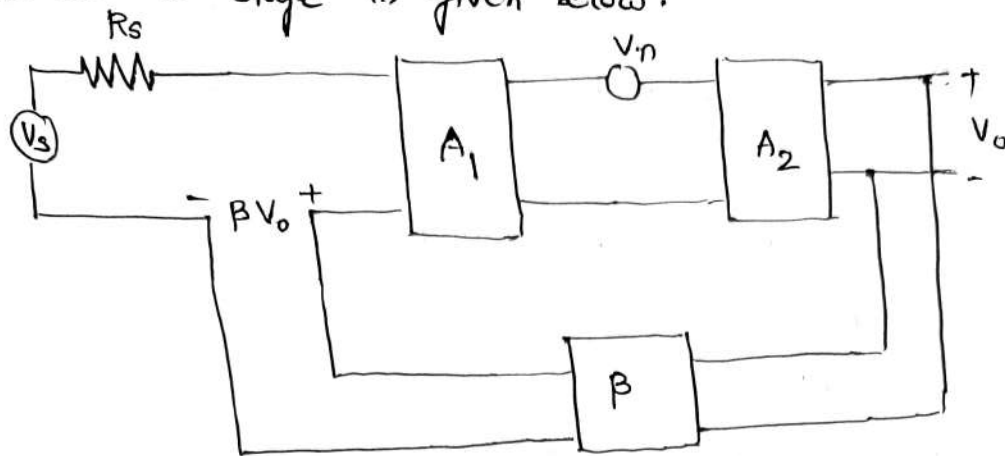
Consider a feedback amplifier with negative feedback, that has a basic amplifier with gain A and assume that the amplifier has the distortion 'D' without feedback and the distortion D_f with feedback. Then the distortion 'D' is reduced by a factor $1+A\beta$ and the distortion with feedback is given by $D_f = \frac{D}{1+A\beta}$.

5) Reduction in noise:

The negative feedback for an amplifier reduces the noise by increasing the ratio of signal to noise. Consider the amplifier block that has noise signal ' V_n ' and gain A_2 . Assume the input signal is V_s and the noise V_n is introduced at the second stage of amplifier as shown below. The signal to noise ratio is given by

$$\frac{S}{N} = \frac{V_s}{V_n}$$

The first stage of the amplifier with gain A_1 does not suffer from noise. This two stage amplifier with negative feedback having noise at 2nd stage is given below.



The output voltage V_o is given by

$$V_o = \frac{V_s A_1 A_2}{1 + A_1 A_2 B} + \frac{V_n A_2}{1 + A_1 A_2 B}$$

$$\text{Signal to noise ratio at the output} = \left(\frac{V_s A_1 A_2}{1 + A_1 A_2 B} \right) / \left(\frac{V_n A_2}{1 + A_1 A_2 B} \right)$$

$$\therefore \frac{S}{N} = \frac{V_s A_1}{V_n}$$

$\therefore$ signal to noise ratio increases by a factor A_1 . This improvement in signal to noise ratio results in reduction in noise.

The effect of negative feedback on input resistance:

consider the negative feedback in an amplifier.

i) when the output of this negative feedback is connected to the input in series with the input signal, the input resistance is increased. Since the feedback signal voltage V_f is out of phase with input voltage V_s that causes the input current I_i to be decreased and hence the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback $\cdot R_i$. Hence the input resistance with feedback (R_{if}) for voltage series feedback and current series feedback is

$$R_{if} = R_i (1 + A B) = R_i D$$

ii) when the negative feedback signal is fed back to the input in shunt

With the amplifier input signal, then the input resistance is decreased.

Since feedback current I_f and input current I_i are in out of phase then $I_i = I_s - I_f$. i.e. $I_s = I_i + I_f$. Then the source input current I_s is increased and the input resistance with feedback $R_{if} = \frac{V_i}{I_s}$ is smaller than the input resistance without feedback i.e. $R_{if} < R_i$. Hence for Voltage shunt and current shunt feedback amplifiers $R_{if} = \frac{R_i}{1+AB} = \frac{R_i}{D}$.

That means the series mixing at input tends to increase the input resistance and the shunt mixing tends to decrease the input resistance.

1) Input resistance for Voltage series feedback amplifier: The following fig shows the voltage series feedback circuit with the input circuit and output circuit replaced by thevenin's model. In this circuit A_v represents the open circuit voltage gain taking R_s into account. We have considered R_s being the part of the amplifier for determining input resistance.

For the voltage series feedback amplifier input resistance with feedback $R_{if} = \frac{V_s}{I_i}$.

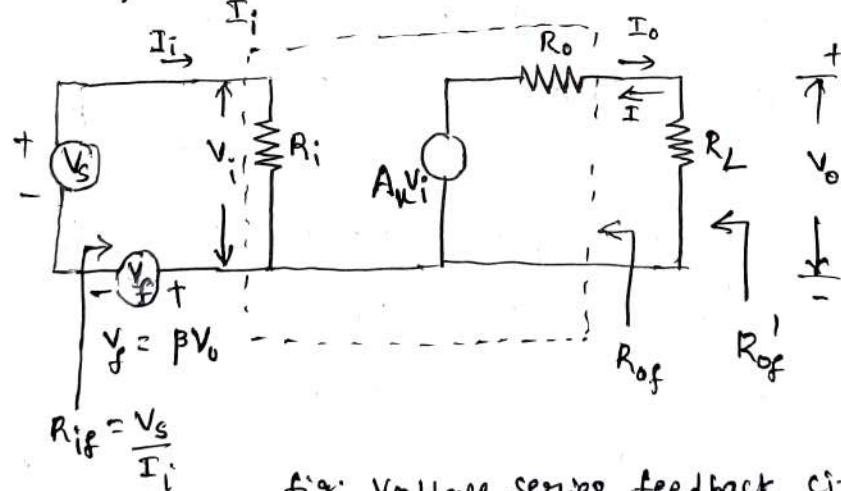


fig: Voltage series feedback circuit

Applying KVL to the input side $V_s = I_i R_i + V_f = I_i R_i + \beta V_o \rightarrow (1)$

out voltage $V_o = \frac{A_v V_i R_L}{R_o + R_L} = A_v V_i$ where $A_v = \frac{A_v R_L}{R_o + R_L} \rightarrow (2)$

From Equation ①, ② $V_s = I_i R_i + \beta V_o = I_i R_i + \beta A_V V_i$

$$\Rightarrow V_s = I_i R_i + \beta A_V I_i R_i$$

$$\Rightarrow V_s = I_i R_i (1 + \beta A_V)$$

$$\therefore \frac{V_s}{I_i} = R_{if} = R_i (1 + \beta A_V)$$

where A_u represents open circuit voltage gain without feedback and A_V indicates the circuit voltage gain without feedback taking R_L into account.

Therefore $A_u = \lim_{R_L \rightarrow \infty} A_V$

2) Input resistance for current series feedback amplifier:

Fig shows the current series feedback amplifier circuit with input circuit represented by Thevenin's model and output circuit by Norton's equivalent circuit. Here input resistance with feedback is given by

$$R_{if} = \frac{V_s}{I_i}$$

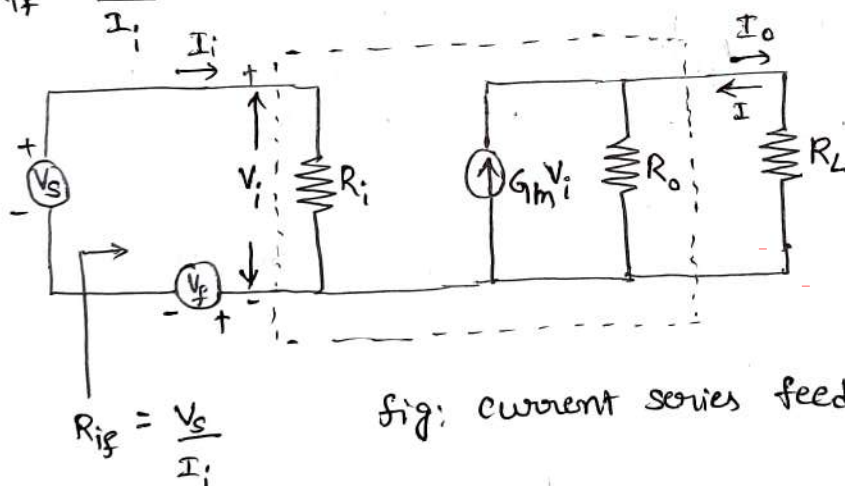


fig: current series feedback amplifier circuit

Applying KVL to the input side,

$$V_s = I_i R_i + V_f = I_i R_i + \beta I_o \quad \rightarrow ①$$

The output current is written as

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \quad \rightarrow ②$$

$$\text{where } G_M = \frac{G_m R_o}{R_o + R_L}$$

From equations ① and ② $V_s = I_i R_i + \beta I_o = I_i R_i + \beta G_M V_i$

$$\Rightarrow V_s = I_i R_i + \beta G_M I_i R_i$$

$$\Rightarrow V_s = I_i R_i (1 + \beta G_M)$$

$$\Rightarrow \frac{V_s}{I_i} = R_i (1 + \beta G_M)$$

$$\therefore \frac{V_s}{I_i} = R_{if} = R_i (1 + \beta G_M)$$

where G_m represents short circuit transconductance without feedback and G_M represents transconductance without feedback taking R_L into account.

$$G_m = \lim_{R_L \rightarrow 0} G_M$$

3) Input resistance for current shunt feedback amplifier:

The fig' below shows the current shunt feedback amplifier circuit with input and output circuits replaced by Norton's equivalent circuits.

Here the input resistance with feedback is given by $R_{if} = \frac{V_i}{I_s}$.

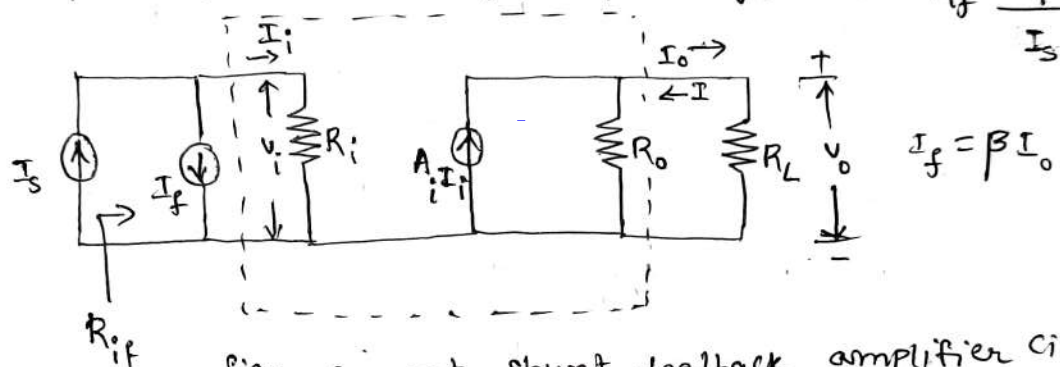


fig: Current shunt feedback amplifier circuit

Applying KCL at the input side $I_s = I_i + I_f = I_i + \beta I_o \rightarrow ①$

$$\text{output current } I_o = \frac{A_i I_i R_o}{R_o + R_L} = A_I I_i \rightarrow ②$$

$$\text{where } A_I = \frac{A_i R_o}{R_o + R_L}$$

From equations ① and ② $I_s = I_i + \beta A_I I_i = I_i (1 + \beta A_I)$

$$\Rightarrow I_s = \frac{V_i}{R_i} (1 + \beta A_I)$$

$$\therefore \frac{V_i}{I_s} = R_{if} = \frac{R_i}{1 + \beta A_I}$$

where A_i represents the short circuit current gain without feedback and A_I represents the current gain without feedback taking R_L into account.

$$\therefore A_i = \lim_{R_L \rightarrow 0} A_I$$

4) Input resistance for voltage shunt feedback amplifier:

The following figure shows the voltage shunt feedback amplifier with input circuit is represented by Norton's equivalent circuit and the output circuit by Thevenin's equivalent circuit. Here the input resistance with feedback is $R_{if} = \frac{V_i}{I_s}$

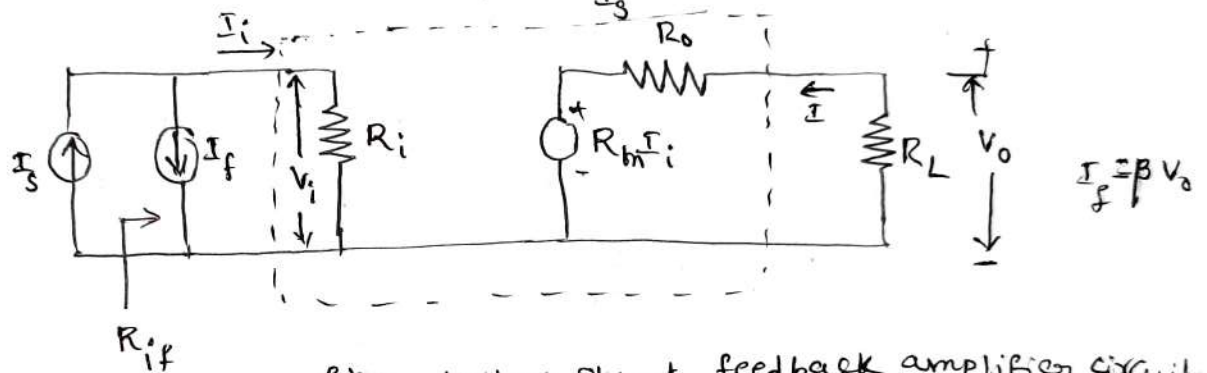


Fig: Voltage shunt feedback amplifier circuit

Applying KCL at input circuit $I_s = I_i + I_f = I_i + \beta V_o \rightarrow \textcircled{1}$

The output voltage $V_o = \frac{R_m I_i R_L}{R_o + R_L} = R_M I_i \rightarrow \textcircled{2}$

where $R_M = \frac{R_m R_L}{R_o + R_L}$

From the equations $\textcircled{1}$ and $\textcircled{2}$ $I_s = I_i + \beta R_M I_i$

$$\Rightarrow I_s = I_i (1 + \beta R_M) = \frac{V_i}{R_i} (1 + \beta R_M)$$

$$\Rightarrow \frac{V_i}{I_s} = \frac{R_i}{1 + \beta R_M}$$

where R_m represents the open circuit transresistance without feedback and R_M represents the transresistance without feedback taking load R_L into account. Therefore $R_m = \lim_{R_L \rightarrow \infty} R_M$

Effect of negative feedback on output resistance

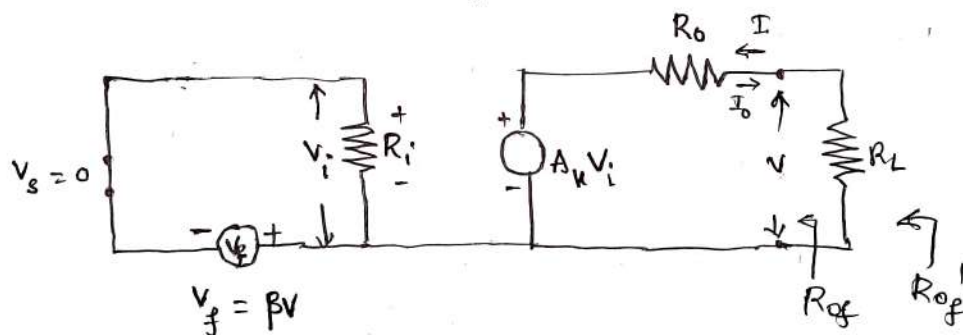
The negative feedback which samples the output voltage irrespective of type of mixing at input side, decreases the output resistance.

i.e. voltage sampling causes the output resistance of the feedback amplifiers to decrease.

Similarly the negative feedback which samples the output current increases the output resistance irrespective of the type of mixing at input side. i.e. current sampling increases the output resistance of the feedback amplifiers.

⇒ output resistance for a voltage series feedback amplifier:

In voltage series feedback amplifier the output resistance R_{of} is obtained by looking into the output terminals by disconnecting R_L (i.e. $R_L = \infty$) and making source voltage V_s zero. (i.e. $V_s = 0$)



Applying KVL to the output circuit

$$A_v V_i + I R_o = V \rightarrow (1)$$

We know that $V_s - V_f = V_i$

Since $V_s = 0$, $V_i = -V_f$.

$$V_i = -(\beta V) \rightarrow (2)$$

From equation (1) and (2)

$$A_v (-\beta V) + I R_o = V$$

($\because V_f = \beta V$ with $V_s = 0$)

$$V (1 + A_v \beta) = I R_o \Rightarrow \frac{V}{I} = \frac{R_o}{1 + A_v \beta}$$

$$\therefore \boxed{R_{of} = \frac{R_o}{1 + A_v \beta}}$$

Now $R_{of}' = R_{of} \parallel R_L$

$$= \left(\frac{R_o}{1+A_u\beta} \cdot R_L \right) / \left(\frac{R_o}{1+A_u\beta} + R_L \right)$$

$$\Rightarrow R_{of}' = \frac{R_o R_L}{R_o + R_L(1+A_u\beta)} = \frac{R_o R_L}{R_o + R_L + R_L A_u \beta}$$

Dividing numerator and denominator with $R_o + R_L$ we get

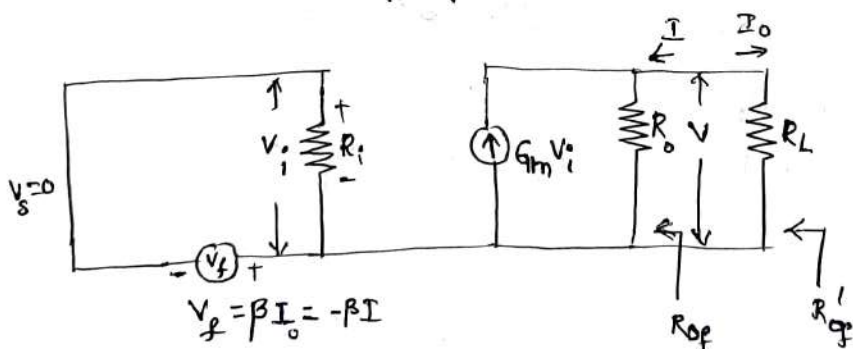
$$R_{of}' = \left(\frac{R_o R_L}{R_o + R_L} \right) / \left(1 + \frac{R_L A_u \beta}{R_o + R_L} \right)$$

$$\boxed{R_{of}' = \frac{R_o'}{1+A_v\beta}}$$

(where $\frac{A_u R_L}{R_o + R_L} = A_v$)
and $R_o' = \frac{R_o R_L}{R_o + R_L}$

where A_u is the open circuit voltage gain without feedback;
and A_v is the voltage gain without feedback taking R_L into account.
2) output resistance for a current series feedback amplifier:

In this amplifier the output resistance is measured by looking into the output terminals disconnecting R_L (i.e. $R_L = \infty$) and the external source voltage signal V_s is made zero.



Applying KCL to the output circuit $G_m V_i = \frac{V}{R_o} - I$

$$\Rightarrow I = \frac{V}{R_o} - G_m V_i \rightarrow (1)$$

we know that $V_s - V_f = V_i$

since $V_s = 0$, $-V_f = V_i$

$$\therefore V_i = -V_f = -(-\beta I) \rightarrow (2)$$

substituting equation (2) in equation (1) we get $I = \frac{V}{R_o} - G_m (-\beta I)$

$$\Rightarrow I(1 + G_m \beta) = \frac{V}{R_o}$$

$$\Rightarrow \frac{V}{I} = R_o(1 + G_m \beta)$$

$$\therefore R_{of} = R_o(1 + G_m \beta)$$

$$R_{of}' = R_{of} \parallel R_L = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{R_o(1 + \beta G_m) R_L}{R_o(1 + \beta G_m) + R_L}$$

$$\Rightarrow R_{of}' = \frac{R_o R_L (1 + \beta G_m)}{R_o + R_L + R_o \beta G_m}$$

Dividing numerator and denominator with $R_o + R_L$

$$R_{of}' = \frac{\left(\frac{R_o R_L}{R_o + R_L} \right) (1 + \beta G_m)}{1 + \frac{R_o \beta G_m}{R_o + R_L}} = \frac{R_o' (1 + \beta G_m)}{1 + \beta G_M}$$

$$\therefore R_{of}' = \frac{R_o' (1 + \beta G_m)}{1 + \beta G_M}$$

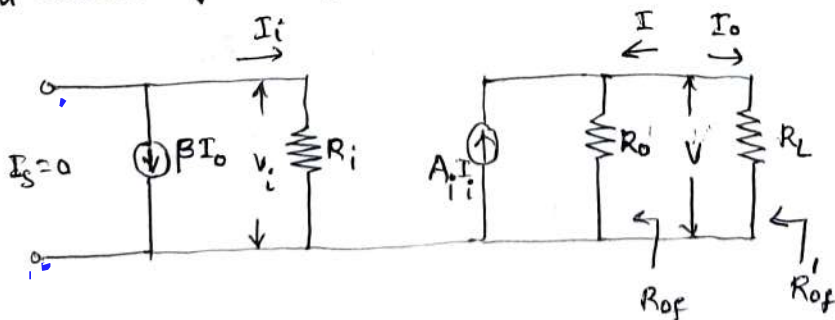
Short circuit

$$\text{where } G_M = \frac{G_m R_o}{R_o + R_L}$$

where G_m is the transconductance without feedback and G_M is the transconductance without feedback taking R_L into account.

3) output resistance for a current shunt feedback amplifier:

In this amplifier the output resistance can be measured by looking into output terminals by disconnecting R_L and making the current source signal I_s zero.



Applying KCL at the output circuit we get

$$A_v I_i = \frac{V}{R_o} - I \Rightarrow I = -A_v I_i + \frac{V}{R_o} \rightarrow (1)$$

We know that $I_s - I_f = I_i$

Since $I_s = 0$, $I_i = -I_f = -\beta I_o = \beta I$ ($\because I_o = -I$)

$$\therefore I_i = \beta I \rightarrow (2)$$

Substituting equation (2) in equation (1) we get

$$I = -A_i \beta I + \frac{V}{R_o}$$

$$\Rightarrow I(1 + A_i \beta) = \frac{V}{R_o}$$

$$\Rightarrow \frac{V}{I} = R_o(1 + A_i \beta)$$

$$\therefore R_{of} = R_o(1 + A_i \beta)$$

$$R_{of}' = R_{of} \parallel R_L = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{R_o(1 + A_i \beta) R_L}{R_o(1 + A_i \beta) + R_L}$$

$$\Rightarrow R_{of}' = \frac{R_o R_L (1 + A_i \beta)}{R_o + R_L + R_o A_i \beta}$$

Divide the numerator and denominator by $R_o + R_L$

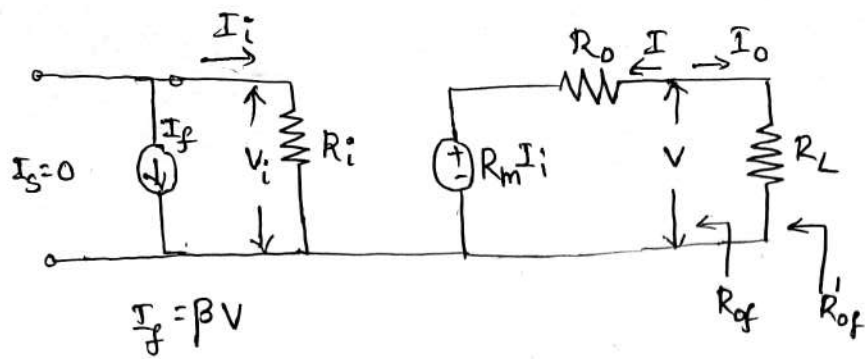
$$R_{of}' = \frac{\frac{R_o R_L}{R_o + R_L} (1 + A_i \beta)}{1 + \left(\frac{R_o}{R_o + R_L} \right) A_i \beta} = \frac{R_o' (1 + A_i \beta)}{1 + A_I \beta}$$

$$\text{where } R_o' = R_o \parallel R_L, \quad A_I = \frac{A_i R_o}{R_o + R_L}$$

where A_i is the short circuit current gain without feedback and A_I is the current gain without feedback taking R_L into account

4) output resistance of a voltage shunt feedback amplifier:

In this amplifier the output resistance is measured by looking into output terminals by disconnecting R_L and making the current source signal I_s zero.



Applying KVL to the output side we get

$$V = R_m I_i + I R_o \rightarrow (1)$$

We know that $I_s - I_f = I_i$

$$\text{Since } I_s = 0 \quad I_i = -I_f = -\beta V \rightarrow (2)$$

substituting equation (2) in equation (1) we get

$$V = R_m (-\beta V) + I R_o$$

$$V(1 + \beta R_m) = + I R_o$$

$$\therefore \frac{V}{I} = \frac{R_o}{1 + \beta R_m}$$

$$\therefore R_{of} = \frac{R_o}{1 + \beta R_m}$$

$$R_{of}' = R_{of} \parallel R_L = \frac{R_{of} R_L}{R_{of} + R_L} = \frac{\frac{R_o}{1 + \beta R_m} R_L}{\frac{R_o}{1 + \beta R_m} + R_L}$$

$$\Rightarrow R_{of}' = \frac{R_o R_L}{R_o + R_L (1 + \beta R_m)} = \frac{R_o R_L}{R_o + R_L + R_L \beta R_m}$$

Dividing the numerator and denominator by $R_o + R_L$

$$R_{of}' = \frac{\left(\frac{R_o R_L}{R_o + R_L} \right)}{1 + \frac{R_L R_m \beta}{R_o + R_L}} = \frac{R_o'}{1 + R_M \beta}$$

$$\text{where } R_o' = \frac{R_o R_L}{R_o + R_L} \quad \text{and} \quad R_M = \frac{R_L R_m}{R_o + R_L}$$

R_m is open circuit transresistance without feedback, R_M is the transresistance without feedback, taking R_L into account.

(13)

Expression for transfer gain of a negative feedback amplifier:

Let the input signal from source as X_s , the output signal X_o , the feedback signal X_f and the input of the basic amplifier as X_i , each of these represents either voltage or current.

Then the difference between the applied input signal X_s and the feedback signal X_f is called as the difference signal (or) error (or) comparison signal denoted by X_i (or) X_d , given as

$$X_d = X_s - X_f = X_i \rightarrow \text{① for negative feed back.}$$

The reverse transmission factor (or) feedback ratio of the feedback network, β is given as $\beta = \frac{X_f}{X_o} \rightarrow \text{②}$

The transfer gain (or) transfer ratio of basic amplifier is A , and is given as $A = \frac{X_o}{X_i} \rightarrow \text{③}$

considering the negative feedback, the transfer gain of the amplifier with negative feedback (A_f) is given as

$$A_f = \frac{X_o}{X_s} \rightarrow \text{④}$$

$$= \frac{X_o}{X_i + X_f} \quad \left(\because \text{from equation ①} \right)$$
$$X_s = X_i + X_f$$

$$= \frac{1}{\frac{X_i}{X_o} + \frac{X_f}{X_o}}$$

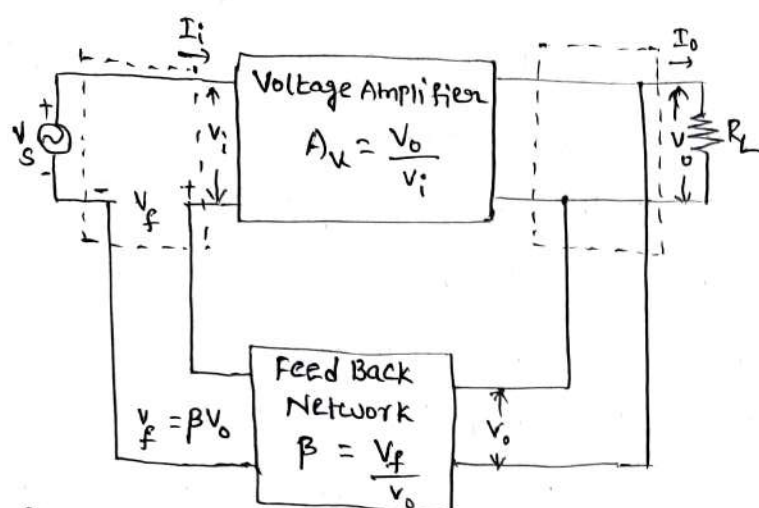
$$= \frac{1}{\frac{1}{A} + \beta} \quad \left(\because \text{from equations ②, ③} \right)$$

$$\therefore \boxed{A_f = \frac{A}{1 + A\beta}}$$

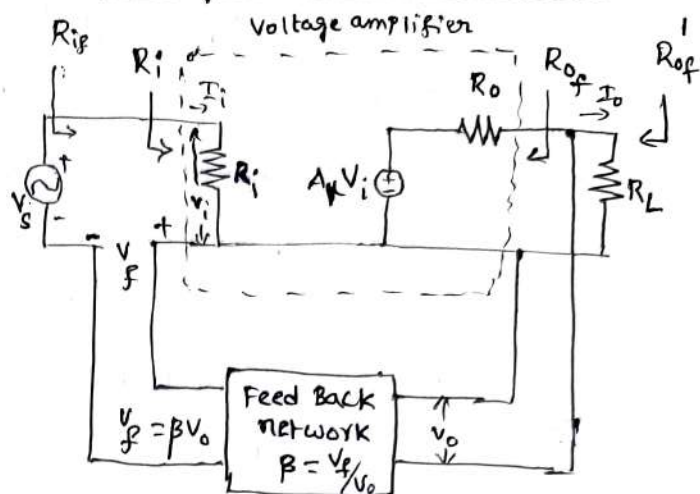
The expression for transfer gain of amplifier with negative feedback is denoted based on the type of basic amplifier.

The expression for transfer gain of negative feedback amplifier for different basic amplifiers is derived below.

1) Transfer gain (or) Transfer ratio of a voltage series feed back amplifier:



fig(a) Voltage series feed back amplifier



fig(b): Equivalent circuit of voltage series feedback amplifier.

- * Figure(a) shows voltage series feedback amplifier, in which a part of the output voltage (V_o) is fed back in series with the input signal (V_s).
- * The sampler used in voltage series feedback amplifier is voltage sampler. For voltage sampling the output voltage V_o is connected in shunt with the input of feedback network that has a feedback ratio of β .
- * For combining the output of feedback network (V_f) with the input voltage (V_s), a series mixer is used i.e. the output voltage of feedback network (V_f) is fed back in series with the input signal (V_s).
- * The difference between V_s and V_f is applied as an input to the voltage amplifier, when the feedback connection is negative feedback.

$$\text{i.e. } V_i = V_s - V_f \rightarrow (1)$$

Feedback ratio of the feedback network is β and is given as

$$\beta = \frac{V_f}{V_o} \rightarrow (2)$$

The transfer gain of the voltage amplifier is A_u and is given as

$$A_u = \frac{V_o}{V_i} \rightarrow (3)$$

The transfer gain of the voltage amplifier with feedback is given as

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{V_i + V_f} \quad \left(\because \text{from equation (1)} \right)$$

$V_s = V_i + V_f$

$$\Rightarrow A_{Vf} = \frac{1}{\frac{V_i}{V_o} + \frac{V_f}{V_o}}$$

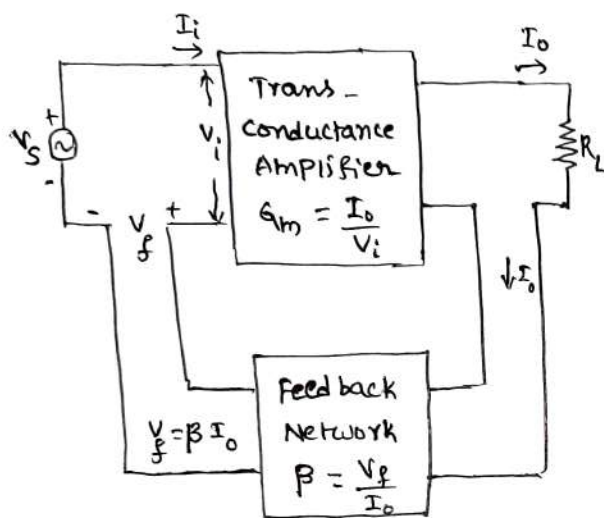
$$\Rightarrow A_{Vf} = \frac{1}{\frac{1}{A_v} + \beta}$$

($\because$ from equations ②, ③)

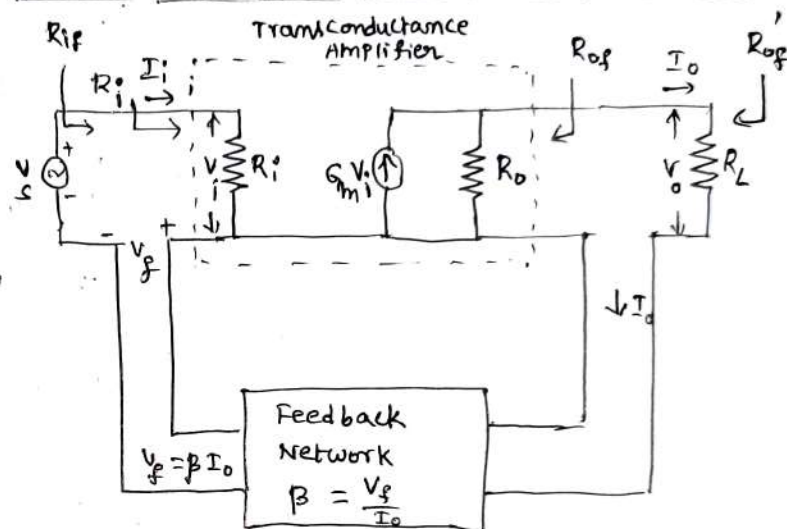
$$\therefore A_{Vf} = \frac{A_v}{1 + A_v \beta}$$

This equation says that the voltage gain with feedback is equal to the voltage amplifier gain reduced by a factor $1 + A_v \beta$.

2) Transfer gain (or) Transfer ratio of a current series feedback amplifier:



fig(a): Current series feedback Amplifier



fig(b): Equivalent Circuit of Current Series feedback amplifier

* Figure (a) shows the current series feedback amplifier in which the value of the output current I_o is proportional to the developed voltage V_i .

* Here current sampler is used in a current series feedback amplifier. For current sampling the output current I_o is connected in series with the input of feedback network.

* For combining the output of feedback network (V_f) and the input voltage (V_s), a series mixer is used. i.e. the output voltage (V_f) of the feedback network is fed back in series with the input voltage (V_s).

* The difference between V_s and V_f is applied as the input to

the transconductance amplifier, when feedback connection is negative feedback ie $V_i = V_s - V_f \rightarrow ①$

Feedback ratio of the feedback network is $\beta = \frac{V_f}{I_o} \rightarrow ②$

The transfer gain of the transconductance amplifier is G_m and is given as $G_m = \frac{I_o}{V_i} \rightarrow ③$

The transfer gain of the trans conductance amplifier with feedback is G_{mf} and is given as $G_{mf} = \frac{I_o}{V_s} = \frac{I_o}{V_i + V_f} \left(\because \text{from eq ①} \right)$
 $V_s = V_i + V_f$

$$\Rightarrow G_{mf} = \frac{1}{\frac{V_i}{I_o} + \frac{V_f}{I_o}}$$

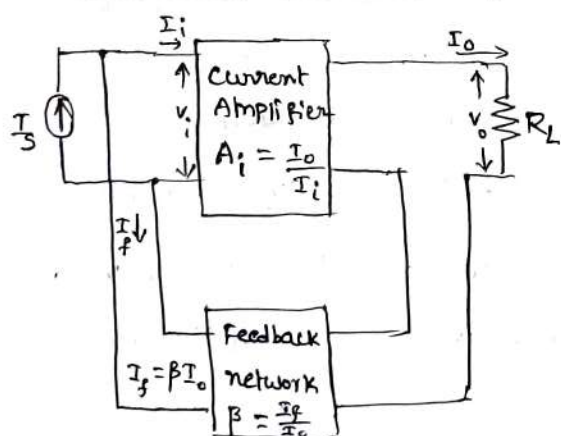
$$\Rightarrow G_{mf} = \frac{1}{\frac{1}{\frac{I_o}{V_i}} + \frac{V_f}{I_o}}$$

$$\Rightarrow G_{mf} = \frac{1}{\frac{1}{G_m} + \beta} \quad \left(\because \text{From equations ②, ③} \right)$$

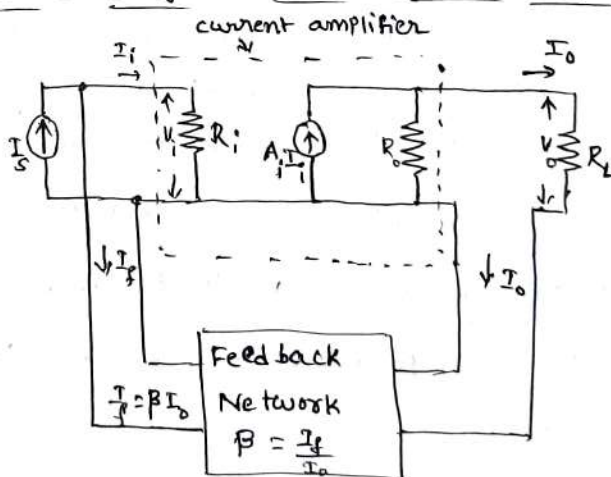
$$\therefore \boxed{G_{mf} = \frac{G_m}{1 + G_m \beta}}$$

This equation says that the transconductance with feedback is equal to transconductance without feedback reduced by a factor $1 + G_m \beta$.

3) Transfer gain (or) transfer ratio of a Current shunt feedback amplifier:



fig(a): Current shunt - feedback amplifier



fig(b): Equivalent circuit of a Current - shunt feedback amplifier.

- * Figure(a) shows the current shunt feedback amplifier block diagram
- * In this amplifier, the current sampler is used. For current sampling the output current I_o is connected in series with the input of the feedback network.
- * For combining the output of feedback network (I_f) and the input current I_s , a shunt mixer is used. i.e the output current I_f of the feedback network is fed back in shunt with the input current I_s .
- * The difference between I_s and I_f is applied as the input to the current amplifier provided the feedback connection is negative feedback.

$$\text{i.e } I_i = I_s - I_f \longrightarrow \textcircled{1}$$

Feed Back ratio of the feedback network is β given as

$$\beta = \frac{I_f}{I_o} \longrightarrow \textcircled{2}$$

The transfer gain of current amplifier is A_i and is given as

$$A_i = \frac{I_o}{I_i} \longrightarrow \textcircled{3}$$

The transfer gain of current amplifier with negative feedback is

$$\text{given as } A_{if} = \frac{I_o}{I_s} = \frac{I_o}{I_i + I_f} \quad \left(\because \text{from equation } \textcircled{1} \right)$$

$$I_s = I_i + I_f$$

$$= \frac{1}{\left(\frac{I_i}{I_o} \right) + \left(\frac{I_f}{I_o} \right)}$$

$$= \frac{1}{\left(\frac{1}{A_i} \right) + \frac{I_f}{I_o}}$$

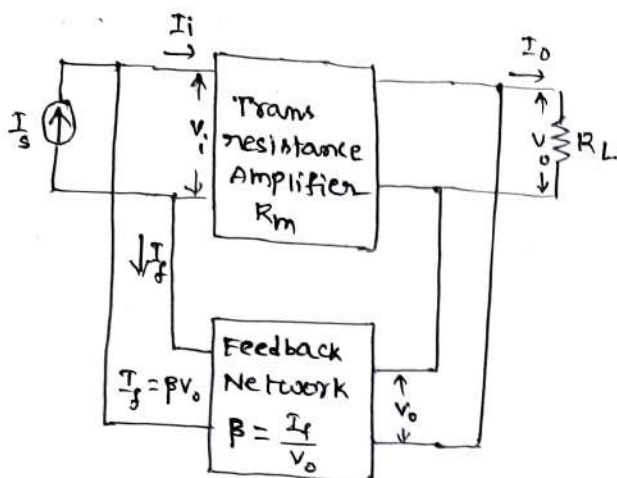
$$= \frac{1}{\frac{1}{A_i} + \beta}$$

$$\left(\because \text{from equations } \textcircled{2}, \textcircled{3} \right)$$

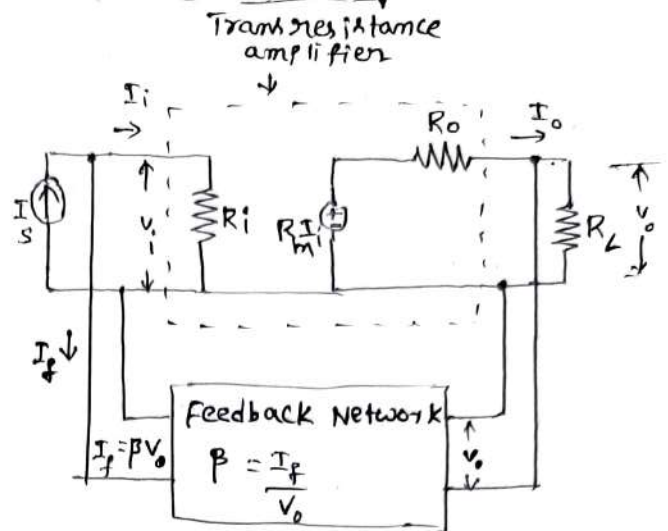
$$\therefore \boxed{A_{if} = \frac{A_i}{1 + A_i \beta}}$$

the above equation says that the current gain with negative feedback is equal to the current gain without feedback reduced by a factor of $1 + A_i \beta$.

4) Transfer gain (or) transfer ratio of a voltage shunt feedback amplifier:



fig(a): voltage shunt feedback Amplifier



fig(b): equivalent circuit of a voltage - shunt feedback amplifier.

- * figure (a) shows the voltage shunt feedback amplifier block diagram.
- * In this amplifier the voltage sampler is used. For voltage sampling the output voltage (V_o) is connected in parallel with the input of the feedback network.
- * For combining the output current (I_f) of the feedback network and the input current I_s , shunt mixing is used. i.e the output current (I_f) of the feedback network is fed back in parallel to the input current (I_s).
- * The difference between I_s and I_f is applied as the input to the trans resistance amplifier provided the feedback is negative feedback.

$$\text{i.e } I_i = I_s - I_f \longrightarrow (1)$$

Feedback ratio of the feedback network is β and is given as

$$\beta = \frac{I_f}{V_o} \longrightarrow (2)$$

The transfer gain of the trans resistance amplifier is R_m given as

$$R_m = \frac{V_o}{I_i} \longrightarrow (3)$$

The transfer gain of the transresistance amplifier with feedback is R_{mf} given as $R_{mf} = \frac{V_o}{I_s} = \frac{V_o}{I_i + I_f}$ ($\because$ from equation ①)
 $I_s = I_i + I_f$

$$\Rightarrow R_{mf} = \frac{1}{\frac{I_i}{V_o} + \frac{I_f}{V_o}}$$

$$= \frac{1}{\frac{1}{R_m} + \beta}$$

($\because$ from equations ②, ③)

$$\therefore \boxed{R_{mf} = \frac{R_m}{1 + R_m \beta}}$$

The above equation says, the transresistance with negative feedback is equal to the transresistance without feedback reduced by a factor of $1 + R_m \beta$.

Method of analysis of a feedback amplifier:

For analysing the feedback amplifier it is necessary to go through the following steps.

STEP 1: Identify the topology (type of feedback)

(a) To identify the type of sampling:

- i) By shorting the output node (ie making $V_o = 0$), if the feedback signal becomes zero, then it is called voltage sampling
- ii) By opening the output loop (ie making $I_o = 0$), if the feedback signal becomes zero, then it is called current sampling

(b) To identify the type of mixing:

- i) If the feedback signal is subtracted from the externally applied signal as a voltage in the input loop it is called series mixing.
- ii) If the feedback signal is subtracted from the externally applied signal as a current in the input loop, it is called shunt mixing.

STEP 2: To find the input circuit

- i) For voltage sampling, the output voltage is made zero by shorting the output node.

ii) for Current sampling, the output current is made zero by opening the output loop.

Step 3: To find the output circuit

i) For series mixing, the input current is made zero by opening the input loop.

ii) For shunt mixing, the input voltage is made zero by shorting the input node.

From step 2 and step 3 ensure that the feedback is reduced to zero, without altering the loading on the basic amplifier.

Step 4: Replace each active device by proper model. for example the hybrid- π model for a transistor at high frequencies, or the h-parameter model at low frequencies.

Step 5: Find A , i.e. the open loop gain of the amplifier (gain without feedback).

Step 6: Indicate X_f (i.e. whether V_f (or) I_f) and X_o (i.e. whether V_o (or) I_o) on the circuit and evaluate $\beta = X_f/X_o$.

Step 7: From A and β find D , A_f , R_{if} , R_{of} and R_{of}' .

Comparison among the characteristics of feedback amplifiers:

Topology	Voltage series	Current series	Current shunt	Voltage shunt
Characteristics				
1) Feedback signal (X_f)	Voltage (V_f)	Voltage (V_f)	Current (I_f)	Current (I_f)
2) Sampled signal (X_o)	Voltage (V_o)	Current (I_o)	Current (I_o)	Voltage (V_o)
3) To find the input circuit	Set $V_o = 0$	Set $I_o = 0$	Set $I_o = 0$	Set $V_o = 0$
4) To find the output circuit	Set $I_i = 0$	Set $I_i = 0$	Set $V_i = 0$	Set $V_i = 0$
5) Signal source	Thevenin	Thevenin	Norton	Norton
6) $\beta = \frac{X_f}{X_o}$	V_f/V_o	V_f/I_o	I_f/I_o	I_f/V_o
7) $A = \frac{X_o}{X_i}$	$A_v = V_o/V_i$	$G_m = I_o/V_i$	$A_I = \frac{I_o}{I_i}$	$R_m = \frac{V_o}{I_i}$
8) Desensitivity $D = 1 + A\beta$	$1 + A_v\beta$	$1 + G_m\beta$	$1 + A_I\beta$	$1 + R_m\beta$
9) $A_f = A/(1 + A\beta)$	$A_{vf} = A_v/(1 + A_v\beta)$	$G_{mf} = G_m/(1 + G_m\beta)$	$A_{If} = A_I/(1 + A_I\beta)$	$R_{mf} = R_m/(1 + R_m\beta)$
10) R_{if}	$R_i(1 + A_v\beta)$	$R_i(1 + G_m\beta)$	$R_i/(1 + A_I\beta)$	$R_i/(1 + R_m\beta)$
11) R_{of}	$R_o/(1 + A_v\beta)$	$R_o(1 + G_m\beta)$	$R_o(1 + A_I\beta)$	$R_o/(1 + R_m\beta)$
12) R_{of}'	$R_o'/(1 + A_v\beta)$	$R_o'(1 + G_m\beta)/(1 + G_{hf}\beta)$	$R_o'(1 + A_I\beta)/(1 + A_I\beta)$	$R_o'/(1 + R_m\beta)$

Problems

(17)

- 1) The distortion in amplifier is found to be 3%, when the feedback ratio of negative feedback amplifier is 0.04. When the feedback is removed, the distortion becomes 15%. Find the open loop gain & closed loop gain.

Sol) Given negative feedback amplifier having feedback ratio $\beta = 0.04$
Distortion in amplifier with negative feedback is $D_f = 3\%$
i.e. $D_f = 0.03$

Distortion in amplifier when feedback is removed $D = 15\% = 0.15$

We know that $D_f = \frac{D}{1+A\beta} \Rightarrow 0.03 = \frac{0.15}{1+A(0.04)}$

$$\Rightarrow 0.03 + A(0.0012) = 0.15$$

$$\therefore \text{open loop gain } (A) = 100$$

Closed loop gain $A_f = \frac{A}{1+A\beta}$ for negative feedback

$$= \frac{100}{1+(100)(0.04)}$$

$$\therefore A_f = 20$$

$\therefore$ open loop gain $A = 100$, closed loop gain $A_f = 20$.

- 2) An amplifier has midband voltage gain 500 with lower and upper cutoff frequencies as 100 Hz and 100 kHz respectively. If 5% feedback is applied find lower and upper cutoff frequencies with feedback.

Sol) Given $A_{v\text{mid}} = 500$, $f_L = 100 \text{ Hz}$, $f_H = 100 \text{ kHz}$

feedback factor $\beta = 5\% = 0.05$

$$f_{Lf} = ? \quad f_{Hf} = ?$$

We know that f_{Lf} for negative feedback is given as

$$f_{Lf} = \frac{f_L}{1+A_{\text{mid}}\beta} = \frac{100}{1+(500)(0.05)} = 3.84615 \text{ Hz}$$

f_{Hf} for negative feedback amplifier is

$$f_{Hf} = f_H (1+A_{\text{mid}}\beta) = 100 \times 10^3 (1+(500)(0.05))$$

$$\therefore f_{Hf} = 2.6 \text{ MHz}$$

$\therefore$ lower cutoff frequency with feedback $f_{Lf} = 3.84615 \text{ Hz}$
upper cutoff frequency with feedback $f_{Hf} = 2.6 \text{ MHz}$.

3) A voltage series negative feedback amplifier has a voltage gain without feedback of $A = 50$, input resistance $R_i = 2\text{ k}\Omega$, output resistance $R_o = 15\text{ k}\Omega$, feedback ratio of 0.01 . Calculate the voltage gain, input resistance and output resistance of amplifier with feedback.

Sol) Given A negative feedback voltage series amplifier.

Voltage gain without feedback $A_V = 50$

Input resistance without feedback $R_i = 2\text{ k}\Omega$

output resistance without feedback $R_o = 15\text{ k}\Omega$

Feedback ratio $\beta = 0.01$

Voltage gain with feedback $A_{V_f} = \frac{A_V}{1 + A_V\beta} = \frac{50}{1 + (50)(0.01)} = 33.3333$

Input resistance with feedback $R_{if} = R_i(1 + A_V\beta)$
 $= 2 \times 10^3(1 + 50(0.01))$

$\therefore R_{if} = 3\text{ k}\Omega$

output resistance with feedback $R_{of} = \frac{R_o}{1 + A_V\beta} = \frac{15 \times 10^3}{1 + (50)(0.01)}$

$\therefore R_{of} = 10\text{ k}\Omega$

4) An amplifier has a midband gain of 1500 and a bandwidth of 4 MHz . The midband gain reduces to 150 when a negative feedback is applied. Determine the value of feedback factor and the bandwidth.

Sol) Given $A_{mid} = 1500$, $BW = 4\text{ MHz} = 4 \times 10^6\text{ Hz}$

mid band gain reduces to 150 when negative feedback is applied.

i.e $A_{fmid} = 150$, let feedback factor $= \beta$

We know that $A_{fmid} = \frac{A_{mid}}{1 + A_{mid}\beta}$

$$\Rightarrow 150 = \frac{1500}{1 + (1500\beta)}$$

$$\Rightarrow 1 + 1500\beta = 10 \Rightarrow 1500\beta = 9$$

$\therefore$ feedback factor $\beta = 0.006$

Bandwidth with negative feedback $BW_f = BW(1 + A_{mid}\beta)$
 $= 4 \times 10^6(1 + (1500 \times 0.006))$

$\therefore$ Bandwidth with negative feedback $(BW_f) = 40\text{ MHz}$

- 5) An amplifier with $2.5\text{ k}\Omega$ input resistance and $50\text{ k}\Omega$ output resistance has a voltage gain of 100. The amplifier is now modified to provide 5% negative feedback in series with the input. Calculate the voltage gain, input resistance, & output resistance with feedback.

sol) Given $A_v = 100$, $R_i = 2.5\text{ k}\Omega$, $R_o = 50\text{ k}\Omega$

Given feedback factor $\beta = 0.05$ ($\because 5\%$) negative feedback.

voltage gain with feed back $A_{vf} = \frac{A_v}{1 + A_v \beta} = \frac{100}{1 + (100)(0.05)} = 16.6666$

According to the given data the amplifier here we have is voltage-series feed back amplifier, for which $R_{if} = R_i (1 + A_v \beta)$ and

$$R_{of} = \frac{R_o}{1 + A_v \beta}$$

Input resistance with feed back $R_{if} = R_i (1 + A_v \beta)$
 $= 2.5 \times 10^3 (1 + (100)(0.05))$

$\therefore R_{if} = 15\text{ k}\Omega$

output resistance with feed back $R_{of} = \frac{R_o}{1 + A_v \beta} = \frac{50 \times 10^3}{1 + (100)(0.05)}$

$\therefore R_{of} = 8.333\text{ k}\Omega$

- 6) An amplifier has an open loop gain of 1000 and feedback ratio of 0.04. If the open loop gain changes by 10% due to temperature, find the Percentage change in gain of the amplifier with feedback.

sol) Given open loop gain $A = 1000$

feedback ratio $\beta = 0.04$

Refer Problem No 13

(Wrong method)

Gain of amplifier with feed back $A_f = \frac{A}{1 + A\beta} = \frac{1000}{1 + (1000)(0.04)}$

$\Rightarrow A_f = 24.39024$

The open loop gain changes by 10% due to temperature variation.

$\therefore$ New open loop gain $A_1 = 1000 + 10\% \text{ of } 1000 = 1100$

Gain of amplifier with feed back $A_{1f} = \frac{A_1}{1 + A_1 \beta} = \frac{1100}{1 + (1100)(0.04)} = 24.444444$

% change in gain of the amplifier with feed back = $\frac{24.444444 - 24.39024}{24.39024} \times 100$

$\therefore$ % change in gain of amplifier with feed back = 0.2222%

- ⑦ The voltage gain of an amplifier without feedback is 60dB. It decreases to 40dB with feedback. Calculate feedback factor.

Sol) Given voltage gain of an amplifier without feedback = 60 dB

$$\text{i.e. } 20 \log_{10} A_v = 60$$

$$\log_{10} (A_v) = 3$$

$$A_v = 1000.$$

voltage gain with feedback = 40 dB

$$\text{i.e. } 20 \log_{10} A_{vf} = 40$$

$$\log_{10} A_{vf} = 2$$

$$A_{vf} = 100.$$

Feedback factor $\beta = ?$

$$\text{we know that } A_{vf} = \frac{A_v}{1 + A_v \beta} \Rightarrow 100 = \frac{1000}{1 + (1000 \beta)}$$

$$\Rightarrow 1 + 1000\beta = 10$$

$$\therefore \text{ feedback factor } (\beta) = \underline{\underline{0.009}}$$

- 8) An amplifier with negative feedback has a gain of 50. It is found that without feedback, an input signal of 0.1V is required to produce a given output. Where as with feedback the input signal must be 0.8V for the same output. Calculate the voltage gain and feedback ratio.

Sol) Given $A_{vf} = 50,$

$$V_i = 0.1V,$$

$$V_o = ?$$

with feedback the _x signal must be equal to 0.8V.

$$\text{i.e. } V_s = V_i + V_f = 0.8V$$

$$\Rightarrow V_s = 0.1 + V_f = 0.8V$$

$$V_f = 0.7V.$$

$$\text{we know that } A_{vf} = \frac{V_o}{V_s} = 50$$

$$\Rightarrow \frac{V_o}{0.8} = 50 \Rightarrow V_o = 40V.$$

(19)

voltage gain with out feed back $A_v = \frac{V_o}{V_i} = \frac{40}{0.1} = 400$

$$\text{Feedback factor } (\beta) = \frac{V_f}{V_o} = \frac{0.7}{40} = 0.0175$$

9) A current shunt feedback amplifier has a current gain of 100, $Z_i = 2k\Omega$, $Z_o = 15k\Omega$, find A_{if} , Z_{if} , Z_{of} . $\beta = 0.05$

sol) Given $A_i = 100$, $\beta = 0.05$, $Z_i = 2k\Omega$, $Z_o = 15k\Omega$

$$A_{if} = \frac{A_i}{1 + A_i \beta} = \frac{100}{1 + (100)(0.05)} = 16.6666$$

$$Z_{if} = \frac{Z_i}{1 + A_i \beta} = \frac{2 \times 10^3}{1 + (100)(0.05)} = 333.333 \Omega$$

$$Z_{of} = Z_o (1 + A_i \beta) = 15 \times 10^3 (1 + (100)(0.05)) = 90k\Omega$$

10) A current series feedback amplifier has $G_M = 500 \Omega$, $R_i = 3k\Omega$, $R_o = 30k\Omega$, $\beta = 0.01$. Find G_{Mf} , R_{if} , R_{of} .

sol) Given $G_M = 500 \Omega$, $R_i = 3k\Omega$ and $R_o = 30k\Omega$. $\beta = 0.01$

$$G_{Mf} = \frac{G_M}{1 + G_M \beta} = \frac{500}{1 + (500)(0.01)} = 83.3333 \Omega$$

$$R_{if} = R_i (1 + G_M \beta) = 3 \times 10^3 (1 + (500)(0.01)) = 18k\Omega$$

$$R_{of} = R_o (1 + G_M \beta) = 30 \times 10^3 (1 + (500)(0.01)) = 180k\Omega$$

11) A voltage shunt feedback amplifier has $R_M = 300 \Omega$, $R_i = 2k\Omega$ and $R_o = 20k\Omega$. $\beta = 0.05$. Find R_{Mf} , R_{if} and R_{of} .

sol) Given $R_M = 300 \Omega$, $R_i = 2k\Omega$, $R_o = 20k\Omega$

$$R_{Mf} = \frac{R_M}{1 + R_M \beta} = \frac{300}{1 + (300)(0.05)} = 18.75 \Omega$$

$$R_{if} = \frac{R_i}{1 + R_M \beta} = \frac{2 \times 10^3}{1 + (300)(0.05)} = 125 \Omega$$

$$R_{of} = \frac{R_o}{1 + R_M \beta} = \frac{20 \times 10^3}{1 + (300)(0.05)} = 1.25k\Omega$$

12) An amplifier has a midband gain of 125 and a bandwidth of 250KHz. a) If 4% -ve feedback is applied find new bandwidth and new gain b) If Bandwidth is restricted to 1MHz find β value

Sol) Given $A_{mid} = 125$, $BW = 250 \text{ KHz}$,

a) $\beta = 4\% = 0.04$ with negative feedback.

$$\text{New Bandwidth } BW_f = BW (1 + A_{mid} \beta) = 250 \times 10^3 (1 + (125 \times 0.04))$$

$$BW_f = 1.5 \text{ MHz}$$

$$\text{New Gain with negative feedback } A_f = \frac{A}{1 + A\beta} = \frac{125}{1 + (125)(0.04)} = 20.8333$$

b) BW_f' is given as $BW_f' = 1 \text{ MHz}$, then $\beta' = ?$

$$BW_f' = BW (1 + A_{mid} \beta')$$

$$1 \times 10^6 = 250 \times 10^3 (1 + 125 \beta')$$

$$\Rightarrow \beta' = 0.024 = 2.4\%$$

13) An amplifier has an open loop gain of 1000, feedback ratio of 0.04. If the open loop gain changes by 10% due to temperature. Find the percentage change in the gain of amplifier with feedback.

Sol) Given open loop gain $(A) = 1000$,

feedback ratio $(\beta) = 0.04$.

Given the fractional change in open loop gain $= \frac{dA}{A} = 10\% = 0.1$

Fractional change (percentage change) in gain of the amplifier,

$$\text{with feedback} = \frac{dA_f}{A_f} = ?$$

$$\text{we know that the sensitivity } S = \frac{\left(\frac{dA_f}{A_f}\right)}{\left(\frac{dA}{A}\right)} = \frac{1}{1 + A\beta}$$

$$\Rightarrow \frac{\left(\frac{dA_f}{A_f}\right)}{0.1} = \frac{1}{1 + (1000)(0.04)}$$

$$\Rightarrow \frac{dA_f}{A_f} = \frac{0.1}{41} = 0.002439$$

$$\Rightarrow \frac{dA_f}{A_f} = 0.2439\%$$

$\therefore$ Percentage change in the gain of the amplifier with feedback
i.e. $\frac{dA_f}{A_f} = 0.2439\%$

- 14) An amplifier has a voltage gain with feedback of 100. If the gain without feedback changes by 20% and the gain with feedback is restricted to 2%, determine the open loop gain and feedback factor. (20)

Sol) Given the voltage gain with feedback $A_f = 100$.

$$\text{Fractional change in the gain without feedback} = \frac{dA}{A} = 20\% = 0.2$$

$$\text{Fractional change in the gain with feedback} = \frac{dA_f}{A_f} = 2\% = 0.02$$

$$\text{we know that } \left(\frac{dA_f}{A_f} \right) / \left(\frac{dA}{A} \right) = \frac{1}{1+A\beta}$$

$$\Rightarrow \frac{0.02}{0.2} = \frac{1}{1+A\beta}$$

$$\Rightarrow 1+A\beta = 10$$

$$\text{we know that } A_f = \frac{A}{1+A\beta} \quad (\because A_f = 100)$$

$$\Rightarrow 100 = \frac{A}{10} \quad (\because 1+A\beta = 10)$$

$$\Rightarrow A = 1000$$

$$1+A\beta = 10 \Rightarrow 1+(1000\beta) = 10$$

$$\therefore \beta = 0.009$$

$\therefore$ open loop gain $A = 1000$, feedback factor $\beta = 0.009$.

- 15) An amplifier has open loop gain of 4000 and a feedback ratio of 0.05. If the open loop gain changes by 15% due to temperature. Find the percentage change in the gain of the amplifier with feedback.

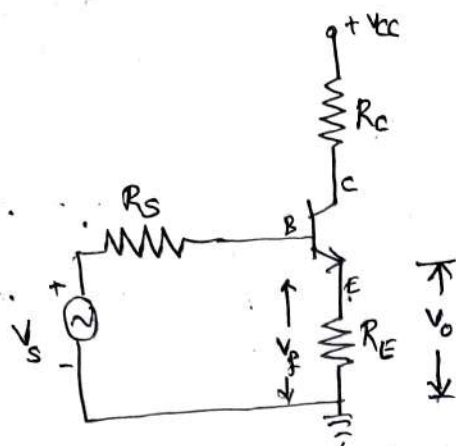
Sol) Given $A = 4000$, $\beta = 0.05$

$$\frac{dA}{A} = 15\% = 0.15, \quad \frac{dA_f}{A_f} = ?$$

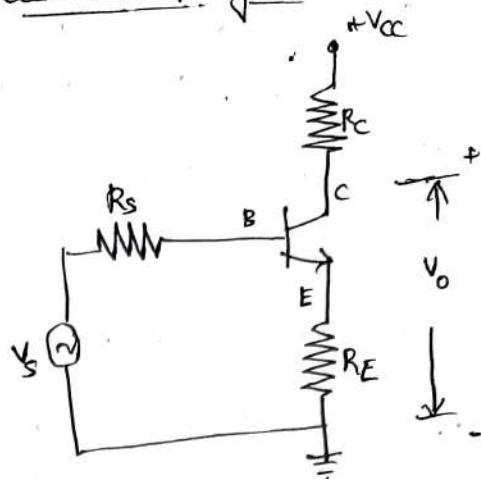
$$\text{we know that } \frac{dA_f}{A_f} = \frac{\left(\frac{dA}{A} \right)}{1+A\beta} = \frac{0.15}{1+(4000)(0.05)}$$

$$\therefore \frac{dA_f}{A_f} = 0.07462\%$$

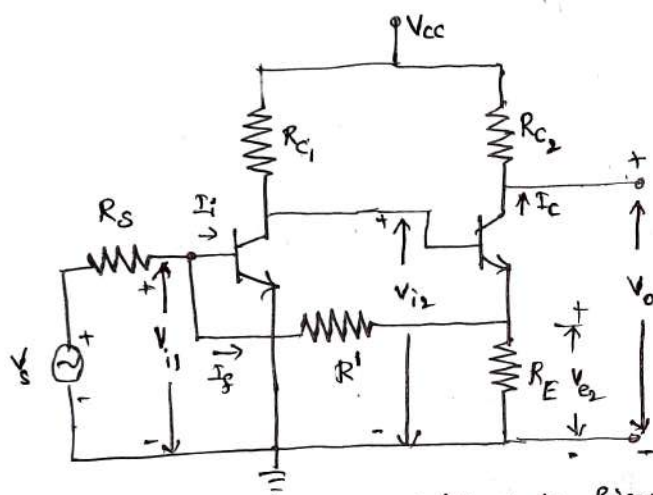
Practical circuits for different feedback topologies:



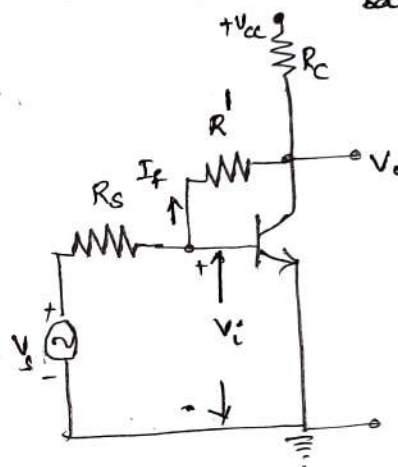
fig(a) BJT emitter follower circuit
(for voltage series feedback Amplifier)



fig(b): CE amplifier with unbypassed emitter resistor (current series feedback amplifier)



fig(c): Second transistor emitter to first transistor base feedback pair
(for current shunt feedback amplifier)



fig(d): Common Emitter with a resistor R' connected between input and output
(for voltage shunt feedback amplifier)

Explain the characteristics of negative feedback (or) Explain the effects of negative feedback on amplifier characteristics:

1) Stabilization of Gain:

The gain of the amplifier with negative feedback is

$$A_f = \frac{A}{1 + A\beta} \rightarrow (1)$$

Differentiating the A_f with respect to A

$$\frac{dA_f}{dA} = \frac{(1 + A\beta)(1) - A(\beta)}{(1 + A\beta)^2} = \frac{1}{(1 + A\beta)^2}$$

$$\Rightarrow dA_f = \frac{dA}{(1 + A\beta)^2}$$

2) Extension of bandwidth:

The difference between the upper cutoff frequency and lower cutoff frequency is called as the bandwidth of an amplifier given as

$$\text{Bandwidth (BW)} = f_H - f_L$$

The bandwidth of the amplifier with feedback increases by a factor of $(1+A\beta)$ i.e. $BW_f = BW(1+A\beta)$. Because, due to negative feedback upper cutoff frequency f_{Hf} is increased by a factor $(1+A\beta)$ and lower cutoff frequency f_{Lf} is decreased by the same factor $(1+A\beta)$. i.e. $f_{Hf} = f_H(1+A\beta)$, $f_{Lf} = \frac{f_L}{1+A\beta}$.

3) Frequency Distortion reduction (or) Phase distortion reduction:

If the feedback network does not contain reactive elements, the gain of the feedback amplifier is not a function of frequency. Under these circumstances the frequency distortion (or) phase-distortion can be reduced.

If feedback factor β is made up of reactive elements, the reactances of those elements will change with frequency, causing β to be changed. As a result feedback amplifier gain will also change with frequency. So feedback network should be made up of passive elements.

4) Reduction in nonlinear distortion and noise:

The negative feedback introduced to an amplifier reduces both noise and non linear distortion by a factor $(1+A\beta)$. Thus noise and nonlinear distortion also reduced by the same factor as that of transfer gain.

5) Increase in input resistance:

An amplifier should have high input resistance. If the feedback signal is combined with the input source signal in series (i.e. if the mixer used is a series mixer) the input resistance R_i increases with a factor $1+A\beta$. i.e. $R_{if} = R_i(1+A\beta)$.

$$\Rightarrow \frac{dA_f}{A_f} = \frac{dA}{A_f(1+A\beta)^2}$$

$$\Rightarrow \frac{dA_f}{A_f} = \frac{\frac{dA}{A}}{\frac{1}{1+A\beta}} (1+A\beta)^2$$

$$\Rightarrow \left(\frac{dA_f}{A_f} \right) / \left(\frac{dA}{A} \right) = \frac{1}{1+A\beta}$$

$$\therefore \text{Sensitivity } S = \left(\frac{dA_f}{A_f} \right) / \left(\frac{dA}{A} \right) = \frac{1}{1+A\beta}$$

$$\text{Desensitivity } D = \frac{1}{S} = 1+A\beta$$

The stability of the amplifier increases if the desensitivity is increased.

The gain of the amplifier is not constant as it depends on the factors such as temperature, aging of components, and temperature dependent parameters. This lack of stability can be reduced by introducing negative feedback.

The gain of amplifier with negative feedback is

$$A_f = \frac{A}{1+A\beta}$$

If $A\beta \gg 1$ then $A_f = \frac{1}{\beta}$ and gain is dependent only on feedback network. Hence maintaining $A\beta \gg 1$ and constructing feedback network only with stable passive elements a good stability is achieved.

Then for voltage series feedback $A_{Vf} = \frac{1}{\beta}$, voltage gain is stabilized

for current series feedback $G_{Mf} = \frac{1}{\beta}$, transconductance is stabilized

for current shunt feedback $A_{If} = \frac{1}{\beta}$, current gain is stabilized

for voltage shunt feedback $R_{Mf} = \frac{1}{\beta}$, transresistance is stabilized

Thus the input resistance is increased with series mixer using negative feedback irrespective of the type of sampling.

6) Decrease in output resistance:

An amplifier with low output resistance is capable of delivering maximum power to the load without much loss. For such a low output resistance negative feedback is very helpful. The output resistance can be decreased by using a voltage sampler irrespective of the type of mixer, by a factor $(1+AB)$.

$$\text{i.e. } R_{of} = \frac{R_o}{1+AB}$$

Effect of negative feedback on amplifier characteristics:

Characteristics	Type of feedback			
	Voltage series	Current series	Current shunt	Voltage shunt
Transfer gain	Decreases	Decreases	Decreases	Decreases
Bandwidth	Increases	Increases	Increases	Increases
Nonlinear Distortion	Decreases	Decreases	Decreases	Decreases
Noise	Decreases	Decreases	Decreases	Decreases
Input resistance	Increases	Increases	Decreases	Decreases
Output resistance	Decreases	Increases	Increases	Decreases

UNIT - II

SINUSOIDAL OSCILLATORS

INTRODUCTION:

- Any circuit which is used to generate a periodic voltage without an ac input signal is called an oscillator. To generate the AC voltage the circuit is supplied with energy from a dc source.
- If the output voltage is a sine wave function of time, the oscillator is called as a sinusoidal oscillator (or) Harmonic oscillator.
- There is an other category of oscillators which generate non-sinusoidal wave forms such as square, sawtooth, triangular or rectangular etc.

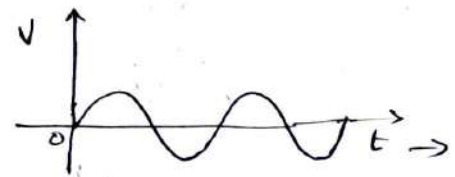
Classification of oscillators:

The oscillators can be classified in different ways.

1) According to the waveforms generated

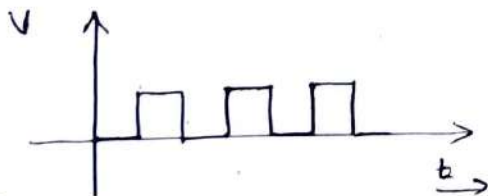
- a) Sinusoidal oscillators
- b) Relaxation oscillators.

- Sinusoidal oscillator generates voltage or current which is a sine wave function of time as shown in figure(a)

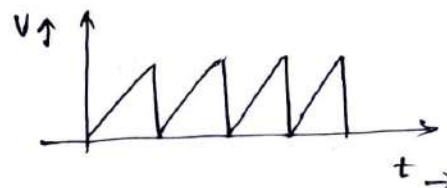


fig(a): Sinusoidal wave form

- A relaxation oscillator generates voltage or current which vary abruptly one or more times in a cycle of oscillation as shown in figure(b) and fig(c).



fig(b) Square waveform



fig(c): Sawtooth wave form.

2) According to the fundamental mechanisms involved

- a) Negative resistance oscillators
- b) Feedback oscillators

- In a negative resistance oscillator the negative resistance of the amplifying device is used to neutralize the positive resistance of the oscillator.

- Feedback oscillator is formed by using the positive feedback in a feedback amplifier such that it satisfies the Barkhausen criterion.

3) According to the frequency generated

- Audio Frequency oscillator : 20Hz to 20kHz
- Radio Frequency oscillator : 20kHz to 30MHz
- Very High Frequency oscillator : 30MHz to 300MHz
- Ultra high Frequency oscillator : 300MHz to 3GHz
- Microwave Frequency oscillator : 3GHz and above.

4) According to the type of the circuit used, sinusoidal oscillators are classified as

- LC Tuned oscillator
- RC Phase shift oscillator.

Concept of positive feedback :

If some portion of the output signal is fed back to the input of the amplifier in phase with the external signal from source, such feedback is known as Positive feedback.

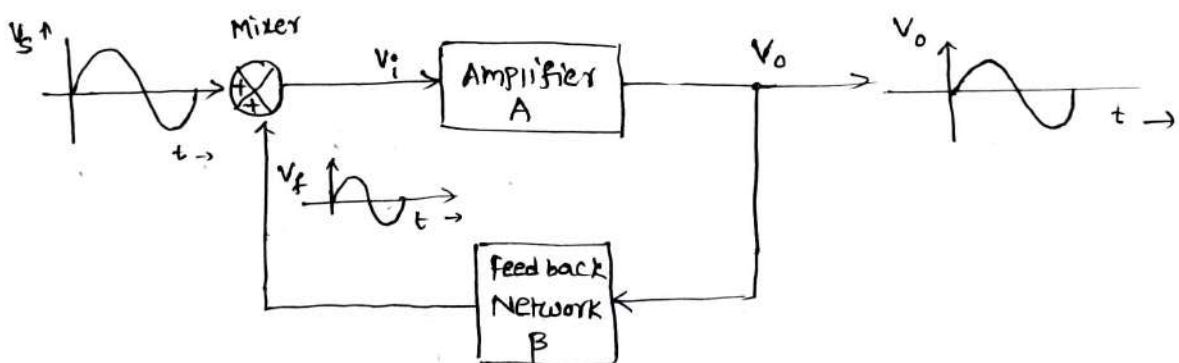


fig: Concept of Positive feedback

Assume that a sinusoidal input signal V_s is applied to the circuit. The output of the amplifier as V_o . Some portion of the output signal is taken from the output of feedback network as V_f which is in phase with V_s . Hence V_f is added with V_s to give the input to the amplifier as V_i i.e. $V_i = V_s + V_f$ $\longrightarrow$ ①

Let the gain of the amplifier without feedback as A

$$\text{Then } A = \frac{V_o}{V_i} \longrightarrow \textcircled{2}$$

the feedback factor of the feedback network ' β ' is given as

$$\beta = \frac{V_f}{V_o} \rightarrow (3)$$

The gain of the amplifier with feedback is A_f given as

$$A_f = \frac{V_o}{V_s} \rightarrow (4)$$

$$= \frac{V_o}{V_i - V_f} \quad \left(\because \text{from eq (1)} \right)$$

$$= \frac{1}{\left(\frac{V_i}{V_o} \right) - \left(\frac{V_f}{V_o} \right)}$$

$$= \frac{1}{\frac{1}{A} - \beta} \quad \left(\because \text{equation (2) and (3)} \right)$$

$$\therefore \boxed{A_f = \frac{A}{1 - A\beta}}$$

Conditions for oscillation (or) Barkhausen Criterion:

The oscillator circuit produces oscillations due to the random variation in the base current due to the noise component (or) a small variation in the DC supply. The noise components of extremely small electrical voltages are always present in the circuit environment, that causes small signal at the output of the amplifier, even in the absence of the external signal. Let the amplifier is tuned to a particular frequency ' f_o ', hence the output signal produced due to noise will also be of frequency ' f_o '. If a small fraction (β) of the output signal is fed back to the input, then this feedback signal will be amplified by the amplifier.

If the amplifier has a gain of more than $\frac{1}{\beta}$, then the output goes on increasing, but as the output increases, the gain of the amplifier decreases and at a particular value of output, the gain of the amplifier is reduced exactly equal to $\frac{1}{\beta}$. Then the output remains constant at frequency ' f_o '. This frequency f_o is called as frequency of oscillation.

The essential conditions for maintaining oscillations are

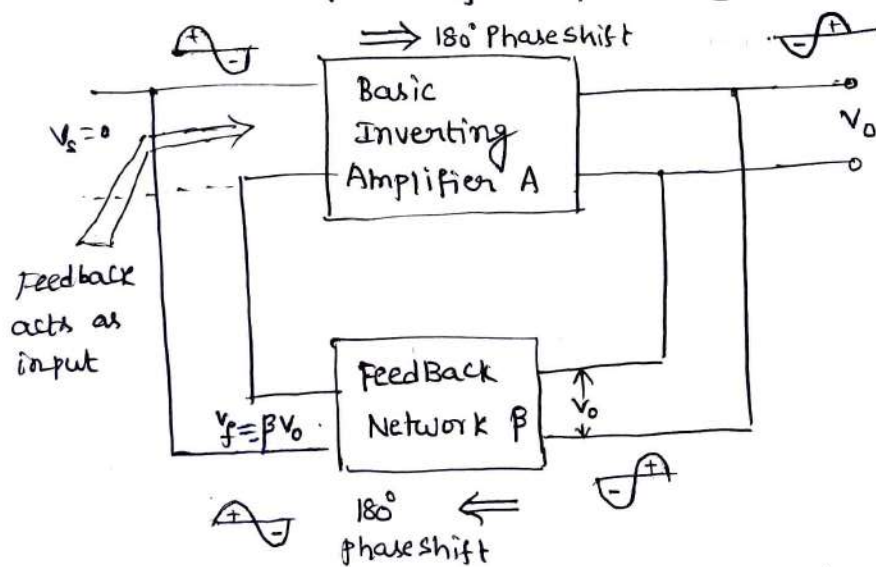
- 1) $|A\beta| = 1$ i.e the magnitude of loop gain must be unity.
- 2) The total Phase shift around the closed loop is zero or 360° .

Consider an inverting basic amplifier with open loop gain A , which produces 180° Phase shift between its input and output. And the feedback network has a feedback factor β . Assume $V_s = 0$.

An output is generated at the amplifier due to the variations in dc (or) due to noise from which a fraction of the output is fed back to the input of the amplifier through feedback network. This feed back signal acts as input V_i to the circuit now.

$$\text{open loop gain } A = \frac{V_o}{V_i} \rightarrow \textcircled{1}$$

$$\text{Feedback signal } V_f = -\beta V_o \rightarrow \textcircled{2} \quad \text{sign indicates } 180^\circ \text{ phase shift}$$



since V_f is going as V_i here $V_f = V_i$

$$\text{eq } \textcircled{1} \Rightarrow V_o = AV_i = AV_f$$

$$\therefore V_o = A \cdot V_f \rightarrow \textcircled{3}$$

substituting equation $\textcircled{3}$ in equation $\textcircled{2}$ we get

$$V_f = -\beta A V_f$$

$$\Rightarrow A\beta = -1$$

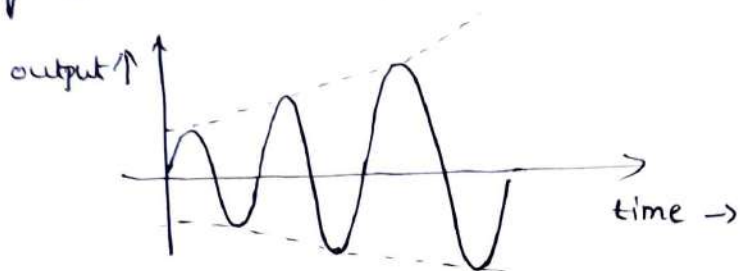
$$\Rightarrow A\beta = -1 + j0$$

$$\therefore |A\beta| = 1$$

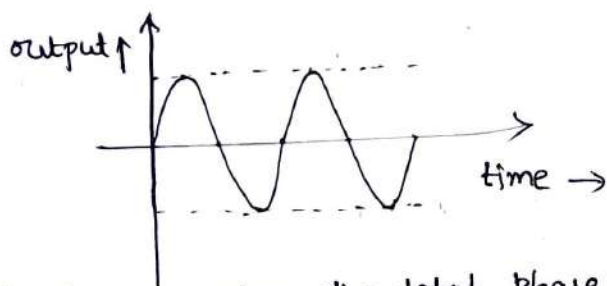
Here the basic inverting amplifier introduces 180° phase shift, in addition to which 180° phase shift should be provided by the feedback network to make the total phase shift around the closed loop as 360° .

Effect of magnitude of loop gain $|A\beta|$ on nature of oscillations:

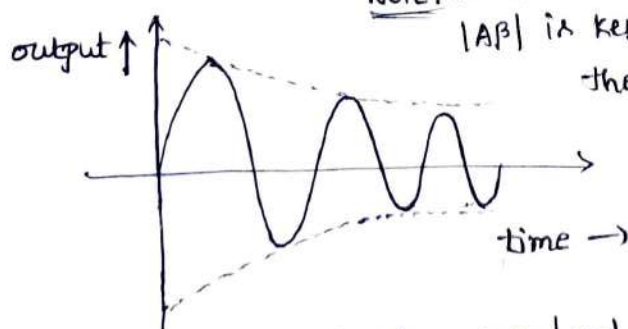
i) when $|A\beta| > 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| > 1$ then the output contains the oscillations of growing type. i.e. the amplitude of oscillations goes on increasing.



ii) when $|A\beta| = 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| = 1$ then the output contains the oscillations with constant frequency and amplitude, these oscillations are called as sustained oscillations. (or) undamped oscillations.



iii) when $|A\beta| < 1$: when the total phase shift around the closed loop is 0° or 360° and $|A\beta| < 1$ then the oscillations are of decaying type i.e. the amplitude decreases exponentially.



NOTE: To start oscillations without input $|A\beta|$ is kept higher than unity and then the circuit adjusts itself to get $|A\beta| = 1$ to result sustained oscillations.

NOTE: The oscillations under $|A\beta| < 1$ (or) $|A\beta| > 1$ are called as under damped (or) over damped oscillations resp.

LC oscillators :

General form of an LC oscillator :

The general form of an LC oscillator requires any one of the active devices such as Transistor, FET, Vacuum tube, and op-amp may be used in the amplifier section.

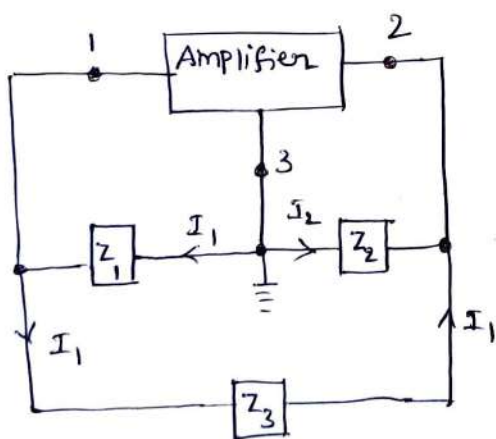
Z_1 , Z_2 , and Z_3 are the reactive elements constituting the feedback tank circuit which determines the frequency of oscillation. Here Z_1 and Z_2 serve as an ac voltage divider for the output voltage and the feedback signal.

The voltage across Z_1 is the feedback signal.

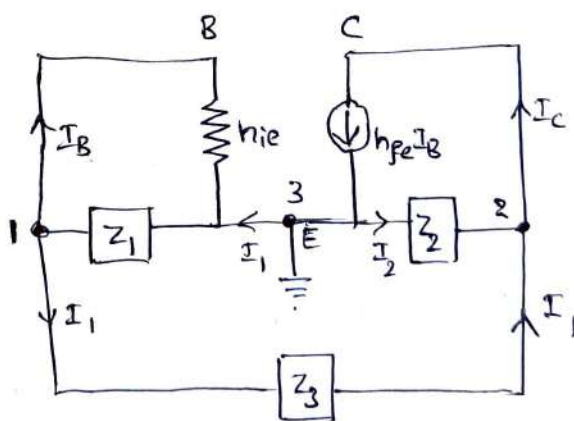
The frequency of oscillation of an LC oscillator is

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The general form of an LC oscillator and its equivalent circuit are as shown in below, in which the output terminals are 2 and 3, and input terminals are 1 and 3.



fig(a) General form of an LC oscillator



fig(b) : Equivalent Circuit of an LC oscillator.

Load impedance : (Z_L)

Since Z_1 is in parallel with the resistance h_{ie} , their equivalent resistance Z' is given by

$$\frac{1}{Z'} = \frac{1}{Z_1} + \frac{1}{h_{ie}}$$

$$\therefore Z' = \frac{Z_1 h_{ie}}{Z_1 + h_{ie}}$$

—————→ ①

Now the load impedance Z_L is the impedance between the terminals 2 and 3 (i.e. output terminals) which is equal to Z_2 in parallel with $Z'_1 + Z_3$.

$$\text{i.e. } \frac{1}{Z_L} = \frac{1}{Z_2} + \frac{1}{Z'_1 + Z_3}$$

$$\Rightarrow \frac{1}{Z_L} = \frac{1}{Z_2} + \frac{1}{\frac{Z_1 h_{ie} + Z_3}{Z_1 + h_{ie}}}$$

$$= \frac{1}{Z_2} + \frac{Z_1 + h_{ie}}{Z_1 h_{ie} + Z_1 Z_3 + Z_3 h_{ie}}$$

$$= \frac{1}{Z_2} + \frac{Z_1 + h_{ie}}{(Z_1 + Z_3) h_{ie} + Z_1 Z_3}$$

$$= \frac{h_{ie}(Z_1 + Z_3) + Z_1 Z_3 + Z_2 h_{ie} + Z_1 Z_2}{Z_2 [h_{ie}(Z_1 + Z_3) + Z_1 Z_3]}$$

$$= \frac{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3}{Z_2 [h_{ie}(Z_1 + Z_3) + Z_1 Z_3]}$$

$$\therefore Z_L = \frac{Z_2 [h_{ie}(Z_1 + Z_3) + Z_1 Z_3]}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} \rightarrow (2)$$

Voltage Gain without feedback (A_V)

$$\text{Voltage Gain } (A_V) = \frac{A_I Z_L}{Z_i} = \frac{-h_{fe} Z_L}{h_{ie}} \rightarrow (3)$$

Feedback factor (β) :

The output voltage between the terminals 3 and 2 in terms of current I_1 is given by $V_o = -I_1 (Z'_1 + Z_3) = -I_1 \left(\frac{Z_1 h_{ie} + Z_3}{Z_1 + h_{ie}} \right)$

$$V_o = -I_1 \left(\frac{h_{ie}(Z_1 + Z_3) + Z_1 Z_3}{Z_1 + h_{ie}} \right) \rightarrow (4)$$

the voltage fed back to the terminals 3 and 1 is given by

$$V_f = -I_1 Z' = -I_1 \left(\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} \right) \rightarrow (5)$$

The feed back ratio $\beta = \frac{V_f}{V_o} = -I_1 \left(\frac{Z_1 h_{ie}}{Z_1 + h_{ie}} \right) \left(\because \text{from eq (4), (5)} \right)$

$$\Rightarrow \beta = \frac{Z_1 h_{ie}}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \rightarrow (6)$$

The equation for the oscillator

For producing oscillations $A_v \beta = 1$ is the condition

substituting eq (3) and eq (6) in this equation we get

$$\frac{-h_{fe} Z_L}{h_{ie}} \left[\frac{Z_1 h_{ie}}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \right] = 1$$

$$\Rightarrow \frac{h_{fe} Z_L Z_1}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} = -1, \text{ substituting } Z_L \text{ from equation (2)}$$

$$\Rightarrow \frac{h_{fe} Z_1}{h_{ie}(Z_1 + Z_3) + Z_1 Z_3} \left[\frac{Z_2 [h_{ie}(Z_1 + Z_3) + Z_1 Z_3]}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} \right] = -1$$

$$\Rightarrow \frac{h_{fe} Z_1 Z_2}{h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3} = -1$$

$$\Rightarrow h_{fe} Z_1 Z_2 = - [h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 + Z_1 Z_3]$$

$$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1 + h_{fe}) + Z_1 Z_3 = 0$$

This is the general equation for the oscillator.

Hartley Oscillator:

In the Hartley oscillator Z_1 and Z_2 are inductors and Z_3 is a capacitor. The Hartley oscillator circuit is as shown in below.

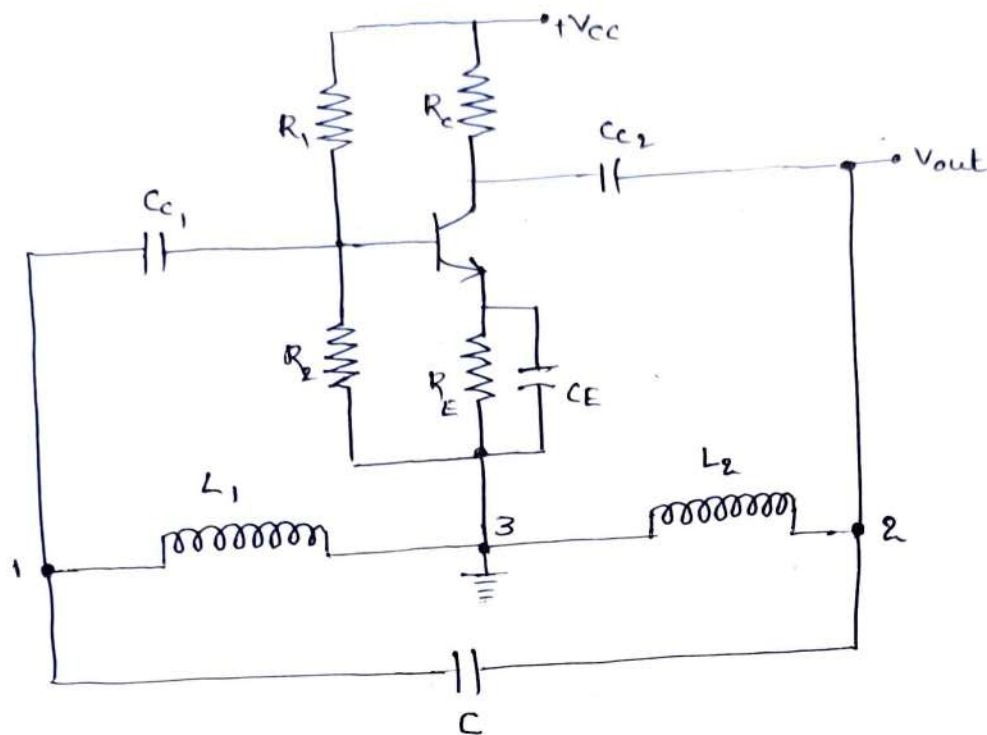


fig: Hartley oscillator

Here the resistors R_1 , R_2 and R_E provides the required bias to the transistor. C_E is a bypass capacitor, C_{C1} and C_{C2} are the coupling capacitors. The feedback network consists of the inductors L_1 and L_2 and capacitor C determines the frequency of oscillation.

When the supply voltage $+V_{CC}$ is turned ON, a transient current is produced in the tank circuit. The current in the tank circuit develops AC voltages across L_1 and L_2 . As the terminal 3 is grounded, it is at zero potential. If terminal 1 is at a positive potential with respect to terminal 3 at any instant, the terminal 2 will be at negative potential with respect to terminal 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180° . In the CE mode, the transistor produces 180° phase difference between input and output. Therefore the total phase shift is 360° . Thus at the frequency determined for the tank circuit, the necessary condition for sustained oscillations is satisfied.

If the feedback is adjusted such that the loop gain $A\beta = 1$, the circuit acts as an oscillator.

The frequency of oscillation is $f_o = \frac{1}{2\pi\sqrt{LC}}$

where $L = L_1 + L_2 + 2M$ and M is the mutual inductance value between L_1 and L_2 coils.

The condition for sustained oscillation is

$$h_{fe} \geq \frac{L_1 + M}{L_2 + M}$$

Analysis: In the Hartley oscillator, Z_1 and Z_2 are inductive reactances and Z_3 is the capacitive reactance. Suppose 'M' is the mutual inductance between the inductors, then

$$Z_1 = j\omega L_1 + j\omega M$$

$$Z_2 = j\omega L_2 + j\omega M$$

$$Z_3 = \frac{1}{j\omega C} = -\frac{j}{\omega C}$$

We know the general equation for the oscillator is

$$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2 (1 + h_{fe}) + Z_1 Z_3 = 0$$

Substituting Z_1, Z_2 and Z_3 in this equation from above equations,

$$h_{ie} \left(j\omega L_1 + j\omega M + j\omega L_2 + j\omega M - \frac{j}{\omega C} \right) + (j\omega L_1 + j\omega M)(j\omega L_2 + j\omega M)(1 + h_{fe}) + (j\omega L_1 + j\omega M) \left(-\frac{j}{\omega C} \right) = 0$$

$$j\omega h_{ie} \left(L_1 + L_2 + 2M - \frac{1}{\omega^2 C} \right) - \omega^2 (L_1 + M)(L_2 + M)(1 + h_{fe}) + (L_1 + M) \frac{1}{C} = 0$$

$$j\omega h_{ie} \left(L_1 + L_2 + 2M - \frac{1}{\omega^2 C} \right) - \omega^2 (L_1 + M) \left[(L_2 + M)(1 + h_{fe}) - \frac{1}{\omega^2 C} \right] = 0$$

The frequency of oscillation $f_o = \frac{\omega_o}{2\pi}$ is determined by $\hookrightarrow \textcircled{1}$

equating the imaginary part of the above equation to zero by

$$\text{substituting } \omega = \omega_o \text{ i.e. } \omega_o h_{ie} \left(L_1 + L_2 + 2M - \frac{1}{\omega_o^2 C} \right) = 0$$

$$\Rightarrow \frac{1}{\omega_0^2 C} = L_1 + L_2 + 2M$$

$$\Rightarrow \omega_0^2 = \frac{1}{(L_1 + L_2 + 2M)C}$$

$$\therefore \omega_0 = \frac{1}{\sqrt{(L_1 + L_2 + 2M)C}} \rightarrow (2)$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi \sqrt{(L_1 + L_2 + 2M)C}} \rightarrow (3)$$

The Condition for maintenance of oscillation is obtained by substituting eq (2) in eq (1) which makes the imaginary part to zero. Hence

$$(L_2 + M)(1 + h_{fe}) - \frac{1}{\omega_0^2 C} = 0$$

$$\Rightarrow (L_2 + M)(1 + h_{fe}) - \frac{1}{C} (L_1 + L_2 + 2M)C = 0$$

$$\Rightarrow (L_2 + M)(1 + h_{fe}) = L_1 + L_2 + 2M$$

$$L_2 + M + (L_2 + M)(h_{fe}) = L_1 + L_2 + 2M$$

$$(L_2 + M)h_{fe} = L_1 + M \Rightarrow h_{fe} = \frac{L_1 + M}{L_2 + M}$$

$\therefore$ The condition for maintenance of oscillations is $\boxed{h_{fe} = \frac{L_1 + M}{L_2 + M}}$

COLPITTS OSCILLATOR:

In the Colpitts oscillator Z_1 and Z_2 are capacitors and Z_3 is an inductor. The Colpitts oscillator circuit is as shown in below fig'.

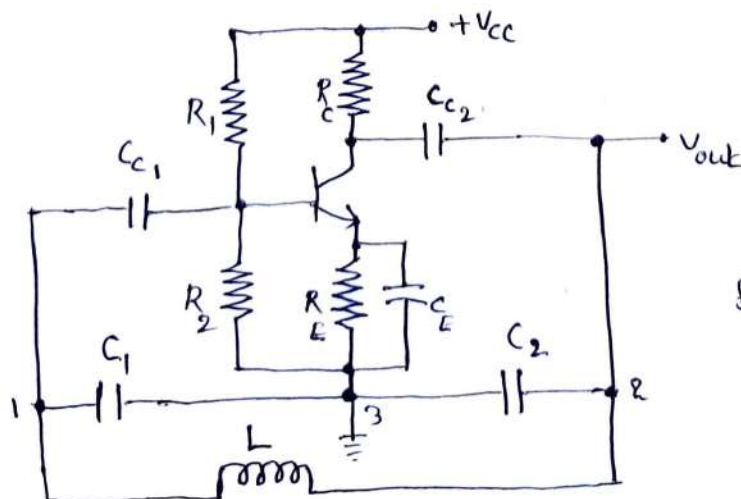


Fig: COLPITTS OSCILLATOR

The resistors R_1, R_2 and R_E provide the necessary DC biasing to the transistor. C_E is the bypass capacitor, C_1 and C_2 are the coupling capacitors. The feedback network consists of C_1 and C_2 and an inductor L determines the frequency of oscillation. Here C_1 and C_2 are capacitors.

When the power supply voltage V_{CC} is switched ON, a transient current is produced in the tank circuit and consequently damped harmonic oscillations are setup in the circuit. The current in the tank circuit produces (or) develops AC voltages across C_1 and C_2 . As terminal 3 is grounded, it will be at zero potential. Now if terminal 1 is at positive potential with respect to 3 at any instant, the terminal 2 will be at negative potential with respect to 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180° . In the common emitter configuration, the transistor provides a phase difference of 180° between the input and output. Therefore the total phase difference is 360° . Thus, at the frequency determined for the tank circuit, the necessary condition for sustained oscillations is satisfied. If the feedback is adjusted such that the loop gain $A\beta = 1$, the circuit acts as oscillator. The frequency of oscillation is

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

$$\text{where } \frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \Rightarrow C = \frac{C_1 C_2}{C_1 + C_2}$$

It is widely used in commercial signal generators for frequencies between 1 MHz to 500 MHz. It is also used as a local oscillator in super heterodyne radio receiver.

Analysis:

For Colpitts oscillator $Z_1 = \frac{1}{j\omega C_1}$, $Z_2 = \frac{1}{j\omega C_2}$, $Z_3 = j\omega L$

i.e $Z_1 = \frac{-j}{\omega C_1}$, $Z_2 = \frac{-j}{\omega C_2}$ and $Z_3 = j\omega L$

we know the general equation of an LC oscillator is

$$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2(1 + h_{fe}) + Z_1 Z_3 = 0$$

substituting $Z_3 = +j\omega L$, $Z_1 = -\frac{j}{\omega C_1}$, $Z_2 = -\frac{j}{\omega C_2}$ in the above eq

$$h_{ie}\left(-\frac{j}{\omega C_1} - \frac{j}{\omega C_2} + j\omega L\right) + \left(-\frac{j}{\omega C_1} \cdot -\frac{j}{\omega C_2}\right)(1 + h_{fe}) + \left(-\frac{j}{\omega C_1}\right)(j\omega L) = 0$$

$$-jh_{ie}\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} - \omega L\right) - \frac{(1 + h_{fe})}{\omega^2 C_1 C_2} + \frac{L}{C_1} = 0$$

$$\Rightarrow \left[\frac{1 + h_{fe}}{\omega^2 C_1 C_2} - \frac{L}{C_1}\right] + jh_{ie}\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} - \omega L\right) = 0 \rightarrow (1)$$

The frequency of oscillation $f_0 = \frac{\omega_0}{2\pi}$ is determined by equating

the imaginary part to zero, by substituting $\omega = \omega_0$.

$$\text{i.e. } h_{ie}\left(\frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2} - \omega_0 L\right) = 0$$

$$\Rightarrow \omega_0 L = \frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2}$$

$$\omega_0^2 = \frac{1}{L} \left(\frac{1}{C_1} + \frac{1}{C_2}\right)$$

$$\omega_0 = \sqrt{\frac{C_1 + C_2}{LC_1 C_2}} \rightarrow (2)$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi} \sqrt{\frac{C_1 + C_2}{LC_1 C_2}} \rightarrow (3)$$

The condition for maintenance of oscillation is obtained by substituting equation (3) in equation (1) which makes the imaginary part to zero.

$$\text{Hence } \frac{1 + h_{fe}}{\omega_0^2 C_1 C_2} - \frac{L}{C_1} = 0$$

$$\Rightarrow \frac{1 + h_{fe}}{\omega_0^2 C_1 C_2} = \frac{L}{C_1}$$

$$\Rightarrow \frac{1 + h_{fe}}{\left(\frac{C_1 + C_2}{LC_1 C_2}\right) \cdot C_1 C_2} = \frac{L}{C_1} \quad \left(\because \text{from eq (2)} \right)$$

$$\omega_0^2 = \frac{C_1 + C_2}{LC_1 C_2}$$

$$\Rightarrow 1+h_{fe} = \left(\frac{L}{C_1}\right)\left(\frac{C_1+C_2}{L}\right)$$

$$\Rightarrow 1+h_{fe} = \frac{C_1+C_2}{C_1}$$

$$\Rightarrow 1+h_{fe} = 1 + \frac{C_2}{C_1}$$

$$\therefore \boxed{h_{fe} = \frac{C_2}{C_1}}$$

Problems: In the Hartley oscillator $L_2 = 0.4 \text{ mH}$ and $C = 0.004 \text{ }\mu\text{F}$. If the frequency of oscillator is 120 kHz , find the value of L_1 . Neglect the mutual inductance.

sol) Given $L_2 = 0.4 \text{ mH} = 0.4 \times 10^{-3} \text{ H}$, $C = 0.004 \text{ }\mu\text{F} = 4 \times 10^{-9} \text{ F}$

$$f_0 = 120 \text{ kHz}, L_1 = ?$$

We know that the frequency of Hartley oscillator is given by

$$f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}$$

Neglecting mutual inductance

$$f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

$$\Rightarrow f_0^2 = \frac{1}{4\pi^2(L_1+L_2)C}$$

$$\Rightarrow (L_1+L_2)C = \frac{1}{4\pi^2 f_0^2}$$

$$\Rightarrow L_1 C + L_2 C = \frac{1}{4\pi^2 f_0^2}$$

$$\Rightarrow L_1 C = \frac{1}{4\pi^2 f_0^2} - L_2 C$$

$$\Rightarrow L_1 = \frac{1}{4\pi^2 f_0^2 C} - L_2$$

$$\Rightarrow L_1 = \frac{1}{4\pi^2 (120 \times 10^3)^2 (4 \times 10^{-9})} - (0.4 \times 10^{-3})$$

$$\Rightarrow L_1 = 0.03976 \text{ mH}$$

② A Hartley oscillator has two inductances as 2mH and $20\mu\text{H}$ while the frequency is to be changed from 950kHz to 2050kHz . Calculate the range over which the capacitor is to be varied.

sol) Given Hartley oscillator has $L_1 = 2\text{mH} = 2 \times 10^{-3}\text{H}$

$$L_2 = 20\mu\text{H} = 20 \times 10^{-6}\text{H}, \quad f_1 = 950\text{kHz} = 950 \times 10^3\text{Hz}$$

$$f_2 = 2050\text{kHz} = 2050 \times 10^3\text{Hz}.$$

We know that the frequency of oscillation for Hartley oscillator is $f_0 = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$

$$\Rightarrow C = \frac{1}{4\pi^2 f_0^2 (L_1+L_2)}$$

$$\text{When } f_0 = 950\text{kHz}, \quad C = \frac{1}{4\pi^2 (950 \times 10^3)^2 (2 \times 10^{-3} + 20 \times 10^{-6})}$$

$$= 13.89\text{PF}$$

$$\text{When } f_0 = 2050\text{kHz}, \quad C = \frac{1}{4\pi^2 (2050 \times 10^3)^2 (2 \times 10^{-3} + 20 \times 10^{-6})}$$

$$C = 2.98\text{PF}$$

Therefore the range of capacitance is from 2.98PF to 13.89PF .

3) A Colpitts oscillator has $C_1 = 0.2\text{PF}$, $C_2 = 0.02\text{PF}$. If the frequency of oscillation is 10kHz , find the value of the inductor L !

sol) Given $C_1 = 0.2\text{PF}$, $C_2 = 0.02\text{PF}$

$$f_0 = 10\text{kHz}$$

$$L = ?$$

We know that the frequency of oscillation for a Colpitts oscillator

$$\text{is given by } f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}} \Rightarrow f_0^2 = \frac{1}{4\pi^2\left(L\frac{C_1 C_2}{C_1 + C_2}\right)}$$

$$\Rightarrow L = \frac{C_1 + C_2}{4\pi^2 f_0^2 C_1 C_2}$$

$$= \frac{(0.2 \times 10^{-12}) + (0.02 \times 10^{-12})}{4\pi^2 \times (10 \times 10^3)^2 \times 0.2 \times 10^{-12} \times 0.02 \times 10^{-12}}$$

$$L = 13931 \text{ H}$$

4) In a Colpitts oscillator the values of the inductors and capacitors are $L = 40 \text{ mH}$, $C_1 = 100 \text{ pF}$, $C_2 = 500 \text{ pF}$ i) find the frequency of oscillations ii) Find the value of h_{fe} for maintaining sustained oscillations

sol)

$$\text{Given } L = 40 \text{ mH}$$

$$C_1 = 100 \text{ pF}$$

$$C_2 = 500 \text{ pF}$$

For a Colpitts oscillator the frequency of oscillations is

$$f_0 = \frac{1}{2\pi \sqrt{L \left(\frac{C_1 C_2}{C_1 + C_2} \right)}}$$

$$= \frac{1}{2\pi \sqrt{40 \times 10^{-3} \times \frac{100 \times 10^{-12} \times 500 \times 10^{-12}}{(100 + 500) \times 10^{-12}}}}$$

$$\therefore f_0 = 87.172 \text{ kHz}$$

ii) The value of h_{fe} for maintaining sustained oscillations in a Colpitts oscillator is given by $h_{fe} = \frac{C_2}{C_1}$

$$h_{fe} = \frac{500 \times 10^{-12}}{100 \times 10^{-12}}$$

$$\therefore h_{fe} = 5$$

CLAPP OSCILLATOR:

To achieve the frequency stability, Colpitts oscillator is slightly modified in practice. This modified Colpitts oscillator is called Clapp oscillator. In Clapp oscillator Z_1 and Z_2 are capacitors and Z_3 is the series combination of an inductor L and a capacitor C_3 as shown in figure below.

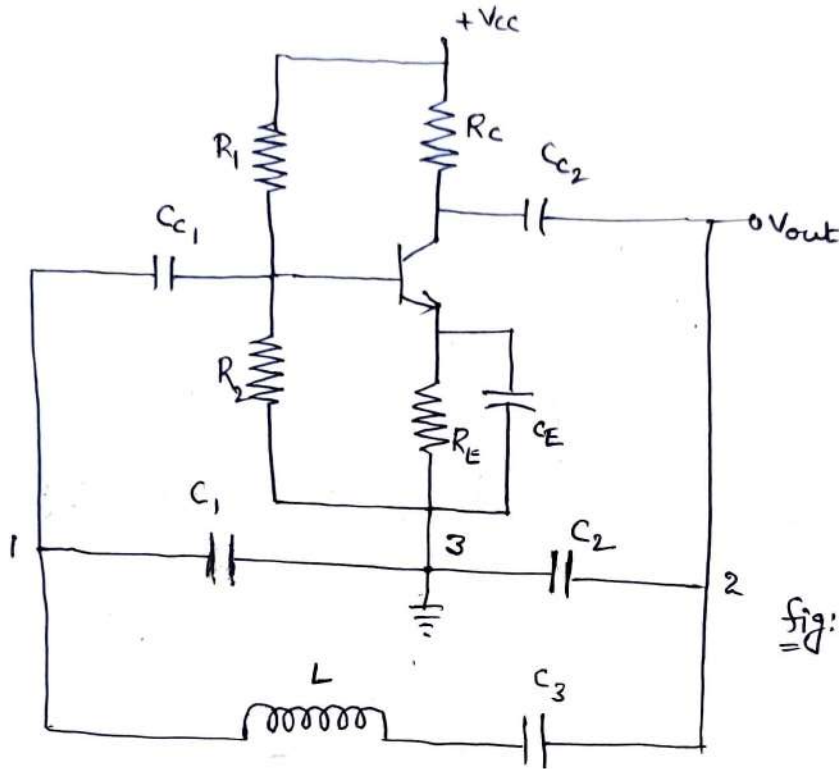


fig: clapp oscillator

The frequency of oscillation for a clapp oscillator is given as

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

where $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$. The value of C_3 is very much

smaller than the value of C_1 and C_2 . So neglecting $\frac{1}{C_1}$ and $\frac{1}{C_2}$ we get

$$\frac{1}{C_{eq}} \approx \frac{1}{C_3}$$

$$\text{i.e. } C_{eq} = C_3$$

$$\therefore f_0 = \frac{1}{2\pi\sqrt{LC_3}}$$

The Analysis of a clapp oscillator is as shown in below.

Analysis:

In a Clapp oscillator Z_1 and Z_2 are the capacitive reactances, Z_3 is a series combination of an inductive reactance and a capacitive reactance.

$$\text{ie } Z_1 = \frac{1}{j\omega C_1} = -\frac{j}{\omega C_1}$$

$$Z_2 = \frac{1}{j\omega C_2} = -\frac{j}{\omega C_2}$$

$$Z_3 = j\omega L + \frac{1}{j\omega C_3} = j\omega L - \frac{j}{\omega C_3}$$

we know the general equation for an LC oscillator is

$$h_{ie}(Z_1 + Z_2 + Z_3) + (1 + h_{fe})Z_1 Z_2 + Z_1 Z_3 = 0$$

substituting Z_1, Z_2, Z_3 in the above equation

$$h_{ie} \left(-\frac{j}{\omega C_1} + -\frac{j}{\omega C_2} + j\omega L - \frac{j}{\omega C_3} \right) + (1 + h_{fe}) \left(-\frac{j}{\omega C_1} \right) \left(-\frac{j}{\omega C_2} \right) + \left(-\frac{j}{\omega C_1} \right) \cdot \left(j\omega L - \frac{j}{\omega C_3} \right) = 0$$

$$\Rightarrow -j h_{ie} \left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} + \frac{1}{\omega C_3} - \omega L \right) - \frac{(1 + h_{fe})}{\omega^2 C_1 C_2} + \frac{1}{\omega C_1} \left(\omega L - \frac{1}{\omega C_3} \right) = 0$$

$$\Rightarrow -j h_{ie} \left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2} + \frac{1}{\omega C_3} - \omega L \right) - \frac{1}{\omega C_1} \left[\frac{(1 + h_{fe})}{\omega C_2} - \omega L + \frac{1}{\omega C_3} \right] = 0$$

The frequency of oscillation $f_0 = \frac{\omega_0}{2\pi}$ can be determined by

equating the imaginary part to zero.

$$-h_{ie} \left(\frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2} + \frac{1}{\omega_0 C_3} - \omega_0 L \right) = 0$$

$$\Rightarrow \frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2} + \frac{1}{\omega_0 C_3} - \omega_0 L = 0$$

$$\Rightarrow \frac{1}{\omega_0} \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \right) = \omega_0 L$$

$$\Rightarrow \omega_0^2 = \frac{1}{LC_{eq}} \quad \text{where} \quad \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} = \frac{1}{C_{eq}}$$

$$\Rightarrow \omega_0 = \frac{1}{\sqrt{LC_{eq}}}$$

$$\Rightarrow f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

where $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$

As C_3 is very much smaller than C_1 and C_2 . we can neglect $\frac{1}{C_1}$ and $\frac{1}{C_2}$.

$$\therefore \frac{1}{C_{eq}} \approx \frac{1}{C_3}$$

$$\Rightarrow C_{eq} = C_3$$

$\therefore$ the frequency of oscillation for Clapp oscillator is

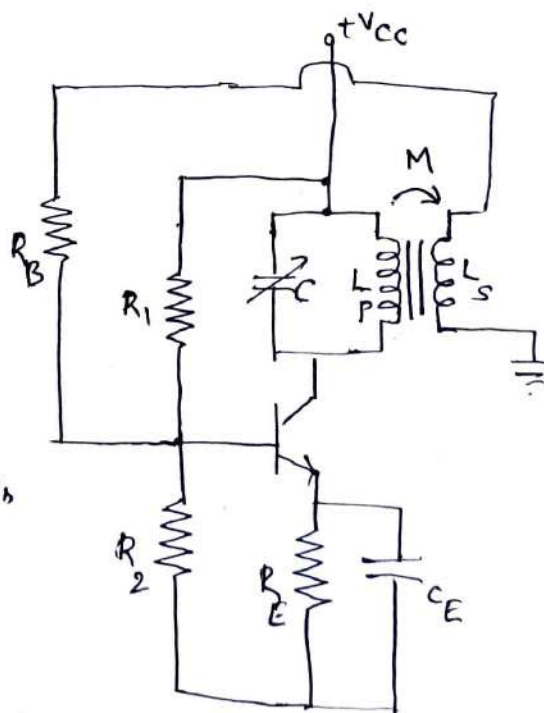
$$f_0 = \frac{1}{2\pi\sqrt{LC_3}}$$

Advantages:

- 1) The frequency is stable and accurate
- 2) The stray capacitances have no effect as C_3 decides the frequency.
- 3) keeping C_3 variable, the frequency can be varied in the desired range.

Tuned Collector oscillator:

A tuned Collector oscillator circuit is as shown in figure. There is a tuned LC circuit in the collector branch, which is connected to power supply $+V_{CC}$. Resistors R_1 , R_2 and R_E are used to establish the proper biasing conditions as in a common emitter amplifier.



The capacitor C_E is a bypass emitter capacitor. The resistor R_B is used to control the amount of feedback to the value just needed for sustained oscillation.

When the power supply is switched on, the capacitor C starts charging. When it is fully charged, it starts to discharge through L_p . The energy stored in capacitor ' C ' is in the form of electrostatic energy which gets converted to electro magnetic energy and gets stored in L_p . Once the capacitor discharges completely, L_p starts charging capacitor again. So the capacitor starts charging again and this cycle continues.

The coil L_s gets charged through the electro magnetic induction and feeds this to the transistor. The transistor amplifies the signal and is taken as the output at collector. A part of the output is fed back to the base through the LC circuit present at collector with positive feedback.

Here, the common emitter amplifier introduces 180° phase shift and the transformer introduces an additional 180° phase shift hence a total 360° phase shift is obtained which satisfies the desired condition for sustained oscillations.

The frequency of oscillation $f_0 = \frac{1}{2\pi\sqrt{L_p C}}$

Drawbacks of LC oscillators:

- 1) Frequency instability
- 2) Waveform is poor
- 3) It cannot be used for deriving low frequencies.
- 4) Inductors are bulky and expensive.

Frequency stability of oscillator:

→ The frequency of oscillations should remain constant. But practically the frequency of oscillations will get changed due to various reasons.

→ The analysis of the dependence of the oscillating frequency on various factors like temperature, internal capacitance etc is called as "frequency stability analysis."

→ The measure of ability of an oscillator to maintain the desired frequency as precisely as possible for as long time as possible is called as the "frequency stability".

→ The transistor parameters are temperature sensitive. Hence as temperature changes, the oscillating frequency also changes and no longer remains stable. So the circuit cannot provide stable frequency.

Factors that affect the frequency stability:

- 1) The operating point of the active devices such as BJT and FET must be in the active region. Due to the change in temperature the parameters of the active devices like BJT, FET may get changed that may lead to the change in frequency of oscillation.
- 2) The circuit components that are temperature dependent may affect the frequency of oscillation.
- 3) The changes in the DC supply voltage applied in the circuit may shift the oscillator's frequency of oscillation.
- 4) The changes in the atmospheric conditions and aging of the components may affect the frequency of oscillation.
- 5) The internal capacitances of the transistor may affect the oscillator's frequency of oscillation.
- 6) The changes in the output load/output resistance that may cause a change in the Q -factor of the tank circuit, thereby causing a change in the frequency oscillation.

The variation of frequency with respect to temperature variation is given by $S_{\omega, T} = \frac{\Delta\omega/\omega_0}{\Delta T/T_0}$ (ppmC Parts per million - per °C)

where ω_0 = The desired frequency of oscillation

T_0 = operating temperature

The frequency stability is defined as $S_{\omega} = \frac{d\theta}{d\omega}$

where θ is the phase shift which introduced due to the variation in the desired frequency (f_0).

The circuit should have $\frac{d\theta}{d\omega}$ as large as possible to have more frequency stability.

Amplitude Stability:

The ability of an oscillator to maintain a constant amplitude in the output waveform for as long time as possible is called as the amplitude stability of the oscillator.

The amplitude against the variations due to aging of the components can be stabilized by replacing the resistors in bridge by thermistors which are temperature dependent resistors.

All the oscillators do not require positive feedback for their operation. If the positive resistance of the LC tank circuit is cancelled by introducing the right amount of -ve resistance across the tank circuit.

There are several devices that exhibit negative resistance such as dynatron, transitron, thermistor, UJT and tunnel diode, with in a particular region in their V-I characteristics. Such devices are operated under that negative resistance region and they are placed in the tank circuit to cancel the positive resistance of the tank circuit.

The negative resistance should be numerically less than the dynamic resistance of the tuned circuit.

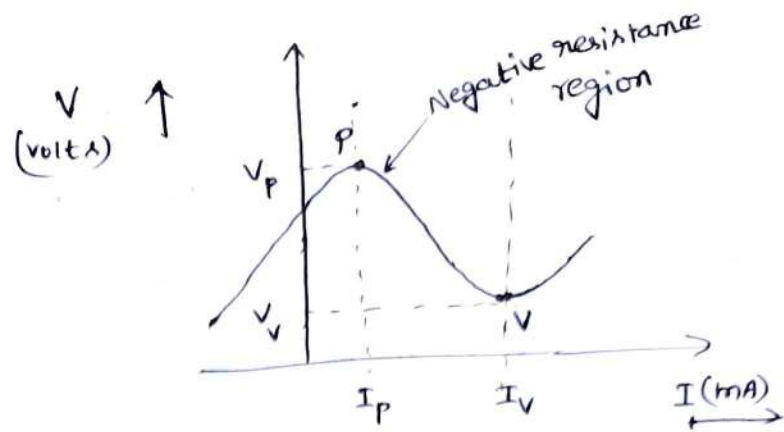
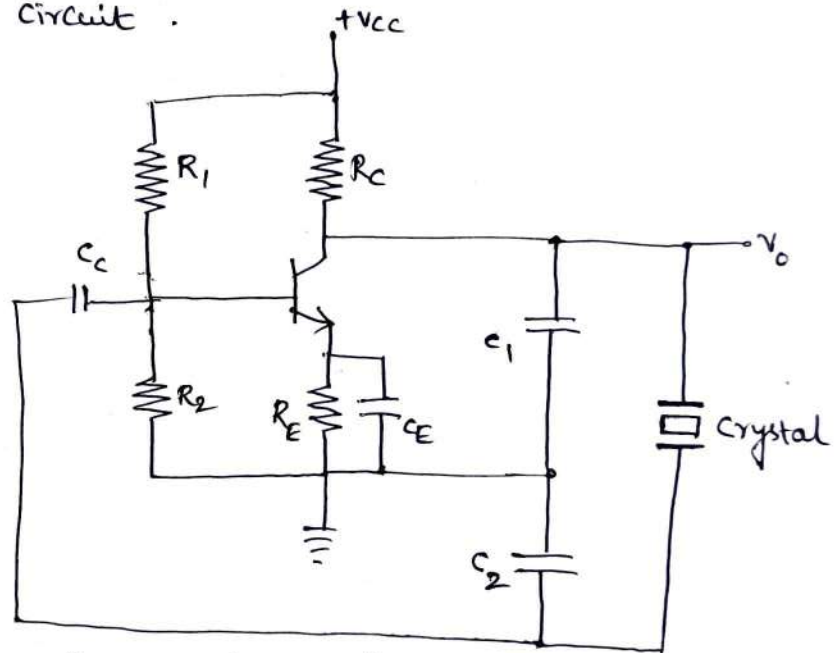


fig: V-I characteristics of negative resistance device.

Crystal oscillators:

The following figure shows a crystal controlled oscillator. Here a Colpitts oscillator is taken in which the inductor is replaced by a crystal. The crystal should be a piezo electric crystal usually quartz is used as a resonant circuit.



Principle of operation:

Figure: Crystal Controlled oscillator.

A crystal is a thin slice of piezo electric material such as quartz, tourmaline and Rochelle salt which exhibit a property called piezo-electric effect.

Piezo electric effect means under the influence of the mechanical pressure on one face of the crystal, an ac voltage is developed across the opposite faces of the crystal. Conversely if the a.c. voltage is applied across two opposite faces, it causes a mechanical vibration in the crystal.

Quartz Crystal Construction:

Generally the crystal is a ground wafer of quartz or tourmaline stone placed between two metal plates. The crystal is placed after cutting crude crystal wafer into slices.

There are two methods of cutting the crystal. Based on the method of cutting the resonant frequency of the crystal and its temperature coefficient is decided.

When the crystal wafer is cut in such a way that its flat surfaces are perpendicular to its electrical axis (X-axis), it is called as an X-cut crystal.

When the crystal wafer is cut in such a way that its flat surfaces are perpendicular to its mechanical axis (Y-axis), it is called as a Y-cut crystal.

If an AC voltage is applied, the crystal is set into vibration. The frequency of vibration is equal to the resonant frequency of the crystal. Usually the resonant frequency of the crystal is determined by the structural characteristics of the crystal. If the frequency of the applied AC voltage is equal to the natural resonant frequency of the crystal the vibration will be obtained with maximum amplitude.

In general the frequency of the vibration is given by

$$f = \frac{p}{2l} \sqrt{\frac{Y}{\rho}}$$

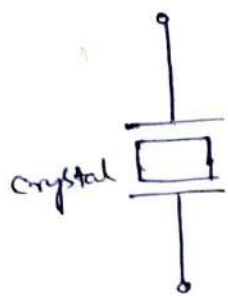
where $p = 1, 2, 3, \dots$, Y is the young modulus,

ρ = density of the material

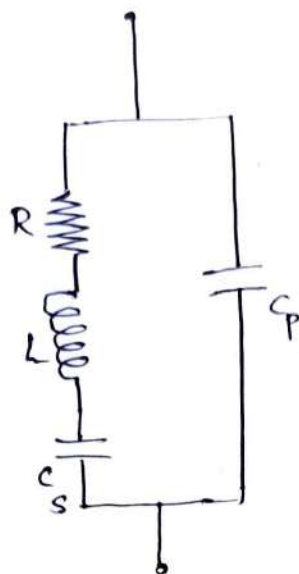
l = length of the material.

The crystal is suitably cut to get the vibrations with the required frequency and is mounted between two metal plates as shown in figure (a). The equivalent circuit of the crystal is

as shown in figure(b).



fig(a) Symbol of a Piezo electric crystal



fig(b) Equivalent circuit of a crystal

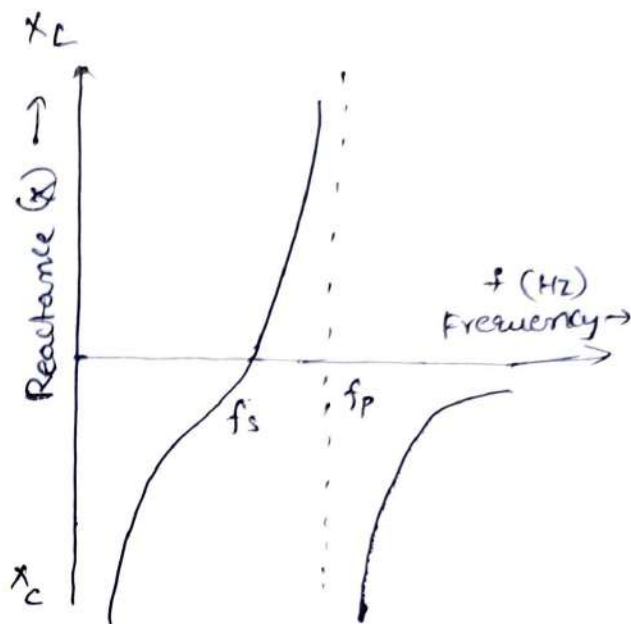


fig: reactance function with respect to frequency when $R=0$.

The reactance of the crystal is given by the formula

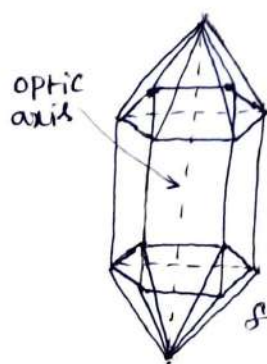
$$jX = \frac{1}{j\omega C_p} \left(\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2} \right) \text{ (neglecting } R \text{)}.$$

Here ω_s = series resonant frequency = $\frac{1}{\sqrt{L C_s}}$

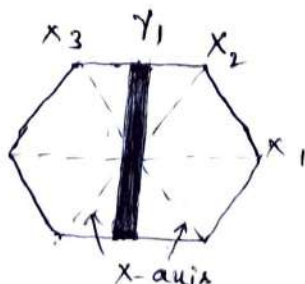
ω_p = parallel resonant frequency = $\frac{1}{\sqrt{L \left(\frac{C_s C_p}{C_s + C_p} \right)}}$

If C_p is very much larger than C_s then the parallel resonant frequency will be approximately equal to series resonant frequency.

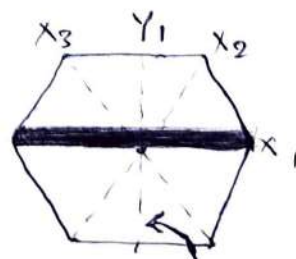
The structure of the quartz crystal and the crystal after cutting, using X-cut and Y-cut are shown in below.



Quartz
fig(a): crystal structure



b) X-cut crystal



c) Y-cut crystal

series resonant frequency is the frequency at which reactance of the inductance L is equal to the reactance of the capacitance C_s . In this case the impedance of the equivalent circuit is equal to resistance ' R '.

The Parallel resonant frequency is the frequency at which the reactance of the RLC branch is equal to the reactance of the capacitor C_p .

Advantages of crystal oscillator:

- 1) crystal oscillator offers very high frequency stability.
- 2) crystal oscillator circuits are less expensive
- 3) Quartz crystal has small size and light weight, which is preferred in crystal oscillator.
- 4) crystals also have very high quality factor (Q).
- 5) It also provides good temperature stability.

Disadvantages of crystal oscillator:

- 1) crystals are very delicate and fragile, so they should be handled carefully.
- 2) The increase in the frequency, decreases the thickness of the crystal. This in turn reduces the mechanical strength of the crystal.
- 3) crystal oscillators have fixed frequency of oscillation. Therefore, for every frequency of oscillation, the entire circuit must be redesigned.
- 4) The crystal oscillators are used only in low power circuits.

Problem

A crystal has $L = 2H$, $C = 0.01PF$ and $R = 2k\Omega$. It has a mounting capacitance of $2PF$. Calculate its series and parallel resonant frequencies.

sol) Given $L = 2H$, $C = C_s = 0.01PF$, $R = 2k\Omega$

Mounting capacitance $C_p = 2PF$

$$\text{series resonant frequency } f_s = \frac{1}{2\pi\sqrt{LC_s}} = \frac{1}{2\pi\sqrt{2 \times 0.01 \times 10^{-12}}} = 1.12 MHz$$

(14)

Parallel resonant frequency $f_p = \frac{1}{2\pi\sqrt{L \frac{C_s C_p}{C_s + C_p}}}$

$$\Rightarrow f_p = \frac{1}{2\pi\sqrt{\frac{2 \times 0.01 \times 10^{-12} \times 2 \times 10^{-12}}{(0.01 + 2) \times 10^{-12}}}}$$

$$\therefore f_p = 1.13 \text{ MHz}$$

Note: In the above problem $f_s \approx f_p$ as the values of C_s and C_p are such that $C_p \gg C_s$.

2) A crystal has $L = 0.5 \text{ H}$, $C_s = 0.06 \text{ PF}$, $C_p = 1 \text{ PF}$, $R = 5 \text{ k}\Omega$. Find the series and Parallel resonant frequency and Q-factor of the crystal at series resonance and parallel resonance.

Sol) Given $L = 0.5 \text{ H}$, $C_s = 0.06 \text{ PF}$, $C_p = 1 \text{ PF}$, $R = 5 \text{ k}\Omega$

$$\text{series resonant frequency } f_s = \frac{1}{2\pi\sqrt{LC_s}} = \frac{1}{2\pi\sqrt{(0.5)(0.06 \times 10^{-12})}}$$

$$\therefore f_s = 918.9 \text{ KHz}$$

$$\text{Q-factor at series resonance is } Q_s = \frac{\omega_s L}{R}$$

$$\Rightarrow Q_s = \frac{2\pi f_s L}{R} = \frac{2\pi \times 918.9 \times 10^3 \times 0.5}{5 \times 10^3}$$

$$\Rightarrow Q_s = 577$$

$$\text{parallel resonant frequency } f_p = \frac{1}{2\pi\sqrt{L \frac{C_s C_p}{C_s + C_p}}}$$

$$\Rightarrow f_p = \frac{1}{2\pi\sqrt{(0.5) \frac{(0.06 \times 10^{-12}) \times (1 \times 10^{-12})}{(0.06 + 1) \times 10^{-12}}}}$$

$$\Rightarrow f_p = 946 \text{ KHz}$$

$$\text{Q-factor at parallel resonance is } Q_p = \frac{\omega_p L}{R} = \frac{2\pi f_p L}{R}$$

$$\Rightarrow Q_p = \frac{2\pi \times (946 \times 10^3) \times 0.5}{5 \times 10^3} = 594$$

Pierce crystal oscillator:

The transistor pierce crystal oscillator is as shown in below figure.

Here the crystal is connected in the feed back path from collector to base.

The resistors R_1 , R_2 and R_E are used to establish proper biasing in the circuit.

The RF choke used in the circuit, is for isolation of ac and dc.

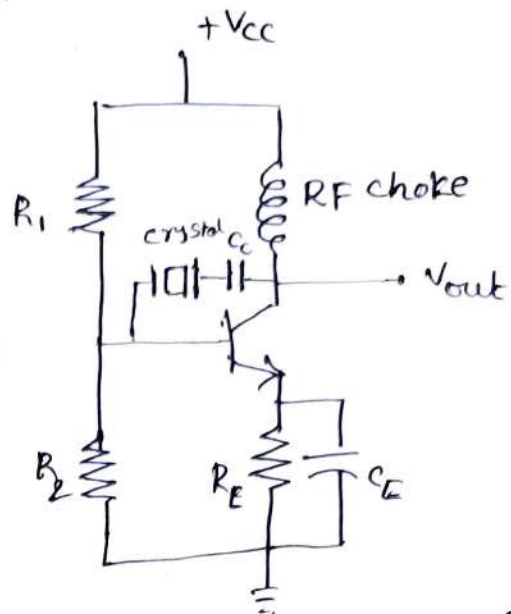


fig: Pierce crystal oscillator

C_c is the coupling capacitance. C_E is the emitter bypass capacitor which is used to prevent the amplification losses. The coupling capacitor C_c blocks the dc voltage between the collector and base and it has a negligible impedance at the frequency of the oscillator.

The frequency of oscillation set by the series resonant frequency of the crystal is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC_s}}$$

The main advantage of the pierce crystal oscillator is its simplicity.

It is the most frequently used crystal oscillator.

15
 $\Rightarrow$ A tuned collector oscillator in a radio receiver has a fixed inductance of $60\mu\text{H}$ and has to be tunable over the frequency band of 400kHz to 1200kHz . Find the range of capacitor to be used.

sd $\rangle$ Given $L_p = 60\mu\text{H}$, $f_{\min} = 400\text{kHz}$, $f_{\max} = 1200\text{kHz}$

Frequency of oscillation for tuned collector oscillator is

$$f_o = \frac{1}{2\pi\sqrt{L_p C}} \quad \text{At } f = f_{\min}, \text{ capacitance } C = C_{\max}$$

$$\Rightarrow C_{\max} = \frac{1}{4\pi^2 f_{\min}^2 L_p} = \frac{1}{4\pi^2 (400 \times 10^3)^2 (60 \times 10^{-6})} = 2641 \text{ PF}$$

At $f = f_{\max}$ capacitance $C = C_{\min}$

$$\therefore C_{\min} = \frac{1}{4\pi^2 f_{\max}^2 L_p} = \frac{1}{4\pi^2 (1200 \times 10^3)^2 (60 \times 10^{-6})}$$

$$\Rightarrow C_{\min} = 293 \text{ PF}$$

$\therefore$ The range of the capacitor is $293 \text{ PF} - 2641 \text{ PF}$.

$\Rightarrow$ Design a hartley oscillator that generates the frequency of oscillation at 1MHz .

sd $\rangle$ In a hartley oscillator the tank circuit contains two inductors L_1 and L_2 and a capacitor C which decides

the frequency of oscillation $f_o = \frac{1}{2\pi\sqrt{(L_1 + L_2 + 2M)C}} \rightarrow (1)$

Let the mutual inductance $M = 0$.

Let us assume $C = 500 \text{ PF}$

given frequency of oscillation $f_o = 1\text{MHz} = 1 \times 10^6 \text{ Hz}$

Substituting $M = 0$ in equation (1) we get

$$f_o = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

$$\Rightarrow f_0^2 = \frac{1}{4\pi^2(L_1+L_2)C}$$

$$\Rightarrow L_1+L_2 = \frac{1}{4\pi^2 f_0^2 C} = \frac{1}{4\pi^2 (1 \times 10^6)^2} \times 500 \times 10^{-12}$$

$$\Rightarrow L_1+L_2 = 5.066 \times 10^{-5} = 50.66 \mu F \approx 50 \mu F$$

Let $L_1 = 32 \mu F$ and $L_2 = 18 \mu F$ such that the sum of L_1 and L_2 is $50 \mu F$.

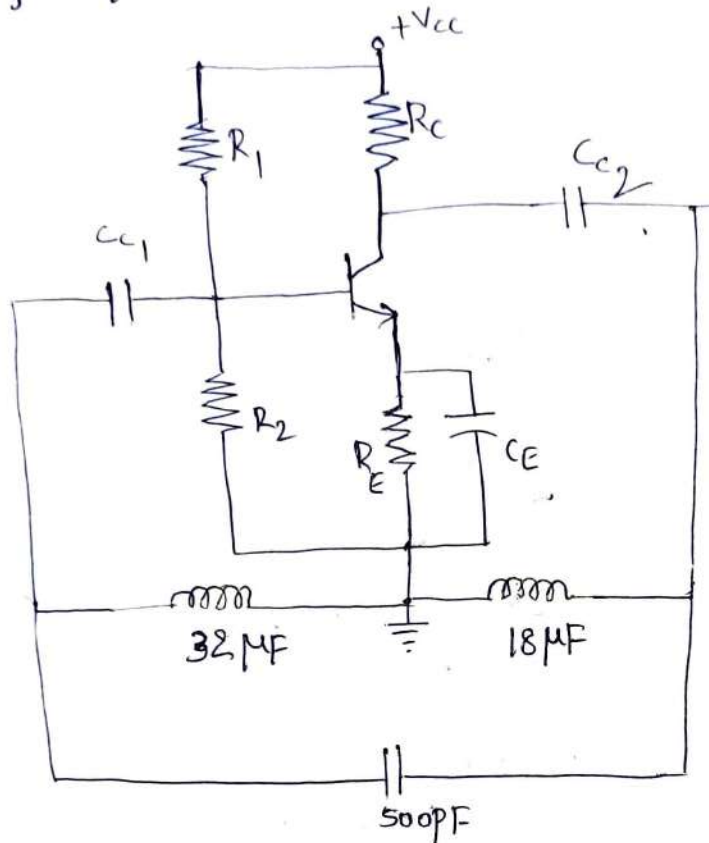


fig: Hartley oscillator

H.W Design a colpitt's oscillator that generates a signal with frequency of oscillation at 1 MHz.

→ Find the value of h_{fe} to satisfy the condition for frequency of a signal (f_0) with sustained oscillations for a hartley oscillator having $L_1 = 10 \mu F$, $L_2 = 2 \mu F$ and $C = 5 \text{ pF}$. Assume $M = 0$.

sol) To get sustained oscillation in hartley oscillator the condition for $h_{fe} = \frac{L_1}{L_2} = \frac{10 \times 10^{-6}}{2 \times 10^{-6}} = 5$ ✓

RC Oscillators :

All the LC oscillators are very useful to generate the signals with high frequencies. But the low frequency signals are generated with higher values of inductance and capacitances. This leads the circuit to be bulky and in fact the circuit becomes expensive. The signals of low frequencies are easily generated with RC oscillators.

RC oscillators are mainly of two types.

i) RC phase shift oscillator ii) Wien bridge oscillator.

i) RC phase shift oscillator using cascade connection of High pass filter:

In this oscillator the required phase shift of 180° in the feedback loop from output to input is obtained by using R and C components instead of tank circuit.

The following figure shows the circuit of RC Phase shift oscillator using cascade connection of high pass filter.

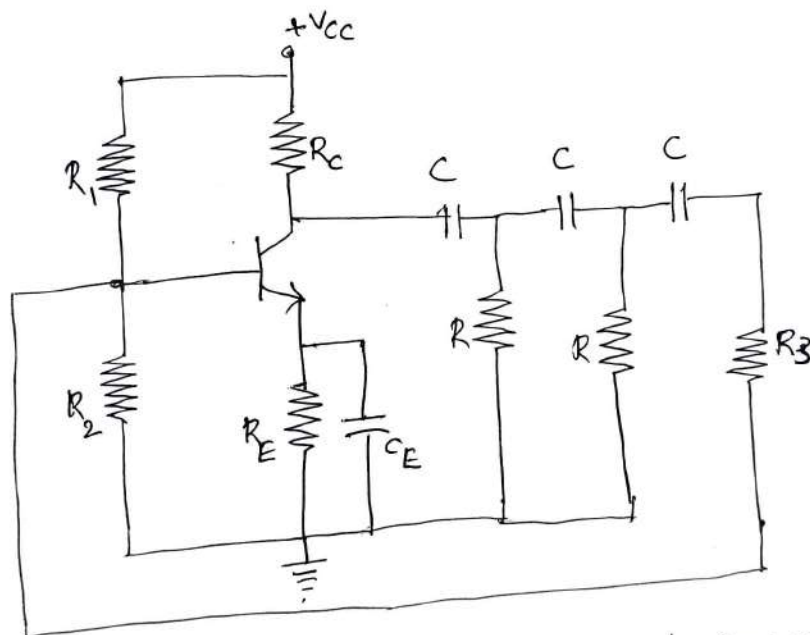


fig a) RC Phase shift oscillator using cascade connection of High Pass filter.

Here a common emitter amplifier is followed by three sections of RC phase shift network. The output of the last section is connected as the input to the base of the transistor.

In order to make the three RC sections identical, R_3 is selected such that $R_3 + R_i = R$, where R_i is the input impedance of circuit.

Since the BJT is connected in CE configuration the input impedance R_i is equal to h_{ie} . That means $R_3 + h_{ie} = R$, neglecting R_1 & R_2 .

The Phase shift of each RC section is given by

$$\phi = \tan^{-1}\left(\frac{1}{\omega CR}\right)$$

If R and C values are chosen such that for a given frequency f_n , the phase shift of each RC section is 60° . Thus the RC ladder network produces a total phase shift of 180° between its input and output voltages for the given frequency. The transistor of CE Configuration provides a phase shift of 180° . Therefore a total phase shift of 360° is obtained, that satisfies the condition for sustained oscillations i.e. satisfying Barkhausen criterion. For RC Phase Shift oscillator the frequency of oscillation

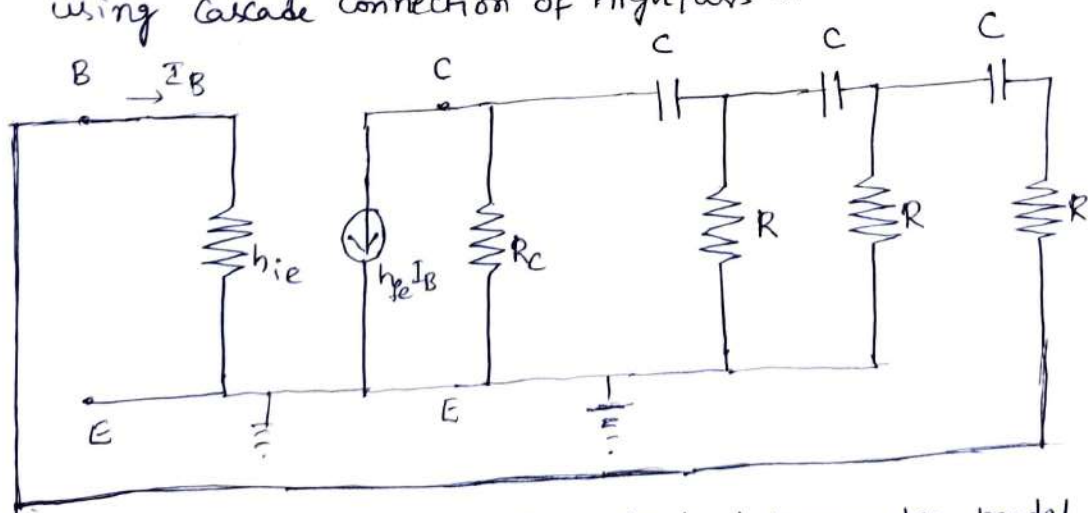
is given by
$$f_o = \frac{1}{2\pi RC \sqrt{6+4K}} \quad \text{where } K = \frac{R_c}{R}$$

At this frequency, it is found that the feedback factor β

is $|\beta| = \frac{1}{29}$.

To get $|A\beta|$ not less than unity the transistor amplifier gain $|A|$ must be greater than or equal to 29.

The equivalent h-parameter model for the RC Phase Shift oscillator using Cascade Connection of high pass filter is as shown in below.

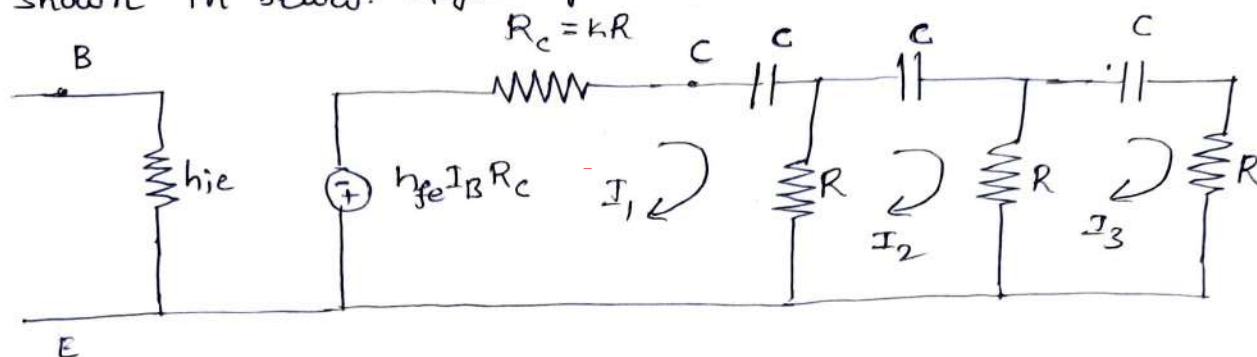


fig(b) Equivalent h-parameter model

Analysis:

(17)

The h-parameter equivalent model for RC phase shift oscillator using cascade connection of highpass filter is modified as shown in below. Neglecting R_1 and R_2 input impedance $R_i \approx h_{ie}$.



Here we have replaced $R_3 + h_{ie}$ with R and the current source $h_{fe} I_B$ is replaced by its equivalent voltage source. Assume the ratio of the resistance R_c to R as k . i.e. $k = \frac{R_c}{R}$

Applying KVL for loop 1 we get

$$I_1 R_c + I_1 \frac{1}{j\omega C} + I_1 R - I_2 R = -h_{fe} I_B R_c$$

Replacing R_c with kR and $j\omega$ by s we get

$$I_1 kR + I_1 \frac{1}{sC} + I_1 R - I_2 R = -h_{fe} I_B kR$$

$$\Rightarrow I_1 \left[(k+1)R + \frac{1}{sC} \right] - I_2 R = -h_{fe} I_B kR \rightarrow (1)$$

Applying KVL for loop 2 we get

$$I_2 \frac{1}{j\omega C} + I_2 R - I_3 R + I_2 R - I_1 R = 0$$

Replace $j\omega$ by s

$$I_2 \frac{1}{sC} + 2I_2 R - I_3 R - I_1 R = 0$$

$$\Rightarrow -I_1 R + I_2 \left(2R + \frac{1}{sC} \right) - I_3 R = 0 \rightarrow (2)$$

Apply KVL for loop 3 we get

$$I_3 \left(\frac{1}{j\omega C} \right) + I_3 R + I_3 R - I_2 R = 0$$

Replace 'sw by s,

$$I_3 \left(\frac{1}{sC} \right) + 2I_3 R - I_2 R = 0$$

$$\Rightarrow -I_2 R + I_3 \left(2R + \frac{1}{sC} \right) = 0 \quad \longrightarrow \quad (3)$$

using Cramer's rule to solve for I_3

$$D = \begin{vmatrix} (k+1)R + \frac{1}{sC} & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{vmatrix}$$

$$\Rightarrow D = \left[(k+1)R + \frac{1}{sC} \right] \cdot \left[\left(2R + \frac{1}{sC} \right)^2 - R^2 \right] - (-R) \left[(-R) \left(2R + \frac{1}{sC} \right) - 0 \right]$$

$$D = \left[(k+1)R + \frac{1}{sC} \right] \left(2R + \frac{1}{sC} \right)^2 - \left[(k+1)R + \frac{1}{sC} \right] \cdot R^2 + 0(R^2)$$

$$- R^2 \left(2R + \frac{1}{sC} \right) \quad \longrightarrow \quad (4)$$

The first term in the above equation is

$$\left[(k+1)R + \frac{1}{sC} \right] \left(2R + \frac{1}{sC} \right)^2 = \left[\frac{(k+1)RSC + 1}{SC} \right] \frac{(2RSC + 1)^2}{s^2 C^2}$$

$$= \frac{(kRSC + RSC + 1)(4R^2 s^2 C^2 + 4RSC + 1)}{s^3 C^3}$$

$$= \frac{4kR^3 s^3 C^3 + 4kR^2 s^2 C^2 + kRSC + 4R^3 s^3 C^3 + 4R^2 s^2 C^2 + RSC + 4R^2 s^2 C^2 + 4RSC + 1}{s^3 C^3}$$

$$= \frac{R^3 s^3 C^3 (4k+4) + R^2 s^2 C^2 (4k+8) + RSC(k+5) + 1}{s^3 C^3}$$

The second and third term in equation (4) are combinedly written as

$$-\left[(k+1)R + \frac{1}{sC} \right] R^2 - R^2 \left(2R + \frac{1}{sC} \right) = -\frac{[(k+1)RSC + 1]R^2}{SC} - \frac{R^2(2RSC + 1)}{SC}$$

$$\begin{aligned}
 &= \frac{-KR^3SC - R^3SC - R^2 - 2R^3SC - R^2}{SC} \\
 &= \frac{-KR^3SC - 3R^3SC - 2R^2}{SC} \\
 &= \frac{-(KR^3SC + 3R^3SC + 2R^2)}{SC}
 \end{aligned}$$

combining the first term equivalent and second & third term equivalent of equation (4) we get

$$\begin{aligned}
 D &= \frac{R^3S^3C^3(4K+4) + R^2S^2C^2(4K+8) + RSC(K+5) + 1}{S^3C^3} - \frac{(KR^3SC + 3R^3SC + 2R^2)}{SC} \\
 \Rightarrow D &= \frac{R^3S^3C^3(4K+4) + R^2S^2C^2(4K+8) + RSC(K+5) + 1}{S^3C^3} - \frac{SC^2(KR^3SC + 3R^3SC + 2R^2)}{S^3C^3} \\
 &= \frac{R^3S^3C^3(4K+4) + R^2S^2C^2(4K+8) + RSC(K+5) + 1 - KR^3S^3C^3 - 3R^3S^3C^3 - 2R^2S^2C^2}{S^3C^3} \\
 D &= \frac{R^3S^3C^3(3K+1) + R^2S^2C^2(4K+6) + RSC(K+5) + 1}{S^3C^3} \rightarrow (5)
 \end{aligned}$$

Now

$$D_3 = \begin{vmatrix} (K+1)R + \frac{1}{SC} & -R & -h_{fe}I_BKR \\ -R & 2R + \frac{1}{SC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= 0 - 0 + (-h_{fe}I_BKR) \cdot (R^2 - 0)$$

$$D_3 = -KR^3h_{fe}I_B \rightarrow (6)$$

$$\therefore I_3 = \frac{D_3}{D} = \frac{-KR^3h_{fe}I_B S^3C^3}{R^3S^3C^3(3K+1) + R^2S^2C^2(4K+6) + RSC(K+5) + 1} \quad \left(\because \text{from equation (5) and (6)} \right) \rightarrow (7)$$

I_3 = output current of the feedback circuit

I_B = Input current of the amplifier

$I_C = h_{fe} I_B$ = Input current of the feedback circuit

Amplifier gain $A = \frac{\text{output of the amplifier}}{\text{Input to the amplifier}} = \frac{I_3}{I_B} = h_{fe}$

$$\text{Loop gain } A\beta = \frac{I_3}{I_B} \cdot \frac{I_3}{I_C} = h_{fe} \cdot \frac{I_3}{h_{fe} I_B} = \frac{I_3}{I_B} \rightarrow (8)$$

$$\left(\because \beta = \text{feed back factor} = \frac{\text{output of feedback circuit} = \frac{I_3}{I_C}}{\text{Input to feedback circuit}} \right)$$

From equation (7) and (8)

$$A\beta = \frac{I_3}{I_B} = \frac{-kR^3 h_{fe} s^3 c^3}{R^3 s^3 c^3 (3k+1) + R^2 s^2 c^2 (4k+6) + R s c (k+5) + 1} \rightarrow (9)$$

Substituting $s = j\omega$, $s^2 = j^2 \omega^2 = -\omega^2$, $s^3 = j^3 \omega^3 = -j\omega^3$
in the above equation we get

$$A\beta = \frac{+j\omega^3 kR^3 h_{fe} c^3}{-j\omega^3 R^3 c^3 (3k+1) - \omega^2 R^2 c^2 (4k+6) + j\omega R c (k+5) + 1}$$

$$= \frac{k h_{fe}}{\frac{-j\omega^3 R^3 c^3 (3k+1)}{j\omega^3 R^3 c^3} - \frac{\omega^2 R^2 c^2 (4k+6)}{j\omega^3 R^3 c^3} + \frac{j\omega R c (k+5)}{j\omega^3 R^3 c^3} + \frac{1}{j\omega^3 R^3 c^3}}$$

$$= \frac{k h_{fe}}{-(3k+1) + j \frac{(4k+6)}{\omega R c} + \frac{k+1}{\omega^2 R c^2} - \frac{j}{\omega^3 R^3 c^3}}$$

$$A\beta = \frac{k h_{fe}}{-(3k+1) + j(4k+6)\alpha + (k+1)\alpha^2 - j\alpha^3} \quad \left(\text{where } \alpha = \frac{1}{\omega R c} \right)$$

$$\Rightarrow A\beta = \frac{k h_{fe}}{[k\alpha^2 + 5\alpha^2 - 3k - 1] + j(-\alpha^3 + 4k\alpha + 6\alpha)} \rightarrow (10)$$

As per Barkhausen Criterion to get sustained oscillations (19)
 $\angle A\beta = 0^\circ$ (or) 360° . To get $\angle A\beta = 0^\circ$, the imaginary part of the denominator should be 0.

$$\therefore -\alpha^3 + 4K\alpha + 6\alpha = 0$$

$$\Rightarrow \alpha(-\alpha^2 + 4K + 6) = 0$$

$$\Rightarrow -\alpha^2 + 4K + 6 = 0$$

$$\Rightarrow \alpha = \sqrt{4K + 6}$$

Replacing $\alpha = \frac{1}{\omega_0 RC}$

$$\frac{1}{\omega_0 RC} = \sqrt{4K + 6}$$

$$\omega_0 = \frac{1}{RC \sqrt{4K + 6}}$$

$$\therefore f_0 = \frac{1}{2\pi RC \sqrt{4K + 6}}$$

This is the frequency at which $\angle A\beta = 0^\circ$. At the same frequency $|A\beta| = 1$, substituting $\alpha = \sqrt{4K + 6}$ in equation (10) we get

$$A\beta = \frac{K h_{fe}}{K(4K + 6) + 5(4K + 6) - 3K - 1}$$

$$= \frac{K h_{fe}}{4K^2 + 6K + 20K + 30 - 3K - 1}$$

$$= \frac{K h_{fe}}{4K^2 + 23K + 29}$$

Now $|A\beta| = 1$

$$\Rightarrow \left(\frac{K h_{fe}}{4K^2 + 23K + 29} \right) = 1 \Rightarrow K h_{fe} = 4K^2 + 23K + 29$$

$$\Rightarrow h_{fe} = 4K + \frac{23 + 29}{K}$$

Minimum value of h_{fe} for the oscillations (or) minimum gain for sustained oscillations:

we know that $h_{fe} = 4K + 23 + \frac{29}{K} \rightarrow \textcircled{11}$

To get minimum value of h_{fe} we have to find $\frac{dh_{fe}}{dK}$ and equate it to zero, in order to get the value of K .

$$\frac{dh_{fe}}{dK} = 4 + 0 + \left(-\frac{29}{K^2}\right) = 0$$

$$\Rightarrow 4 - \frac{29}{K^2} = 0$$

$$\Rightarrow K^2 = \frac{29}{4}$$

$$\Rightarrow K = 2.6925$$

$$\therefore K = 2.6925 \text{ for minimum } h_{fe}$$

substituting this in equation $\textcircled{11}$ we get

$$h_{fe_{\min}} = 4(2.6925) + 23 + \frac{29}{2.6925}$$

$$\therefore h_{fe_{\min}} = 44.54$$

Therefore the minimum gain for sustained oscillations in an RC-

Phase shift oscillator is $h_{fe_{\min}} = 44.54$.

problem Find the capacitor C and h_{fe} for the transistor to provide the frequency of 10KHz of a transistorized Phase shift oscillator.

Assume $R_1 = 25k\Omega$, $R_2 = 57k\Omega$, $R_C = 20k\Omega$, $R = 7.1k\Omega$, and $h_{ie} = 1.8k\Omega$.

Sol) Given $f_0 = 10\text{KHz}$, $R_1 = 25k\Omega$, $R_2 = 57k\Omega$, $h_{ie} = 1.8k\Omega$, $R = 7.1k\Omega$

Input impedance $z_i = h_{ie} = 1.8k\Omega$

$$z_i' = z_i \parallel R_1 \parallel R_2 = 1.8k\Omega \parallel 25k\Omega \parallel 57k\Omega = 1.631k\Omega$$

$$R_3 + z_i' = R \Rightarrow R_3 = R - z_i' = 7.1k\Omega - 1.631k\Omega = 5.469k\Omega$$

$$K = \frac{R_C}{R} = \frac{20 \times 10^3}{7.1 \times 10^3} = 2.8169$$

$$\therefore f = \frac{1}{2\pi RC \sqrt{6+4K}} \Rightarrow 10 \times 10^3 = \frac{1}{2\pi \times 7.1 \times 10^3 \times C \sqrt{6+4(2.8169)}}$$

$$\Rightarrow C = \frac{1}{2\pi \times 7.1 \times 10^3 \times 10 \times 10^3} \sqrt{6 + 11.2676}$$

$$\therefore C = 539.44 \text{ PF}$$

we know that $h_{fe} \geq 4K + 23 + \frac{29}{K}$

$$\Rightarrow h_{fe} \geq 4(2.8169) + 23 + \frac{29}{2.8169}$$

$$\therefore h_{fe} \geq 44.5626$$

Advantages and disadvantages of RC Phase Shift Oscillator:

- 1> The circuit is simple to design.
- 2> It can produce the output over audio frequency range.
- 3> It produces sinusoidal output waveform.

The drawbacks of RC Phase Shift Oscillator are

- 1> To change the frequency of oscillation in an RC Phase shift oscillator, all the three capacitors or resistors should be changed simultaneously.
- 2> It is difficult to control the amplitude of the output signal, without affecting the frequency of oscillation.
- 3> Frequency stability is poor.

Problem: Find the capacitor C and h_{fe} for the transistor to provide a transistor to provide the frequency of oscillation of 10KHz of a transistorized oscillator designed with RC Phase Shift. Assume $R_1 = 25\text{k}\Omega$, $R_2 = 60\text{k}\Omega$, $R_c = 40\text{k}\Omega$, $R = 7.1\text{k}\Omega$ and $h_{ie} = 1.8\text{k}\Omega$.

sol> Given $f_0 = 10\text{KHz}$, $R_1 = 25\text{k}\Omega$, $R_2 = 60\text{k}\Omega$, $R_c = 40\text{k}\Omega$, $R = 7.1\text{k}\Omega$ and $h_{ie} = 1.8\text{k}\Omega$.

$$\text{Frequency of oscillation } f_0 = \frac{1}{2\pi RC} \sqrt{6 + 4K}$$

$$\Rightarrow C = \frac{1}{2\pi f_0 R \sqrt{6 + 4K}} = \frac{1}{2\pi f_0 R \sqrt{6 + 4 \frac{R_c}{R}}}$$

$$\Rightarrow C = \frac{1}{2\pi \times 10 \times 10^3 \times 7.1 \times 10^3 \sqrt{6 + 4 \left(\frac{40}{7.1 \times 10^3} \right)}}$$

$$C = 0.417 \text{ nF}$$

we know that $h_{fe} \geq 4R + 23 + \frac{29}{R}$

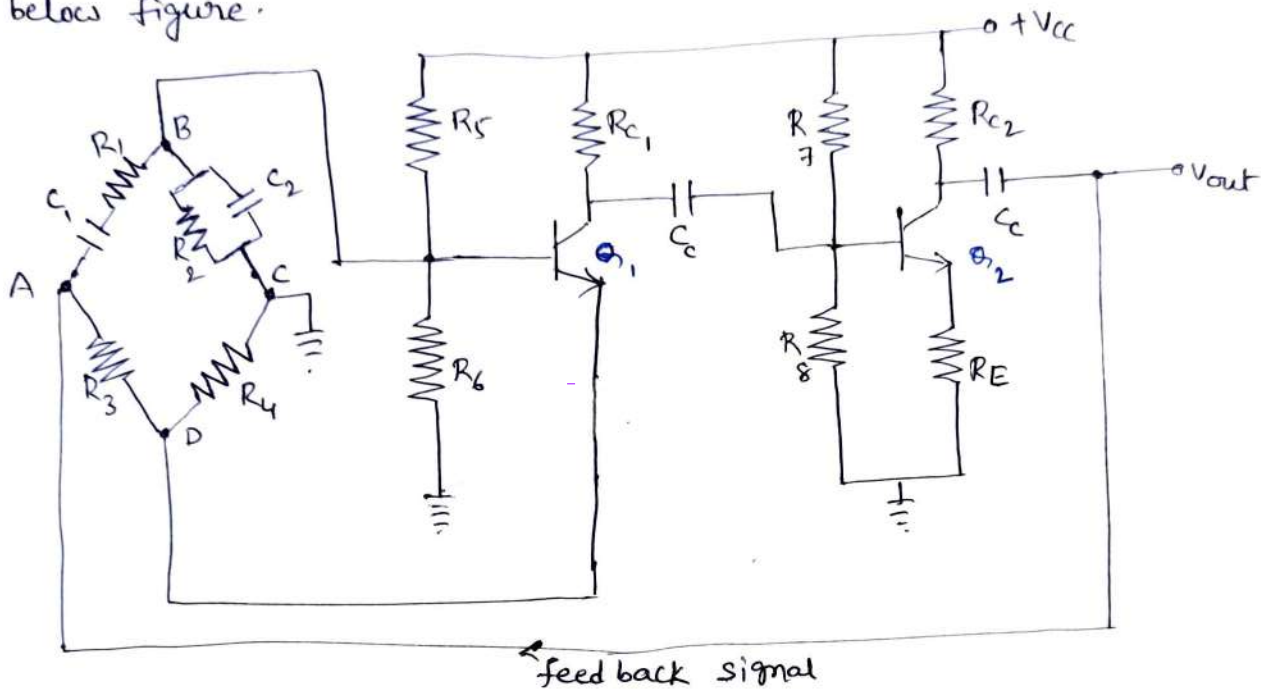
$$\Rightarrow h_{fe} \geq 4\left(\frac{R_c}{R}\right) + 23 + \frac{29}{\left(\frac{R_c}{R}\right)}$$

$$\Rightarrow h_{fe} \geq 4\left(\frac{40 \times 10^3}{7.1 \times 10^3}\right) + 23 + \frac{29 \times 7.1 \times 10^3}{40 \times 10^3}$$

$$\therefore h_{fe} \geq 50.67$$

Wien-Bridge Oscillator:

The circuit diagram for a wien-bridge oscillator is as shown in below figure.

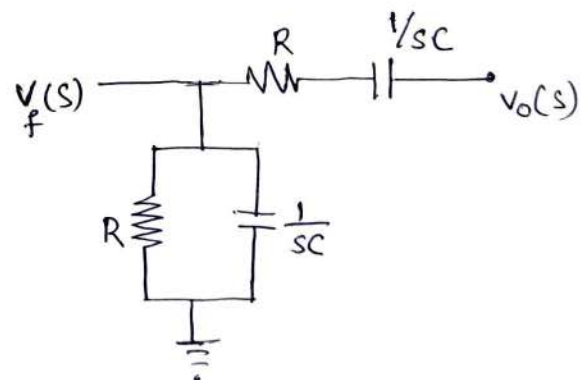


fig(a): Wien-Bridge oscillator circuit

A wien-bridge oscillator circuit contains a two stage RC coupled amplifier which provides a phase shift of 360° (or) 0° .

A balanced bridge is used as a feedback network in which there is no necessity for any additional phase shift.

The feedback network consists of a lead-lag network R_1-C_1 and R_2-C_2 and a Potential divider R_3-R_4 . The lead-lag network provides a positive feedback to the input of the first stage transistor Q_1 i.e base



fig(b): Equivalent circuit

of the transistor Q_1 and the voltage divider provides a negative feedback to the emitter of Q_1 .

The frequency of oscillations is determined by the series element R_1, C_1 and parallel elements R_2, C_2 of the bridge and it is given as $f_0 = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then $f_0 = \frac{1}{2\pi\sqrt{R^2 C^2}}$

$$\therefore f_0 = \frac{1}{2\pi RC}$$

The bridge is said to be balanced if $\frac{R_3}{R_4} = \frac{R_1 + \frac{1}{j\omega C_1}}{R_2 \parallel \frac{1}{j\omega C_2}} = \frac{R_1 - \frac{j}{\omega C_1}}{R_2 \parallel -\frac{j}{\omega C_2}}$

$$\Rightarrow \frac{R_3}{R_4} = \frac{R_1 - \frac{j}{\omega C_1}}{\left(-\frac{j R_2}{\omega C_2}\right) / R_2 - \frac{j}{\omega C_2}}$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2} \left(R_1 - \frac{j}{\omega C_1}\right) \left(R_2 - \frac{j}{\omega C_2}\right)$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2} \left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} - \frac{j R_2}{\omega C_1} - \frac{j R_1}{\omega C_2} \right]$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2} \left[\left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} \right] - \frac{j}{\omega} \left[\frac{R_2}{C_1} + \frac{R_1}{C_2} \right] \right]$$

$$\Rightarrow \frac{R_3}{R_4} = \frac{j\omega C_2}{R_2} \left[R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} \right] + \frac{C_2}{R_2} \left[\frac{R_2}{C_1} + \frac{R_1}{C_2} \right]$$

Comparing imaginary parts on both sides we get

$$\frac{\omega C_2}{R_2} \left(R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} \right) = 0 \Rightarrow R_1 R_2 - \frac{1}{\omega^2 C_1 C_2} = 0$$

$$\Rightarrow \omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\Rightarrow \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\therefore f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (\because \omega = 2\pi f_0)$$

If $R_1 = R_2 = R$, $C_1 = C_2 = C$ then

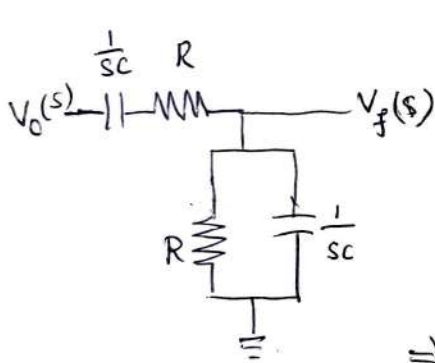
$$f_0 = \frac{1}{2\pi RC}$$

The ratio of R_3 and R_4 should be greater than 2 to provide a sufficient gain for the circuit to provide the desired frequency of oscillation.

Gain of the BJT amplifier used in Wien bridge oscillator.

Assume $R_1 = R_2 = R$ and $C_1 = C_2 = C$. Then feedback circuit is as shown in figure (b).

From figure (b) $V_f(s) = \frac{V_o(s) \cdot (R \parallel \frac{1}{sC})}{(R \parallel \frac{1}{sC}) + R + \frac{1}{sC}}$



$$\Rightarrow \frac{V_f(s)}{V_o(s)} = \left[\frac{R \cdot \frac{1}{sC}}{R + \frac{1}{sC}} \right]$$

$$\frac{R \cdot \frac{1}{sC}}{R + \frac{1}{sC}} + R + \frac{1}{sC}$$

$$\Rightarrow \frac{V_f(s)}{V_o(s)} = \frac{R}{RSC + 1} \cdot \frac{R}{RSC + 1} + R + \frac{1}{sC} = \frac{R}{RSC + 1} \cdot \frac{RSC + 3RSC + 1}{RSC + 1}$$

$$\therefore \beta = \frac{V_f(s)}{V_o(s)} = \frac{RSC}{R^2 s^2 C^2 + 3RSC + 1}$$

We know that $A\beta = 1 \Rightarrow A = \frac{1}{\beta} = \frac{R^2 s^2 C^2 + 3RSC + 1}{RSC}$

$$\Rightarrow A = RSC + 3 + \frac{1}{RSC}$$

Substituting

$$s = j\omega = \frac{j}{RC}$$

$$\Rightarrow A = R \left(\frac{j}{RC} \right) C + 3 + \frac{1}{R \left(\frac{j}{RC} \right) C}$$

$$A = j + 3 + \frac{1}{j} \Rightarrow \boxed{A \approx 3}$$

Therefore the gain of the BJT amplifier is at least equal to 3 for oscillations to be occurred in a Wienbridge oscillator.
i.e. $A \geq 3$

Problem: In a Wien bridge oscillator if the value of R is $100\text{K}\Omega$, frequency of oscillation is 10kHz find the value of Capacitor C .

sol) For Wien bridge oscillator the frequency of oscillation is

$$f_0 = \frac{1}{2\pi RC} \Rightarrow C = \frac{1}{2\pi R f_0} = \frac{1}{2\pi (100 \times 10^3)(10 \times 10^3)}$$

$$\therefore C = 159\text{PF}$$

UNIT III

POWER AMPLIFIERS AND TUNED AMPLIFIERS

POWER AMPLIFIERS: Types, Class A large signal Amplifiers, Transformer Coupled Audio power amplifier- Efficiency, Class B Amplifiers, Efficiency, Complementary Symmetry push pull amplifier, Crossover Distortion.

TUNED AMPLIFIERS

Introduction, Single Tuned Amplifier, Double Tuned Amplifiers, Effect of Cascading Single tuned amplifiers on Band width, Staggered tuned amplifiers, Stability of tuned amplifiers.

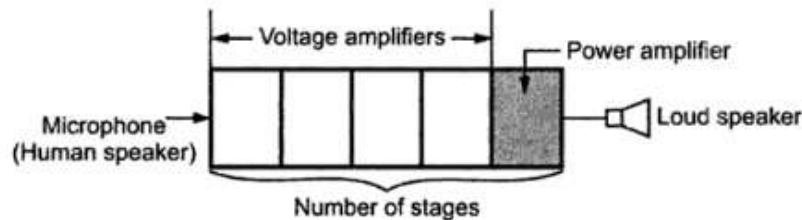
POWER AMPLIFIERS:

5.1 Concept of Large Signal Amplification

Consider a public address system (P.A.) or amplifying system as shown in the Fig. 5.1.

► **Figure 5.1**

Amplifying or P. A. system



The system consists of many stages connected in cascade. Hence basically it is a multistage amplifier. The input is sound signal of a human speaker and the output is given to the loud speaker which is an amplified input signal. The input and the intermediate stages are small signal amplifiers. The sufficient voltage gain is obtained by all the intermediate stages. Hence these stages are called **voltage amplifiers**.

But the last stage gives an output to the load like a loud speaker. Hence the last stage must be capable of delivering an appreciable amount of a.c. power to the load. So it must be capable of handling large voltage or current swings or in other words large signals. The main aim is to develop sufficient power hence the voltage gain is not important, in the last stage. Such a stage, which develops and feeds sufficient power to the load like loudspeaker, servomotor, handling the large signals is called **Large Signal Amplifier** or **Power Amplifier**.

Power amplifiers find their applications in the public address systems, radio receivers, driving servomotor in industrial control systems, tape players, T.V. receivers, cathode ray tubes etc.

5.2 Features of Power Amplifiers

The various features of power amplifiers are,

1. A power amplifier is the last stage of multistage amplifier. The previous stages develop sufficient gain and the **input signal level or amplitude of a power amplifier is large** of the order of few volts.
2. The **output of power amplifier has large current and voltage swings**. As it handles large signals called power amplifiers.
3. The **h-parameter analysis** is applicable to the small signal amplifiers and hence **can not be used for the analysis of power amplifiers**. The analysis of power amplifiers is carried out graphically by drawing a load line on the output characteristics of the transistors used in it.

4. The power amplifiers i.e large signal amplifiers are used to feed the loads like loud speakers having low impedance. So for maximum power transfer the impedance matching is important. Hence **the power amplifiers must have low output impedance**. Hence common collector or emitter follower circuit is very common in power amplifiers. The common emitter circuit with a step down transformer for impedance matching is also commonly used in power amplifiers.
5. The power amplifiers develop an a.c. power of the order of few watts. Similarly large power gets dissipated in the form of heat, at the junctions of the transistors used in the power amplifiers. Hence **the transistors used in the power amplifiers are of large size, having large power dissipation rating, called power transistors**. Such transistors have heat sinks. A heat sink is a metal cap having bigger surface area, press fit on the body of a transistor, to get more surface area, in order to dissipate the heat to the surroundings. In general, the power amplifiers have bulky components.
6. A faithful reproduction of the signal, after the conversion, is important. Due to nonlinear nature of the transistor characteristics, there exists a harmonic distortion in the signal. Ideally signal should not be distorted. Hence **the analysis of signal distortion in case of the power amplifiers is important**.
7. Many a times, the power amplifiers are used in public address systems and many audio circuits to supply large power to the loud speakers. Hence **power amplifiers are also called audio amplifiers or audio frequency (A.F.) power amplifiers**.

5.3 Classification of Large Signal Amplifiers

For an amplifier, a quiescent operating point (Q point) is fixed by selecting the proper d.c. biasing to the transistors used. The quiescent operating point is shown on the load line, which is plotted on the output characteristics of the transistor. The position of the quiescent point on the load line decides the class of operation of the power amplifier. The various classes of the power amplifiers are :

i) Class A ii) Class B iii) Class C and iv) Class AB

5.3.1 Class A Amplifiers

The power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

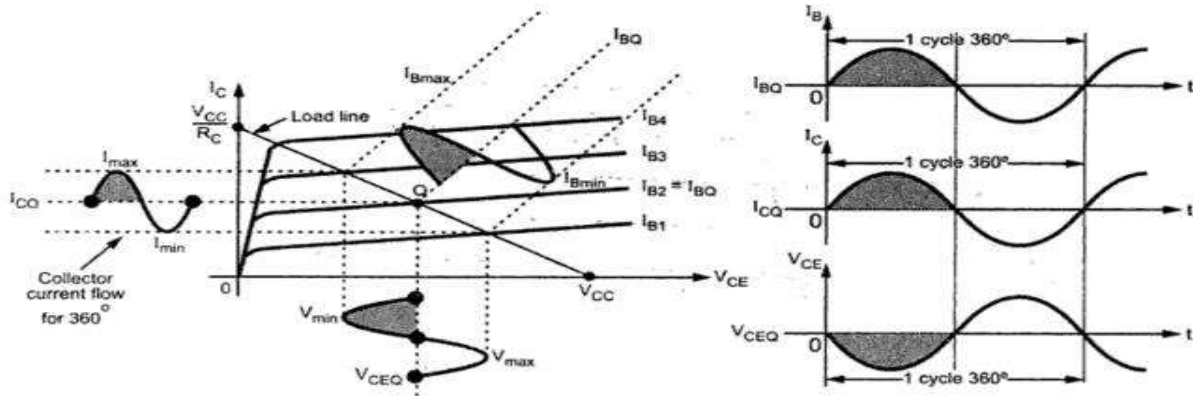
Key Point: *For this class, position of the Q point is approximately at the midpoint of the load line.*

For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c. input signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for 360° (full cycle) of the input signal. In other words, the angle of the collector current flow is 360° i.e. one full cycle.

The current and voltage waveforms for a class A operation are shown with the help of output characteristics and the load line, in the Fig. 5.6.

As shown in the Fig. 5.6, for full input cycle, a full output cycle is obtained. Here signal is faithfully reproduced, at the output, without any distortion. This is an important feature of a class A operation. The efficiency of class A operation is very small.

► **Figure 5.6**
Waveforms representing class A operation



5.3.2 Class B Amplifiers

The power amplifier is said to be class B amplifier if the Q point and the input signal are selected, such that the output signal is obtained only for one half cycle for a full input cycle.

Key Point: For this operation, the Q point is shifted on X-axis i.e. transistor is biased to cut-off.

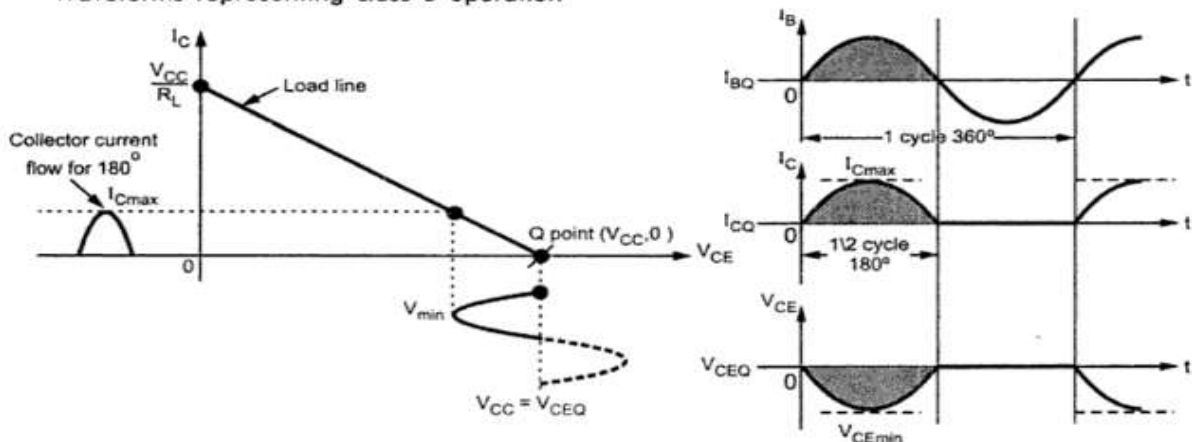
Due to the selection of Q point on the X-axis, the transistor remains, in the active region, only for positive half cycle of the input signal. Hence this half cycle is reproduced at the output. But in a negative half cycle of the input signal, the transistor enters into a cut-off region and no signal is produced at the output. The collector current flows only for 180° (half cycle) of the input signal. In other words, the angle of the collector current flow is 180° i.e. one half cycle.

The current and voltage waveforms for a class B operation are shown in the Fig. 5.7.

As only a half cycle is obtained at the output, for full input cycle, the output signal is distorted in this mode of operation. To eliminate this distortion, practically two transistors are used in the alternate half cycles of the input signal. Thus overall a full cycle of output signal is obtained across the load. Each transistor conducts only for a half cycle of the input signal.

The efficiency of class B operation is much higher than the class A operation.

► **Figure 5.7**
Waveforms representing class B operation



5.3.3 Class C Amplifiers

The power amplifiers is said to be class C amplifier, if the Q point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle.

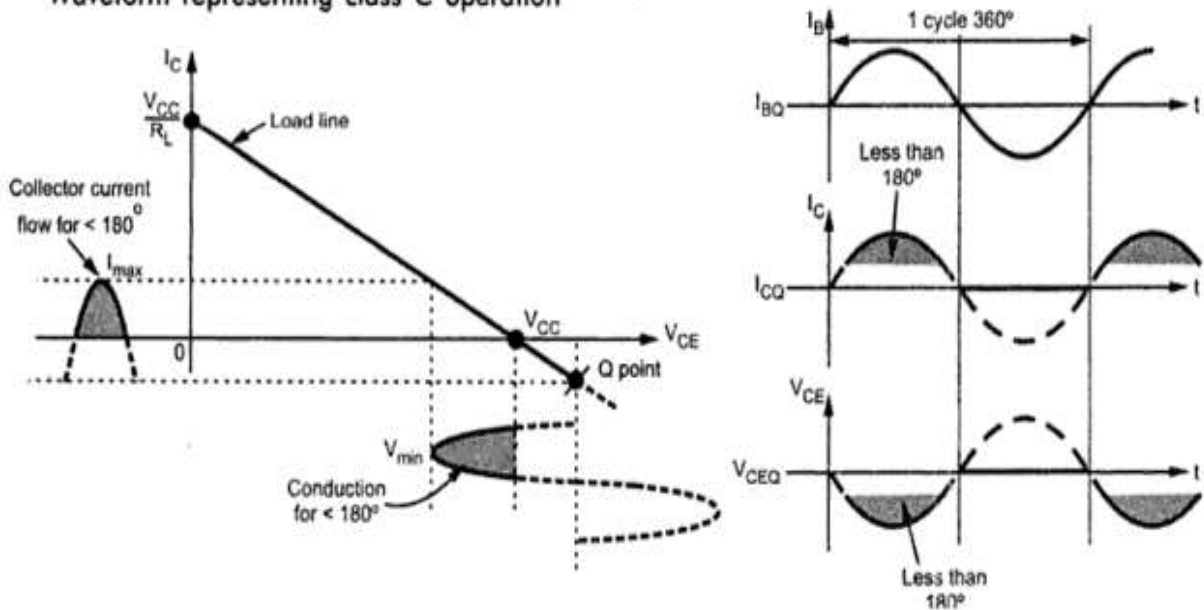
Key Point: For this operation, the Q point is to be shifted below X-axis.

Due to such a selection of the Q point, transistor remains active, for less than a half cycle. Hence only that much part is reproduced at the output. For remaining cycle of the input cycle, the transistor remains cut-off and no signal is produced at the output. The angle of the collector current flow is less than 180° .

The current and voltage waveforms for a class C amplifier operation are shown in the Fig. 5.8.

► **Figure 5.8**

Waveform representing class C operation



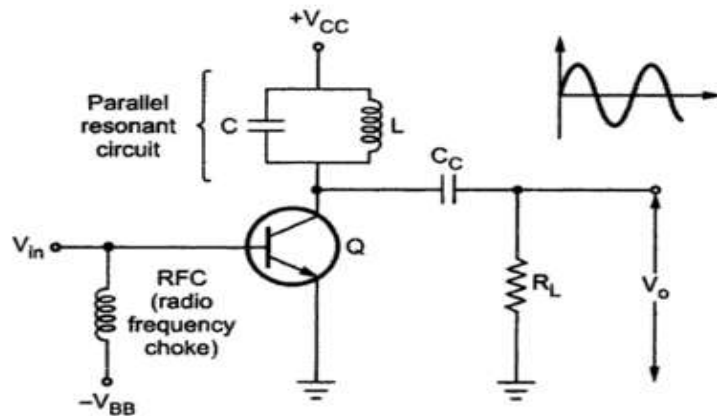
Key Point: In class C operation, the transistor is biased well beyond cut-off. As the collector current flows for less than 180° , the output is much more distorted and hence the class C mode is never used for A.F. power amplifiers.

But the efficiency of this class of operation is much higher and can reach very close to 100%.

Applications : The class C operation is not suitable for audio frequency power amplifiers. The class C amplifiers are used in tuned circuits used in communication areas and in radio frequency (RF) circuits with tuned RLC loads. As used in tuned circuits, class C amplifiers are called **tuned amplifiers**. These are also used in mixer or converter circuits used in radio receivers and wireless communication systems.

The Fig. 5.9 shows the class C tuned amplifier.

► **Figure 5.9**
Class C tuned amplifier



The LC parallel circuit is a parallel resonant circuit. This circuit acts as a load impedance. Due to class C operation, the collector current consists of a series of pulses containing harmonics i.e. many other frequency components along with the fundamental frequency component of input. The parallel tuned circuit is designed to be tuned to the fundamental input frequency. Hence it eliminates the harmonics and produce a sine

wave of fundamental component of input signal. As the transistor and coil losses are small, the most of the d.c. input power is converted to a.c. load power. Hence efficiency of class C is very high.

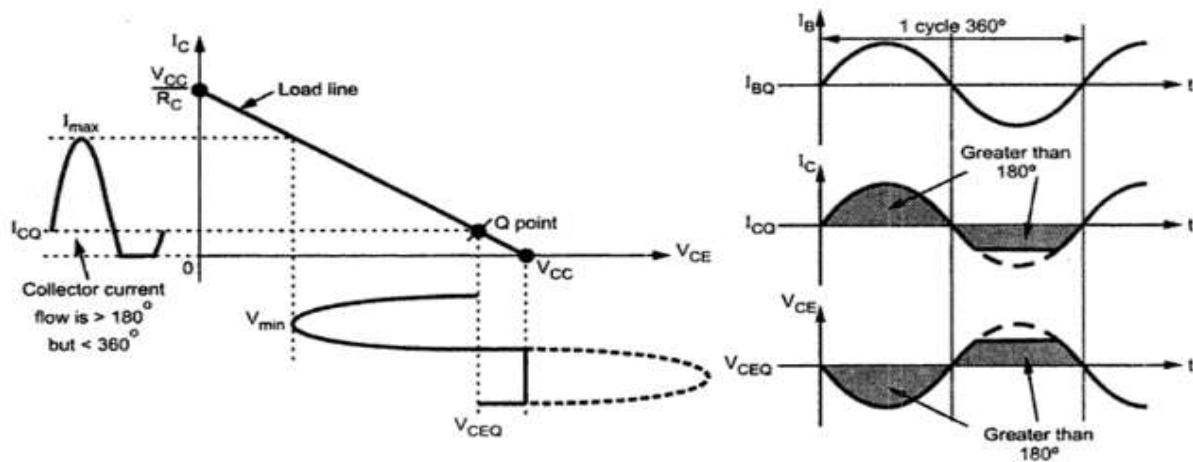
5.3.4 Class AB Amplifiers

The power amplifier is said to be class AB amplifier, if the Q point and the input signal are selected such that the output signal is obtained for more than 180° but less than 360° , for a full input cycle.

Key Point: The Q point position is above X-axis but below the midpoint of a load line.

The current and voltage waveforms for a class AB operation, are shown in the Fig. 5.10.

► **Figure 5.10**
Waveforms representing class AB operation



The output signal is distorted in class AB operation. The efficiency is more than class A but less than class B operation. The class AB operation is important to eliminate cross over distortion.

In general as the Q point moves away from the centre of the load line below towards the X-axis, the efficiency of class of operation increases.

5.5 Comparison of Amplifier Classes

The comparison of various amplifier classes is summarized in Table 5.1.

► **Table 5.1**

Class	A	B	C	AB
Operating Cycle	360°	180°	Less than 180°	180° to 360°
Position of Q point	Centre of load line	On X axis	Below X axis	Above X-axis but below the centre of load line
Efficiency	Poor, 25% to 50%	Better, 78.5%	High	Higher than A but less than B 50% to 78.5%
Distortion	Absent No distortion	Present More than class A	Highest	Present

Key Point: It is important to note that class C operation is never used for audio frequency amplifiers.

This class is used in special areas of tuned circuits, such as radio or communications.

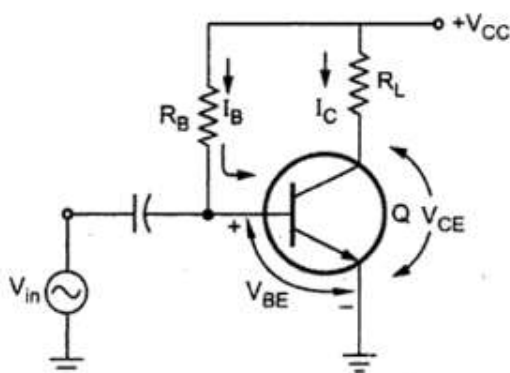
5.6 Analysis of Class A Amplifiers

The class A amplifiers are further classified as **directly coupled** and **transformer coupled** amplifiers. In directly coupled type, the load is directly connected in the collector circuit. While in the transformer coupled type, the load is coupled to the collector using a transformer called an output transformer. Let us study in detail the various aspects of the two types of Class A amplifiers.

5.7 Series Fed, Directly Coupled Class A Amplifier

► **Figure 5.13**

Large signal class A amplifier



A simple fixed-bias circuit can be used as a large signal class A amplifier as shown in the Fig. 5.13.

The difference between small signal version of this circuit is that the signals handled by this large signal circuit are of the order of few volts. Similarly the transistor used, is a power transistor. The value of R_B is selected in such a way that the Q point lies at the centre of the d.c. load line.

The circuit represents the directly coupled class A amplifier as the load resistance is directly connected in the collector circuit. Most of the times the load is a loudspeaker, the

impedance of which varies from 3 to 4 ohms to 16 ohms. The beta of the transistor used is less than 100.

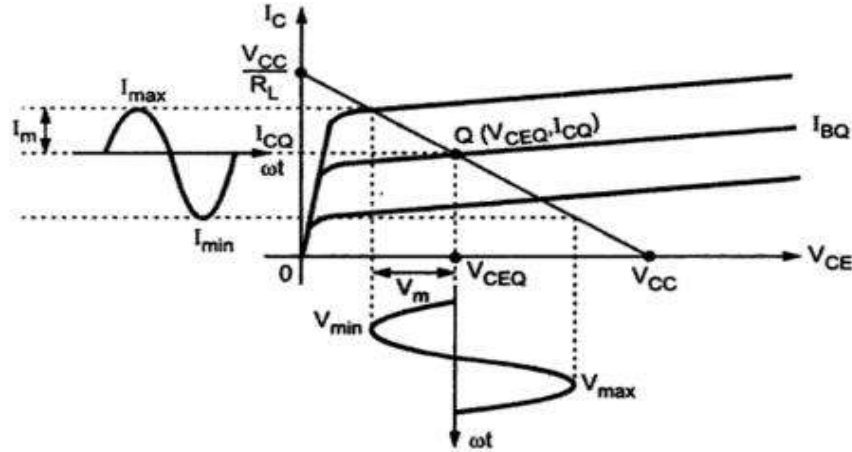
Key Point: This is called *directly coupled*, as the load R_L is directly connected in the collector circuit of power transistor.

The overall circuit handles large power, in the range of a few to tens of watts without providing much voltage gain.

The graphical representation of a class A amplifier is shown in the Fig. 5.14.

► **Figure 5.14**

Graphical representation of class A amplifier



Applying Kirchhoff's voltage law to the circuit shown in the Fig. 5.13, we get

$$\begin{aligned} V_{CC} &= I_C R_L + V_{CE} \\ \therefore I_C R_L &= -V_{CE} + V_{CC} \\ \therefore I_C &= \left[-\frac{1}{R_L} \right] V_{CE} + \frac{V_{CC}}{R_L} \quad \dots (1) \end{aligned}$$

The equation is similar to equation (1) of section 7.3 and thus the slope of the load line is $-\frac{1}{R_L}$ while the Y-intercept is $\frac{V_{CC}}{R_L}$.

The change is because the collector resistance R_C is named as load resistance R_L in this circuit. The Q point is adjusted approximately at the centre of the load line.

5.7.1 D.C.Operation

The collector supply voltage V_{CC} and resistance R_B decides the d.c. base-bias current I_{BQ} . The expression is obtained applying KVL to the B-E loop and with $V_{BE} = 0.7$ V.

$$\therefore I_{BQ} = \frac{V_{CC} - 0.7}{R_B} \quad \dots (2)$$

The corresponding collector current is then,

$$I_{CQ} = \beta I_{BQ} \quad \dots (3)$$

From the equation (1), the corresponding collector to emitter voltage is,

$$V_{CEQ} = V_{CC} - I_{CQ} R_L \quad \dots (4)$$

Hence the Q point can be defined as $Q (V_{CEQ}, I_{CQ})$.

5.7.2 D.C.Power Input

The d.c. power input is provided by the supply. With no a.c input signal, the d.c. current drawn is the collector bias current I_{CQ} . Hence d.c. power input is,

$$P_{DC} = V_{CC} \cdot I_{CQ} \quad \dots (5)$$

It is important to note that even if a.c. input signal is applied, the average current drawn from the d.c. supply remains same. Hence equation (5) represents d.c. power input to the class A series fed amplifier.

5.7.3 A.C. Operation

When an input a.c. signal is applied, the base current varies sinusoidally.

Assuming that the nonlinear distortion is absent, the nature of the collector current and collector to emitter voltage also vary sinusoidally as shown graphically in the Fig. 5.14.

The output current i.e. collector current varies around its quiescent value while the output voltage i.e collector to emitter voltage varies around its quiescent value. The varying output voltage and output current deliver an a.c. power to the load. Let us find the expressions for the a.c. power delivered to the load.

5.7.4 A.C.Power Output

For an alternating output voltage and output current swings, shown in the Fig. 5.14, we can write,

V_{min} = Minimum instantaneous value of the collector (output) voltage

V_{max} = Maximum instantaneous value of the collector (output) voltage

and V_{pp} = Peak to peak value of a.c. output voltage across the load.

$$\therefore V_{pp} = V_{max} - V_{min} \quad \dots (6)$$

Now V_m = Amplitude (peak) of a.c. output voltage as shown in the Fig. 5.14.

$$\therefore V_m = \frac{V_{pp}}{2} = \frac{V_{max} - V_{min}}{2} \quad \dots (7)$$

Similarly we can write for the output current as,

I_{min} = Minimum instantaneous value of the collector (output) current

I_{max} = Maximum instantaneous value of the collector (output) current

and I_{pp} = Peak to peak value of a.c. output (load) current

$$\therefore I_{pp} = I_{max} - I_{min} \quad \dots (8)$$

Now I_m = Amplitude (peak) of a.c. output (load) current as shown in the Fig. 5.14

$$\therefore I_m = \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2} \quad \dots (9)$$

Hence the r.m.s. values of alternating output voltage and current can be obtained as,

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad \dots (10)$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \dots (11)$$

Hence we can write,

$$V_{rms} = I_{rms} R_L \quad \dots (12)$$

$$\text{i.e. } V_m = I_m R_L \quad \dots (13)$$

The a.c. power delivered by the amplifier to the load can be expressed by using r.m.s values, maximum i.e. peak values and peak to peak values of output voltage and current.

i) Using r.m.s values

$$P_{ac} = V_{rms} I_{rms} \quad \dots (14)$$

$$\text{or } P_{ac} = I_{rms}^2 R_L \quad \dots (15)$$

$$\text{or } P_{ac} = \frac{V_{rms}^2}{R_L} \quad \dots (16)$$

ii) Using peak values

$$P_{ac} = V_{rms} I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$$\therefore P_{ac} = \frac{V_m I_m}{2} \quad \dots (17)$$

$$\text{or } P_{ac} = \frac{I_m^2 R_L}{2} \quad \dots (18)$$

$$\text{or } P_{ac} = \frac{V_m^2}{2 R_L} \quad \dots (19)$$

iii) Using peak to peak values

$$P_{ac} = \frac{V_m I_m}{2} = \left(\frac{V_{pp}}{2} \right) \left(\frac{I_{pp}}{2} \right)$$

$$P_{ac} = \frac{V_{pp} I_{pp}}{8} \quad \dots (20)$$

$$\text{or } P_{ac} = \frac{I_{pp}^2 R_L}{8} \quad \dots (21)$$

$$\text{or } P_{ac} = \frac{V_{pp}^2}{8 R_L} \quad \dots (22)$$

But as $V_{pp} = V_{max} - V_{min}$ and $I_{pp} = I_{max} - I_{min}$; from equation (20), the a.c. power can be expressed as below, for graphical calculations.

$$P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \quad \dots (22)$$

5.7.5 Efficiency

The efficiency of an amplifier represents the amount of a.c. power delivered or transferred to the load, from the d.c. source i.e. accepting the d.c. power input. The generalised expression for an efficiency of an amplifier is,

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 \quad \dots (24)$$

Now for class A operation, we have derived the expressions for P_{ac} and P_{dc} , hence using equations (5) and (23), we can write

$$\% \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100 \quad \dots (25)$$

The efficiency is also called **conversion efficiency** of an amplifier.

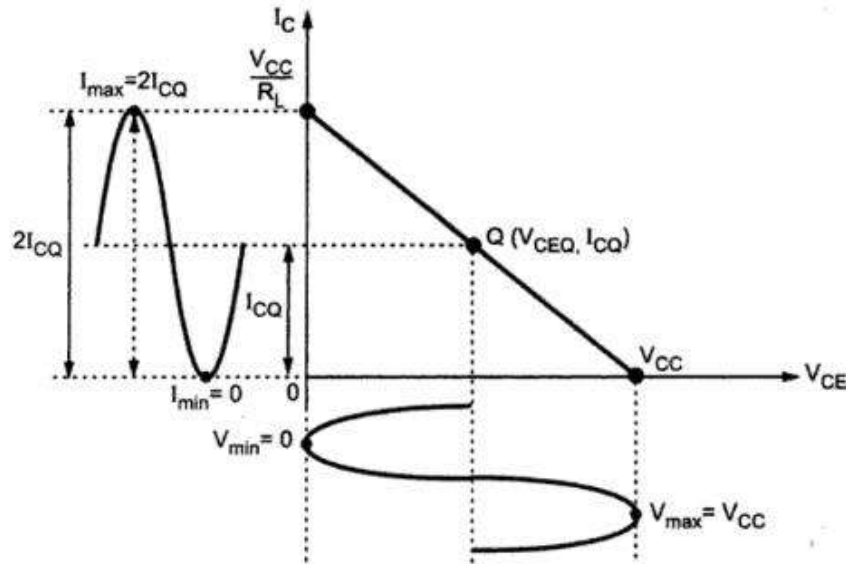
5.7.6 Maximum Efficiency

For maximum efficiency calculation, assume maximum swings of both the output voltage and the output current. The maximum swings are shown in the Fig. 5.15.

From the Fig. 5.15, we can see that the minimum voltage possible is zero and maximum voltage possible is V_{CC} , for a maximum swing. Similarly the minimum current is zero and the maximum current possible is $2 I_{CQ}$, for a maximum swing.

► **Figure 5.15**

Maximum voltage and current swings



$$\left. \begin{array}{l} V_{max} = V_{CC} \text{ and } V_{min} = 0 \\ I_{max} = 2 I_{CQ} \text{ and } I_{min} = 0 \end{array} \right\} \text{ for maximum swing}$$

Using equation (25) we can write,

$$\begin{aligned}\% \eta_{\max} &= \frac{(V_{CC}-0)(2I_{CQ}-0)}{8V_{CC}I_{CQ}} \times 100 = \frac{2V_{CC}I_{CQ}}{8V_{CC}I_{CQ}} \times 100 \\ &= 25\%\end{aligned}$$

Key Point: Thus the maximum efficiency possible in case of directly coupled series fed class A amplifier is just 25%.

This maximum efficiency is an ideal value. For a practical circuit, it is much less than 25%, of the order of 10 to 15%.

Key Point: Very low efficiency is the biggest disadvantage of class A amplifier.

5.7.7 Power Dissipation

As stated earlier, power dissipation in large signal amplifier is also large. The amount of power that must be dissipated by the transistor is the difference between the d.c. power input P_{dc} and the a.c. power delivered to the load P_{ac} .

$$\begin{aligned}P_d &= \text{Power dissipation} \\ \text{i.e. } P_d &= P_{DC} - P_{ac} \quad \dots (26)\end{aligned}$$

The maximum power dissipation occurs when there is zero a.c. input signal. When a.c. input is zero, the a.c. power output is also zero. But transistor operates at quiescent condition, drawing d.c. input power from the supply equal to $V_{CC} I_{CQ}$. This entire power gets dissipated in the form of heat. Thus d.c. power input without a.c. input signal is the maximum power dissipation.

$$(P_d)_{\max} = V_{CC} I_{CQ} \quad \dots (27)$$

Key Point: Thus value of maximum power dissipation decides the maximum power dissipation rating of the transistor to be selected for the amplifier.

5.7.8 Advantages and Disadvantages

The **advantages** of directly coupled class A amplifier can be stated as,

1. The circuit is simple to design and to implement
2. The load is connected directly in the collector circuit hence the output transformer is not necessary. This makes the circuit cheaper.
3. Less number of components required as load is directly coupled.

The **disadvantages** are :

1. The load resistance is directly connected in collector and carries the quiescent collector current. This causes considerable wastage of power.
2. Power dissipation is more. Hence power dissipation arrangements like heat sink are essential.
3. The output impedance is high hence circuit cannot be used for low impedance loads, such as loudspeakers.
4. The efficiency is very poor, due to large power dissipation.

➡ **Example 5.1 :** A series fed class A amplifier shown in Fig. 5.16, operates from D.C. source and applied sinusoidal input signal generates peak base current 9 mA. Calculate :

i) Quiescent current I_{CQ}

ii) Quiescent voltage V_{CEQ}

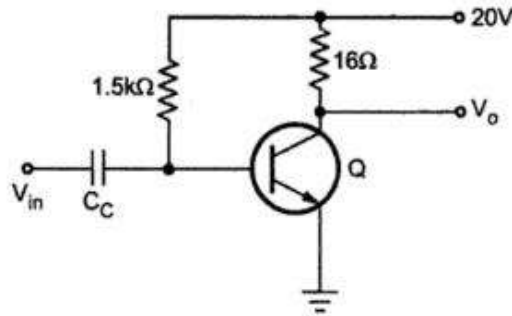
iii) D.C. input power P_{DC}

iv) A.C. output power P_{ac}

v) Efficiency.

Assume $\beta = 50$ and $V_{BE} = 0.7$ V.

► **Figure 5.16**



Solution :

$$\text{i) } I_{CQ} \quad I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{1.5 \times 10^3} = 12.87 \text{ mA}$$

$$I_{CQ} = \beta \times I_{BQ} = 50 \times 12.87 = 643.50 \text{ mA}$$

$$\text{ii) } V_{CEQ} \quad V_{CC} = I_{CQ} R_L + V_{CEQ}$$

$$\therefore V_{CEQ} = V_{CC} - I_{CQ} R_L = 20 - 643.50 \times 10^{-3} \times 16 = 9.70 \text{ volts}$$

$$\text{iii) } P_{DC} \quad P_{DC} = V_{CC} \times I_{CQ} = 20 \times 643.5 \times 10^{-3} = 12.87 \text{ watt}$$

$$\text{iv) } P_{ac} \text{ Peak current } i_b = 9 \text{ mA}$$

$$i_c = \beta i_b = 50 \times 9 = 450 \text{ mA (peak)}$$

$$\therefore i_{c(rms)} = \frac{i_c(\text{peak})}{\sqrt{2}} = \frac{450}{\sqrt{2}} = 318.19 \text{ mA} = I_{rms}$$

$$\therefore P_{ac} = I_{rms}^2 R_L = (318.19 \times 10^{-3})^2 \times 16 = 1.619 \text{ watt.}$$

$$\text{v) Efficiency } \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{1.619}{12.87} \times 100 = 12.58 \%$$

Ans. : $I_{CQ} = 643.5 \text{ mA}$, $V_{CEQ} = 9.7 \text{ V}$, $P_{DC} = 12.87 \text{ W}$, $P_{ac} = 1.619 \text{ W}$, $\eta = 12.58\%$

5.8 Transformer Coupled Class A Amplifier

As stated earlier, for maximum power transfer to the load, the impedance matching is necessary. For loads like loudspeaker, having low impedance values, impedance matching is difficult using directly coupled amplifier circuit. This is because loudspeaker resistance is in the range of 3 to 4 ohms to 16 ohms while the output impedance of series fed directly coupled class A amplifier is very much high. This problem can be eliminated by using a transformer to deliver power to the load.

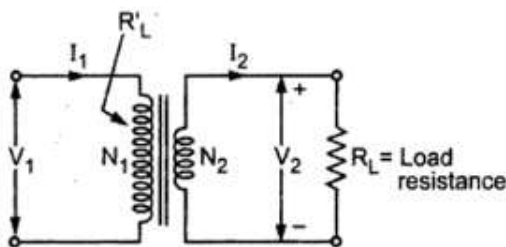
Key Point: The transformer is called an *output transformer* and the amplifier is called *transformer coupled class A amplifier*.

Before studying the operation of the amplifier, let us revise few concepts regarding the transformer.

5.8.1 Properties of Transformer

► **Figure 5.17**

Transformer with load



Consider a transformer as shown in the Fig. 5.17 which is connected to a load of resistance R_L .

While analysing the transformer, it is assumed that the transformer is ideal and there are no losses in the transformer. Similarly the winding resistances are assumed to be zero.

- Let
- N_1 = Number of turns on primary
 - N_2 = Number of turns on secondary
 - V_1 = Voltage applied to primary
 - V_2 = Voltage on secondary
 - I_2 = Primary current

i) Turns Ratio : The ratio of number of turns on secondary to the number of turns on primary is called turns ratio of the transformer denoted by n .

$$\therefore n = \text{Turns ratio} = \frac{N_2}{N_1} \quad \dots (1)$$

Some times it is specified as $\frac{N_2}{N_1} : 1$ or $\frac{N_1}{N_2} : 1$.

ii) Voltage Transformation : The transformer transforms the voltage applied on one side to other side proportional to the turns ratio. The transformer can be step up or step down transformer.

$$\therefore \frac{V_2}{V_1} = \frac{N_2}{N_1} = n \quad \dots (2)$$

In the amplifier analysis, the load impedance is going to be small. And the transformer is to be used for impedance matching. Hence it has to be a step down transformer. Hence

number of turns on primary are more than the secondary and turns ratio is less than unity, for such a step down transformer.

iii) Current Transformation : The current in the secondary winding is inversely proportional to the number of turns of the windings.

$$\therefore \frac{I_2}{I_1} = \frac{N_1}{N_2} = \frac{1}{n} \quad \dots (3)$$

iv) Impedance Transformation : As current and voltage get transformed from primary to secondary, an impedance 'seen' from either side (primary or secondary) also changes.

Now the impedance of the load on secondary is R_L as shown in the Fig. 5.17. The primary and secondary winding resistances are assumed to be zero. This load impedance R_L , gets reflected on the primary side and behaves as if connected in the primary side. Such impedance transferred from secondary to primary is denoted as R'_L .

Now using the equations (2) and (3) and the Fig. 5.17, we can write,

$$R_L = \frac{V_2}{I_2} \text{ and } R'_L = \frac{V_1}{I_1}$$

but $V_1 = \frac{N_1}{N_2} V_2$ and $I_1 = \frac{N_2}{N_1} I_2$

$$\therefore R'_L = \frac{\frac{N_1}{N_2} V_2}{\frac{N_2}{N_1} I_2} = \left(\frac{N_1}{N_2} \right)^2 \times \frac{V_2}{I_2} = \frac{R_L}{\left(\frac{N_2}{N_1} \right)^2} = \frac{R_L}{n^2}$$

$$\therefore R'_L = \frac{R_L}{n^2} = \left(\frac{N_1}{N_2} \right)^2 R_L \quad \dots (4)$$

The R'_L is the **reflected impedance** and is related to the square of the turns ratio of the transformer. Remember that for a step down transformer, the secondary voltage is less than the primary. And high voltage side is always high impedance side. **Hence R'_L is always higher than R_L , for a stepdown transformer.**

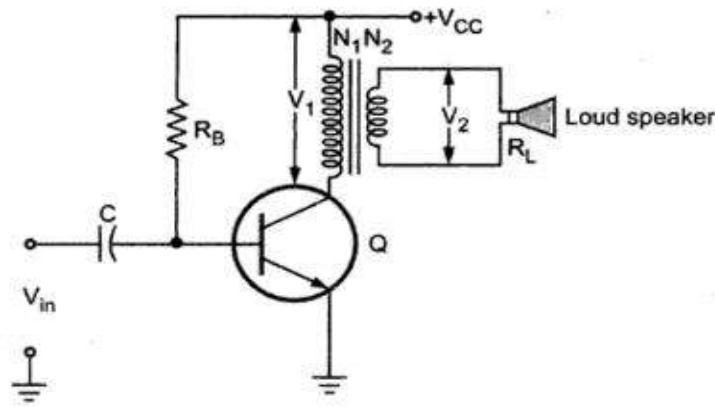
Key Point: In the amplifier analysis, the load is on secondary while the active device, the transistor is on primary. Hence in all the calculations related to the transistor, the reflected load impedance R'_L must be considered rather than actual load impedance R_L .

5.8.2 Circuit Diagram of Transformer Coupled Amplifier

The basic circuit of a transformer coupled amplifier is shown in the Fig. 5.18. The loudspeaker connected to the secondary acts as a load having impedance of R_L ohms.

► **Figure 5.18**

Transformer coupled class A amplifier



The transformer used is a step down transformer with the turns ratio as

$$n = N_2 / N_1$$

5.8.3 D.C. Operation

It is assumed that the winding resistances are zero ohms. Hence for d.c. purposes, the resistance is 0Ω . There is no d.c. voltage drop across the primary winding of the transformer. The slope of the d.c. load line is reciprocal of the d.c. resistance in the collector circuit, which is zero in this case. Hence slope of the d.c. load line is ideally infinite. This tells that the d.c. load line in the ideal condition is a vertically straight line.

Applying Kirchhoff's voltage law to the collector circuit we get,

$$V_{CC} - V_{CE} = 0$$

$$\text{i.e. } V_{CC} = V_{CE}$$

... drop across winding is zero

This is the d.c. bias voltage V_{CEQ} for the transistor.

$$\text{So } V_{CEQ} = V_{CC} \quad \dots (5)$$

Hence the d.c. load line is a vertical straight line passing through a voltage point on the X-axis which is $V_{CEQ} = V_{CC}$.

The intersection of d.c. load line and the base current set by the circuit is the quiescent operating point of the circuit. The corresponding collector current is I_{CQ} .

The d.c. load line is shown in the Fig. 5.19.

5.8.4 D.C Power Input

The d.c. power input is provided by the supply voltage with no signal input, the d.c. current drawn is the collector bias current I_{CQ} .

Hence the d.c. power input is given by,

$$\text{So } P_{DC} = V_{CC} I_{CQ} \quad \dots (6)$$

The expression is same as derived earlier for series fed directly coupled class A amplifier.

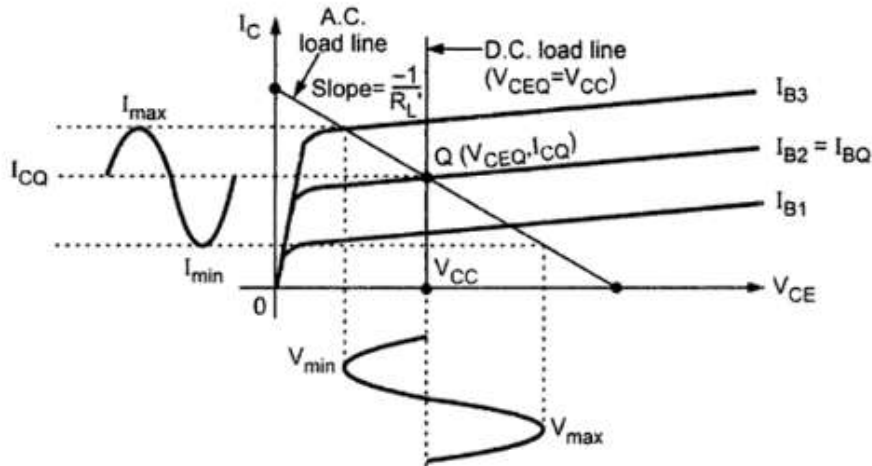
5.8.5 A.C. Operation

For the a.c. analysis, it is necessary to draw an a.c. load line on the output characteristics.

For a.c. purposes, the load on the secondary is the load impedance R_L ohms. And the reflected load on the primary i.e. R'_L can be calculated using the equation (4). The load line drawn with a slope of $\left(\frac{-1}{R'_L}\right)$ and passing through the operating point i.e. quiescent point Q is called a.c. load line. The d.c. and a.c. load lines are shown in the Fig. 5.19.

► **Figure 5.19**

Load lines for transformer coupled class A amplifier



The output current i.e. collector current varies around its quiescent value I_{CQ} , when a.c. input signal is applied to the amplifier. The corresponding output voltage also varies sinusoidally around its quiescent value V_{CEQ} which is V_{CC} in this case.

5.8.6 A.C. Output Power

The a.c. power developed is on the primary side of the transformer. While calculating this power, the primary values of voltage and current and reflected load R'_L must be considered. The a.c. power delivered to the load is on the secondary side of the transformer. While calculating load voltage, load current, load power the secondary voltage, current and the load R_L must be considered.

Let V_{1m} = Magnitude or peak value of primary voltage

V_{1rms} = R.M.S value of primary voltage

I_{1m} = Peak value of primary current

I_{1rms} = R.M.S value of primary current.

Hence the a.c. power developed on the primary is given by,

$$P_{ac} = V_{1rms} I_{1rms} \quad \dots (7)$$

$$P_{ac} = I_{1rms}^2 R'_L \quad \dots (8)$$

$$P_{ac} = \frac{V_{1rms}^2}{R'_L} \quad \dots (9)$$

$$P_{ac} = \frac{V_{1m}}{\sqrt{2}} \cdot \frac{I_{1m}}{\sqrt{2}} = \frac{V_{1m} I_{1m}}{2} \quad \dots (10)$$

$$P_{ac} = \frac{I_{1m}^2 R'_L}{2} \quad \dots (11)$$

$$P_{ac} = \frac{V_{1m}^2}{2 R'_L} \quad \dots (12)$$

Similarly the a.c. power delivered to the load on secondary, also can be calculated, using secondary quantities.

Let V_{2m} = Magnitude or peak value of secondary or load voltage

V_{2rms} = R.M.S value of secondary or load voltage

I_{2m} = Magnitude or peak value of secondary or load current.

I_{2rms} = R.M.S. value of secondary or load current

$$P_{ac} = V_{2rms} I_{2rms} = I_{2rms}^2 R_L = \frac{V_{2rms}^2}{R_L} \quad \dots (13)$$

or

$$P_{ac} = \frac{V_{2m} I_{2m}}{2} = \frac{I_{2m}^2 R_L}{2} = \frac{V_{2m}^2}{2 R_L} \quad \dots (14)$$

Power delivered on primary is same as power delivered to the load on secondary, assuming **ideal transformer**. Primary and Secondary values of voltages and currents are related to each other through the turns ratio of the transformer.

Key Point: In practical circuit, the transformer can not be ideal. Hence the power delivered to the load on the secondary is slightly less than power developed on the primary. In such case, the transformer efficiency must be considered for calculating various parameters on the primary and secondary sides of the transformer.

The slope of the a.c. load line can be expressed in terms of the primary current and the primary voltage.

The slope of the a.c. load line is,

$$= \frac{1}{R'_L} = \frac{I_{1m}}{V_{1m}}$$

... (15)

The generalised expression for a.c. power output represented by the equation (24) in section (5.7), can be used as it is for transformer coupled amplifier. The expression is mentioned again for the convenience of the reader.

$$\therefore P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}$$

... (16)

Key Point: The a.c. power calculated is the power developed across the primary winding of the output transformer. Assuming ideal transformer, the power delivered to the load on secondary, is same as that developed across the primary. If the transformer efficiency is known, the power delivered to the load must be calculated from the power developed on the primary, considering the efficiency of the transformer.

5.8.7 Efficiency

The general expression for the efficiency remains same as that given by equations (24) and (25) in section 5.7.

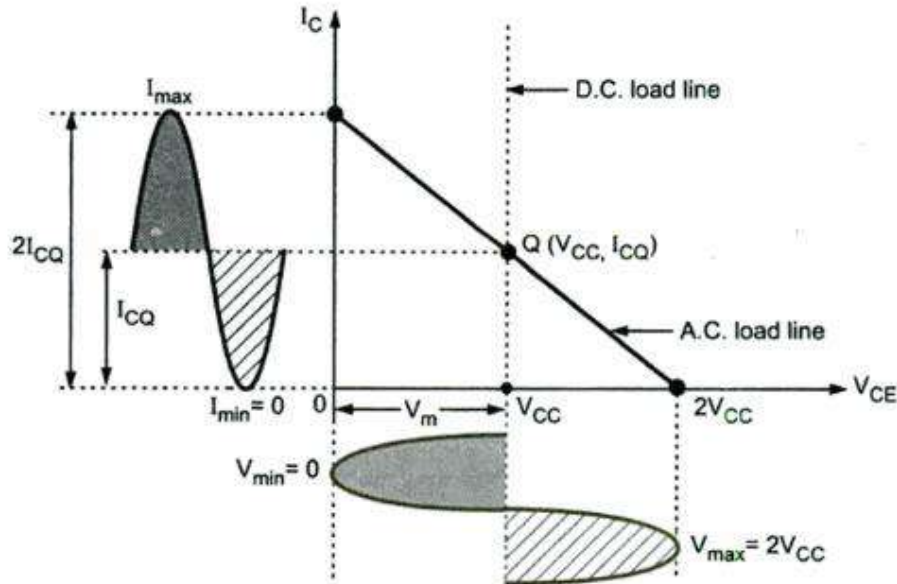
$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100$$

5.8.8 Maximum Efficiency

Assume maximum swings of both the output voltage and output current, to calculate maximum efficiency, as shown in the Fig. 5.20.

► **Figure 5.20**

Maximum voltage and current swings



From the Fig. 5.20, assuming that the Q point is exactly at the centre of the load line, for maximum swing we can write,

$$\left. \begin{array}{l} V_{min} = 0 \text{ and } V_{max} = 2 V_{CC} \\ I_{min} = 0 \text{ and } I_{max} = 2 I_{CQ} \end{array} \right\} \text{ for maximum swing}$$

Using equation (25) of section 5.7,

$$\begin{aligned} \% \eta_{max} &= \frac{(2V_{CC} - 0)(2I_{CQ} - 0)}{8 V_{CC} I_{CQ}} \times 100 \\ &= \frac{4 V_{CC} I_{CQ}}{8 V_{CC} I_{CQ}} \times 100 = 50\% \end{aligned}$$

Key Point: Hence maximum possible theoretical efficiency in case of transformer coupled class A amplifier is 50%.

For practical circuit it is about 30 to 35%, which is still much more than the directly coupled amplifier. For maximum efficiency, the power output is also maximum. For such maximum output power condition, it is seen that

$$\begin{aligned} V_{\min} &= 0 \text{ and } V_{\max} = 2 V_{CC} \\ \text{i.e. } V_{\text{im}} &= \text{peak value of primary voltage} \\ &= \frac{V_{\max} - V_{\min}}{2} = V_{CC} \end{aligned}$$

$$\therefore V_{\text{im}} = V_{CC} \text{ for maximum output power.}$$

Similarly from the maximum output current swing shown in the Fig. 5.20, we can say that the peak value of the output current is magnitude wise equal to the biasing collector current.

$$\therefore I_{\text{im}} = I_{CQ} \text{ magnitude wise for maximum output power.}$$

Hence the equation (15) written for the magnitude of the slope of the a.c. load line can be modified as,

$$R'_L = \frac{V_{\text{im}}}{I_{\text{im}}} = \frac{V_{CC}}{I_{CQ}} \quad \dots (15 \text{ a})$$

Key Point: This expression is applicable only in case of maximum power output condition.

$$(P_{ac})_{\max} = \frac{1}{2} \frac{V_{CC}^2}{R'_L} \quad \dots \text{ as } V_{\text{im}} = V_{CC}$$

5.8.9 Power Dissipation

The power dissipation by the transistor is the difference between the a.c. power output and the d.c. power input. The power dissipated by the transformer is very small due to negligible (d.c.) winding resistances and can be neglected.

$$\therefore P_d = P_{DC} - P_{ac} \quad \dots (16)$$

When the input signal is larger, more power is delivered to the load and less is the power dissipation. But when there is no input signal, the entire d.c. input power gets dissipated in the form of heat, which is the maximum power dissipation.

$$\therefore (P_d)_{\max} = V_{CC} I_{CQ} \quad \dots (17)$$

Thus the class A amplifier dissipates less power when delivers maximum power to the load. While it dissipates maximum power while delivering zero power to the load i.e. when load is removed and there is no a.c. input signal. The maximum power dissipation decides the maximum power dissipation rating for the power transistor to be selected for an amplifier.

5.8.10 Advantages and Disadvantages

The **advantages** of transformer coupled class A amplifier circuit are,

1. The efficiency of the operation is higher than directly coupled amplifier.
2. The d.c. bias current that flows through the load in case of directly coupled amplifier is stopped in case of transformer coupled.
3. The impedance matching required for maximum power transfer is possible.

The **disadvantages** are,

1. Due to the transformer, the circuit becomes bulkier, heavier and costlier compared to directly coupled circuit.
2. The circuit is complicated to design and implement compared to directly coupled circuit.
3. The frequency response of the circuit is poor.

► **Example 5.4 :** The loudspeaker of $8\ \Omega$ is connected to the secondary of the output transformer of a class A amplifier circuit. The quiescent collector current is 140 mA . The turns ratio of the transformer is $3:1$. The collector supply voltage is 10V . If a.c. power delivered to the loudspeaker is 0.48 W , assuming ideal transformer, calculate :

1. A.C. power developed across primary
2. R.M.S. value of load voltage
3. R.M.S. value of primary voltage
4. R.M.S. value of load current
5. R.M.S. value of primary current
6. The D.C. power input
7. The efficiency
8. The power dissipation

Solution : $R_L = 8\ \Omega$, $I_{CQ} = 140\text{ mA}$, $V_{CC} = 10\text{ V}$

$$P_{ac} = 0.48\text{ W}$$

The turns ratio are specified as $\frac{N_1}{N_2} : 1$ i.e. $3:1$

$$\therefore \frac{N_1}{N_2} = 3$$

$$\therefore n = \frac{N_2}{N_1} = \frac{1}{3} = 0.3333$$

$$\begin{aligned}\therefore R'_L &= \frac{R_L}{n^2} \\ &= \frac{8}{(0.333)^2} = 72\ \Omega\end{aligned}$$

1. As the transformer is ideal, whatever is the power delivered to the load, same is the power developed across primary.

$$\therefore P_{ac} (\text{across primary}) = 0.48\text{ W}$$

2. Using equation (9),

$$\text{we get, } P_{ac} = \frac{V_{1rms}^2}{R'_L}$$

$$\therefore 0.48 = \frac{V_{1rms}^2}{72}$$

$$V_{1rms}^2 = 34.56$$

$$\therefore V_{1rms} = 5.8787 \text{ V on primary.}$$

But r.m.s. value of the load voltage is V_{2rms}

$$\text{So } \frac{(V_1)_{rms}}{(V_2)_{rms}} = \frac{N_1}{N_2} = \frac{3}{1}$$

$$\therefore (V_2)_{rms} = \frac{(V_1)_{rms}}{3} = \frac{5.8787}{3} = 1.9595 \text{ V}$$

This is the r.m.s. value of the load voltage.

3. The r.m.s value of the primary voltage is $(V_1)_{rms}$ as calculated above.

$$\therefore (V_1)_{rms} = 5.8787 \text{ V}$$

4. The power delivered to the load $= I_{2rms}^2 \times R_L$... refer eq. 13.

$$\therefore 0.48 = I_{2rms}^2 \times 8$$

$$\therefore I_{2rms}^2 = 0.06$$

$$\therefore I_{2rms} = 0.2449 \text{ A}$$

This is the r.m.s value of the load current as the resistance value used is R_L and not R'_L .

5. The r.m.s values of primary and secondary are related through the transformation ratio.

$$\therefore \frac{(I_1)_{rms}}{(I_2)_{rms}} = \frac{N_2}{N_1} = n = 0.333$$

$$\therefore (I_1)_{rms} = (I_2)_{rms} \times n = 0.2449 \times 0.333 = 0.0816 \text{ A} = 81.64 \text{ mA.}$$

6. The d.c. power input is,

$$P_{DC} = V_{CC} I_{CQ} = 10 \times 140 \times 10^{-3} = 1.4 \text{ W}$$

$$7. \quad \% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{0.48}{1.4} \times 100 = 34.28\%$$

$$8. \quad P_d = P_{DC} - P_{ac} = 1.4 - 0.48 = 0.92 \text{ W}$$

This is the power dissipation. ■

5.10 Analysis of Class B Amplifiers

As stated earlier, for class B operation, the quiescent operating point is located on the X-axis itself. Due to this collector current flows only for a half cycle for a full cycle of the input signal. Hence the output signal is distorted. To get a full cycle across the load, a pair of transistors is used in class-B operation. The two transistors conduct in alternate half cycles of the input signal and a full cycle across the load is obtained. The two transistors are identical in characteristics and called matched transistors.

Depending upon the types of the two transistors whether p-n-p or n-p-n, the two circuit configurations of class B amplifier are possible. These are,

1. When both the transistors are of same type i.e. either n-p-n or p-n-p then the circuit is called **push-pull class B A.F. power amplifier circuit**.
2. When the two transistors form a complementary pair i.e. one n-p-n and other p-n-p then the circuit is called **complementary symmetry class B A.F. power amplifier circuit**. Let us analyse these two circuits of class B amplifiers in detail.

5.11 Push Pull Class B Amplifier

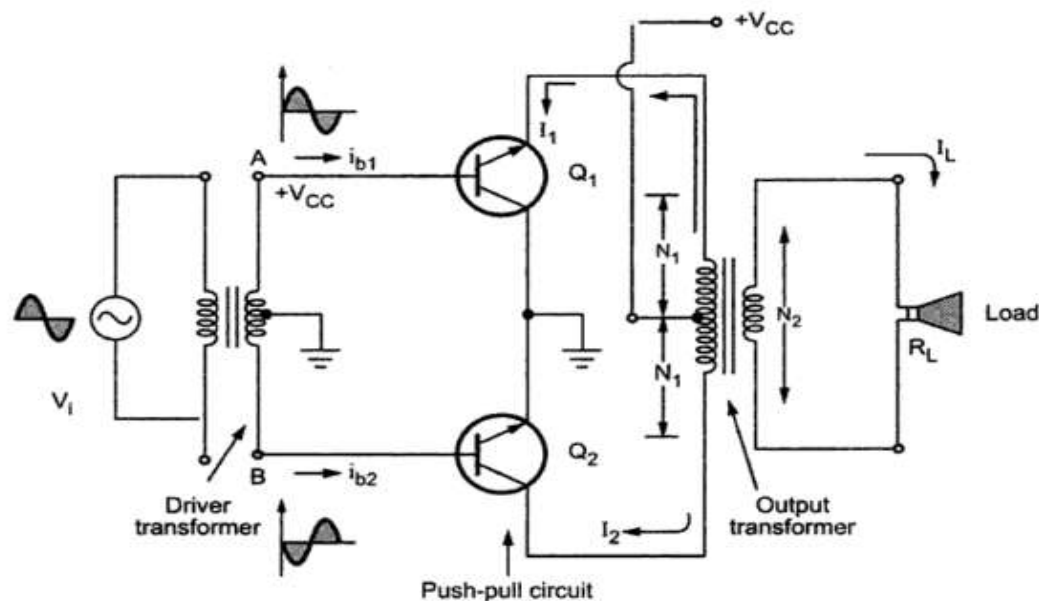
The push pull circuit requires two transformers, one as input transformer called **driver transformer** and the other to connect the load called **output transformer**. The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers. The push pull class B amplifier circuit is shown in the Fig. 5.25.

In the circuit, both Q_1 and Q_2 transistors are of n-p-n type. The circuit can use both Q_1 and Q_2 of p-n-p type. In such a case, the only change is that the supply voltage must be $-V_{CC}$, the basic circuit remains the same. Generally the circuit using n-p-n transistors is used. Both the transistors are in common emitter configuration.

The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer. The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage $+V_{CC}$.

► **Figure 5.25**

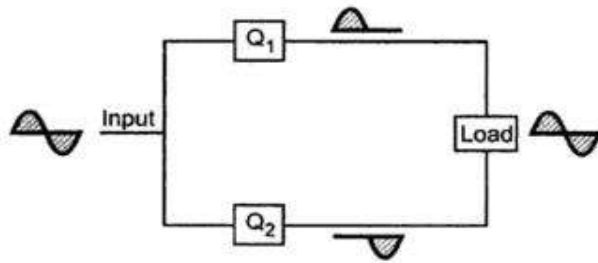
Push pull class B amplifier



With respect to the centre tap, for a positive half cycle of input signal, the point A shown on the secondary of the driver transformer will be positive. While the point B will be negative. Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity. Hence the input signals applied to the base of the transistors Q_1 and Q_2 will be 180° out of phase.

► **Figure 5.26**

Basic push pull operation



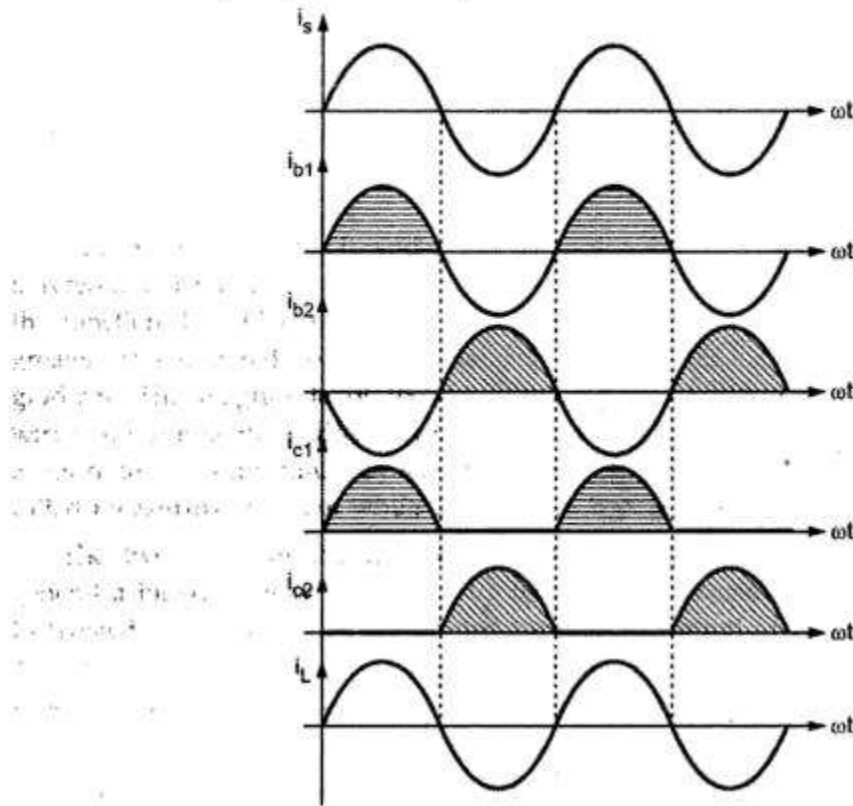
The transistor Q_1 conducts for the positive half cycle of the input producing positive half cycle across the load. While the transistor Q_2 conducts for the negative half cycle of the input producing negative half cycle across the load. Thus across the load, we get a full cycle for a full input cycle. The basic push pull operation is shown in the Fig. 5.26.

When point A is positive, the transistor Q_1 gets driven into an active region while the transistor Q_2 is in cut off region. While when point A is negative, the point B is positive, hence the transistor Q_2 gets driven into an active region while the transistor Q_1 is in cut off region.

The waveforms of the input current, base currents, collector currents and the load current are shown in the Fig. 5.27.

► **Figure 5.27**

Waveforms for push pull class B amplifier



Key Point: For the output transformer, the number of the turns of each half of the primary is N_1 while the number of the turns on the secondary is N_2 . Hence the total number of primary turns is $2N_1$. So turns ratio of the output transformer is specified as $2N_1 : N_2$.

5.11.1 D.C.Operation

The d.c. biasing point i.e. Q point is adjusted on the X-axis such that $V_{CEQ} = V_{CC}$ and I_{CEQ} is zero. Hence the co-ordinates of the Q point are $(V_{CC}, 0)$. There is no d.c. base bias voltage.

5.11.2 D.C.Power Input

Each transistor output is in the form of half rectified waveform. Hence if I_m is the peak value of the output current of each transistor, the d.c. or average value is $\frac{I_m}{\pi}$, due to half rectified waveform. The two currents, drawn by the two transistors, form the d.c. supply are in the same direction. Hence the total d.c. or average current drawn from the supply is the algebraic sum of the individual average current drawn by each transistor.

$$\therefore I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2 I_m}{\pi} \quad \dots (1)$$

The total d.c. power input is given by,

$$P_{DC} = V_{CC} \times I_{dc}$$

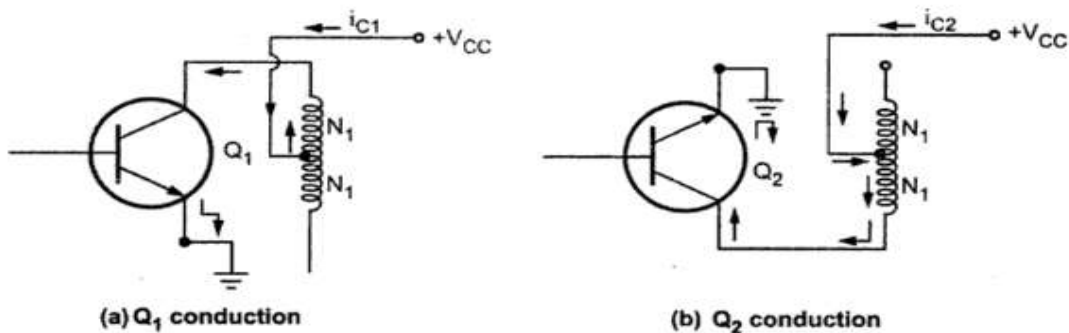
$$\therefore P_{DC} = \frac{2}{\pi} V_{CC} I_m \quad \dots (2)$$

5.11.3 A.C.Operation

When the a.c. signal is applied to the driver transformer, for positive half cycle Q_1 conducts. The path of the current drawn by the Q_1 is shown in the Fig. 5.28.

For the negative half cycle Q_2 conducts. The path of the current drawn by the Q_2 is shown in the Fig. 5.28 (b).

► **Figure 5.28**



It can be seen that when Q_1 conducts, lower half of the primary of the output transformer does not carry any current. Hence only N_1 number of turns carry the current. While when Q_2 conducts, upper half of the primary does not carry any current. Hence again only N_1 number of turns carry the current. Hence the reflected load on the primary can be written as,

$$\therefore \boxed{R'_L = \frac{R_L}{n^2}} \quad \dots (3)$$

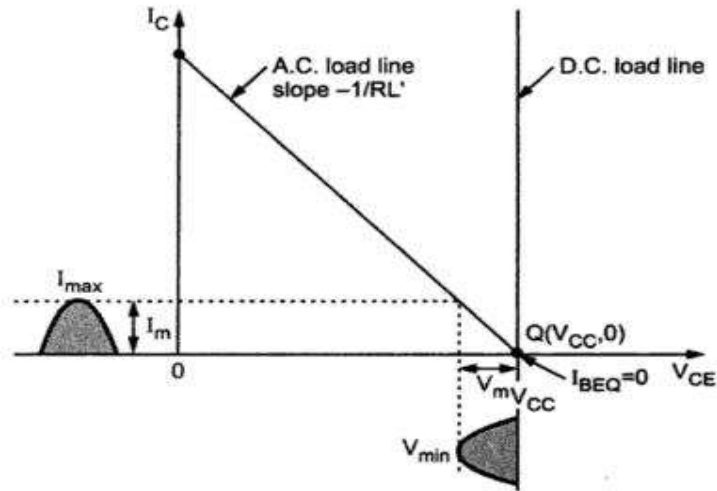
where $n = \frac{N_2}{N_1}$

It is important to note that the step down turns ratio is $2N_1 : N_2$ but while calculating the reflected load, the ratio n becomes N_2/N_1 . So each transistor shares equal load which is the reflected load R'_L given by the equation (3).

The slope of the a.c. load line is $-1/R'_L$ while the d.c. load line is the vertical line passing through the operating point Q on the x-axis. The load lines are shown in the Fig. 5.29.

► **Figure 5.29**

Load lines for push pull class B amplifier



The slope of the a.c. load line (magnitude of slope) can be represented in terms of V_m and I_m as,

$$\frac{1}{R'_L} = \frac{I_m}{V_m}$$

$$\therefore \boxed{R'_L = \frac{V_m}{I_m}} \quad \dots (4)$$

where I_m = Peak value of the collector current

5.11.4 A.C. Power Output

As I_m and V_m are the peak values of the output current and the output voltage respectively, then

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

and $I_{rms} = \frac{I_m}{\sqrt{2}}$

Hence the a.c. power output is expressed as,

$$P_{ac} = V_{rms} I_{rms} = I_{rms}^2 R'_L = \frac{V_{rms}^2}{R'_L} \quad \dots (5)$$

While using peak values it can be expressed as,

$$\therefore \boxed{P_{ac} = \frac{V_m I_m}{2} = \frac{I_m^2 R'_L}{2} = \frac{V_m^2}{2R'_L}} \quad \dots (6)$$

5.11.5 Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation.

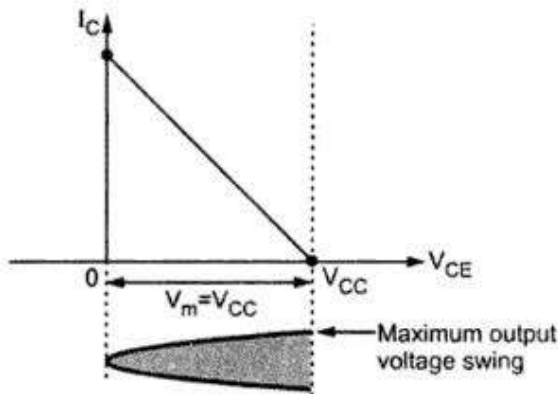
$$\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{\left(\frac{V_m I_m}{2} \right)}{\frac{2}{\pi} V_{CC} I_m} \times 100$$

$$\therefore \boxed{\% \eta = \frac{\pi}{4} \frac{V_m}{V_{CC}} \times 100} \quad \dots (7)$$

5.11.6 Maximum Efficiency

From the equation (7), it is clear that as the peak value of the collector voltage V_m increases, the efficiency increases. The maximum value of V_m possible is equal to V_{CC} as shown in the Fig. 5.30.

► **Figure 5.30**



$$\boxed{V_m = V_{CC} \text{ for maximum } \eta}$$

$$\therefore \% \eta_{\max} = \frac{\pi}{4} \times \frac{V_{CC}}{V_{CC}} \times 100 = 78.5 \%$$

Key Point: Thus the maximum possible theoretical efficiency in case of push pull class B amplifier is 78.5% which is much higher than the transformer coupled class A amplifier.

For practical circuits it is upto 65 to 70%.

Key Point: Practically the collector-emitter voltage of transistor is neglected as small. But if $V_{CE(\min)}$ is given then maximum collector voltage V_m reduces by $V_{CE(\min)}$ and becomes $V_m = V_{CC} - V_{CE(\min)}$ under maximum efficiency condition.

5.11.7 Power Dissipation

The power dissipation by both the transistors is the difference between a.c. power output and d.c. power input.

$$\therefore P_d = P_{DC} - P_{ac} = \frac{2}{\pi} V_{CC} I_m - \frac{V_m I_m}{2}$$

$$\therefore P_d = \frac{2}{\pi} V_{CC} \frac{V_m}{R'_L} - \frac{V_m^2}{2R'_L} \quad \dots (8)$$

Let us find out the condition for maximum power dissipation. In case of class A amplifier, it is maximum when no input signal is there. But in class B operation, when the input signal is zero, $V_m = 0$ hence the power dissipation is zero and not the maximum.

Maximum power dissipation : The condition for maximum power dissipation can be obtained by differentiating the equation (8) with respect to V_m and equating it to zero.

$$\therefore \frac{d P_d}{d V_m} = \frac{2}{\pi} \frac{V_{CC}}{R'_L} - \frac{2V_m}{2R'_L} = 0$$

$$\therefore \frac{2}{\pi} \frac{V_{CC}}{R'_L} = \frac{V_m}{R'_L}$$

$$\boxed{V_m = \frac{2}{\pi} V_{CC}} \quad \dots \text{ For maximum power dissipation} \quad \dots (9)$$

This is the condition for maximum power dissipation. Hence the maximum power dissipation is,

$$\begin{aligned} (P_d)_{\max} &= \frac{2}{\pi} V_{CC} \times \frac{2}{\pi} \frac{V_{CC}}{R'_L} - \frac{4}{\pi^2} \frac{V_{CC}^2}{2 R'_L} \\ &= \frac{4}{\pi^2} \frac{V_{CC}^2}{R'_L} - \frac{2}{\pi^2} \frac{V_{CC}^2}{R'_L} \end{aligned}$$

$$\therefore \boxed{(P_d)_{\max} = \frac{2}{\pi^2} \frac{V_{CC}^2}{R'_L}} \quad \dots (10)$$

Key Point : For maximum efficiency, $V_m = V_{CC}$ hence the power dissipation is not maximum when the efficiency is maximum. And when power dissipation is maximum, efficiency is not maximum. So maximum efficiency and maximum power dissipation do not occur simultaneously, in case of class B amplifiers.

$$\text{Now } P_{ac} = \frac{V_m^2}{2 R'_L}$$

and $V_m = V_{CC}$ is the maximum condition.

$$\text{Hence } (P_{ac})_{\max} = \frac{V_{CC}^2}{2 R'_L} \quad \dots (11)$$

$$\text{Now } (P_d)_{\max} = \frac{2V_{CC}^2}{\pi^2 R'_L} = \frac{4}{\pi^2} \left(\frac{V_{CC}^2}{2 R'_L} \right)$$

$$\therefore (P_d)_{\max} = \frac{4}{\pi^2} (P_{ac})_{\max} \quad \dots (12)$$

This much power is dissipated by both the transistors hence the maximum power dissipation per transistor is $(P_d)_{\max} / 2$.

$$\therefore (P_d)_{\max} \text{ per transistor} = \frac{\frac{4}{\pi^2} (P_{ac})_{\max}}{2}$$

$$\therefore (P_d)_{\max} \text{ per transistor} = \frac{2}{\pi^2} (P_{ac})_{\max} \quad \dots (13)$$

This is the **maximum power dissipation rating** of each transistor. For example, if 10 W maximum power is to be supplied to the load, then power dissipation rating of each transistor should be $\frac{2}{\pi^2} \times 10$ i.e. 2.02 W.

5.11.8 Harmonic Distortion

Let the base input currents are sinusoidal in nature and given by,

$$i_{b1} = I_{Bm} \cos \omega t \text{ and } i_{b2} = -I_{Bm} \cos \omega t$$

The negative sign indicates that both are 180° out of phase.

Due to nonlinear dynamic characteristics, the collector current of the two transistors can be expressed in terms of harmonic components as,

$$i_{c1} = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \dots \quad \dots (14)$$

$$\text{Now } i_{b1} = -I_{Bm} \cos \omega t = I_{Bm} \cos (\omega t + \pi)$$

Hence the collector current for the second transistor can be obtained by replacing ωt by $\omega t + \pi$ in the expression for i_{c1} .

$$\begin{aligned} \therefore i_{c2} &= I_{CQ} + B_0 + B_1 \cos (\omega t + \pi) + B_2 \cos 2(\omega t + \pi) + \dots \\ &= I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \dots \end{aligned} \quad \dots (15)$$

Now the load current is the difference between the two. This is because, in the primary of the transformer the two currents are in opposite direction.

$$\begin{aligned} \therefore i_L &= i_{c1} - i_{c2} \\ &= (I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \dots) \\ &\quad - (I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \dots) \\ \therefore i_L &= 2 B_1 \cos \omega t + 2 B_3 \cos 3\omega t + \dots \end{aligned} \quad \dots (16)$$

It can be seen that the **even harmonic components** 2nd, 4th, 6th and so on, get **eliminated**. Similarly the **d.c. component** also gets **eliminated**. Hence the total distortion is less and as d.c. component flowing is zero, there is no possibility of d.c. saturation of the core. Hence the percentage harmonic distortion is only due to odd harmonics given by,

$$\% D_3 = \frac{|B_3|}{|B_1|} \times 100, \quad \% D_5 = \frac{|B_5|}{|B_1|} \times 100 \quad \dots$$

Hence the total harmonic distortion is,

$$\% D = \sqrt{D_3^2 + D_5^2 + D_7^2 + \dots} \times 100 \quad \dots (17)$$

This is based on the assumption that the two transistors are exactly matched. Otherwise even harmonics may be present in the output signal.

5.11.9 Advantages and Disadvantages

The advantages of push pull class B operation are :

1. The efficiency is much higher than the class A operation.
2. When there is no input signal, the power dissipation is zero.
3. The even harmonics get cancelled. This reduces the harmonic distortion.
4. As the d.c. current components flow in opposite direction through the primary winding, there is no possibility of d.c. saturation of the core.
5. Ripples present in supply voltage also get eliminated.
6. Due to the transformer, impedance matching is possible.

The disadvantages of the circuit are :

1. Two center tap transformers are necessary.
2. The transformers, make the circuit bulky and hence costlier.
3. Frequency response is poor.

► **Example 5.9** A class B, push pull amplifier drives a load of 16Ω , connected to the secondary of the ideal transformer. The supply voltage is 25 V. If the number of turns on the primary is 200 and the number of turns on the secondary is 50, calculate maximum power output, d.c. power input, efficiency and maximum power dissipation per transistor.

Solution : $R_L = 16 \Omega$ $V_{CC} = 25 \text{ V}$

$$\text{Now } 2N_1 = 200 \quad N_2 = 50$$

$$\therefore N_1 = 100$$

$$\therefore n = \frac{N_2}{N_1} = \frac{50}{100} = 0.5$$

$$\begin{aligned} \therefore R'_L &= \frac{R_L}{n^2} = \frac{16}{(0.5)^2} \\ &= 64 \Omega \end{aligned}$$

For maximum power output, $V_m = V_{CC}$

$$\begin{aligned} \text{i) } (P_{ac})_{\max} &= \frac{1}{2} \frac{V_{CC}^2}{R'_L} = \frac{1}{2} \times \frac{(25)^2}{64} \\ &= 4.8828 \text{ W} \end{aligned}$$

$$\text{ii) } P_{dc} = \frac{2}{\pi} V_{CC} I_m$$

$$\text{Now } \frac{V_m}{I_m} = R'_L$$

$$\text{and } V_m = V_{CC}$$

... refer equation (4)

$$\therefore I_m = \frac{V_{CC}}{R'_L} = \frac{25}{64} = 0.3906 \text{ A}$$

$$\begin{aligned} \therefore P_{DC} &= \frac{2}{\pi} \times 25 \times 0.3906 \\ &= 6.2169 \text{ W} \end{aligned}$$

$$\begin{aligned} \text{iii) } \% \eta &= \frac{P_{ac}}{P_{DC}} \times 100 = \frac{4.8828}{6.2169} \times 100 \\ &= 78.5\% \end{aligned}$$

$$\begin{aligned}
 \text{iv) } (P_d)_{\max} &= \frac{2}{\pi^2} \times (P_{ac})_{\max} \text{ for each transistor} \\
 &= \frac{2}{\pi^2} \times 4.8828 \\
 &= 0.9894 \text{ W} = 1 \text{ W}
 \end{aligned}$$

5.12 Complementary Symmetry Class B Amplifier

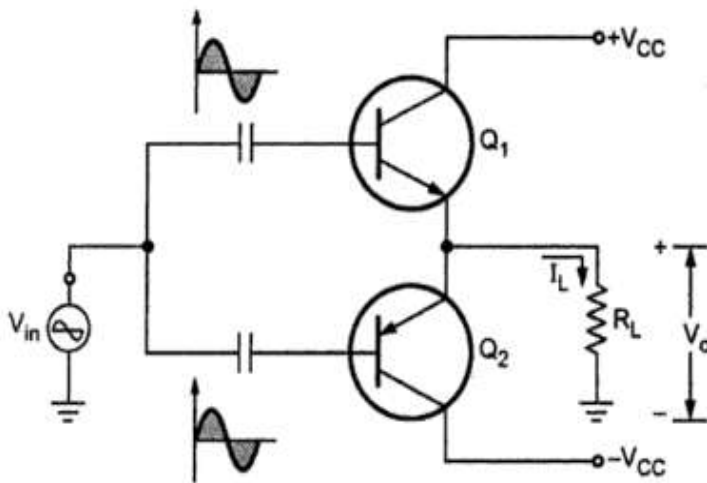
As stated earlier, instead of using same type of transistors (n-p-n or p-n-p), one n-p-n and other p-n-p is used, the amplifier circuit is called as complementary symmetry class B amplifier. This circuit is transformer less circuit. But with common emitter configuration, it becomes difficult to match the output impedance for maximum power transfer without an output transformers. Hence the matched pair of complementary transistors are used in common collector (emitter follower) configuration, in this circuit.

Key Point: This is because common collector configuration has lowest output impedance and hence the impedance matching is possible.

In addition, voltage feedback can be used to reduce the output impedance for matching.

► **Figure 5.32**

Complementary symmetry class B amplifier



The basic circuit of complementary symmetry class-B amplifier is shown in the Fig. 5.32.

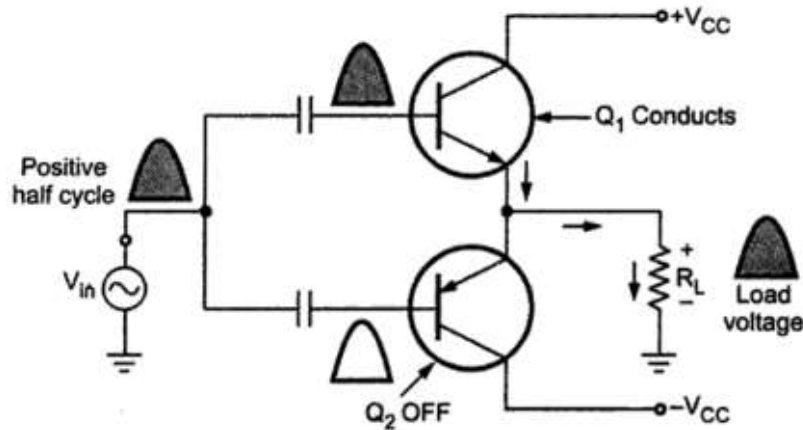
The circuit is driven from a dual supply of $\pm V_{CC}$. The transistor Q_1 is n-p-n while Q_2 is of p-n-p type.

In the positive half cycle of the input signal, the transistor Q_1 gets driven into active region and starts conducting. The same signal gets applied to the base of the Q_2

but as it is of complementary type, remains in off condition, during positive half cycle. This results into positive half cycle across the load R_L . This is shown in the Fig. 5.33.

► **Figure 5.33**

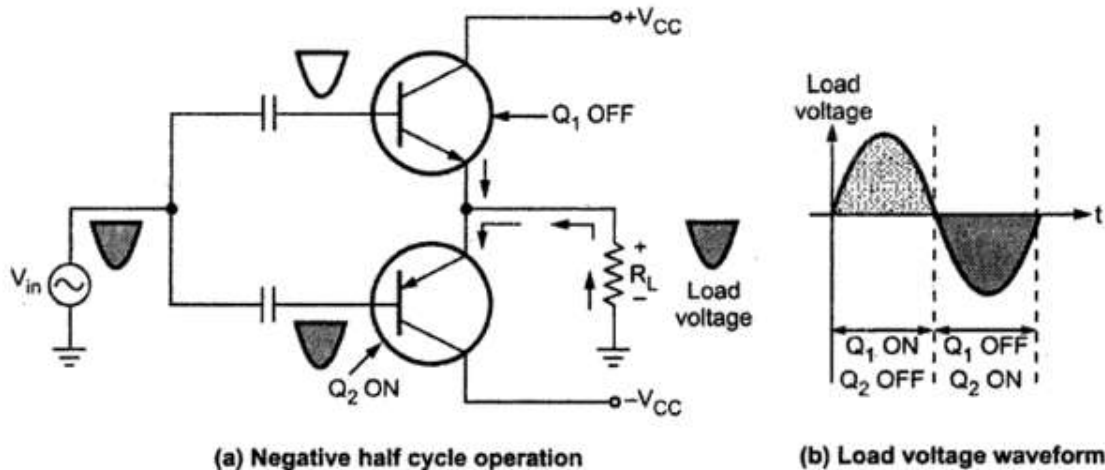
Positive half cycle operation



During the negative half cycle of the signal, the transistor Q_2 being p-n-p gets biased into conduction. While the transistor Q_1 gets driven into cut off region. Hence only Q_2 conducts during negative half cycle of the input, producing negative half cycle across the load R_L , as shown in the Fig. 5.34 (a).

Thus for a complete cycle of input, a complete cycle of output signal is developed across the load as shown in the Fig. 5.34 (b)

► **Figure 5.34**



5.12.1 Mathematical Analysis

All the results derived for push pull transformer coupled class B amplifier are applicable to the complementary class B amplifier. The **only change is that as the output transformer is not present, hence in the expressions, R_L value must be used as it is, instead of R'_L .**

5.12.2 Advantages and Disadvantages

The advantages are :

1. As the circuit is transformerless, its weight, size and cost are less.
2. Due to common collector configuration, impedance matching is possible.
3. The frequency response improves, due to transformerless class B amplifier circuit.

The disadvantages are :

1. The circuit needs two separate voltage supplies.
2. The output is distorted to cross-over distortion.

Key Point: While solving the problems on class B large signal amplifiers, given power is to be assumed maximum unless and otherwise specified and use

$$(P_{ac})_{\max} = \frac{1}{2} \frac{V_{CC}^2}{R_L} \text{ or } \frac{1}{2} \frac{V_{CC}^2}{R_L} \text{ depending upon type of the circuit.}$$

If V_{in} is given then as common collector circuit has unity gain, $V_{out} = V_{in}$ and then voltage across R_L is same as V_{in} . The peak value of V_{in} is V_m and $V_m \neq V_{CC}$ in such a case.

If supply given is dual such as $V_{CC} = \pm 12 \text{ V}$, $\pm 20 \text{ V}$ etc. , it is dual supply version.

But if supply given is $V_{CC} = 12 \text{ V}$, 20 V then it is single supply version and in such a case use $V_{CC} = \frac{1}{2} (\text{given} + V_{CC})$ i.e. $\frac{12}{2} = 6 \text{ V}$, $\frac{20}{2} = 10 \text{ V}$ etc. The single supply version is discussed in the section 5.16.

5.13 Comparison of Push Pull and Complementary Symmetry Circuits

► Table 5.2

	Push Pull Class B	Complementary Symmetry Class B
1.	Both the transistors are similar either pnp or npn.	Transistors are complementary type i.e. one npn other pnp.
2.	The transformer is used to connect the load as well as input.	The circuit is transformerless.
3.	The impedance matching is possible due to the output transformer.	The impedance matching is possible due to common collector circuit.
4.	Frequency response is poor.	Frequency response is improved.
5.	Due to transformers, the circuit is bulky, costly and heavier.	As transformerless, the circuit is not bulky and costly.
6.	Dual power supply is not required.	Dual power supply is required.
7.	Efficiency is higher than class A.	The efficiency is higher than the push pull.

5.14 Cross-Over Distortion

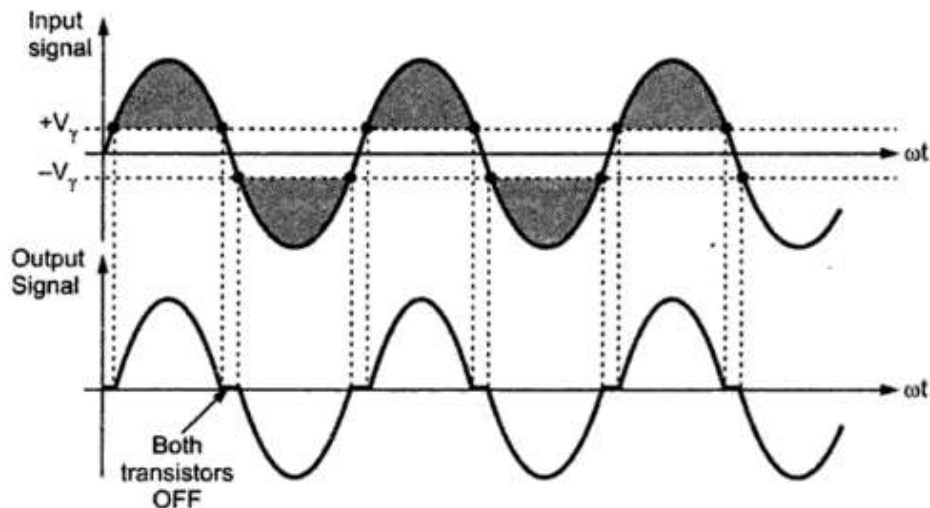
For a transistor to be in active region the base emitter junction must be forward biased. The junction cannot be made forward biased till the voltage applied becomes greater than cut-in voltage (V_γ) of the junction, which is generally 0.7 V for silicon and 0.2V for germanium transistors. Hence as long as the magnitude of the input signal is less than the cut in voltage of the base emitter junction, the collector current remain zero and transistor remains in cut-off region,

Hence there is a period between the crossing of the half cycles of the input signal, for which none of the transistors is active and the output is zero. Hence the nature of the output signal gets distorted and no longer remains same as that of input. Such a distorted output wave form due to cut-in voltage is shown in the Fig. 5.36.

Such a distortion in the output signal is called a **cross-over distortion**. Due to cross-over distortion each transistor conducts for less than a half cycle rather than the complete half cycle. The part of the input cycles for which the two transistors conduct alternately is shown shaded in the Fig. 5.36. The cross-over distortion is common in both the types of class B amplifiers.

► **Figure 5.36**

Cross-over distortion



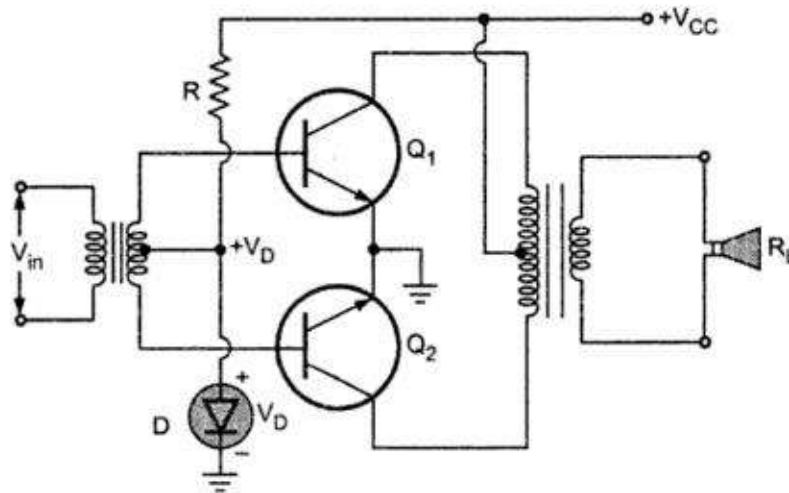
5.15 Elimination of Cross-Over Distortion

To eliminate the cross-over distortion some modifications are necessary, in the basic circuits of the class B amplifiers. The basic reason for the cross over distortion is the cut in voltage of the transistor junction. To overcome this cut-in voltage, a small forward biased is applied to the transistors. Let us see the practical circuits used to apply such forward biased, in the two types of class B amplifiers.

5.15.1 Push Pull Class B Amplifier

► **Figure 5.37**

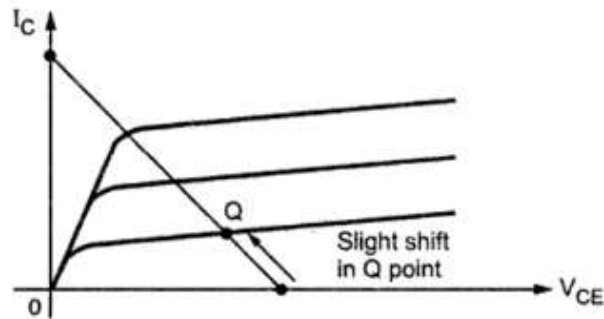
Use of Diode



The forward biased across the base-emitter junction of each transistor is provided by using a diode as shown in the Fig. 5.37.

The drop across the diode D is equal to the cut-in voltage of the base-emitter junction of the transistor. Hence both the transistors conduct for full half cycle, eliminating the cross-over distortion.

► **Figure 5.38**



Due to the forward biased provided to eliminate the cross over distortion, the Q point shifts upwards on the load line as shown in the Fig. 5.38. Hence the operation of the amplifier no longer remains class-B but becomes class AB operation.

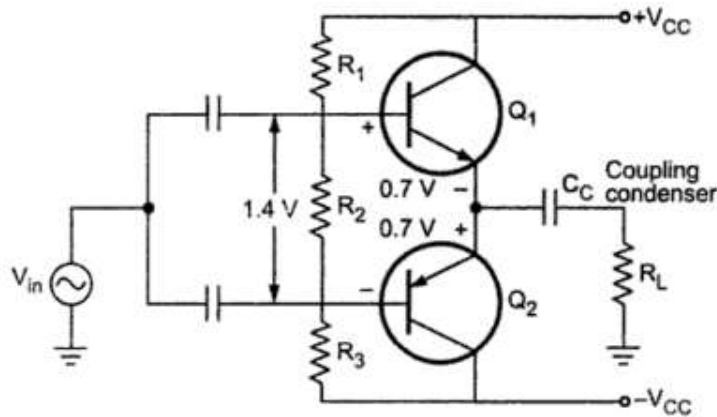
But as the amplifier handles the large signals in the range of volts, compared to these signals the shift in Q point is negligibly small.

Key Point: For all the practical purposes, the operation is treated as class B operation and all the expression derived are applicable to these modified circuits.

5.15.2 Complementary Symmetry Class B Amplifier

► **Figure 5.39**

Use of potential divider



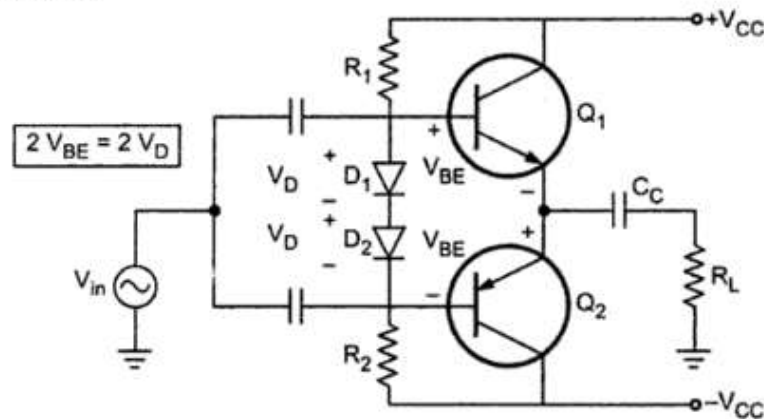
In push pull, transformer coupled type, the drop across forward biased one diode is sufficient, to provide necessary cut in voltage. But in case of complementary symmetry circuit, base emitter junctions of both Q_1 and Q_2 , are required to provide a fixed bias. Hence for silicon transistors a fixed bias of 0.7

$+ 0.7 = 1.4\text{ V}$ is required. This can be achieved by using a potential divider arrangement as shown in the Fig. 5.39.

But in this circuit, the fixed bias provided is fixed equal to say 1.4 V . While the junction cut-in voltage changes with respect to the temperature. Hence there is still possibility of a distortion when there is temperature change. Hence instead of R_2 , the two diodes can be used to provide the required fixed bias. As the temperature changes, along with the junction characteristics, the diode characteristics get changed and maintain the necessary biasing required to overcome the cross-over distortion when there is temperature change. The arrangement of the circuit with the two diodes is shown in the Fig. 5.40.

► **Figure 5.40**

Use of pair of diodes



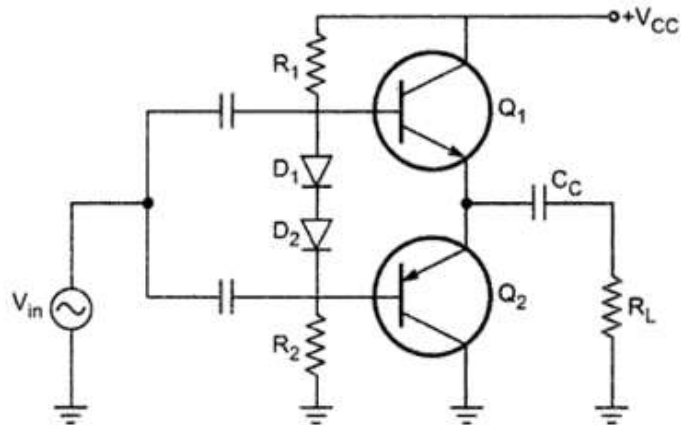
5.16 Complementary Symmetry Single Supply Version

The main disadvantage as seen earlier of complementary amplifier is the use of dual supply. But in practice the circuit can be modified by grounding $-V_{CC}$ terminal. The

resulting circuit is called single supply version of complementary symmetry class B amplifier as shown in the Fig. 5.41.

► **Figure 5.41**

Single supply version of complementary symmetry class B amplifier



Key Point: All the expression derived for dual supply version are still applicable to single supply version. Only change required is that the value of V_{CC} must be taken as $V_{CC}/2$, while calculating the various parameters of the circuit. ■

TUNED AMPLIFIERS

3.1 Introduction:

To amplify the selective range of frequencies, the resistive load R_C is replaced by a tuned circuit. The tuned circuit is capable of amplifying a signal over a narrow band of frequencies centered at f_r . The amplifiers with such a tuned circuit as a load are known as tuned amplifier.

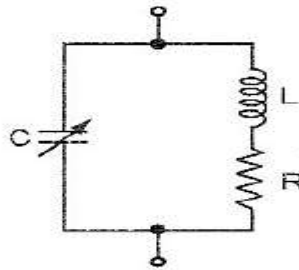


Fig. 3.1 Tuned circuit

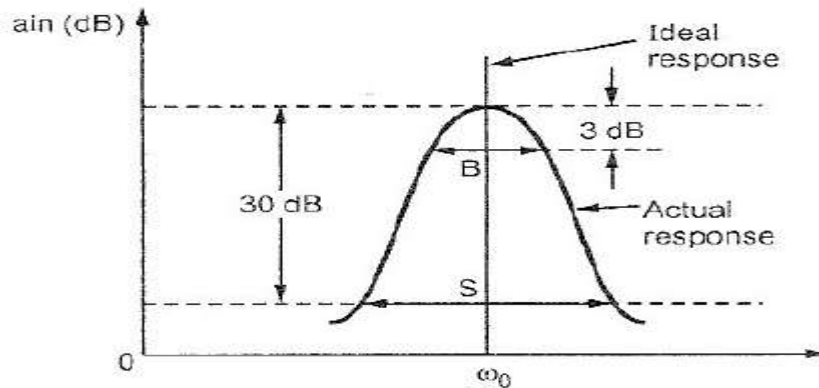


Fig. 3.2 Frequency response of a tuned amplifier

The Fig. 3.1 shows the tuned parallel LC circuit which resonates at a particular frequency. The resonance frequency and impedance of tuned circuit is given as,

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad \dots (1)$$

$$\text{and} \quad Z_r = \frac{L}{CR} \quad \dots (2)$$

The response of tuned amplifiers is maximum at resonant frequency and it falls sharply for frequencies below and above the resonant frequency, as shown in the Fig. 3.2. In the Fig. 3.2, 3 dB bandwidth is denoted as B and 30dB bandwidth is denoted as S . The ratio of the 30dB bandwidth (S) to the 3 dB bandwidth (B) is known as Skirt selectivity.

At resonance, inductive and capacitive effects of tuned circuit cancel each other. As a result, circuit is like resistive and $\cos \phi = 1$ i.e. voltage and current are in phase. For frequencies above resonance, circuit is capacitive and for frequencies below resonance, circuit is inductive. Since tuned circuit is purely resistive at resonance it can be used as a load for amplifier.

3.1.1 Coil Losses:

As shown in the Fig. 3.1, the tuned circuit consists of a coil. Practically, coil is not purely inductive. It consists of few losses and they are represented in the form of leakage resistance in with the inductor. The total loss of the coil is comprised of copper loss, eddy current loss and hysteresis loss. The copper loss at low frequencies is equivalent to the d.c. resistance of the coil. Copper loss is inversely proportional to frequency. Therefore, as frequency increases, the

copper loss decreases. Eddy current loss in iron and copper coil are due to currents flowing within the copper or core based by induction. The result of eddy currents is a loss due to heating within the inductors copper or core. Eddy current losses are directly proportional to frequency. Hysteresis loss is proportional to the area enclosed by the hysteresis loop and to the rate at which this loop is transversed. It is a function of signal level and increase with frequency. Hysteresis loss is however independent of frequency.

As mentioned earlier, the total losses in the coil or inductor is represented by inductance in series with leakage resistance of the coil. It is shown in the Fig.3.3

3.1.2 Q Factor:

Quality Factor (Q) is important characteristics of inductor. The Q is the ratio of reactance to resistance and therefore it is unitless. It is the measure of how 'pure' or 'real' an inductor is (i.e. the inductor consists only reactance). The higher the Q of an inductor, the fewer losses there are in the inductor. The Q factor also can be defined as the measure of efficiency with which inductor can store the energy. The dissipation factor (D) that can be referred to as the total loss within a component is defined as $1/Q$. The fig. 3.4 shows the quality factor equations for series and parallel circuits and its relation with dissipation factor.

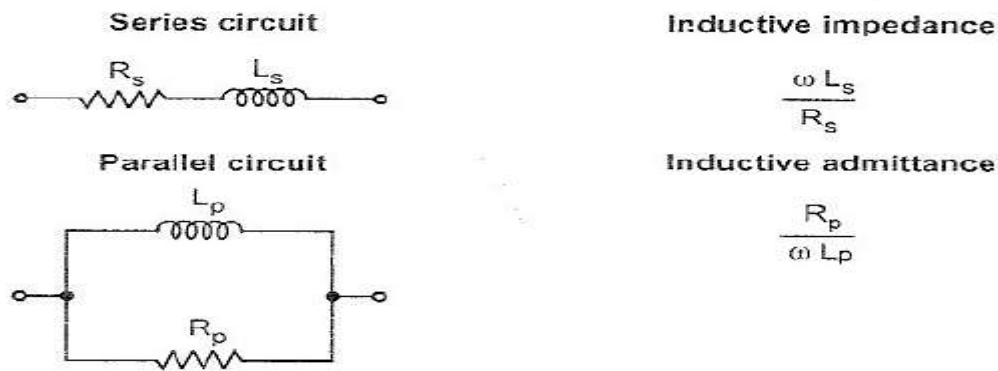


Fig. 3.4 Quality factor equations

$$\text{Quality factor equation } Q = \frac{1}{D} = \frac{\omega L_s}{R_s} = \frac{R_p}{\omega L_p}$$

3.1.3 Unloaded and Loaded Q:

Unloaded Q is the ratio of stored energy to dissipated energy in a reactor or resonator. The unloaded Q or Q_U , of an inductor or capacitor is X/R_s , where X represents the reactance and R_s represents the series resistance. The loaded Q or Q_L , of a resonator is determined by how tightly the resonator is coupled to its terminations.

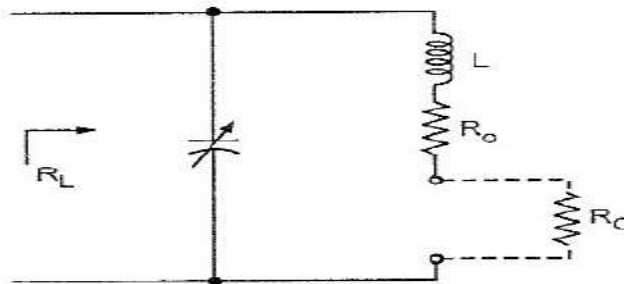


Fig. 3.5 Tuned load circuit

Let us consider the tuned load circuit as shown in the Fig. 3.5. Here, L and C represent tank circuit. The internal circuit losses of inductor are represented by R_o and R_c represents the coupled in load.

For this circuit we can write,

$$R_o = \frac{\omega_o L}{Q_U} \text{ and } R_C = \frac{\omega_o L}{Q_L}$$

where Q_U is unloaded Q and Q_L is loaded Q.

The circuit efficiency for the above tank circuit is given as,

$$\eta = \frac{I^2 R_C}{I^2 (R_C + R_o)} = \frac{Q_U}{Q_U + Q_L} \times 100 \%$$

From above equation, it can be easily realized that for high overall power efficiency, the coupled-in load R_C should be large in comparison to the internal circuit losses represented by R_o of the inductor.

The quality factor Q_L determines the 3 dB bandwidth for the resonant circuit. The 3 dB bandwidth for the resonant circuit is given as,

$$BW = \frac{f_r}{Q_L}$$

Where f_r represents the centre frequency of a resonator and BW represents the bandwidth.

If Q is large, bandwidth is small and circuit will be highly selective. For small Q values, bandwidth is high and selectivity of the circuit is lost, as shown in the Fig. 3.6.

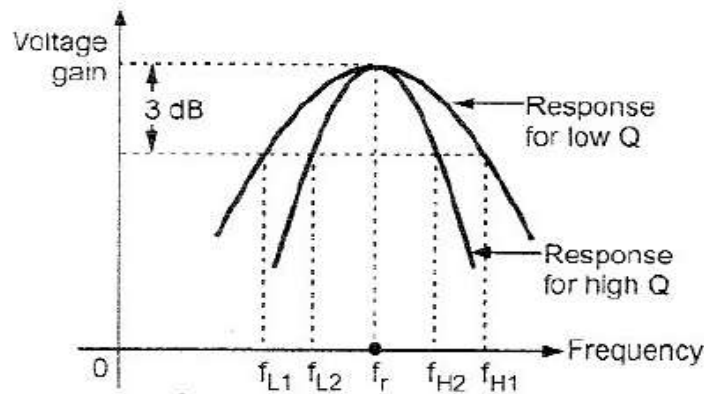


Fig. 3.6 Variation of 3dB bandwidth with variation in quality factor

Thus in tuned amplifier Q is kept as high as possible to get the better selectivity. Such tuned amplifiers are used in communication or broadcast receivers where it is necessary to amplify only selected band of frequencies.

3.1.4 Requirements of Tuned Amplifier:

The basic requirements of Tuned Amplifiers are:

1. The amplifier should provide selectivity of resonant frequency over a very narrow band.
2. The signal should be amplified equally well at all frequencies in the selected narrow band.
3. The tuned circuit should be so mounted that it can be easily tuned. If there is more than one circuit to be tuned, there should be an arrangement to tune all circuit simultaneously.
4. The amplifier must provide the simplicity in tuning of the amplifier components to the desired frequency over a considerable range of band of frequencies.

3.1.5 Classification of Tuned Amplifier:

We know that, multistage amplifiers are used to obtain large overall gain. The cascaded stages of multistage tuned amplifiers can be categorized as given below:

1. Single Tuned Amplifiers
2. Double Tuned Amplifiers
3. Stagger Tuned Amplifiers

These amplifiers are further classified according to coupling used to cascade the stages of multistage amplifier. They are,

1. Capacitive Coupled
2. Inductive Coupled
3. Transformer Coupled

3.2 Small Signal Tuned Amplifier:

A common emitter amplifier can be converted into a single tuned amplifier by including a parallel tuned circuit as shown in the Fig. 3.7. The biasing components are not shown for simplicity.

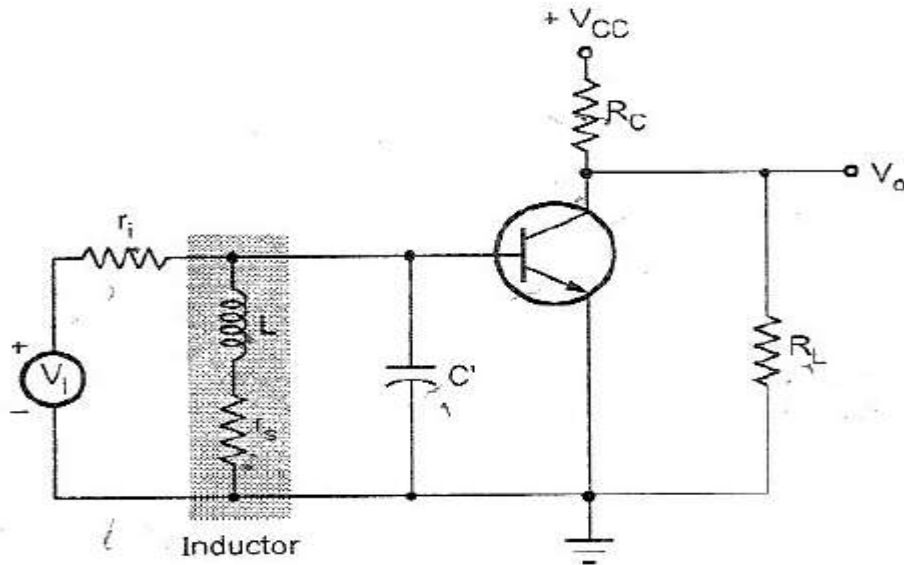


Fig. 3.7 Single tuned transistor amplifier

Before going to study the analysis of this amplifier, the practical assumptions to simplify the analysis are:

Assumptions:

1. $R_L \ll R_C$
2. $r_{bb'} = 0$

With these assumptions, the simplified equivalent circuit for a single tuned amplifier is shown in Fig 3.8.

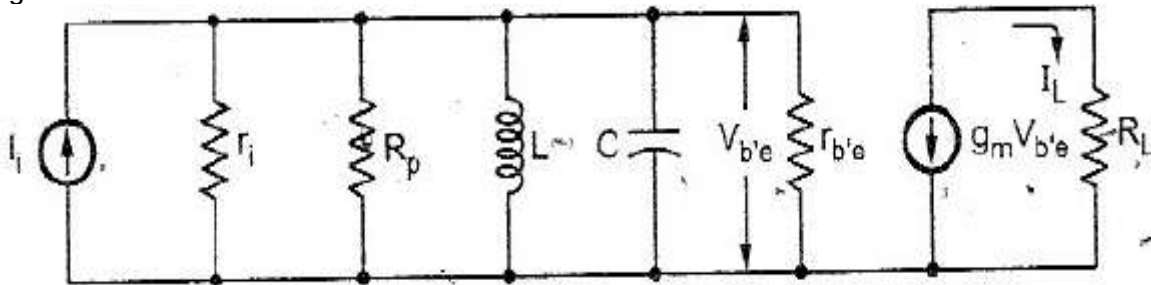


Fig. 3.8 Equivalent circuit of single tuned amplifier

Where $C_{eq} = C' + C_{b'e} + (1 + g_m R_L) C_{b'c}$ and C' is the external capacitance used to tune the circuit, $(1 + g_m R_L) C_{b'c}$ is the Miller Capacitance. r_s represents the losses in the coil. The series RL circuit in Fig. 3.7 is replaced by the equivalent RL circuit in Fig 3.8 assuming coil losses are low over the frequency band of interest, i.e. the coil Q is high.

$$Q_c \equiv \frac{\omega L}{r_c} \gg 1$$

The conditions for equivalence are most easily established by equating the admittances of the two circuits shown in the Fig. 3.9.

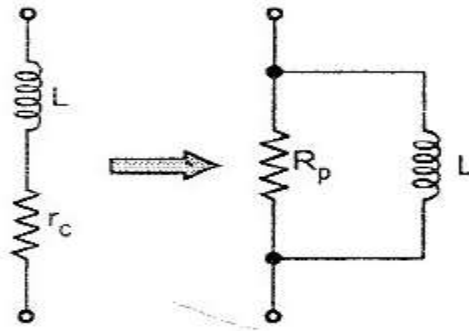


Fig. 3.9 Equivalent circuits

$$Y_1 = \frac{1}{r_c + j\omega L} = \frac{r_c - j\omega L}{r_c^2 + \omega^2 L^2}$$

$$\approx \frac{r_c}{r_c^2 + \omega^2 L^2} - \frac{j\omega L}{r_c^2 + \omega^2 L^2}$$

$$Y_1 = \frac{r_c}{\omega^2 L^2} + \frac{1}{j\omega L}$$

$\because \omega L \gg r_c$ from equation (1)

$$Y_2 = \frac{1}{R_p} + \frac{1}{j\omega L}$$

$\therefore$ Therefore, equating Y_1 and Y_2 we get,

$$\frac{r_c}{\omega^2 L^2} + \frac{1}{j\omega L} = \frac{1}{R_p} + \frac{1}{j\omega L}$$

$$\therefore \frac{1}{R_p} = \frac{r_c}{\omega^2 L^2}$$

$$= \frac{r_c^2}{r_c \omega^2 L^2} = \frac{1}{r_c Q_c^2}$$

$$\boxed{\frac{1}{Q_c} = \frac{r_c}{\omega L}} \Rightarrow Q_c = \frac{\omega L}{r_c}$$

$$\therefore \boxed{R_p = r_c Q_c^2 = \omega L Q_c} \quad \because \omega L = Q_c r_c \text{ from equation (1)} \quad \dots (2)$$

Looking at Fig. 3.8 we have,

$$\therefore \boxed{R = r_i \parallel R_p \parallel r_{b'e}} \quad \dots (3)$$

The current gain of the amplifier is then

$$A_i = \frac{-g_m R}{1 + j(\omega RC - R/\omega L)} = \frac{-g_m R}{1 + j\omega_0 RC(\omega/\omega_0 - \omega_0/\omega)} \quad \dots (4)$$

where $\omega_0^2 = \frac{1}{LC}$

We define the Q of the tuned circuit at the resonant frequency ω_0 to be

$$Q_i = \frac{R}{\omega_o L} = \omega_o RC \quad \dots(5)$$

$$\therefore \quad A_i = \frac{-g_m R}{1 + jQ_i (\omega / \omega_o - \omega_o / \omega)}$$

At $\omega = \omega_o$, gain is maximum and it is given as,

$$\therefore \quad A_{i(\max)} = -g_m R \quad \dots(6)$$

The Fig. 3.10 shows the gain versus frequency plot for the single tuned amplifier. It shows the variation of the magnitude of the gain as a function of frequency.

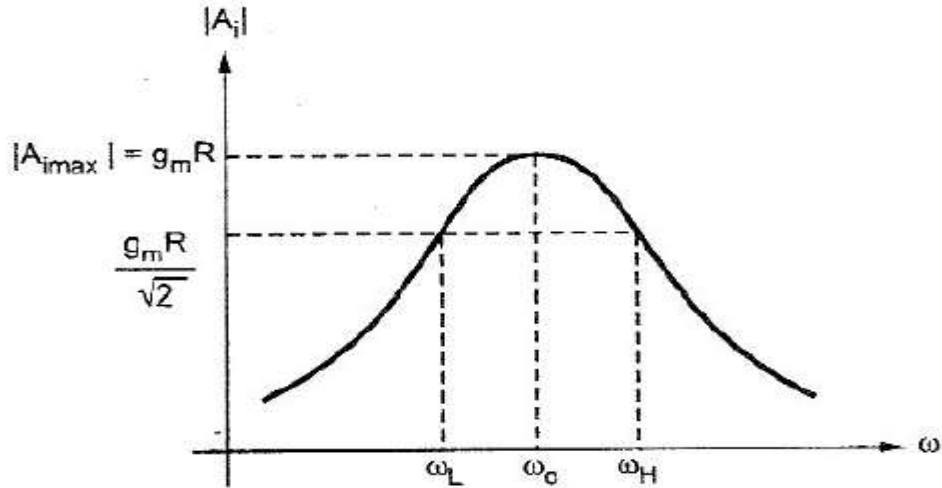


Fig. 3.10 Gain versus frequency for single tuned amplifier

At 3 dB frequency,

$$|A_i| = \frac{g_m R}{\sqrt{2}} \quad \dots (7)$$

$\therefore$ At 3 dB frequency

$$1 + jQ_i [(\omega / \omega_o) - (\omega_o / \omega)] = \sqrt{2}$$

$$\therefore \quad 1 + Q_i^2 \left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega} \right)^2 = 2 \quad \dots (8)$$

This equation is quadratic in ω^2 and has two positive solutions, ω_H and ω_L . After solving equation (8), 3 dB bandwidth is given below:

$$BW = f_H - f_L = \omega_o / 2\pi Q_i = 1 / 2\pi RC \quad (\text{since } Q_i = \omega_o RC) \quad \dots (9)$$

$$\therefore \quad BW = \frac{1}{2\pi RC}$$

►► **Example 3.1 :** Design a single tuned amplifier for following specifications :

1. Centre frequency = 500 kHz

2. Bandwidth = 10 kHz

Assume transistor parameters : $g_m = 0.04$ S, $h_{fe} = 100$, $C_{b'e} = 1000$ pF and $C_{b'c} = 100$ pF. The bias network and the input resistance are adjusted so that $r_i = 4$ k Ω and $R_L = 510$ Ω .

Solution : From equation (9) we have,

$$BW = \frac{1}{2\pi RC}$$

$$\begin{aligned} \therefore RC &= \frac{1}{2\pi BW} = \frac{1}{2\pi \times 10 \times 10^3} \\ &= 15.912 \times 10^{-6} \end{aligned}$$

From equation (3) we have,

$$R = r_i \parallel R_p \parallel r_{b'e}$$

where

$$r_i = 4 \text{ k}\Omega$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{0.04} = 2500 \text{ } \Omega$$

$$R_p = Q_c \omega_o L = \frac{Q_c}{\omega_o C}$$

$$\therefore R = 4 \times 10^3 \parallel 2500 \parallel \frac{Q_c}{\omega_o C}$$

$$C = \frac{1}{2\pi \times 10 \times 10^3 \times R}$$

$$\therefore C = \frac{1}{2\pi \times 10 \times 10^3 \times \left[4 \times 10^3 \parallel 2500 \parallel \frac{Q_c}{2\pi \times 500 \times 10^3 \times C} \right]}$$

The typical range for Q_c is 10 to 150. However, we have to assume Q such that value of C_p should be positive. Let us assume $Q = 100$.

$$\begin{aligned} \therefore C &= \frac{1}{2\pi \times 10 \times 10^3 \left[1538.5 \parallel \frac{1}{2\pi \times 5000 \times C} \right]} \\ &= \frac{1}{2\pi \times 10 \times 10^3 \left[\frac{1}{\frac{1}{1538.5} + 2\pi \times 5000 \times C} \right]} \end{aligned}$$

Solving for C we get,

$$C = 0.02 \mu\text{F}$$

We have,

$$C = C' + C_{b'e} + (1 + g_m R_L) C_{b'c}$$

$$\begin{aligned} \therefore C' &= C - [C_{b'e} + (1 + g_m R_L) C_{b'c}] \\ &= 0.02 \times 10^{-6} - [1000 \times 10^{-12} + (1 + 0.04 \times 510) \times 100 \times 10^{-12}] \end{aligned}$$

$$\therefore C' = 0.01686 \mu\text{F}$$

We have,

$$\omega_o^2 = \frac{1}{LC}$$

$$\begin{aligned} \therefore L &= \frac{1}{\omega_o^2 C} = \frac{1}{(2\pi \times 500 \times 10^3)^2 \times 0.02 \times 10^{-6}} \\ &= 5 \mu\text{H} \end{aligned}$$

From equation (2) we have,

$$\begin{aligned} R_p &= \omega L Q_c = 2\pi \times 500 \times 10^3 \times 5 \times 10^{-6} \times 100 \\ &= 1570 \Omega \end{aligned}$$

$$\begin{aligned} \therefore R &= r_i \parallel R_p \parallel r_{b'e} \\ &= 4 \times 10^3 \parallel 1570 \parallel 2500 \\ &= 777 \Omega \end{aligned}$$

We have mid frequency gain as,

$$A_{i \max} = -g_m R = (-0.04)(777) = -31$$

3.3 Single Tuned Capacitive Coupled Amplifier:

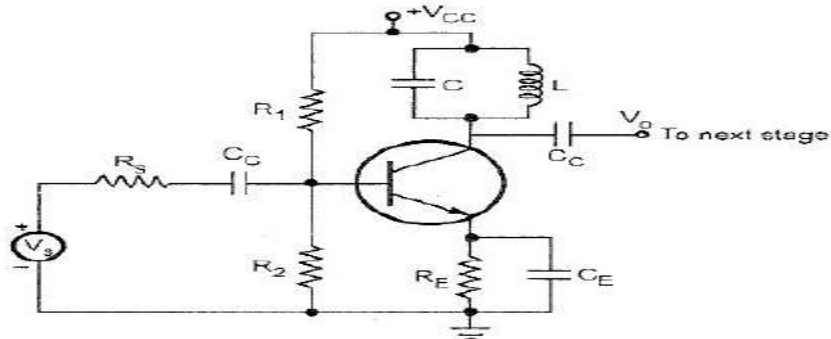


Fig. 3.13 Single tuned capacitive coupled transistor amplifier

Single Tuned multistage amplifier circuit uses one parallel tuned circuit as a load in each stage with tuned circuits in all stages tuned to same frequency. Fig 3.13 shows a typical single tuned amplifier in CE configuration. As shown in Fig.3.13, tuned circuit formed by L and C acts as collector load and resonates at frequency of operation. Resistors R_1 , R_2 and R_E along with capacitor C_E provides self bias for the circuit.

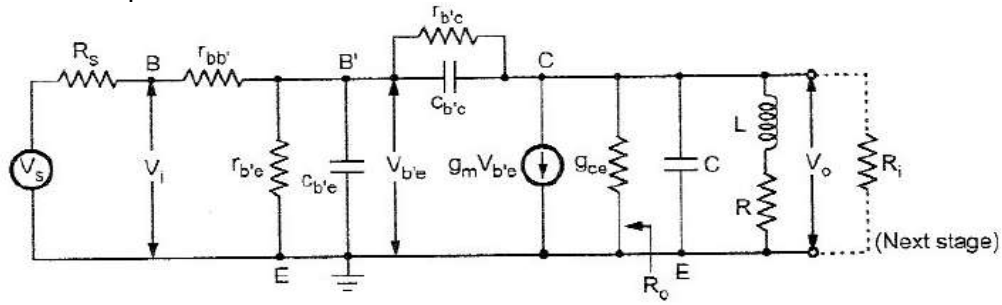


Fig. 3.14 Equivalent circuit of single tuned amplifier

The Fig. 3.14 shows the equivalent circuit for single tuned amplifier using hybrid π parameters.

As shown in the Fig. 3.14, R_i is the input resistance of the next stage and R_o is the output resistance of the current generator $g_m V_{be}$. The reactances of the bypass capacitor C_E and the coupling capacitors C_C are negligibly small at the operating frequency and hence these elements are neglected in the equivalent circuit shown in the Fig. 3.14.

The equivalent circuit shown in Fig. 3.14 can be simplified by applying Miller's theorem. Fig. 3.15 shows the simplified equivalent circuit for single tuned amplifier.

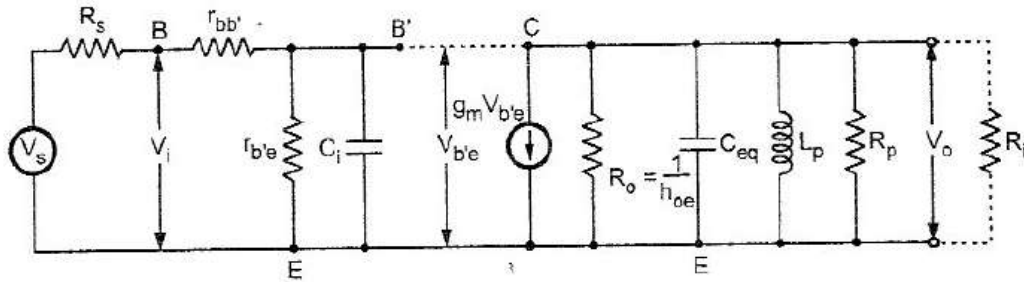


Fig. 3.15 Simplified equivalent circuit for single tuned amplifier

Here C_i and C_{eq} represent input and output circuit capacitances, respectively. They can be given as,

$$C_i = C_{be} + C_{bc}(1 - A) \quad \text{where } A \text{ is the voltage gain of the amplifier.} \quad \dots(1)$$

$$C_{eq} = C_{bc} \left(\frac{A - 1}{A} \right) + C \quad \text{where } C \text{ is the tuned circuit capacitance.} \quad \dots (2)$$

The g_{ce} is represented as the output resistance of current generator $g_m V_{be}$.

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_m h_{re} \approx h_{oe} = \frac{1}{R_o} \quad \dots (3)$$

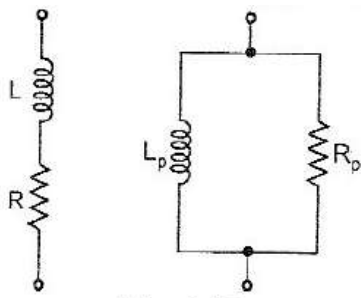


Fig. 3.16

The series RL circuit is represented by its equivalent parallel circuit. The conditions for equivalence are most easily established by equating the admittances of the two circuits shown in Fig. 3.16.

Admittance of the series combination of RL is given as,

$$Y = \frac{1}{R + j\omega L}$$

Multiplying numerator and denominator by $R - j\omega L$ we get,

$$\begin{aligned} Y &= \frac{R - j\omega L}{R^2 + \omega^2 L^2} = \frac{R}{R^2 + \omega^2 L^2} - \frac{j\omega L}{R^2 + \omega^2 L^2} \\ &= \frac{R}{R^2 + \omega^2 L^2} - \frac{j\omega^2 L}{\omega(R^2 + \omega^2 L^2)} \\ &= \frac{1}{R_p} + \frac{1}{j\omega L_p} \end{aligned}$$

where $R_p = \frac{R^2 + \omega^2 L^2}{R} \quad \dots (4)$

and $L_p = \frac{R^2 + \omega^2 L^2}{\omega^2 L} \quad \dots (5)$

Centre frequency

The centre frequency or resonant frequency is given as,

$$f_r = \frac{1}{2\pi\sqrt{L_p C_{eq}}} \quad \dots (6)$$

where $L_p = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$

and $C_{eq} = C_{b'c} \left(\frac{A-1}{A} \right) + C \quad \dots (7)$
 $= C_0 + C$

Therefore, C_{eq} is the summation of transistor output capacitance and the tuned circuit capacitance.

Quality factor Q

The quality factor Q of the coil at resonance is given by,

$$Q_r = \frac{\omega_r L}{R} \quad \dots (8)$$

where ω_r is the centre frequency or resonant frequency.

This quality factor is also called unloaded Q. But in practice, transistor output resistance and input resistance of next stage act as a load for the tuned circuit. The quality factor including load is called as loaded Q and it can be given as follows :

The Q of the coil is usually large so that $\omega L \gg R$ in the frequency range of operation.

From equation (4) we have,

$$R_p = \frac{R^2 + \omega^2 L^2}{R} = R + \frac{\omega^2 L^2}{R}$$

$$\text{As } \frac{\omega^2 L^2}{R} \gg 1, \quad R_p \approx \frac{\omega^2 L^2}{R} \quad \dots(9)$$

From equation (5) we have,

$$\begin{aligned} L_p &= \frac{R^2 + \omega^2 L^2}{\omega^2 L} = \frac{R^2}{\omega^2 L} + L \\ &\approx L \quad \because \omega L \gg R \end{aligned} \quad \dots (10)$$

From equation (9), we can express R_p at resonance as,

$$\begin{aligned} R_p &= \frac{\omega_r^2 L^2}{R} \\ &= \omega_r Q_r L \quad \because Q_r = \frac{\omega_r L}{R} \end{aligned} \quad \dots (11)$$

Therefore, Q_r can be expressed in terms of R_p as,

$$Q_r = \frac{R_p}{\omega_r L} \quad \dots(12)$$

The effective quality factor including load can be calculated looking at the simplified equivalent output circuit for single tuned amplifier.

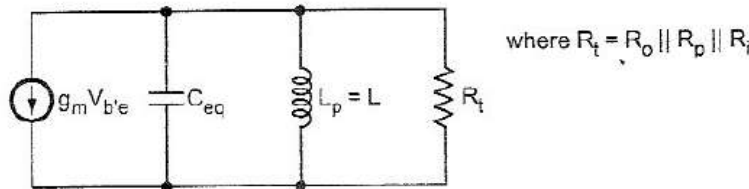


Fig. 3.17 Simplified output circuit for single tuned amplifier

$$\begin{aligned} \text{Effective quality factor } Q_{\text{eff}} &= \frac{\text{Susceptance of inductance } L \text{ or capacitance } C}{\text{Conductance of shunt resistance } R_t} \\ &= \frac{R_t}{\omega_r L} \text{ or } \omega_r C_{eq} R_t \end{aligned} \quad \dots (13)$$

Voltage gain (A_v)

The voltage gain for single tuned amplifier is given by,

$$A_v = -g_m \frac{r_{b'e}}{r_{bb'} + r_{b'e}} \times \frac{R_t}{1 + 2jQ_{eff}\delta}$$

where

$$R_t = R_o || R_p || R_i$$

δ = Fraction variation in the resonant frequency

$$A_v \text{ (at resonance)} = -g_m \frac{r_{b'e}}{r_{bb'} + r_{b'e}} \times R_t$$

$$\therefore \left| \frac{A_v}{A_v \text{ (at resonance)}} \right| = \frac{1}{\sqrt{1 + (2\delta Q_{eff})^2}} \quad \dots (14)$$

3 dB bandwidth

The 3 dB bandwidth of a single tuned amplifier is given by,

$$\begin{aligned} \Delta f &= \frac{1}{2\pi R_t C_{eq}} \\ &= \frac{\omega_r}{2\pi Q_{eff}} \quad \because Q_{eff} = \omega_r R_t C_{eq} \end{aligned} \quad \dots (15)$$

$$= \frac{f_r}{Q_{eff}} \quad \because \omega_r = 2\pi f_r \quad \dots (16)$$

► **Example 3.2 :** A single tuned RF amplifier uses a transistor with an output resistance of 50 K, output capacitance of 15 pF and input resistance of next stage is 20 k Ω . The tuned circuit consists of 47 pF capacitance in parallel with series combination of 1 μ H inductance and 2 Ω resistance. Calculate

i) Resonant frequency

ii) Effective quality factor

iii) Bandwidth of the circuit

Solution : i) Resonant frequency f_r is given as,

$$\begin{aligned} f_r &= \frac{1}{2\pi \sqrt{L C_{eq}}} \\ &= \frac{1}{2\pi \sqrt{1 \mu\text{H} \times (15 \text{ pF} + 47 \text{ pF})}} \\ &= 20.2 \text{ MHz} \end{aligned}$$

ii) Effective quality factor is given as,

$$\begin{aligned} Q_{eff} &= \omega_r C_{eq} R_t \\ &= 2\pi f_r C_{eq} \times (R_o || R_p || R_i) \end{aligned}$$

$$\begin{aligned} \text{where } R_p &= \frac{\omega_r^2 L^2}{R} = \frac{(2\pi \times 20.2 \times 10^6)^2 (1 \times 10^{-6})^2}{2} \\ &= 8054 \Omega \end{aligned}$$

$$\begin{aligned} \therefore Q_{eff} &= 2\pi \times 20.2 \times 10^6 \times (15 \text{ pF} + 47 \text{ pF}) \times (50 \text{ K} || 8.054 \text{ K} || 20 \text{ K}) \\ &= 40.52 \end{aligned}$$

iii) Bandwidth of the circuit is given as,

$$\begin{aligned} BW &= \frac{f_r}{Q_{\text{eff}}} = \frac{20.2 \times 10^6}{40.52} \\ &= 498.5 \text{ kHz} \end{aligned}$$

► **Example 3.3 :** A single tuned transistor amplifier is used to amplify modulated RF carrier of 600 kHz and bandwidth of 15 kHz. The circuit has a total output resistance, $R_t = 20 \text{ k}\Omega$ and output capacitance $C_o = 50 \text{ pF}$. Calculate values of inductance and capacitance of the tuned circuit.

Solution : Given : $f_r = 600 \text{ kHz}$

$$BW = 15 \text{ kHz}$$

$$R_t = 20 \text{ k}\Omega$$

$$C_o = 50 \text{ pF}$$

$$C_{\text{eq}} = (50 \text{ pF} + C)$$

$$\begin{aligned} Q_{\text{eff}} &= \frac{f_r}{BW} = \frac{600 \text{ kHz}}{15 \text{ kHz}} \\ &= 40 \end{aligned}$$

i) We know that,

$$Q_{\text{eff}} = \omega_r C_{\text{eq}} R_t$$

$$\begin{aligned} \therefore C_{\text{eq}} &= \frac{Q_{\text{eff}}}{\omega_r R_t} = \frac{40}{2\pi \times 600 \times 10^3 \times 20 \times 10^3} \\ &= 530.5 \text{ pF} \end{aligned}$$

$$C_{\text{eq}} = (50 \text{ pF} + C)$$

$$\begin{aligned} \therefore C &= 530.5 \text{ pF} - 50 \text{ pF} \\ &= 480.5 \text{ pF} \end{aligned}$$

ii) We know that,

$$f_r = \frac{1}{2\pi \sqrt{LC_{\text{eq}}}}$$

$$\begin{aligned} \therefore L &= \frac{1}{(2\pi f_r)^2 C_{\text{eq}}} = \frac{1}{(2\pi \times 600 \times 10^3)^2 \times 530.5 \times 10^{-12}} \\ &= 132.6 \text{ }\mu\text{H} \end{aligned}$$

3.4 Double Tuned Amplifier:

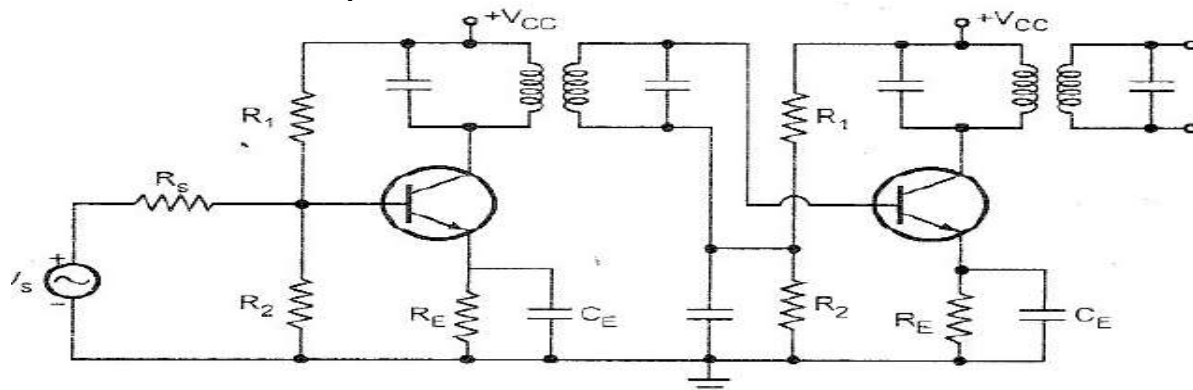


Fig. 3.18 Double tuned amplifier

Fig 3.18 shows double tuned RF amplifier in CE configuration. Here, voltage developed across tuned circuit is coupled inductively to another tuned circuit. Both tuned circuits are tuned to the same frequency. The double tuned circuit can provide a bandwidth of several percent of the resonant frequency and gives steep sides to the response curve. Let us analyze the double tuned circuit.

Analysis:

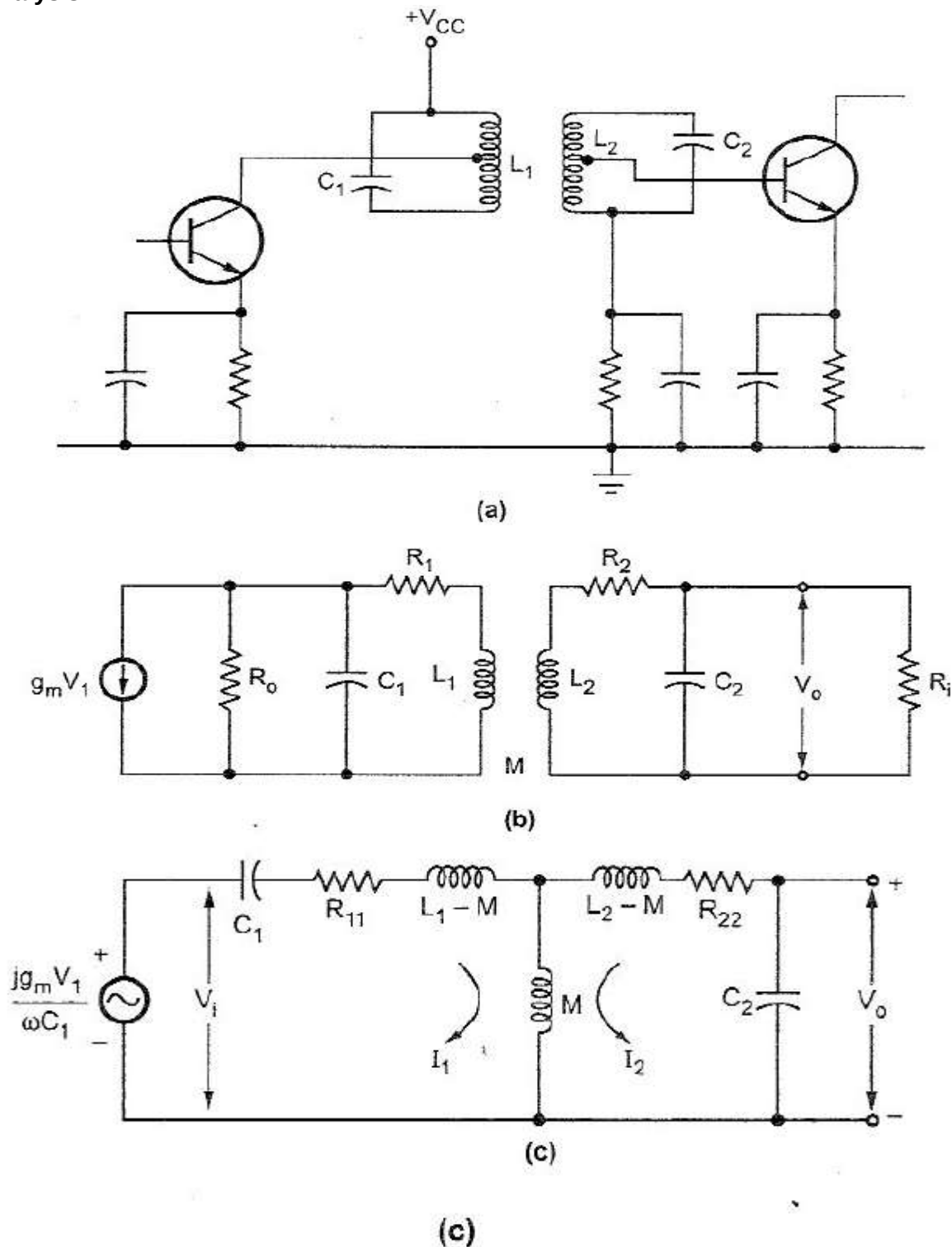


Fig. 3.19 Equivalent circuits for double tuned amplifier

The Fig. 3.19 (a) shows the coupling section of a transformer coupled double tuned amplifier. The Fig. 3.19 (b) shows the equivalent circuit for it, in which transistor is replaced by the current source with its output resistance (R_o). The C_1 and L_1 are the tank circuit components of the primary side. The resistance R_1 is the series resistance of the inductance L_1 . Similarly on the second side L_2 and C_2 represent the tank circuit components of the secondary side and R_2 represents resistance of the inductance L_2 . The resistance R_i represents the input resistance of the next stage.

The Fig. 3.19 (c) shows the simplified equivalent circuit for the Fig. 3.19 (b). In simplified equivalent circuit the series and parallel resistances are combined into series elements. Referring equation (9) we have,

$$R_p = \frac{\omega^2 L^2}{R} \text{ i.e. } R = \frac{\omega^2 L^2}{R_p}$$

where R represents series resistance and R_p represents parallel resistance.

Therefore we can write,

$$R_{11} = \frac{\omega_o^2 L_1^2}{R_o} + R_1$$

$$R_{12} = \frac{\omega_o^2 L_2^2}{R_i} + R_2$$

In the simplified circuit the current source is replaced by voltage source, which is now in series with C_1 . It also shows the effect of mutual inductance on primary and secondary sides.

We know that, $Q = \frac{\omega_r L}{R}$

Therefore, the Q factors of the individual tank circuits are

$$Q_1 = \frac{\omega_r L_1}{R_{11}} \text{ and } Q_2 = \frac{\omega_r L_2}{R_{22}} \quad \dots(1)$$

Usually, the Q factors for both circuits are kept same. Therefore, $Q_1 = Q_2 = Q$ and the resonant frequency $\omega_r^2 = 1/L_1 C_1 = 1/L_2 C_2$.

Looking at Fig. 3.19 (c), the output voltage can be given as,

$$V_o = -\frac{j}{\omega_r C_2} I_2 \quad \dots (2)$$

To calculate V_o/V_i it is necessary to represent I_2 in terms of V_i . For this we have to find the transfer admittance Y_T . Let us consider the circuit shown in Fig. 3.20. For this circuit, the transfer admittance can be given as,

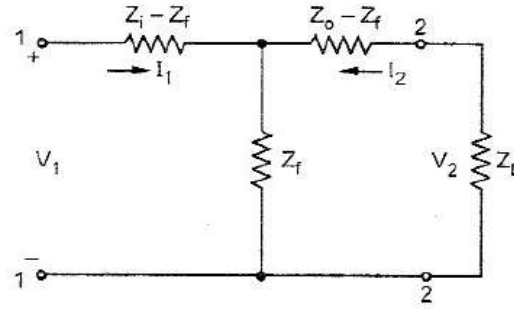


Fig. 3.20

$$Y_T = \frac{I_2}{V_1} = \frac{I_2}{I_1 Z_{11}} = \frac{A_i}{Z_{11}}$$

$$= \frac{Z_f}{Z_f^2 - Z_i (Z_o + Z_L)}$$

where

$$Z_{11} = \frac{V_1}{I_1} = Z_i - \frac{Z_f^2}{Z_o + Z_L} \text{ and}$$

$$A_i = \frac{I_2}{I_1} = \frac{-Z_f}{Z_o + Z_L}$$

The simplified equivalent circuit for double tuned amplifier is similar to the circuit shown in Fig. 3.20 with

$$Z_f = j \omega_r M$$

$$Z_i = R_{11} + j \left(\omega L_1 - \frac{1}{\omega C_1} \right)$$

$$Z_o + Z_L = R_{22} + j \left(\omega L_2 - \frac{1}{\omega C_2} \right)$$

The equations for Z_f , Z_i and $Z_o + Z_L$ can be further simplified as shown below.

$$Z_f = j \omega_r M = j \omega_r k \sqrt{L_1 L_2}$$

where, k is the coefficient of coupling.

Multiplying numerator and denominator by $\omega_r L_1$ for Z_i we get,

$$\begin{aligned}
 Z_i &= \frac{R_{11} \omega_r L_1}{\omega_r L_1} + j \omega_r L_1 \left(\frac{\omega L_1}{\omega_r L_1} - \frac{1}{\omega C_1 \omega_r L_1} \right) \\
 &= \frac{\omega_r L_1}{Q} + j \omega_r L_1 \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega} \right) \quad \because Q = \frac{\omega_r L}{R_{11}} \text{ and } \frac{1}{\omega_r L} = \omega_r C \\
 &= \frac{\omega_r L_1}{Q} + j \omega_r L_1 (2\delta) \quad \because \frac{\omega}{\omega_r} - \frac{\omega_r}{\omega} = 1 + \delta - (1 - \delta) = 2\delta \\
 &= \frac{\omega_r L_1}{Q} + (1 + j 2 Q \delta)
 \end{aligned}$$

$$Z_o + Z_L = R_{22} + j \left(\omega L_2 - \frac{1}{\omega C_2} \right)$$

By doing similar analysis as for Z_i we can write,

$$Z_o + Z_L = \frac{\omega_r L_2}{Q} + (1 + j 2 Q \delta)$$

Then

$$\begin{aligned}
 Y_T &= \frac{Z_f}{Z_f^2 - Z_i (Z_o + Z_L)} = \frac{1}{Z_f - Z_i (Z_o + Z_L) / Z_f} \\
 Y_T &= \frac{1}{j \omega_r k \sqrt{L_1 L_2} - \left[\frac{\omega_r L_1}{Q} (1 + j 2 Q \delta) \left\{ \frac{\omega_r L_2}{Q} (1 + j 2 Q \delta) \right\} \right]} \\
 Y_T &= \frac{k Q^2}{\omega_r \sqrt{L_1 L_2} [4 Q \delta - j (1 + k^2 Q^2 - 4 Q^2 \delta^2)]} \quad \dots (3)
 \end{aligned}$$

Substituting value of I_2 , i.e. $V_i \times Y_T$ we get,

$$\begin{aligned}
 V_o &= \frac{-j}{\omega_r C_2} \frac{j g_m V_i}{\omega_r C_1} \left[\frac{k Q^2}{\omega_r \sqrt{L_1 L_2} [4 Q \delta - j (1 + k^2 Q^2 - 4 Q^2 \delta^2)]} \right] \\
 \therefore V_i &= \frac{j g_m V_1}{\omega C_1}
 \end{aligned}$$

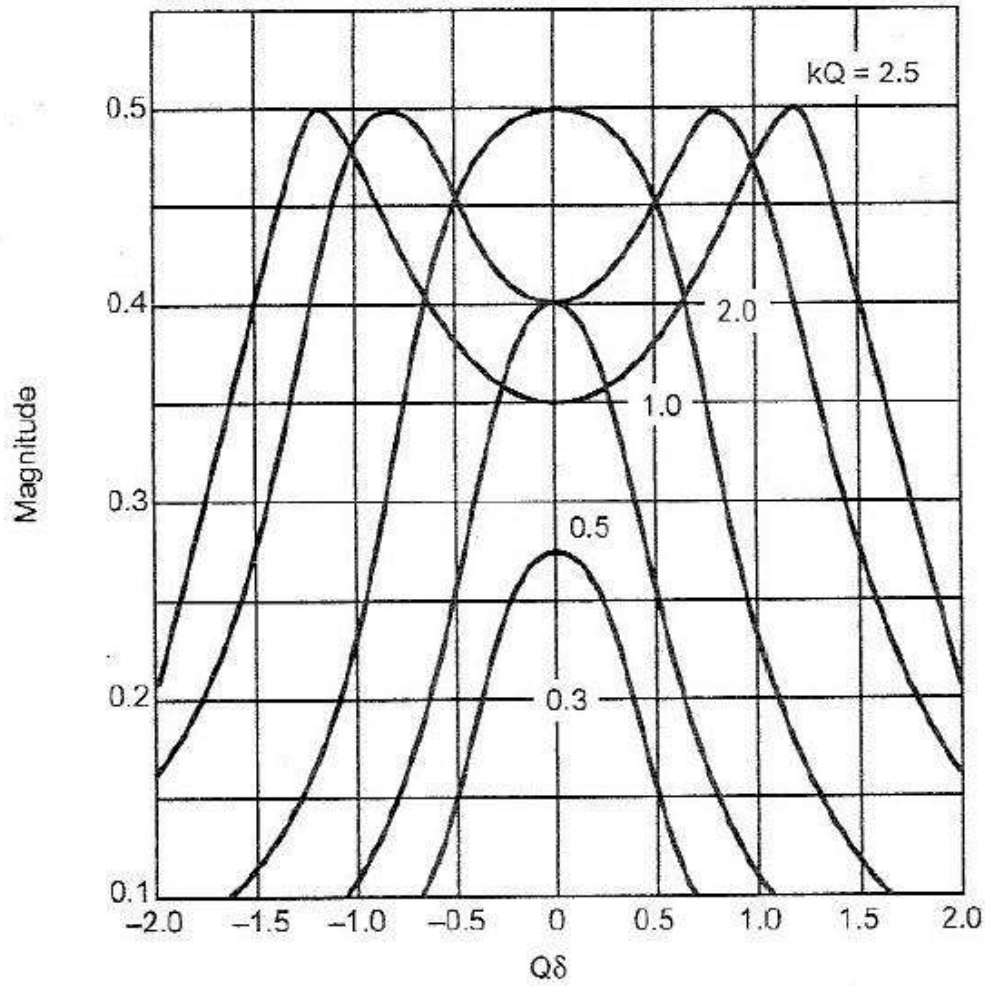


Fig. 3.21

$$A_v = \frac{V_o}{V_i} = g_m \omega_r^2 L_1 L_2 \left[\frac{kQ^2}{\omega_r \sqrt{L_1 L_2} [4Q\delta - j(1 + k^2Q^2 - 4Q^2\delta^2)]} \right]$$

$$\because \frac{1}{\omega_r C} = \omega_r L$$

$$= \left[\frac{g_m \omega_r \sqrt{L_1 L_2} kQ^2}{4Q\delta - j(1 + k^2Q^2 - 4Q^2\delta^2)} \right] \quad \dots (4)$$

Taking the magnitude of equation (4) we have,

$$|A_v| = g_m \omega_r \sqrt{L_1 L_2} Q \frac{kQ}{\sqrt{1 + k^2Q^2 - 4Q^2\delta^2 + 16Q^2\delta^2}} \quad \dots (5)$$

The Fig. 3.21 shows the universal response curve for double tuned amplifier plotted with kQ as a parameter.

The frequency deviation δ at which the gain peaks occur can be found by maximizing equation (4), i.e.

$$4Q\delta - j(1 + k^2Q^2 - 4Q^2\delta^2) = 0 \quad \dots (6)$$

As shown in the Fig. 3.22, two gain peaks in the frequency response of the double tuned amplifier can be given at frequencies :

$$f_1 = f_r \left(1 - \frac{1}{2Q} \sqrt{k^2 Q^2 - 1} \right) \text{ and}$$

$$f_2 = f_r \left(1 + \frac{1}{2Q} \sqrt{k^2 Q^2 - 1} \right) \quad \dots (7)$$

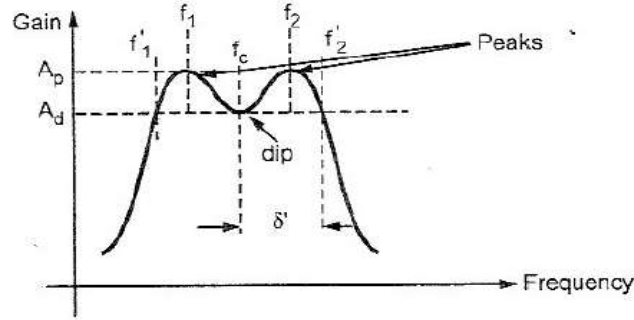


Fig. 3.22

At $k^2 Q^2 = 1$, i.e. $k = \frac{1}{Q}$, $f_1 = f_2 = f_r$. This condition is known as **critical coupling**. For values of $k < 1/Q$, the peak gain is less than maximum gain and the coupling is poor.

At $k > 1/Q$, the circuit is overcoupled and the response shows the double peak. Such double peak response is useful when more bandwidth is required.

The gain magnitude at peak is given as,

$$|A_p| = \frac{g_m \omega_0 \sqrt{L_1 L_2} kQ}{2} \quad \dots (8)$$

And gain at the dip at $\delta = 0$ is given as,

$$|A_d| = |A_p| \frac{2 kQ}{1 + k^2 Q^2} \quad \dots (9)$$

The ratio of peak gain and dip gain is denoted as γ and it represents the magnitude of the ripple in the gain curve.

$$\gamma = \frac{|A_p|}{|A_d|} = \frac{1 + k^2 Q^2}{2 kQ} \quad \dots (10)$$

Using quadratic simplification and choosing positive sign we get,

$$kQ = \gamma + \sqrt{\gamma^2 - 1} \quad \dots (11)$$

The bandwidth between the frequencies at which the gain is $|A_d|$ is the useful bandwidth of the double tuned amplifier. It is given as,

$$BW = 2 \delta' = \sqrt{2} (f_2 - f_1) \quad \dots (12)$$

At 3 dB bandwidth,

$$\gamma = \sqrt{2}$$

$$\therefore kQ = \gamma + \sqrt{\gamma^2 + 1} = \sqrt{2} + \sqrt{\sqrt{2}^2 + 1} = 2.414$$

$$\begin{aligned} \therefore 3 \text{ dB BW} &= 2 \delta' = \sqrt{2} (f_2 - f_1) \\ &= \sqrt{2} \left[f_r \left(1 + \frac{1}{2Q} \sqrt{k^2 Q^2 - 1} \right) - f_r \left(1 - \frac{1}{2Q} \sqrt{k^2 Q^2 - 1} \right) \right] \\ &= \sqrt{2} \left[\left(\frac{f_r}{Q} \sqrt{k^2 Q^2 - 1} \right) \right] \\ &= \sqrt{2} \left[\frac{f_r}{Q} \sqrt{(2.414)^2 - 1} \right] = \frac{3.1 f_r}{Q} \end{aligned}$$

We know that, the 3 dB bandwidth for single tuned amplifier is $2f_r / Q$. Therefore, the 3 dB bandwidth provided by double tuned amplifier ($3.1f_r / Q$) is substantially greater than the 3 dB bandwidth of single tuned amplifier.

Compared with a single tuned amplifier, the double tuned amplifier

1. Possesses a flatter response having steeper sides.
2. Provides larger 3 dB bandwidth.
3. Provides large gain-bandwidth product.

3.6 Effect of cascading Single Tuned Amplifier on Bandwidth:

In order to obtain a high overall gain, several identical stages of amplifiers can be used in cascade. The overall gain is the product of the voltage gains of the individual stages. Let us see the effect of cascading of stages on bandwidth.

Consider n stages of single tuned direct coupled amplifiers connected in cascade. We know that the relative gain of a single tuned amplifier w.r.t. the gain at resonant frequency f_r is given from equation (14).

$$\left| \frac{A_v}{A_v(\text{at resonance})} \right| = \frac{1}{\sqrt{1 + (2\delta Q_{\text{eff}})^2}}$$

Therefore, the relative gain of n stage cascaded amplifier becomes

$$\left| \frac{A_v}{A_v(\text{at resonance})} \right|^n = \left[\frac{1}{\sqrt{1 + (2\delta Q_{\text{eff}})^2}} \right]^n = \frac{1}{[1 + (2\delta Q_{\text{eff}})^2]^{\frac{n}{2}}}$$

The 3 dB frequencies for the n stage cascaded amplifier can be found by equating

$$\left| \frac{A_v}{A_v(\text{at resonance})} \right|^n = \frac{1}{\sqrt{2}}$$

$$\therefore \left| \frac{A_v}{A_v(\text{at resonance})} \right|^n = \frac{1}{[1+(2\delta Q_{\text{eff}})^2]^{\frac{n}{2}}} = \frac{1}{\sqrt{2}}$$

$$\therefore [1+(2\delta Q_{\text{eff}})^2]^{\frac{n}{2}} = 2^{\frac{1}{2}}$$

$$\therefore [1+(2\delta Q_{\text{eff}})^2]^n = 2$$

$$\therefore 1+(2\delta Q_{\text{eff}})^2 = 2^{\frac{1}{n}}$$

$$\therefore 2\delta Q_{\text{eff}} = \pm \sqrt{2^{\frac{1}{n}} - 1}$$

Substituting for δ , the fractional frequency variation, i.e.

$$\delta = \frac{\omega - \omega_r}{\omega_r} = \frac{f - f_r}{f_r}$$

$$\therefore 2 \left(\frac{f - f_r}{f_r} \right) Q_{\text{eff}} = \pm \sqrt{2^{\frac{1}{n}} - 1}$$

$$\therefore 2 (f - f_r) Q_{\text{eff}} = \pm f_r \sqrt{2^{\frac{1}{n}} - 1}$$

$$\therefore f - f_r = \pm \frac{f_r}{2 Q_{\text{eff}}} \sqrt{2^{\frac{1}{n}} - 1}$$

Let us assume f_1 and f_2 are the lower 3 dB and upper 3 dB frequencies, respectively. Then we have

$$f_2 - f_r = + \frac{f_r}{2 Q_{\text{eff}}} \sqrt{2^{\frac{1}{n}} - 1} \text{ and similarly,}$$

$$f_r - f_1 = + \frac{f_r}{2 Q_{\text{eff}}} \sqrt{2^{\frac{1}{n}} - 1}$$

The bandwidth of n stage identical amplifier is given as,

$$\begin{aligned}
 BW_n &= f_2 - f_1 = (f_2 - f_r) + (f_r - f_1) \\
 &= \frac{f_r}{2Q_{eff}} \sqrt{2^{\frac{1}{n}} - 1} + \frac{f_r}{2Q_{eff}} \sqrt{2^{\frac{1}{n}} - 1} \\
 &= \frac{f_r}{Q_{eff}} \sqrt{2^{\frac{1}{n}} - 1} \\
 &= BW_1 \sqrt{2^{\frac{1}{n}} - 1} \quad \dots (1)
 \end{aligned}$$

where BW_1 is the bandwidth of single stage and BW_n is the bandwidth of n stages.

►►► **Example 3.4 :** The bandwidth for single tuned amplifier is 20 kHz. Calculate the bandwidth if such three stages are cascaded. Also calculate the bandwidth for four stages.

Solution : i) We know that,

$$\begin{aligned}
 BW_n &= BW_1 \sqrt{2^{\frac{1}{n}} - 1} = 20 \times 10^3 \times \sqrt{2^{\frac{1}{3}} - 1} \\
 &= 10.196 \text{ kHz}
 \end{aligned}$$

$$\text{ii) } BW_n = 20 \times 10^3 \times \sqrt{2^{\frac{1}{4}} - 1} = 8.7 \text{ kHz}$$

The above example shows that bandwidth decreases as number of stages increase.

3.7 Effect of cascading Double Tuned Amplifiers on Bandwidth:

When a number of identical double tuned amplifier stages are connected in cascade, the overall bandwidth, of the system is thereby narrowed and the steepness of the sides of the response is increased, just as when single tuned stages are cascaded. The quantitative relation between the 3 dB bandwidth of n identical double tuned critically coupled stages compared with the bandwidth Δ_2 of such a system can be shown to be 3 dB bandwidth for n identical stages double tuned amplifiers is,

$$\Delta_2 \times \left(2^{\frac{1}{n}} - 1 \right)^{\frac{1}{4}}$$

where Δ_2 is the 3 dB bandwidth of single stage double tuned amplifier.

The above equation assumes that the bandwidth Δ_2 is small compared with the resonant frequency.

►►► **Example 3.5 :** The bandwidth for double tuned amplifier is 20 kHz. Calculate the bandwidth if such three stages are cascaded.

Solution : We know that for double tuned cascaded stages,

$$\begin{aligned}
 BW_n &= BW_1 \times \left(2^{1/n} - 1 \right)^{\frac{1}{4}} \\
 &= 20 \text{ K} \times \left(2^{1/3} - 1 \right)^{\frac{1}{4}} \\
 &= 14.28 \text{ kHz}
 \end{aligned}$$

➡ **Example 3.6 :** A three stage double tuned amplifier system is to have a half power BW of 20 kHz centred on a centre frequency of 450 kHz. Assuming that all stages are identical, determine the half power bandwidth of single stage. Assume that each stage couple to get maximum flatness.

Solution : We get maximum flat response when each stage is critically coupled. When stages are critically coupled we have

$$BW_n = BW_1 \times (2^{1/n} - 1)^{1/4}$$

$$BW_n = \frac{BW_1}{(2^{1/n} - 1)^{1/4}}$$

For $n = 3$

$$BW_n = \frac{BW_1}{(2^{1/3} - 1)^{1/4}}$$

$$= \frac{20 \times 10^3}{(2^{1/3} - 1)^{1/4}}$$

$$= 28.01 \text{ kHz}$$

3.8 Staggered Tuned Amplifier:

Double tuned amplifiers give greater 3 dB bandwidth having steeper sides and flat top. But alignment of double tuned amplifier is difficult. To overcome this problem, two single tuned cascaded amplifiers having certain bandwidth are taken and their resonant frequencies are so that they are separated by an amount equal to the bandwidth of each stage. Since the resonant frequencies are displaced or staggered, they are known as stagger tuned amplifiers. The advantage of stagger tuned amplifier is to have better flat, wideband characteristics in contrast with a very sharp, narrow band characteristic of synchronously tuned circuits (tuned to same resonant frequencies). Fig 3.23 shows the relation of amplification characteristics of individual stages in a staggered pair to the overall amplification of the two stages.

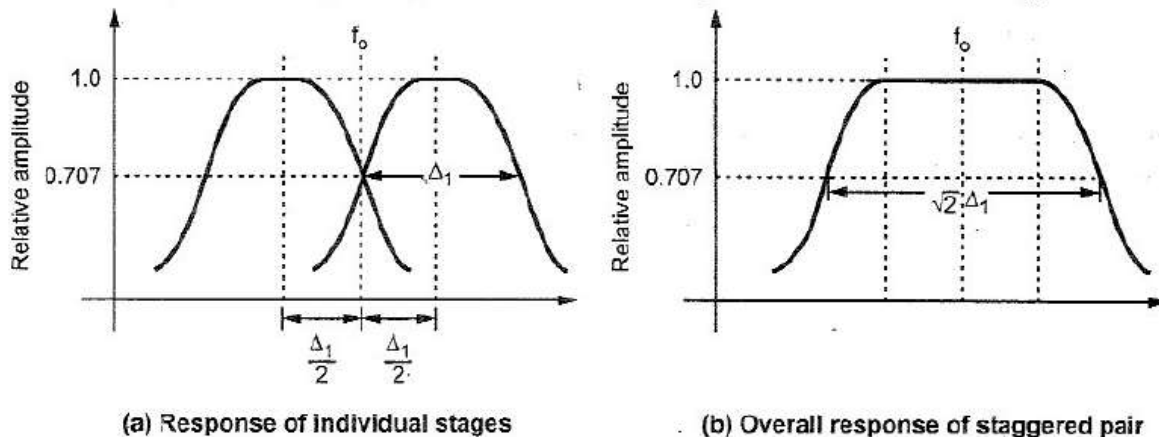


Fig. 3.23

The overall response of the two stage stagger tuned pair is compared in the Fig. 3.24 with the corresponding individual single tuned stages having same resonant circuits. Looking at Fig 3.24, it can be seen that staggering reduces the total amplification of the centre frequency to 0.5 of the peak amplification of the individual stage and at the centre frequency each stage has amplification that is 0.707 of the peak amplification of the individual stage. Thus the equivalent voltage amplification per stage of the staggered pair is 0.707 times as great as when the same two stages are used without staggering. However, the half power (3 dB) bandwidth of the staggered pair is $\sqrt{2}$ times as great as the half power (3 dB) bandwidth of on individual single tuned stage. Hence the equivalent gain bandwidth product per stage of a stagger tuned pair is $0.707 \times \sqrt{2} = 1.00$ times that of the individual single tuned stages.

The stagger tuned idea can be easily extended to more stages. In case of three stages staggering, the first tuning circuit is tuned to a frequency lower than centre frequency while the third circuit is tuned to higher frequency than centre frequency. The middle tuned circuit is tuned at exact centre frequency.

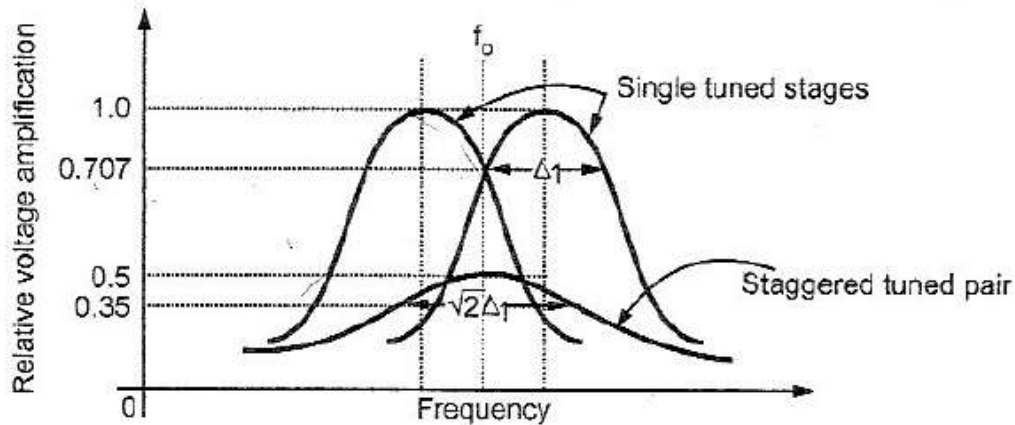


Fig. 3.24 Response of individually tuned and staggered tuned pair

Analysis:

Form equation (14), the gain of the single stage tuned amplifier can be written as,

$$\begin{aligned} \frac{A_v}{A_v \text{ (at resonance)}} &= \frac{1}{1 + 2jQ_{eff}\delta} \\ &= \frac{1}{1 + jX} \text{ where } X = 2Q_{eff}\delta \end{aligned}$$

Since in stagger tuned amplifiers the two single tuned cascaded amplifiers with separate resonant frequencies are used, we can assume that the one stage is tuned to the frequency $f_r + \delta$ and other stage is tuned to the frequency $f_r - \delta$. Therefore we have,

$$f_{r1} = f_r + \delta$$

and

$$f_{r2} = f_r - \delta$$

According to these tuned frequencies the selectivity functions can be given as,

$$\begin{aligned} \frac{A_v}{A_v \text{ (at resonance)}_1} &= \frac{1}{1 + j(X+1)} \text{ and} \\ \frac{A_v}{A_v \text{ (at resonance)}_2} &= \frac{1}{1 + j(X-1)} \end{aligned}$$

The overall gain of these two stages is the product of individual gains of the two stages.

$$\begin{aligned}
\therefore \frac{A_v}{A_v \text{ (at resonance)}_{\text{cascaded}}} &= \frac{A_v}{A_v \text{ (at resonance)}_1} \times \frac{A_v}{A_v \text{ (at resonance)}_2} \\
&= \frac{1}{1+j(X+1)} \times \frac{1}{1+j(X-1)} \\
&= \frac{1}{2+2jX-X^2} = \frac{1}{(2-X^2)+(2jX)} \\
\therefore \left| \frac{A_v}{A_v \text{ (at resonance)}_{\text{cascaded}}} \right| &= \frac{1}{\sqrt{(2-X^2)^2 + (2X)^2}} \\
&= \frac{1}{\sqrt{4-4X^2+X^4+4X^2}} = \frac{1}{\sqrt{4+X^4}}
\end{aligned}$$

Substituting the value of X we get,

$$\begin{aligned}
\left| \frac{A_v}{A_v \text{ (at resonance)}_{\text{cascaded}}} \right| &= \frac{1}{\sqrt{4+(2Q_{\text{eff}}\delta)^4}} = \frac{1}{\sqrt{4+16Q_{\text{eff}}^4\delta^4}} \\
&= \frac{1}{2\sqrt{1+4Q_{\text{eff}}^4\delta^4}}
\end{aligned}$$

Applications of mixer or converter circuits

1. One of the most common applications for mixer is in radio receivers. The mixer is used to convert incoming signal to a lower frequency where it is easier to obtain the high gain and selectivity required.
2. Mixer circuits are used to translate signal frequency to some lower frequency or to some higher frequency. When it is used to translate signal to lower frequency it is called down converter. When it is used to translate signal to higher frequency, it is called up converter.

3.10 Stability of Tuned Amplifiers

In tuned RF amplifiers, transistors are used at the frequencies nearer to their unity gain bandwidths (i.e. f_T), to amplify a narrow band of high frequencies centred around a radio frequency. At this frequency, the inter junction capacitance between base and collector, C_{bc} of the transistor becomes dominant, i.e. its reactance becomes low enough to be considered, which is otherwise infinite to be neglected as open circuit. Being CE configuration capacitance C_{bc} , shown in the Fig. 3.35 come across input and output circuits of an amplifier. As reactance of C_{bc} at RF is low enough it provides the feedback path from collector to base. With this circuit condition, if some feedback signal manages to reach the input from output in a positive manner with proper phase shift, then there is possibility of circuit converted to an unstable one, generating its own oscillations and can stop working as an amplifier. This circuit will always oscillate if enough energy is fed back from the collector to the base in the correct phase to overcome circuit losses. Unfortunately, the conditions for best gain and selectivity are also those which promote oscillation. In order to prevent oscillations in tuned RF amplifiers it was necessary to reduce the stage gain to a level that ensured circuit stability. This could be accomplished in several ways such as lowering the Q of tune circuits; stagger tuning, loose coupling

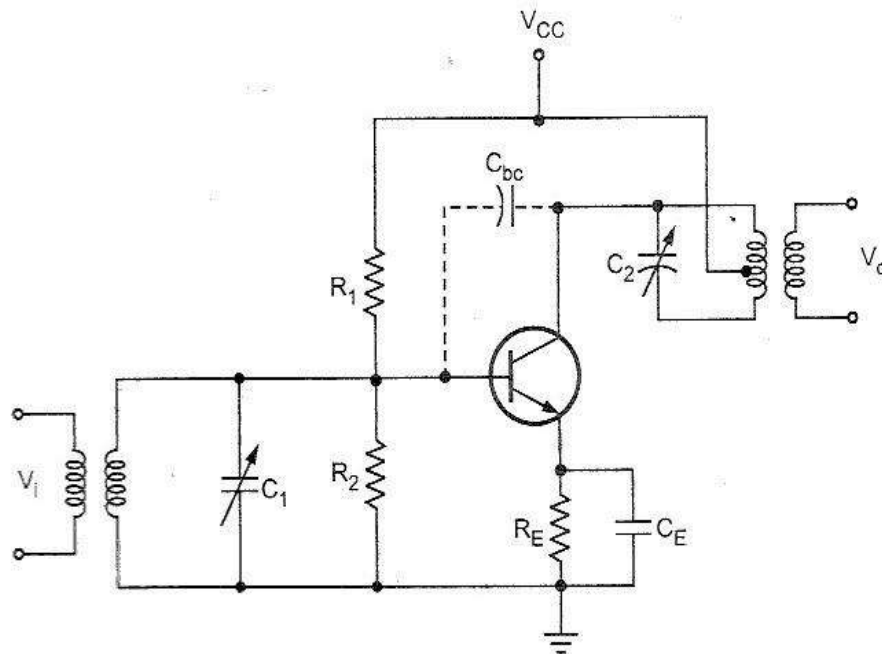


Fig. 3.35 Tuned RF stage

between the stages or inserting a 'loser' element into the circuit. While all these methods reduced gain, detuning and Q reduction had detrimental effects on selectivity. Instead of loosing the circuit performance to achieve stability, the professor L.A. Hazeltine introduced a circuit in which the troublesome effect of the collector to base capacitance of the transistor was neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance. He proved that the neutralization can be achieved by deliberately feeding back a portion of the output signal to the input in such a way that it has the same amplitude as the unwanted feedback but the opposite phase. Later on many neutralizing circuits were introduced. Let us study some of these circuits.

3.10.1 Hazeltine Neutralization

The Fig. 3.36 shows one variation of the Hazeltine circuit. In this circuit a small value of variable capacitance C_N is connected from the bottom of coil, point B, to the base. Therefore, the internal capacitance C_{bc} , shown dotted, feeds a signal from the top end of the coil, point A, to the transistor base and the C_N feeds a signal of equal magnitude but opposite polarity from the bottom of coil, point B, to the base. The neutralizing capacitor, C_N , can be adjusted correctly to completely nullify the signal fed through the C_{bc} .

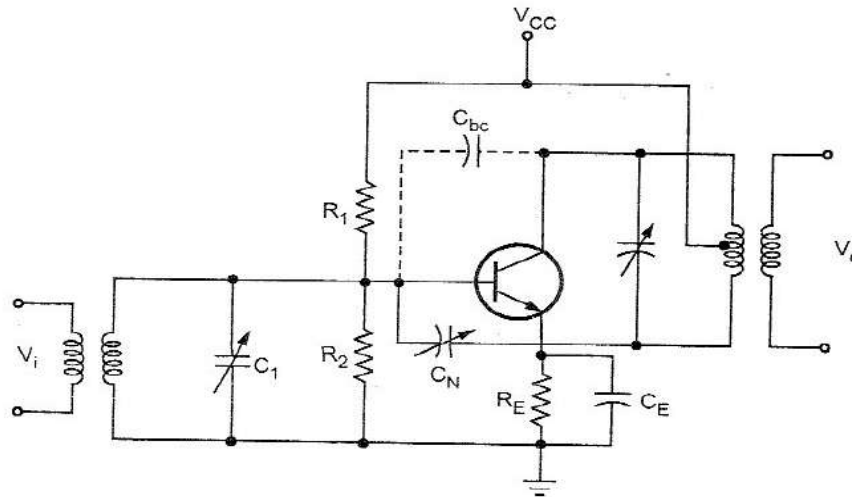


Fig. 3.36 Tuned RF amplifier with Hazeltine neutralization

3.10.2 Neutrodyne Neutralization

The Fig. 3.37 shows typical neutrodyne circuit. In this circuit the neutralization capacitor is connected from the lower end of the base coil of the next stage to the base of the transistor.

In principle, this circuit functions in the same manner as the Hazeltine neutralization circuit with the advantage that the neutralizing capacitor does not have the supply voltage across it.

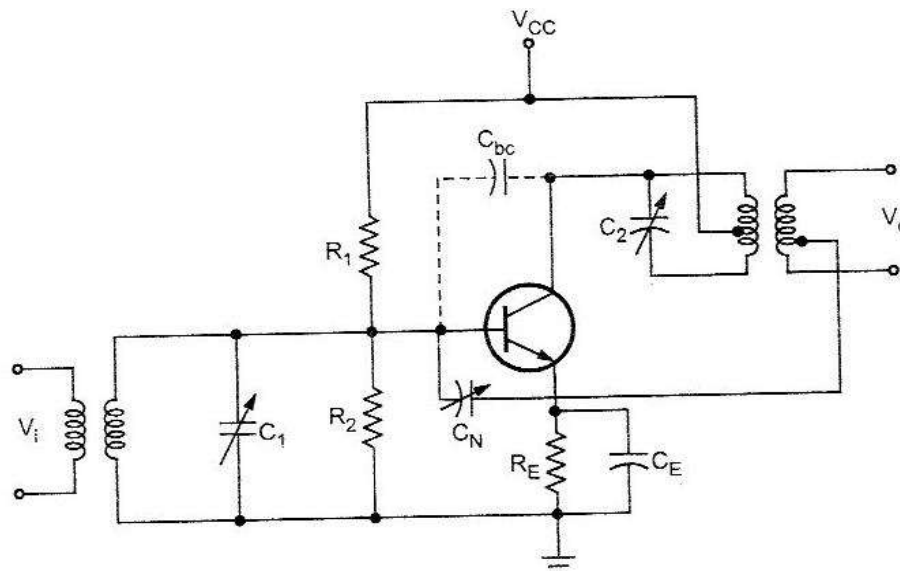


Fig. 3.37 Tuned RF amplifier with Neutrodyne neutralization

3.10.3 Neutralization using Coil

The Fig. 3.38 shows the neutralization of RF amplifier using coil. In this circuit, L part of the tuned circuit at the base of next stage is oriented for minimum coupling to the other windings. It is wound on a separate form and is mounted at right angles to the coupled windings. If the windings are properly polarized, the voltage across L due to the circulating current in the base circuit will have the proper phase to cancel the signal coupled through the base to collector, C_{bc} capacitance.

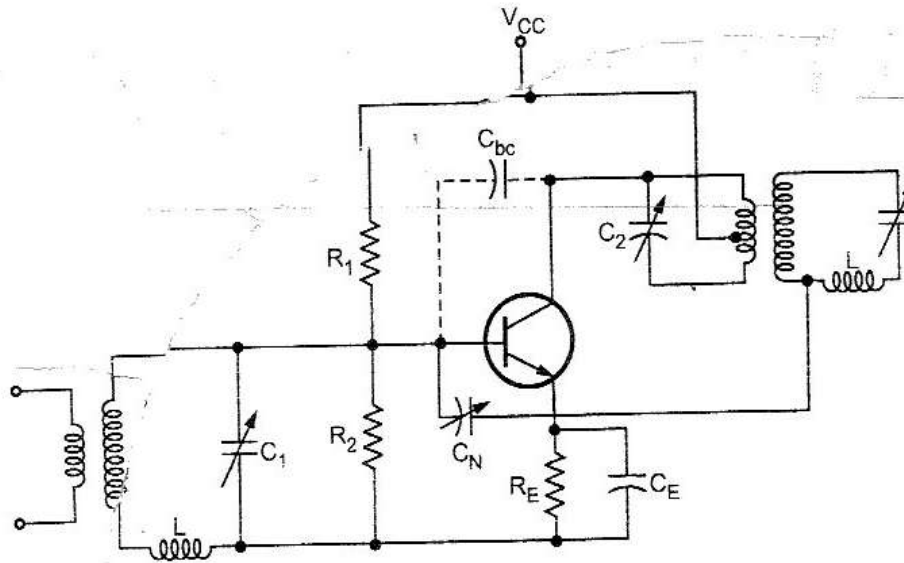


Fig. 3.38 Tuned RF amplifier using coil

3.10.4 Rice Neutralization

The Fig. 3.39 shows the Rice circuit of neutralization. It uses a centre tapped coil in the base circuit. With this arrangement the signal voltages at the ends of the tuned base coil are equal and out of phase.

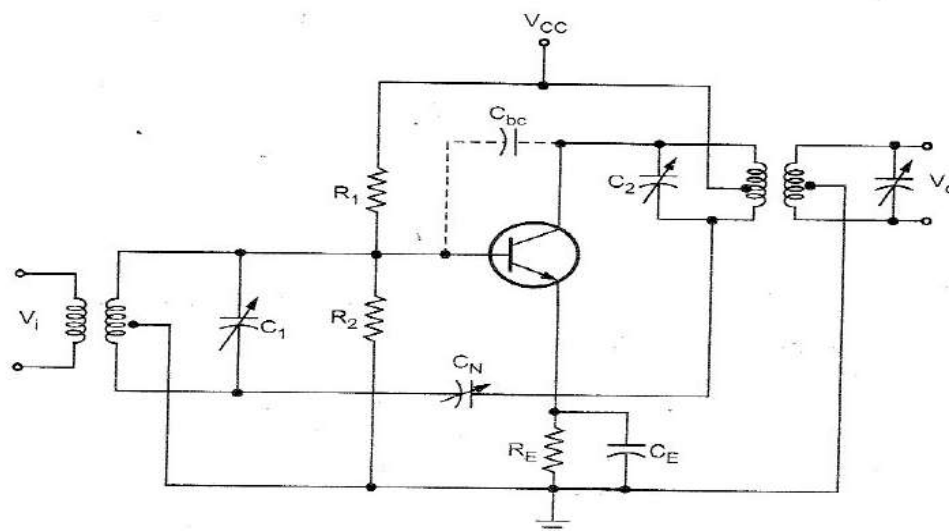


Fig. 3.39 Tuned RF amplifier using Rice neutralization

3.11 Advantages and Disadvantages of Tuned Amplifiers

Advantages :

- 1) They amplify defined frequencies.
- 2) Signal to noise ratio at output is good.
- 3) They are well suited for radio transmitters and receivers.
- 4) The band of frequencies over which amplification is required can be varied.

Disadvantages :

- 1) Since they use inductors and capacitors as tuning elements, the circuit is bulky and costly.
- 2) If the band of frequency is increased, design becomes complex.
- 3) They are not suitable to amplify audio frequencies.

3.12 Applications of Tuned Amplifiers

The important applications of tuned amplifiers are as follows :

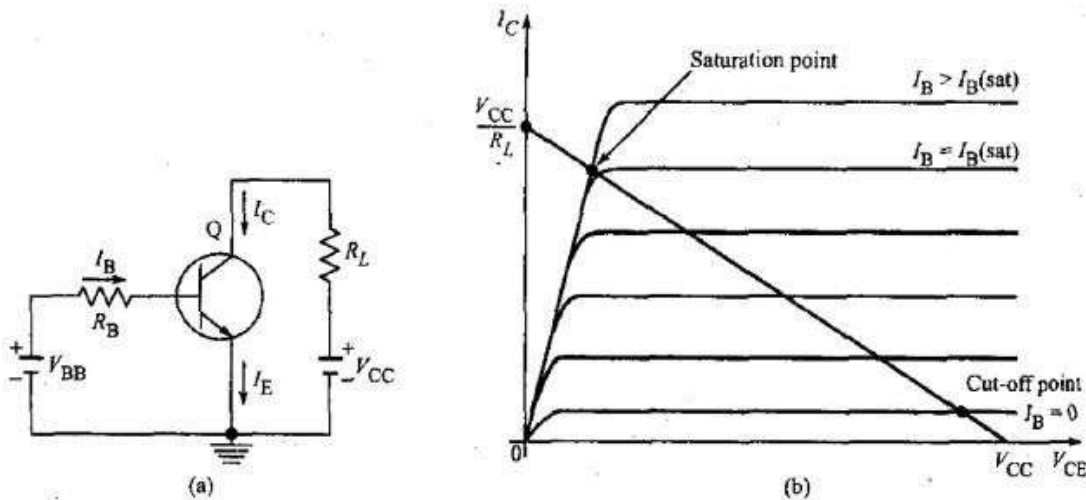
1. Tuned amplifiers are used in radio receivers to amplify a particular band of frequencies for which the radio receiver is tuned.
2. Tuned class B and class C amplifiers are used as an output RF amplifiers in radio transmitters to increase the output efficiency and to reduce the harmonics.
3. Tuned amplifiers are used in active filters such as low pass, high pass and band pass to allow amplification of signal only in the desired narrow band.

UNIT IV MULTIVIBRATORS

TRANSISTOR AS A SWITCH

A transistor can be used as a switch. It has three regions of operation. When both Emitter-to-base and collector-base junctions are reverse biased, the transistor operates in the cut-off region and it acts as an open switch. When the emitter base junction is forward biased and the Collector base junction is reverse biased, it operates in the active region and acts as an amplifier. When both the emitter-base and collector-base junctions are forward biased, it operates in the saturation region and acts as a closed switch. When the transistor is switched! from cut-off to saturation and from saturation to cut-off with negligible active region, the transistor is operated as a switch. When the transistor is in saturation, junction voltages are very small but the operating currents are large. When the transistor is in cut-off, the currents are zero (except small leakage current) but the junction voltages are large.

In Below Figure the transistor Q can be used to connect and disconnect the load R_L from the source V_{CC} When Q is saturated it is like a closed switch from collector to emitter and when Q is cutoff it is like an open switch from collector to emitter.



$$I_C = \frac{V_{CC} - V_{CE}}{R_L} \quad \text{and} \quad I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

Referring to the output characteristics shown in Figure (b), the region below the $I_B = 0$ curve is the cut-off region. The intersection of the load line with $I_B = 0$ curve is the cut-off point. At this point, the base current is zero and the collector current is negligible. The emitter diode comes out of forward bias and the normal transistor action is lost, i.e, $V_{CE}(\text{cut-off}) = V_{CC}$. The transistor appears like an open switch.

The intersection of the load line with the $I_B = I_{B(sat)}$ curve is called the saturation point. At this point, the base current is $I_{B(sat)}$ and the collector current is maximum. At saturation, the collector diode comes out of cut-off and again the normal transistor action is lost, i.e. $I_{C(sat)} = V_{CC} / R_L$. $I_{B(sat)}$ represents the minimum base current required to bring the transistor into saturation. For $0 < I_B < I_{B(sat)}$, the transistor operates in the active region. If the base current is greater than $I_{B(sat)}$, the collector current approximately equals V_{CC} / R_L and the transistor appears like a closed switch.

TRANSISTOR SWITCHING TIMES

When the transistor acts as a switch, it is either in cut-off or in saturation. To consider the behaviour of the transistor as it makes transition from one state to the other, consider the circuit shown in below figure (a) driven by the pulse waveform shown in Figure (b). The pulse waveform makes transitions between the voltage levels V_2 and V_1 . At V_2 the transistor is at cutoff and at V_1 the transistor is in saturation. The input waveform v_i is applied between the base and the emitter through a resistor R_B .

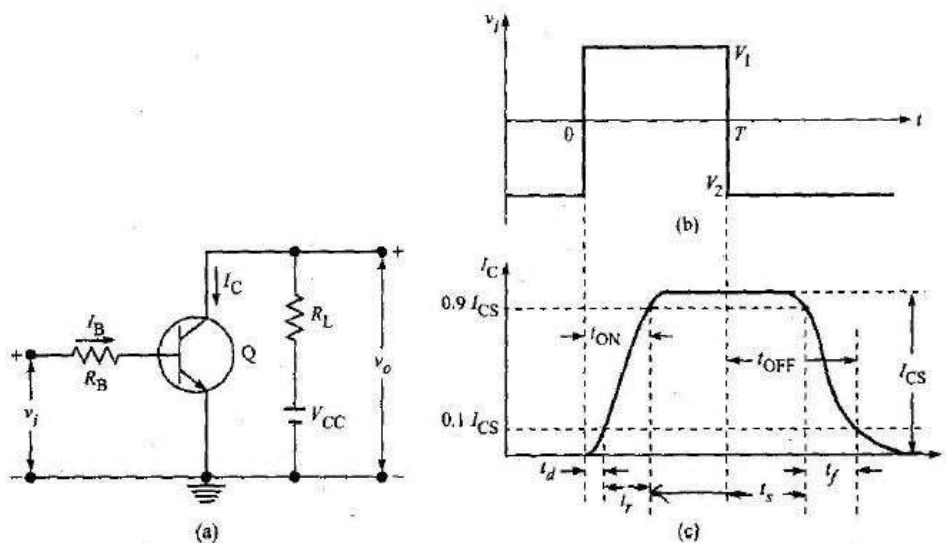


Figure a) Transistor as a Switch b) input waveform c) the response of collector current versus time

The response of the collector current i_C to the input waveform, together with its time relationship to the waveform is shown in Figure (c). The collector current does not immediately respond to the input signal. Instead there is a delay, and the time that elapses during this delay, together with the time required for the current to rise to 10% of its maximum (saturation) value ($I_{CS} = V_{CC} / R_L$) is called the delay time t_d . The current waveform has a nonzero rise time t_r , which

is the rise time required for the current to rise from 10% to 90% of I_{cs} - The total turn-on time T_{ON} is the sum of the *delay time* and the rise time, i.e. $T_{ON} = t_d + t_r$.

When the input signal returns to its initial state, the collector current again fails to respond immediately. The interval which elapses between the transition of the input waveform and the time when I_c has dropped to 90% of I_{cs} is called the *storage time* t_s . The storage interval is followed by the fall time t_f , which is the time required for I_c to fall from 90% to 10% of I_{cs} - The turn-off time t_{OFF} is defined as the sum of the storage and fall times, i.e. $t_{OFF} = t_s + t_f$ We shall now consider the physical reasons for the existence of each of these times.

The delay time

There are three factors that contribute to the delay time. First there is a delay which results from the fact that, when the driving signal is applied to the transistor input, a non-zero time is required to charge up the junction capacitance so that the transistor may be brought, from cut-off to the active region. Second, even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a nonzero time is required before these carriers can cross the base region to the collector junction and be recorded as collector current. Finally, a nonzero time is required before the collector current can rise to 10% of its maximum value. Rise time and fall time. The rise time and fall time are due to the fact that, if a base current step is used to saturate the transistor or to return it from saturation into cutoff, the collector current must traverse the active region. The collector current increases or decreases along an exponential curve. Storage time The failure of the transistor to respond to the trailing edge of the driving pulse for the time interval t_s , results from the fact that a transistor in saturation has a saturation charge of excess minority carriers stored in the base. The transistor cannot respond until the saturation excess charge has been removed.

MULTIVIBRATORS

Multi means many; vibrator means oscillator. A circuit which can oscillate at a number of frequencies is called a multivibrator. Basically there are three types of multivibrators:

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

Each of these multivibrators has two states. As the names indicate, a bistable multivibrator has got two stable states, a monostable multivibrator has got only one stable state (the other state being quasi stable) and the astable multivibrator has got no stable state (both the

states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

BISTABLE MULTIVIBRATOR

A bistable multivibrator is a multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling). The bistable multivibrator is also called a multi, Eccles-Jordan circuit (after its inventors), trigger circuit, scale-of-two toggle circuit, flip-flop, and binary. There are two types of bistable multivibrators:

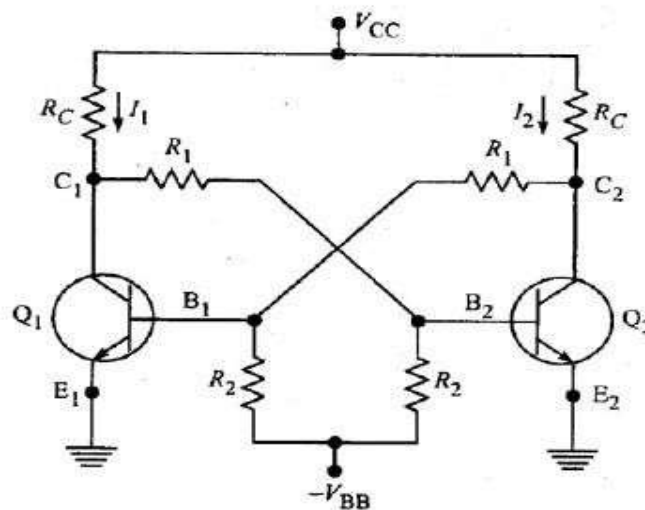
1. Collector coupled bistable multivibrator
2. Emitter coupled bistable multivibrator

There are two types of collector-coupled bistable multivibrators:

1. Fixed-bias bistable multivibrator
2. Self-bias bistable multivibrator

A FIXED-BIAS BISTABLE MULTIVIBRATOR

The Figure below shows the circuit diagram of a fixed-bias bistable multivibrator using transistors (inverters). Note, that the output of each amplifier is direct coupled to the input of the other amplifier.



In one of the stable states, transistor Q_1 is ON (i.e. in saturation) and Q_2 is OFF (i.e. in cut-off), and in the other stable state Q_1 is OFF and Q_2 is ON. Even though the circuit is symmetrical, it is not possible for the circuit to remain in a stable state with both the transistors conducting (i.e. both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents I_1 and I_2 and suppose there is a minute fluctuation in the current I_1 —let us say it increases by a small amount—then the voltage at the collector of Q_1 decreases. This will result in a decrease in voltage at the base of Q_2 . So Q_2 conducts less and I_2 decreases and hence the potential at the collector of Q_2 increases. This results in an increase in the base potential of Q_1 . So, Q_1 conducts still more and I_1 is further increased and the potential at the collector of Q_1 is further reduced, and so on. So, the current I_1 keeps on increasing and the current I_2 keeps on decreasing till Q_1 goes into saturation and Q_2 goes into cut-off. This action takes place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one. *A stable state of a binary is one in which the voltages and currents satisfy the Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than unity is satisfied.*

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is in cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temperature changes or the devices age and the device parameters vary, the quiescent point changes and the quiescent output voltage may also change appreciably. Sometimes the drift may

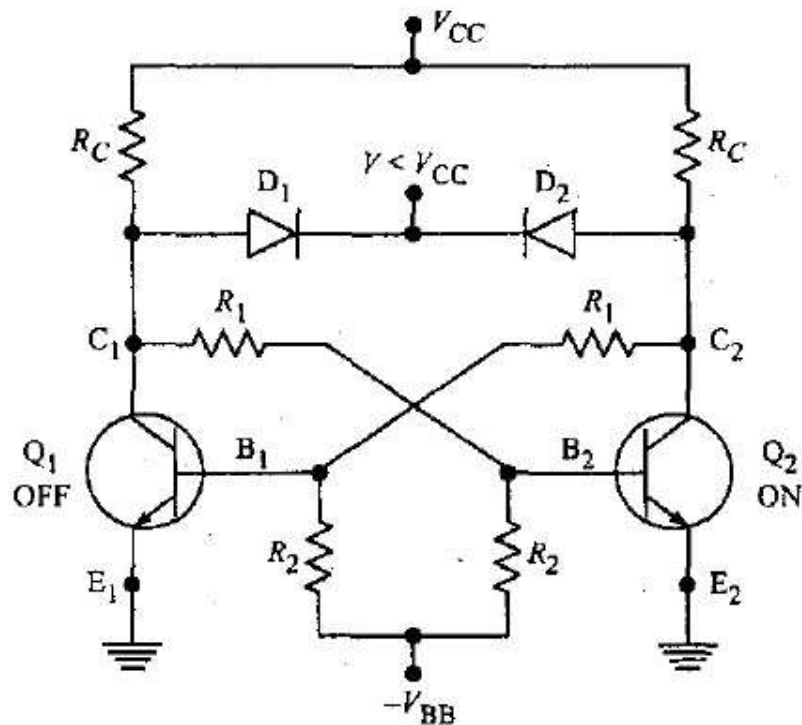
be so much that the device operating in the active region may go into cut-off, and with both the devices in cut-off the circuit will be useless.

Selection of components in the fixed-bias bistable multivibrator

In the fixed-bias binary shown in Figure 4.1., nearly the full supply voltage V_{CC} will appear across the transistor that is OFF. Since this supply voltage V_{CC} is to be reasonably smaller than the collector breakdown voltage SV_{ce} . V_{CC} restricted to a maximum of a few tens of volts. Under saturation conditions the collector current I_c is maximum. Hence RC must be chosen so that this value of C ($= V_{CC}/\Delta V$) does not exceed the maximum permissible limit. The values of R_1 , R_2 and V_{BB} must be selected such that in one stable state the base current is large enough to drive the transistor into saturation whereas in the second stable state the emitter junction must be below cut-off. The signal at a collector called the output swing V_w is the change in collector voltage resulting from a transistor going from one state to the other, i.e. $V_w = V_{C1} - V_{C2}$. If the loading caused by R_L can be neglected, then the collector voltage of the OFF transistor is V_{CC} . Since the collector saturation voltage is few tenths of a volt, then the swing $V_w = V_{CC}$, independently of R_Q . The component values, the supply voltages and the values of β_{CBO} , h_{fe} , $V_{BE}(sat)$, and $V_{CE}(sat)$ are sufficient for the analysis of transistor binary circuits.

Loading

The bistable multivibrator may be used to drive other circuits and hence at one or both the collectors there are shunting loads, which are not shown in Figure 4.1. These loads reduce the magnitude of the collector voltage V_{C1} of the OFF transistor. This will result in reduction of the output voltage swing. A reduced V_{C1} will decrease V_{B2} and it is possible that Q_2 may not be driven into saturation. Hence the flip-flop circuit components must be chosen such that under the heaviest load, which the binary drives, one transistor remains in saturation while the other is in cut-off. Since the resistor R_L also loads the OFF transistor, to reduce loading, the value of R_L should be as large as possible compared to the value of R_c . But to ensure a loop gain in excess of unity during the transition between the states, R_L should be selected such that For some applications, the loading varies with the operation being performed. In such cases, the extent to which a transistor is driven into saturation is variable. A constant output swing $V_w = V$, and a constant base saturation current I_{B2} can be obtained by clamping the collectors to an auxiliary voltage $V < V_{CC}$ through the diodes D_1 and D_2 as indicated in Figure 4.2. As Q_1 cuts OFF, its collector voltage rises and when it reaches V , the "collector catching diode" D_1 conducts and clamps the output to V .



Standard specifications

In the cut-off region, i.e. for the OFF state

$$V_{BE} \text{ (cut-off)} : \leq 0 \text{ V for silicon transistor} \\ \leq -0.1 \text{ V for germanium transistor}$$

In the saturation region, i.e. for the ON state

$$V_{BE} \text{ (sat)} : 0.7 \text{ V for silicon transistor} \\ 0.3 \text{ V for germanium transistor} \\ V_{CE} \text{ (sat)} : 0.3 \text{ V for silicon transistor} \\ 0.1 \text{ V for germanium transistor}$$

The above values hold good for n-p-n transistors. For p-n-p transistors the above values with opposite sign are to be taken.

Test for saturation

To test whether a transistor is really in saturation or not evaluate the collector current i_C and the base current i_B independently.

If $i_B > i_B \text{ (min)}$, where $i_B \text{ (min)} = i_C / h_{FE} \text{ (min)}$ the transistor is really in saturation.

If $i_B \leq i_B \text{ (min)}$, the transistor is not in saturation.

Test for cut-off

To test whether a transistor is really cut-off or not, find its base-to-emitter voltage. If V_{BE} is negative for an n-p-n transistor or positive for a p-n-p transistor, the transistor is really cut-off.

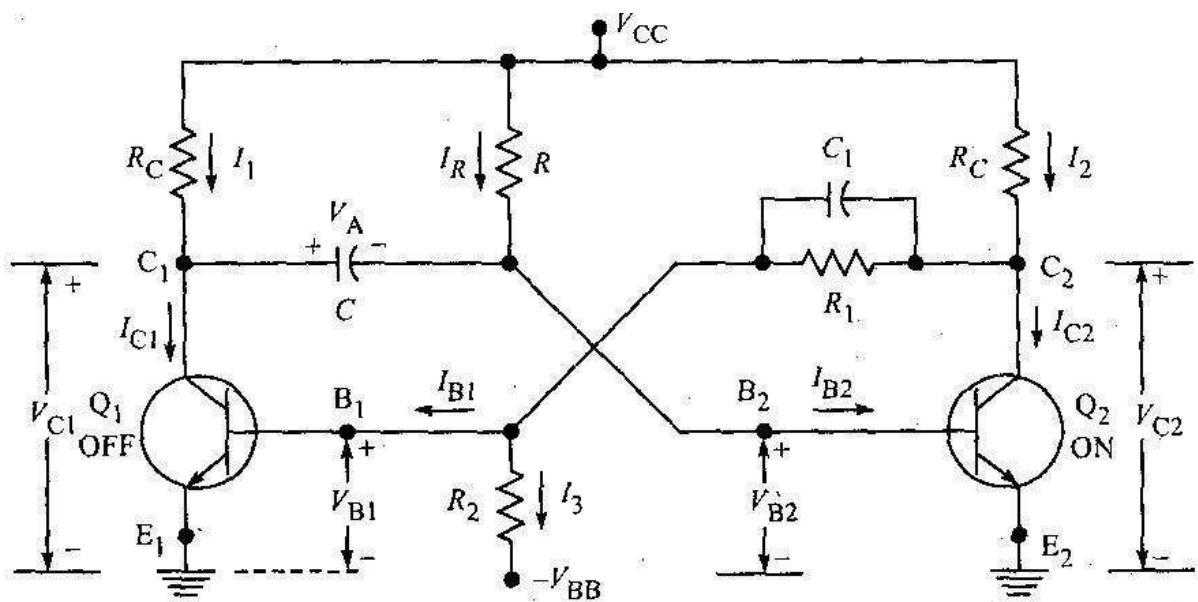
MONOSTABLE MULTIVIBRATOR

Monostable Multivibrators have only **one** stable state (hence their name: "Mono"), and produce a single output pulse when it is triggered externally. Monostable multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

Monostable multivibrators or "One-Shot Multivibrators" as they are also called, are used to generate a single output pulse of a specified width, either "HIGH" or "LOW" when a suitable external trigger signal or pulse T is applied. This trigger signal initiates a timing cycle which causes the output of the monostable to change its state at the start of the timing cycle and will remain in this second state, which is determined by the time constant of the timing capacitor, C_T and the resistor, R_T until it resets or returns itself back to its original (stable) state. It will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Then, **Monostable Multivibrators** have only **ONE** stable state and go through a full cycle in response to a single triggering input pulse.

THE COLLECTOR COUPLED MONOSTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-to-base coupled (simply called collectorcoupled) monostable multivibrator using n-p-n transistors. The collector of Q_2 is coupled to the base of Q_1 by a resistor R_f (dc coupling) and the collector of Q_1 is coupled to the base of Q_2 by a capacitor C (ac coupling). C_i is the commutating capacitor introduced to increase the speed of operation. The base of Q_1 is connected to $-V_{BB}$ through a resistor R_2 , to ensure that Q_1 is cut off under quiescent conditions. The base of Q_2 is connected to V_{CC} through R to ensure that Q_2 is ON under quiescent conditions. In fact, R may be returned to even a small positive voltage but connecting it to V_{CC} is advantageous. The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q_2 ON (i.e. in saturation) and Q_1 OFF (i.e. in cut-off)- The multivibrator may be induced to make a transition out of its stable state by the application of a negative trigger at the base of Q_2 or at the collector of Q_1 . Since the triggering signal is applied to only one device and not to both the devices simultaneously, unsymmetrical triggering is employed. When a negative signal is applied at the base of Q_2 at $t \sim 0$, due to regenerative action Q_2 goes to OFF state and Q_1 goes to ON state. When Q_1 is ON, a current I_i flows through its R_c and hence its collector voltage drops suddenly by $I_i R_c$. This drop will be instantaneously



transmitted through the coupling capacitor C to the base of Q_2 . So at $t = 0+$, the base voltage of Q_2 is

$$V_{BE}(\text{sat}) - I_1 R_C$$

The circuit cannot remain in this state for a long time (it stays in this state only for a finite time T) because when Q_1 conducts, the coupling capacitor C charges from V_{CC} through the conducting transistor Q_1 and hence the potential at the base of Q_2 rises exponentially with a time constant

$(R + R_o)C \approx RC$, where R_o is the conducting transistor output impedance including the resistance R_C . When it passes the cut-in voltage V_y of Q_2 (at a time $t = T$), a regenerative action takes place turning Q_1 OFF and eventually returning the multivibrator to its initial stable state. The transition from the stable state to the quasi-stable state takes place at $t = 0$, and the reverse transition from the quasi-stable state to the stable state takes place at $t = T$. The time T for which the circuit is in its quasi-stable state is also referred to as the delay time, and also as the gate width, pulse width, or pulse duration. The delay time may be varied by varying the time constant $t(= RC)$.

Expression for the gate width T of a monostable multivibrator neglecting the reverse saturation current /CBO

The below Figure (a) shows the waveform at the base of transistor Q_2 of the monostable multivibrator

For $t < 0$, Q2 is ON and so $v_{B2} = V_{BE(sat)}$. At $t = 0$, a negative signal applied brings Q2 to OFF state and Q1 into saturation. A current I flows through R_C of Q1 and hence v_{C1} drops abruptly by $I R_C$ volts and so v_{B2} also drops by $I R_C$ instantaneously. So at $t = 0^+$, $v_{B2} = V_{BE(sat)} - I R_C$. For $t > 0$, the capacitor charges with a time constant RC , and hence the base voltage of Q2 rises exponentially towards V_{CC} with the same time constant. At $t = T$, when this base voltage rises to the cut-in voltage level V_γ of the transistor, Q2 goes to ON state, and Q1 to OFF state and the pulse ends. In the interval $0 < t < T$, the base voltage of Q2, i.e. v_{B2} is given by

$$v_{B2} = V_{CC} - (V_{CC} - \{V_{BE(sat)} - I_1 R_C\})e^{-t/\tau}$$

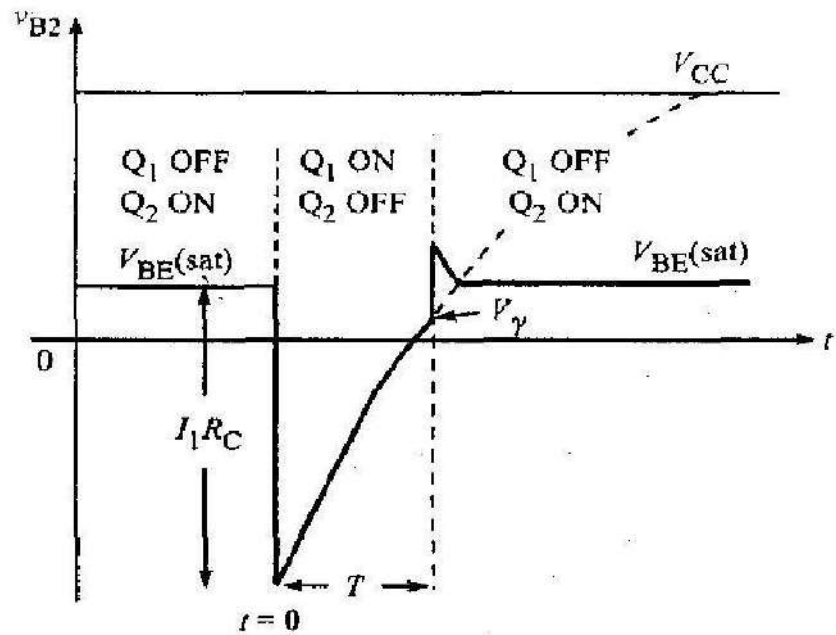


Fig a) Voltage variation at the base of Q2 during the quasi-stable state

But $I_1 R_C = V_{CC} - V_{CE(sat)}$ (because at $t = 0^-$, $v_{C1} = V_{CC}$ and at $t = 0^+$, $v_{C1} = V_{CE(sat)}$)

$$\therefore v_{B2} = V_{CC} - [V_{CC} - \{V_{BE(sat)} - (V_{CC} - V_{CE(sat)})\}]e^{-t/\tau}$$

$$= V_{CC} - [2V_{CC} - \{V_{BE(sat)} + V_{CE(sat)}\}]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore V_\gamma = V_{CC} - [2V_{CC} - \{V_{CE(sat)} + V_{BE(sat)}\}]e^{-T/\tau}$$

$$\text{i.e. } e^{T/\tau} = \frac{2V_{CC} - \{V_{CE(sat)} + V_{BE(sat)}\}}{V_{CC} - V_\gamma}$$

$$\therefore \frac{T}{\tau} = \ln \left[2 \left(V_{CC} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2} \right) \right]$$

$$\frac{T}{\tau} = \ln \left[\frac{2V_{CC} - V_{CE(sat)} - V_{BE(sat)}}{V_{CC} - V_\gamma} \right]$$

$$\text{i.e. } T = \tau \ln 2 + \tau \ln \frac{V_{CC} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2}}{V_{CC} - V_\gamma}$$

Normally for a transistor, at room temperature, the cut-in voltage is the average of the saturation junction

$$V_{\gamma} = \frac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}$$

voltages for either Ge or Si transistors, i.e.

Neglecting the second term in the expression for T

$$T = \tau \ln 2$$

$$T = (R + R_o)C \ln 2 = 0.693(R + R_o)C$$

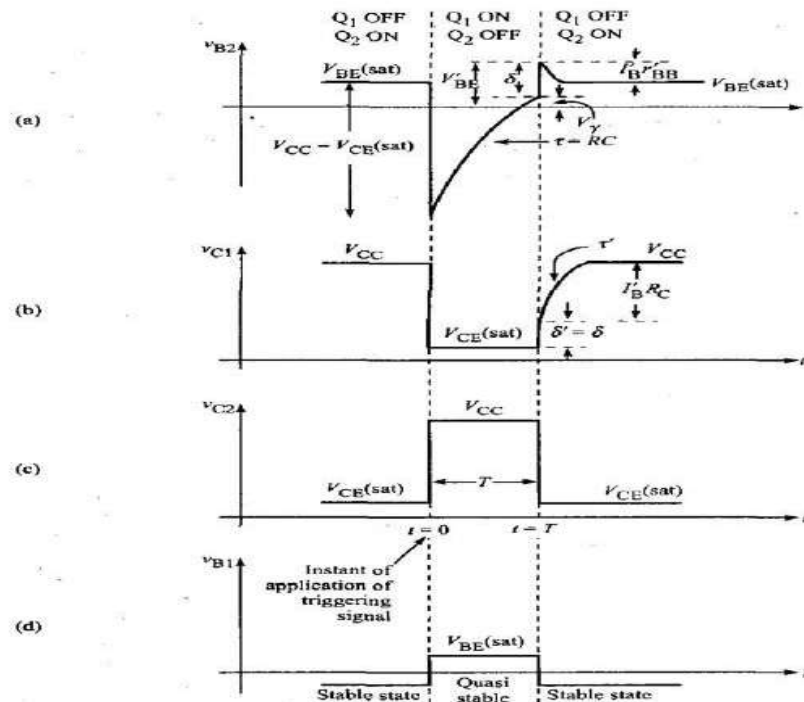
but for a transistor in saturation $R_o \ll R$.

$$\text{Gate width, } T = 0.693RC$$

The larger the V_{CC} is, compared to the saturation junction voltages, the more accurate the result is. The gate width can be made very stable (almost independent of transistor characteristic supply voltages, and resistance values) if Q1 is driven into saturation during the quasi-stable state.

Waveforms of the collector-coupled monostable multivibrator

The waveforms at the collectors and bases of both the transistors Q1 and Q2 are shown below



(a) at the base of Q2, (b) at the collector of Q1, (c) at the collector of Q2, and (d) at the base of Q1

ASTABLE MULTIVIBRATOR

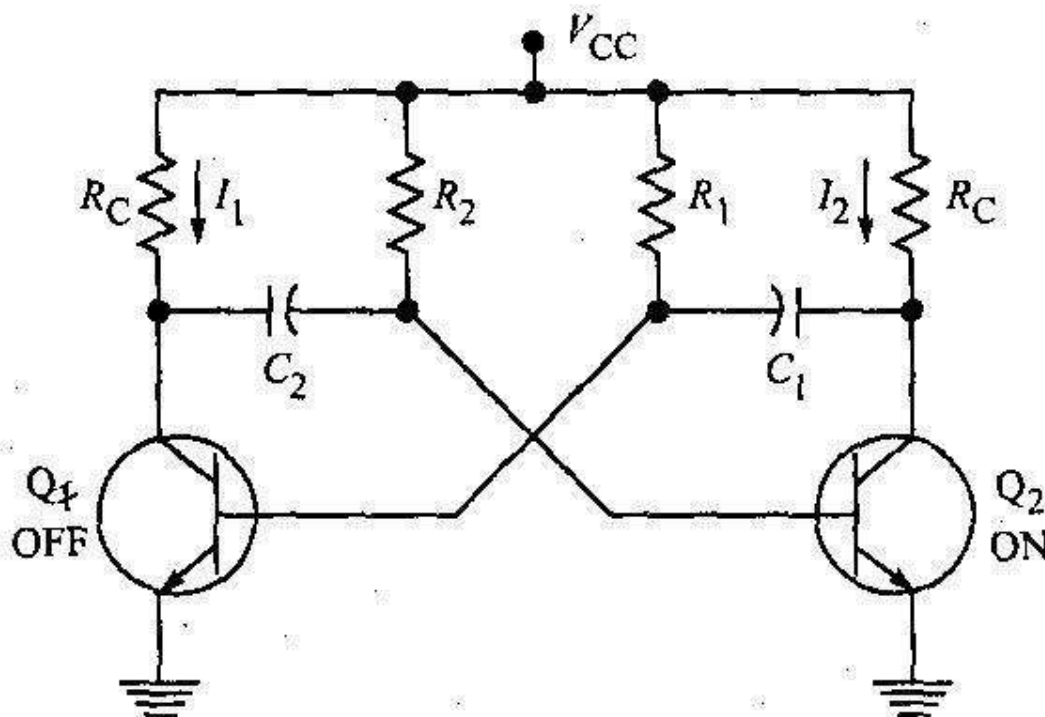
As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

There are two types of astable multivibrators:

1. Collector-coupled astable multivibrator
2. Emitter-coupled astable multivibrator

THE COLLECTOR-COUPLED ASTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-coupled astable multivibrator using n-p-n transistors. The collectors of both the transistors Q_1 and Q_2 are connected to the bases



of the other transistors through the coupling capacitors C_1 and C_2 . Since both are ac couplings, neither transistor can remain permanently at cut-off. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states. Hence it is used as a master oscillator. No triggering signal is required for this multivibrator. The component values are selected such that, the moment it is connected to the supply, due to supply transients one

transistor will go into saturation and the other into cut-off, and also due to capacitive couplings it keeps on oscillating between its two quasi stable states.

The waveforms at the bases and collectors for the astable multivibrator, are shown in below Figure. Let us say at $t = 0$, Q2 goes to ON state and Q1 to OFF state. So, for $t < 0$, Q2 was OFF and Q1 was ON

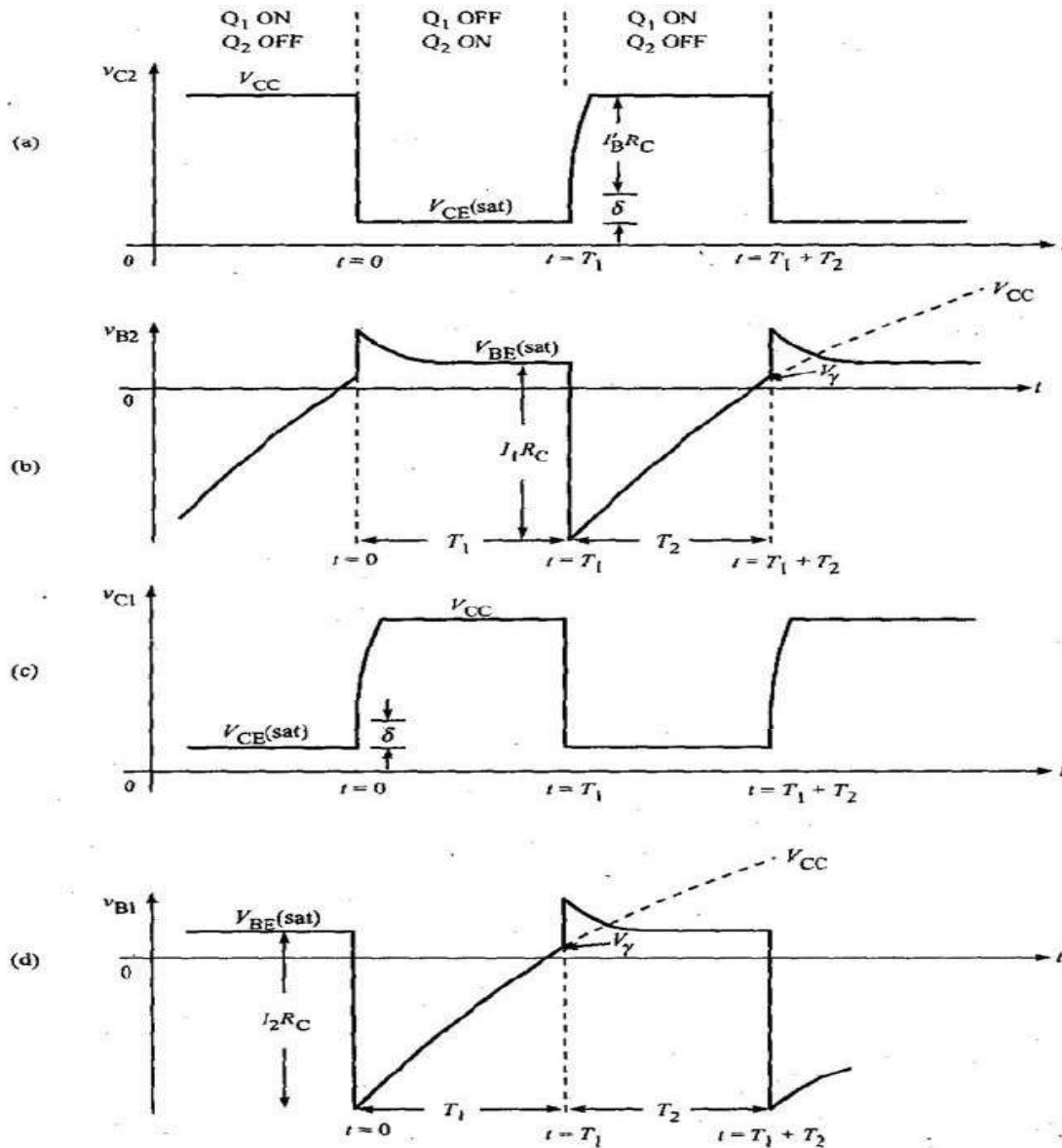


Fig: waveforms at the bases and collectors of a collector-coupled astable multivibrator

Hence for $t < 0$, v_{B2} is negative, $v_{C2} = V_{CC}$, $v_{B1} = V_{BE(sat)}$ and $v_{C1} = V_{CE(sat)}$. The capacitor C_2 charges from V_{CC} through R_2 and v_{B2} rises exponentially towards V_{CC} . At $t = 0$, v_{B2} reaches the cut-in voltage V_Y and Q_2 conducts. As Q_2 conducts, its collector voltage v_{C2} drops by $I_B R_C - V_{CE(sat)}$. This drop in v_{C2} is transmitted to the base of Q_1 through the coupling capacitor C_2 .

and hence v_{B1} also falls by $V_{CE(sat)}$. Q_1 goes to OFF state. So, $V_{B1} = V_{BE(sat)} - V_{CE(sat)}$, and its collector voltage v_{C1} rises towards V_{CC} . This rise in v_{C1} is coupled through the coupling capacitor C_2 to the base of Q_2 , causing an overshoot δ in v_{B2} and the abrupt rise by the same amount δ in V_{C1} as shown in Figure 4.51(c). Now since Q_2 is ON, C_2 charges from V_{CC} through R_2 and hence V_{B1} rises exponentially. At $t = T_1$, when V_{B1} rises to V_Y , Q_1 conducts and due to regenerative action Q_1 goes into saturation and Q_2 to cut-off. Now, for $t > T_1$, the coupling capacitor C_2 charges from V_{CC} through R_2 and at $t = T_1 + T_2$, when v_{B2} rises to the cut-in voltage V_r , Q_2 conducts and due to regenerative feedback Q_2 goes to ON state and Q_1 to OFF state. The cycle of events repeats and the circuit keeps on oscillating between its two quasi-stable states. Hence the output is a square wave. It is called a square wave generator or square wave oscillator or relaxation oscillator. It is a free running oscillator.

Expression for the frequency of oscillation of an astable multivibrator

Consider the waveform at the base of Q_1 shown in Figure 4.54(d). At $t = 0$,

$$v_{B1} = V_{BE(sat)} - I_2 R_C$$

But

$$I_2 R_C = V_{CC} - V_{CE(sat)}$$

$\therefore$

$$\text{At } t = 0, v_{B1} = V_{BE(sat)} - V_{CC} + V_{CE(sat)}$$

For $0 < t < T_1$, v_{B1} rises exponentially towards V_{CC} given by the equation,

$$v_o = v_f - (v_f - v_i)e^{-t/\tau}$$

$$\therefore v_{B1} = V_{CC} - [V_{CC} - (V_{BE(sat)} - V_{CC} + V_{CE(sat)})]e^{-t/\tau_1}, \text{ where } \tau_1 = R_1 C_1$$

At $t = T_1$, when v_{B1} rises to V_Y , Q_1 conducts

$$\therefore V_Y = V_{CC} - [2V_{CC} - (V_{BE(sat)} + V_{CE(sat)})]e^{-T_1/R_1 C_1}$$

or

$$e^{T_1/R_1 C_1} = \frac{2 \left[V_{CC} - \frac{V_{BE(sat)} + V_{CE(sat)}}{2} \right]}{V_{CC} - V_Y}$$

$$T_1 = R_1 C_1 \ln \frac{2 \left[V_{CC} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2} \right]}{V_{CC} - V_Y}$$

$$T_1 = R_1 C_1 \ln 2 + R_1 C_1 \ln \frac{\left[V_{CC} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2} \right]}{V_{CC} - V_Y}$$

At room temperature for a transistor,

$$V_Y = \frac{V_{CE(sat)} + V_{BE(sat)}}{2}$$

$\therefore$

$$T_1 = R_1 C_1 \ln 2 = 0.693 R_1 C_1$$

On similar lines considering the waveform of above Figure , we can show that the time T_2 for which Q_2 is OFF and Q_1 is ON is given by The period of the waveform, The frequency of oscillation, If $R_1 = R_2 = R$, and $C_1 = C_2 = C$, then $T_1 = T_2 = T$.

$$T = 2 \times 0.693RC = 1.386RC \quad \text{and} \quad f = \frac{1}{1.386RC}$$

The frequency of oscillation may be varied over the range from cycles to mega cycles by varying RC . It is also possible to vary the frequency electrically by connecting R_1 and R_2 to an auxiliary voltage source V (the collector supply remains $+V_{CC}$) and then varying this voltage V .

THE EMITTER-COUPLED ASTABLE MULTIVIBRATOR

An emitter-coupled astable multivibrator may be obtained by using three power supplies or a single power supply. The below Figure (a) shows the circuit diagram of a free-running emitter coupled multivibrator using n-p-n transistors. Figure 4.64 shows its waveforms. Three power supplies are indicated for the sake of simplifying the analysis. A more practical circuit using a single supply is indicated in below Figure (b). Let us assume that the circuit operates in such a manner that Q_1 switches between cut-off and saturation and Q_2 switches between cut-off and its active region.

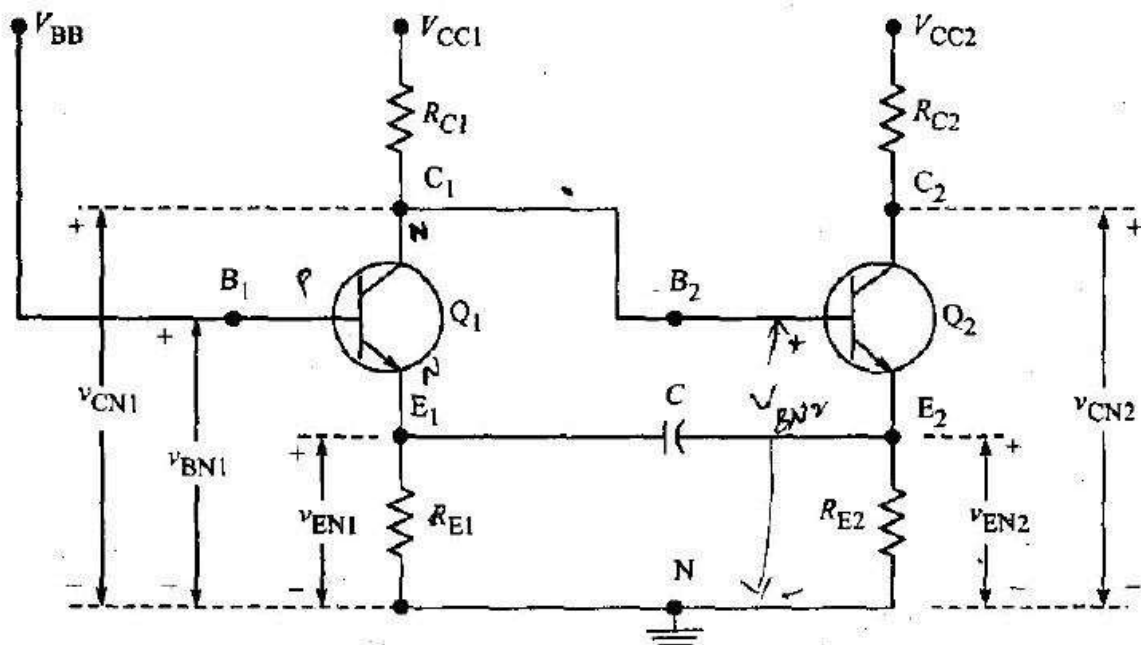


Fig a) Astable Emitter-Coupled Multivibrator

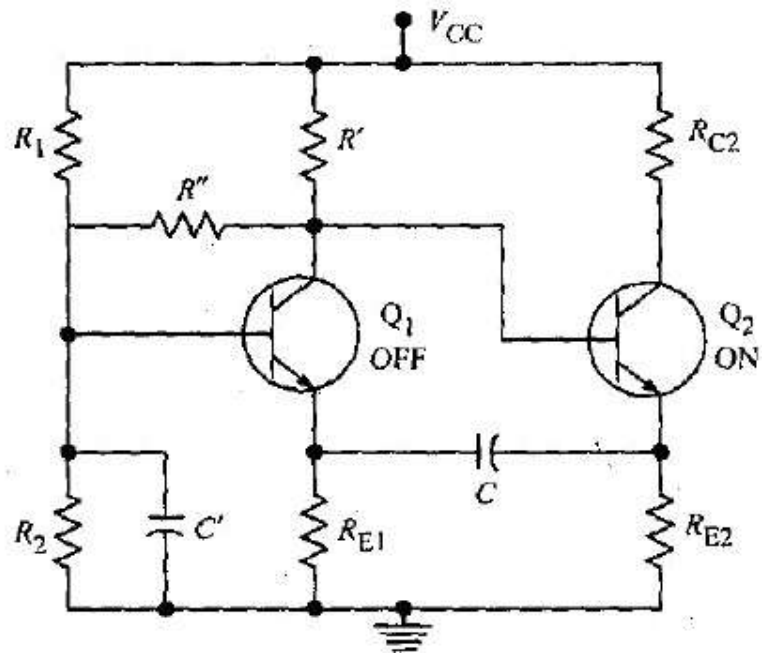


Fig b) Emitter Coupled multivibrator

The waveforms at the base and collector are as shown below:

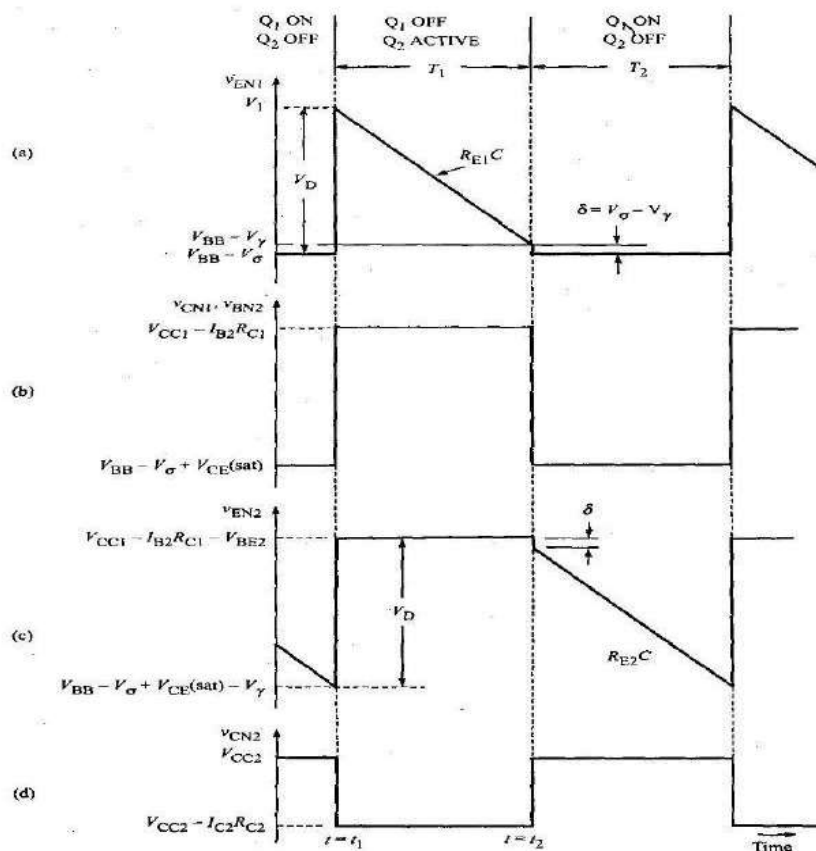


Fig waveforms of the emitter-coupled astable multivibrator

Advantages

1. It is inherently self-starting.
2. The collector of Q2 where the output is taken may be loaded heavily even capacitively.
3. The output is free of recovery transients.
4. Because it has an isolated input at the base of Q1, synchronization is convenient.
5. Frequency adjustment is convenient because only one capacitor is used.

Disadvantages

1. This circuit is more difficult to adjust for proper operating conditions.
2. This circuit cannot be operated with T_1 and T_2 widely different.
3. This circuit uses more components than does the collector-coupled circuit.

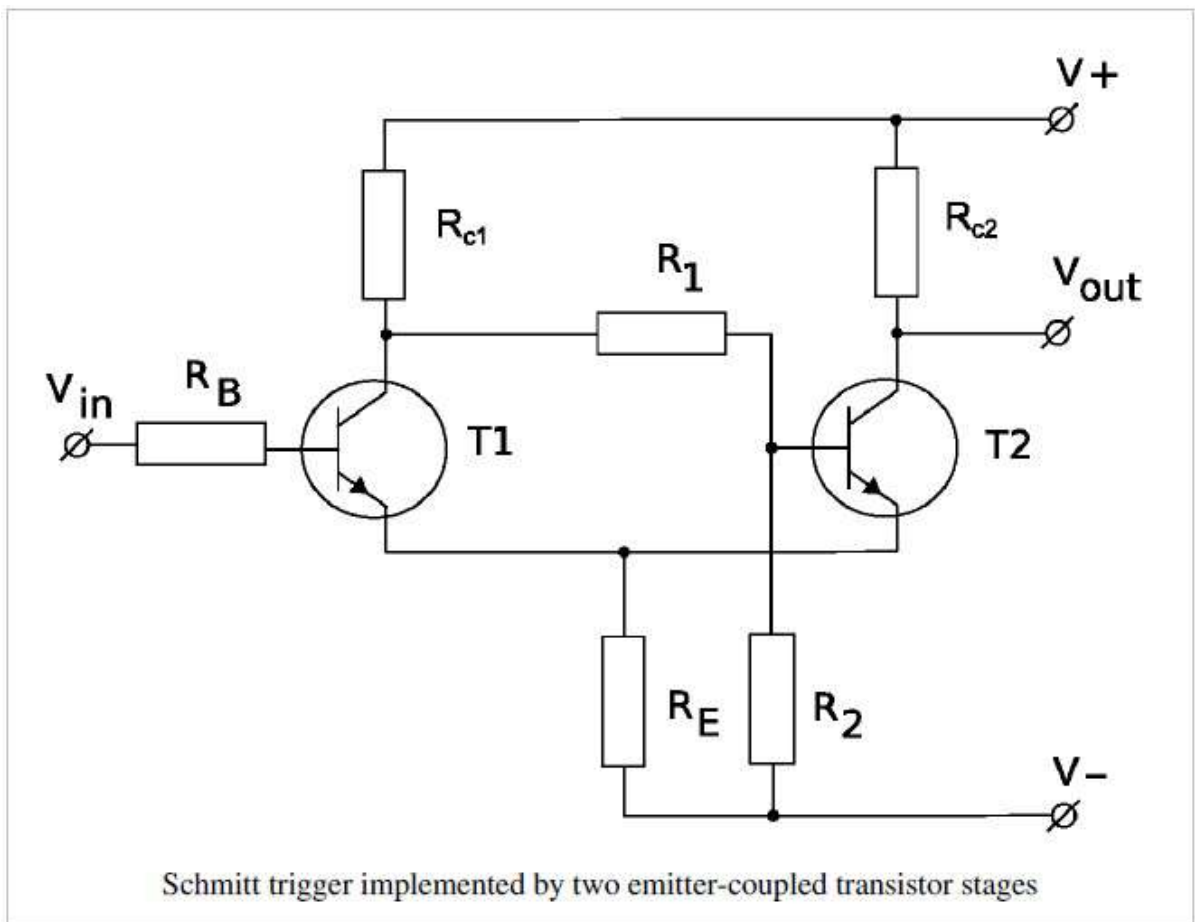
Schmitt trigger

In electronics, **Schmitt trigger** is a circuit with positive feedback and a loop gain >1 . The circuit is named "trigger" because the output retains its value until the input changes sufficiently to trigger a change: in the non-inverting configuration, when the input is higher than a certain chosen threshold, the output is high; when the input is below a different (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. This dual threshold action is called *hysteresis* and implies that the Schmitt trigger possesses memory and can act as a bi-stable circuit (latch). There is a close relation between the two kinds of circuits: a Schmitt trigger can be converted into a latch and a latch can be converted into a Schmitt trigger. Schmitt trigger devices are typically used in open-loop controller configurations for noise immunity and closed loop negative feedback configurations to implement bi-stable regulators, triangle/square wave generators, etc.

The original Schmitt trigger is based on the dynamic threshold idea that is implemented by a voltage divider with a switchable upper leg (the collector resistors R_{c1} and R_{c2}) and a steady lower leg (R_E). T_1 acts as a comparator with a differential input (T_1 base-emitter junction) consisting of an inverting (T_1 base) and a non-inverting (T_1 emitter) inputs. The input voltage is applied to the inverting input; the output voltage of the voltage divider is applied to the non-inverting input thus determining its threshold. The comparator output drives the second common collector stage T_2 (an *emitter follower*) through the voltage follower R_1 - R_2 . The emitter-coupled transistors T_1 and T_2 actually compose an electronic double throw switch that switches over the

upper legs of the voltage divider and changes the threshold in a different (to the input voltage) direction.

This configuration can be considered as a differential amplifier with series positive feedback between its non-inverting input (T2 base) and output (T1 collector) that forces the transition process. There is also a smaller negative feedback introduced by the emitter resistor R_E . To make the positive feedback dominate over the negative one and to obtain a hysteresis, the proportion between the two collector resistors is chosen $R_{c1} > R_{c2}$. Thus less current flows through and less voltage drop is across R_E when T1 is switched on than in the case when T2 is switched on. As a result, the circuit has two different thresholds in regard to ground.



Operation:

Initial state. For NPN transistors as shown, imagine the input voltage is below the shared emitter voltage (high threshold for concreteness) so that T1 base-emitter junction is backward-biased and T1 does not conduct. T2 base voltage is determined by the mentioned divider so that T2 is conducting and the trigger output is in the low state. The two resistors R_{c2} and R_E form

another voltage divider that determines the high threshold. Neglecting V_{BE} , the high threshold value is approximately

$$V_{HT} = \frac{R_E}{R_E + R_{c2}} V_+$$

The output voltage is low but well above the ground. It is approximately equal to the high threshold and may not be low enough to be a logical zero for next digital circuits. This may require additional shifting circuit following the trigger circuit.

Crossing up the high threshold:

When the input voltage (T1 base voltage) rises slightly above the voltage across the emitter resistor R_E (the high threshold), T1 begins conducting. Its collector voltage goes down and T2 begins going cut-off, because the voltage divider now provides lower T2 base voltage. The common emitter voltage follows this change and goes down thus making T1 conduct more. The current begins steering from the right leg of the circuit to the left one. Although T1 is more conducting, it passes less current through R_E (since $R_{c1} > R_{c2}$); the emitter voltage continues dropping and the effective T1 base-emitter voltage continuously increases. This avalanche-like process continues until T1 becomes completely turned on (saturated) and T2 turned off. The trigger is transitioned to the high state and the output (T2 collector) voltage is close to V_+ . Now, the two resistors R_{c1} and R_E form a voltage divider that determines the low threshold. Its value is approximately

$$V_{LT} = \frac{R_E}{R_E + R_{c1}} V_+$$

Crossing down the low threshold:

With the trigger now in the high state, if the input voltage lowers enough (below the low threshold), T1 begins cutting-off. Its collector current reduces; as a result, the shared emitter voltage lowers slightly and T1 collector voltage rises significantly. R_1 - R_2 voltage divider conveys this change to T2 base voltage and it begins conducting. The voltage across R_E rises, further reducing the T1 base-emitter potential in the same avalanche-like manner, and T1 ceases to conduct. T2 becomes completely turned-on (saturated) and the output voltage becomes low again.

ELECTRONIC CIRCUITS ANALYSIS (HM23)
DEPT. OF ELECTRONICS & COMMUNICATION ENGINEERING
IMPORTANT QUESTIONS

PART-A

2MARKS

- 1) What is the coupling schemes used in multistage amplifiers?
- 2) What are the advantages of differential amplifier?
- 3) What are the types Frequency ranges?
- 4) What are the components of feedback amplifier?
- 5) Sketch ac load line in case of class a power amplifier.
- 6) Mention the efficiency of class B amplifier
- 7) Define cross over distortion.
- 8) What are the different types of tuned Amplifiers?
- 9) Define the Astable multivibrator.
- 10) Mention the application of bistable multivibrator.
- 11) Define the Barkhausen criterion.
- 12) What is feedback Amplifier?
- 13) Define Bandwidth.
- 14) Define cascode Amplifier.
- 15) Define bandwidth in terms of frequency response.
- 16) What are the three frequency regions in an amplifier's response?
- 17) What are the components of feedback amplifier?
- 18) Sketch ac load line in case of class a power amplifier
- 19) Mention the efficiency of class B amplifier
- 20) Define cross over distortion
- 21) What are the different types of tuned Amplifiers?
- 22) Define the Astable multivibrator

PART-B

10 MARKS

1. What is Darlington pair Amplifier and derive the analysis of Voltage gain, input Impedance and Output impedance.
2. Draw the circuit diagram of TWO stage RC Coupled amplifier using BJT and explain it's Working operation with frequency response.
3. With Neat diagram explain the BJT Differential Pair Amplifiers.
4. What is Differential Pair Amplifiers with Neat diagram explain the BJT Differential Pair Amplifiers And derive the expression for gain A_d & A_{cm} .
5. Derive the expression for A_d and CMRR by using small signal operation of the MOS differential pair Amplifier.
6. What is frequency response? Explain with neat diagram low frequency response of CE Amplifier.
7. Write the comparison among the characterizes of feedback amplifier
8. Show that the bandwidth increases in negative feedback amplifiers
9. Briefly explain about the high-frequency response of the CS amplifiers.
10. What is effect of negative feedback on output resistance and derive the expression for voltage Series & Current series.

11. What are the different types of feedback amplifiers? Give their equivalent circuits.
12. Derive an expression for frequency oscillation of Hartley oscillator using transistor.
13. What is oscillator? Derive the expression for general equation of LC tuned oscillator.
14. Derive the expression for frequency of oscillation of Colpitts oscillator and explain its operation.
15. Explain Barkhausen criterion for oscillation in feedback oscillator.
16. Explain about collector coupled astable multivibrator.
17. With neat diagram explain the Class B Push pull amplifier.
18. Explain about Transformer coupled Class-A power amplifier and derive the Expression for Efficiency
19. What is power amplifier? With neat sketch explain about MOS power transistors.
20. What is tuned amplifier? Explain in detail Double tuned Amplifier.
21. Explain the operation of single stage amplifier with neat diagram.
22. With neat diagram, explain and derive expression of the class A power amplifier.
23. Define multivibrator & explain about analysis, design of monostable multivibrator.