



ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES

(AUTONOMOUS)

UTUKUR, C. K. DINNE (V & M), KADAPA, YSR DIST.

**Approved by AICTE, New Delhi & Affiliation to JNTUA, Anantapuramu.
Accredited by NAAC with 'A' Grade, Bangalore & NBA (EEE, ECE & CSE)**

**DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING**



ANALOG AND DIGITAL IC APPLICATIONS

(23HPC0412)

COURSE MATERIAL

B. TECH III YEAR I SEM

III B.Tech I Sem (E.C.E)

23HPC0412	<u>ANALOG AND DIGITAL IC APPLICATIONS</u>	L	T	P	C
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Course Objectives:

1. To introduce the classification of Integrated Circuits, internal blocks and characteristics of Op-Amp.
2. To analyse linear and non-linear applications of Op-Amp .
3. To gain knowledge on active filters, timers and phased locked loops.
4. To understand the working of Voltage Regulators and Converters.
5. To study about different types of Digital ICs and their applications.

Course Outcomes: At the end of the course, the students will be able to

1. Understand the classification of Integrated Circuits, internal blocks and characteristics of Op-Amp.
2. Analyse linear and non-linear applications of Op-Amp .
3. Gain knowledge on active filters, timers and phased locked loops.
4. Understand the working of Voltage Regulators and Converters.
5. Know about different types of Digital ICs and their applications.

UNIT I ICs and OP- AMPS

Integrated Circuits and Operational Amplifier: Introduction, Classification of IC's, IC chip size and circuit complexity, basic information of Op-Amp IC741 and its features, the ideal Operational amplifier, Op-Amp internal circuit, Op-Amp characteristics - DC and AC, Features of 741 Op-Amp.

UNIT II Applications of OP- AMP

Linear Applications of Op-Amp: Inverting, non-inverting, Differential amplifiers, adder, subtractor, Instrumentation amplifier, AC amplifier, V to I and I to V converters, Integrator and differentiator.

Non-Linear Applications of Op-Amp: Sample and Hold circuit, Log and Antilog amplifier, multiplier and divider, Comparators, Schmitt trigger, Multi vibrators, Triangular and Square waveform generators, Oscillators.

UNIT III Active Filters and other ICs

Active Filters: Introduction, Butterworth filters – 1st order, 2nd order low pass and high pass filters, band pass, band reject and all pass filters.

Timer and Phase Locked Loops: Introduction to IC 555 timer, description of functional diagram, monostable and a stable operations and applications, Schmitt trigger, PLL - introduction, basic principle, phase detector/comparator, voltage controlled oscillator (IC 566)



UNIT IV Voltage Regulators and Converters

Voltage Regulator: Introduction, Series Op-Amp regulator, IC Voltage Regulators, IC 723 general purpose regulators, Switching Regulator.

D to A and A to D Converters: Introduction, basic DAC techniques - weighted resistor DAC, R-2R ladder DAC, inverted R-2R DAC, A to D converters - parallel comparator type ADC, counter type ADC, successive approximation ADC.

UNIT V Digital ICs

CMOS Logic: CMOS logic levels, MOS transistors, Basic CMOS Inverter, NAND and NOR gates, CMOS AND-OR-INVERT and OR-AND-INVERT gates, implementation of any function using CMOS logic.

Combinational Logic IC's: Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs - Code Converters, Decoders, Encoders, Priority Encoders, Multiplexers, Demultiplexers, Parallel Binary Adder/ Subtractor, Magnitude Comparators.

Sequential Logic IC's: Familiarity with commonly available 74XX, Synchronous Counters, Decade Counters, and Shift Registers.

Textbooks:

1. D. Roy Choudhury, Shail B. Jain, —Linear Integrated Circuitsl, 4th edition (2012), New Age International Pvt.Ltd., New Delhi, India
2. Floyd, Jain, —Digital Fundamentalsl, 8th edition (2009), Pearson Education, New Delhi.

References:

1. Ramakant A. Gayakwad, —OP-AMP and Linear Integrated Circuitsl, 4th edition (2012), Prentice Hall / Pearson Education, New Delhi.
2. Sergio Franco (1997), Design with operational amplifiers and analog integrated circuits, McGraw Hill, New Delhi.
3. Gray, Meyer (1995), Analysis and Design of Analog Integrated Circuits, Wiley International, New Delhi.



Integrated Circuits

Unit-3
IC's and OP-Amps

IC's is a Miniaturized low cost electronic Circuit Consisting of active and passive Components fabricated together on a substrate (silicon)

- Miniaturized and hence Increased component density
- Batch processing results in cost reduction.
- Matched devices
- Increased operating speeds
- Better functional performance
- Reduction in power consumption
- Increased Systems reliability due to elimination of soldered joints.

Application of an IC's:

- * Communication
- * Control
- * Instrumentation
- * Computers
- * Electronics

Classifications of IC's:

1. Linear IC's - op-Amp

2. Digital IC's - Logic gates

The various technology used to fabricate these IC's

- 1) Mono Lithic Technology
- 2) Thin-Thick film Technology
- 3) Hybrid Technology (Multichip Technology)

1) Mono Lithic Technology:

The word is from "Greek Language" mono means single "Lithos" means Crystal (or) Stone.

In a mono lithic IC's all active and passive Components are fabricated on a single Silicon chip. most of the IC's are mono lithic

Advantages:

- Low Cost
- High Reliability
- It Can be made identical.

Disadvantage:

- There is no method available to fabricate transformers and large values of inductors.

Thin-Thick film Technology:

In this placing the Diodes and Transistors Connected are the discrete Components.

- Larger than the Monolithic IC's but smaller than Discrete Circuits.

Advantages:

- Better isolation between Components
- Better tolerance
- Flexibility in circuit design

Disadvantages:

- Thin-Thick film Technology can not be used to fabricate active Components.

Hybrid Technology:

- In these connecting the number of individual chip
- These used for high power audio amplification application.

IC chip Size & Circuit Complexity

Parameter	Gate level	Year
Invention of Transistor (Ge)		1947
Development of Silicon transistor		1955-1959
Silicon planar Technology		1959
SSI (Small Scale Integration)	3 to 30 Gates/chip approx. (or) 100 transistors/chip App: logic gates, flip flop	1960
MSI (Medium Scale Integration)	30 to 300 Gates/chip approx. (or) 1000 transistors/chip App: Counters, Address	1965 to 1970
LSI (Large Scale Integration)	300 to 3000 Gates/chip approx. (or) 10000 transistors/chip App: 8-bit Microprocessor RAM, ROM	1970 to 1980
VLSI Very large Scale Integration	>3000 Gates/chip approx. (or) 20,000 to 10^6 transistor/chip App: 16 bit, 32 bit Microprocessor	1980 to 1990
ULSI (Ultra Large Scale Integration)	10^6 to 10^7 transistors/chip App: 64-bit Microprocessor Small Sensors, virtual reality Machines	1990 to 2000
GIS (Giant Scale Integration)	$>10^7$ transistors/chip	-

Selection of IC :

Type

Metal Can package

DIP

Flat pack

Package criterion

- ① Heat dissipation is important
- ② for high power applications like Power Amplifier voltage Regulators etc.

③ For experimental or bread . Purposes as easy to mount

④ If bending or soldering of the leads is not measured.

⑤ Suitable for printed circuit boards as lead spacing is more.

⑥ More reliability is required

⑦ light in weight

⑧ Suitable for air born applications.

Factors affecting selection of IC package:

1. Relative cost
2. Reliability
3. Weight of the package
4. Case of fabrication
5. power to be dissipated
6. Need of external heat sink.

Temperature Ranges:

1) Military temperature range:

-55°C to $+125^{\circ}\text{C}$ (-55°C to $+85^{\circ}\text{C}$)

2) Industrial temperature range:

-20°C to $+85^{\circ}\text{C}$ (-40°C to $+85^{\circ}\text{C}$)

3) Commercial temperature Range:

0°C to $+70^{\circ}\text{C}$ (0°C to $+75^{\circ}\text{C}$)

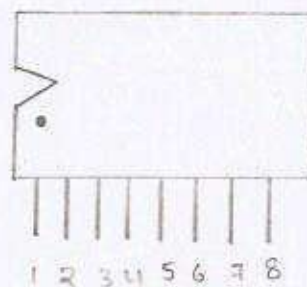
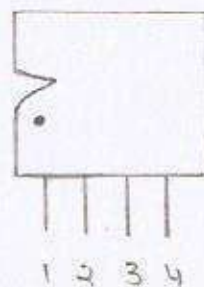
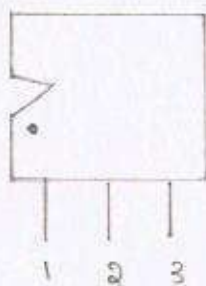
Introduction :-

Integrated Circuits (IC) play a very important part in Electronics.

Most of the IC's specially made for a specific task and contains upto thousands of Transistors, Diodes & Resistors.

Special purpose IC's such as Audio amplifiers, FM radios, logic blocks, regulators and even a whole micro computer in the form of a micro controller can be fitted inside a tiny package.

Some of simple integrated circuits are shown in below figures.



Depending on the way of manufacturing integrated circuits can be divided into two groups.

1. Hybrid
2. Monolithic

Hybrid :

Hybrid contains more than one layer.

Monolithic :

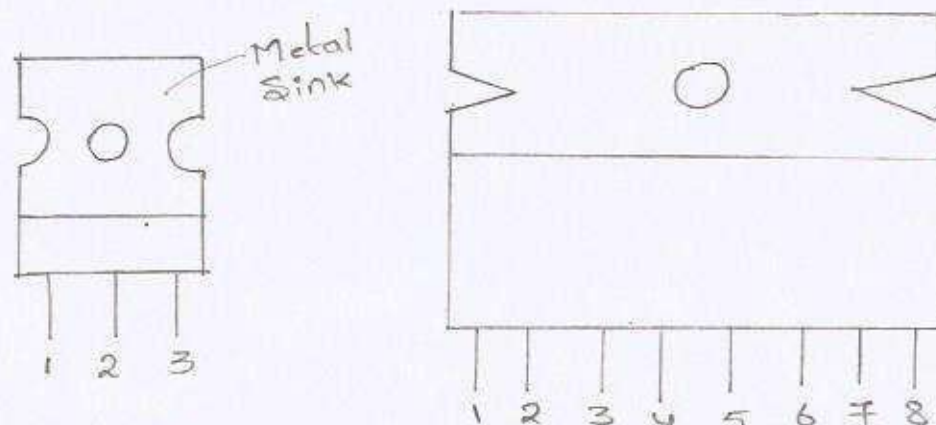
It contains only one layer.

Most of the integrated circuits are in DIL (Dual

in line) package. This means that there are two rows of pins.

The device is view from the top and the pins are numbered in an anticlockwise direction.

High power IC's can generate more heat and they have metal tag that can be connected to a heat sink to dissipate the heat.



IC's can be divided into two further groups.

1. Analog
2. Digital

Analog IC's :

Analog IC's is referred to as a output voltage of a linear circuit is continuous and follows changes any input.

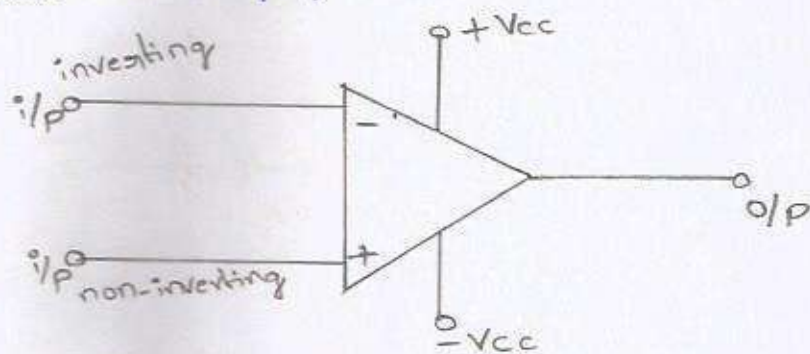
Ex: Audio Amplifier

When signal from a microphone is connected to the input, the output will vary in the same way as the voltage from microphone.

Digital IC's :

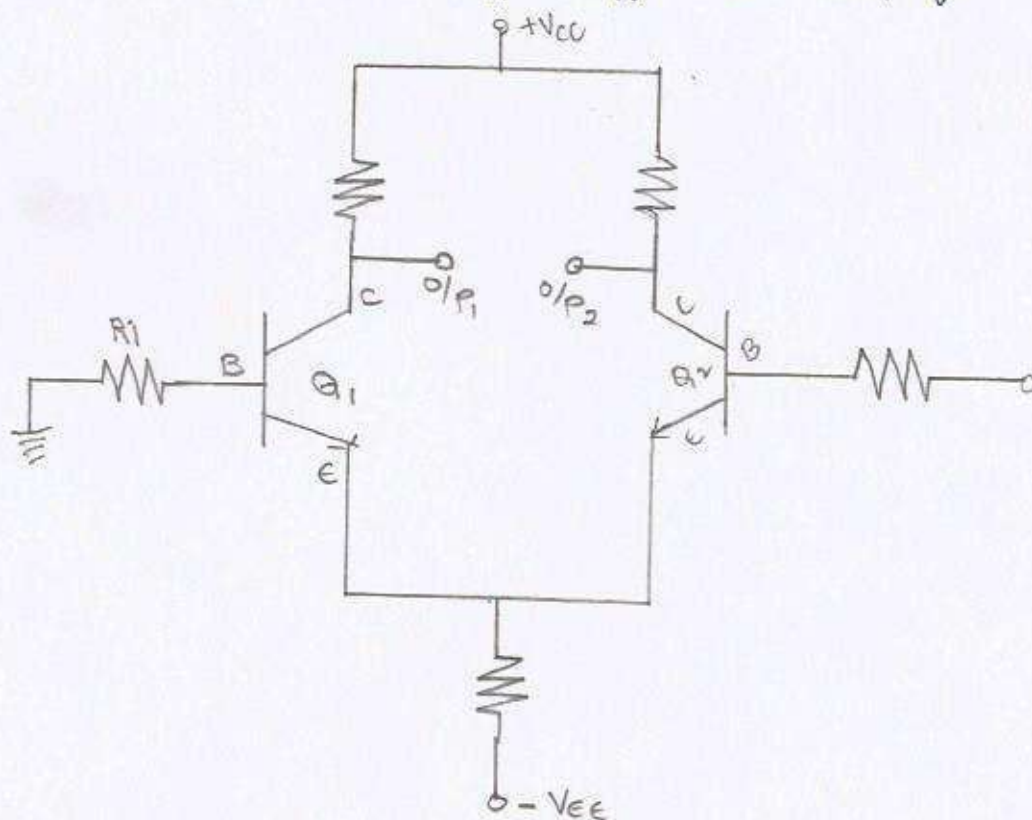
It is referred to as a output voltage is not continuous. It is either low or high. and it changed from one state to other very quickly.

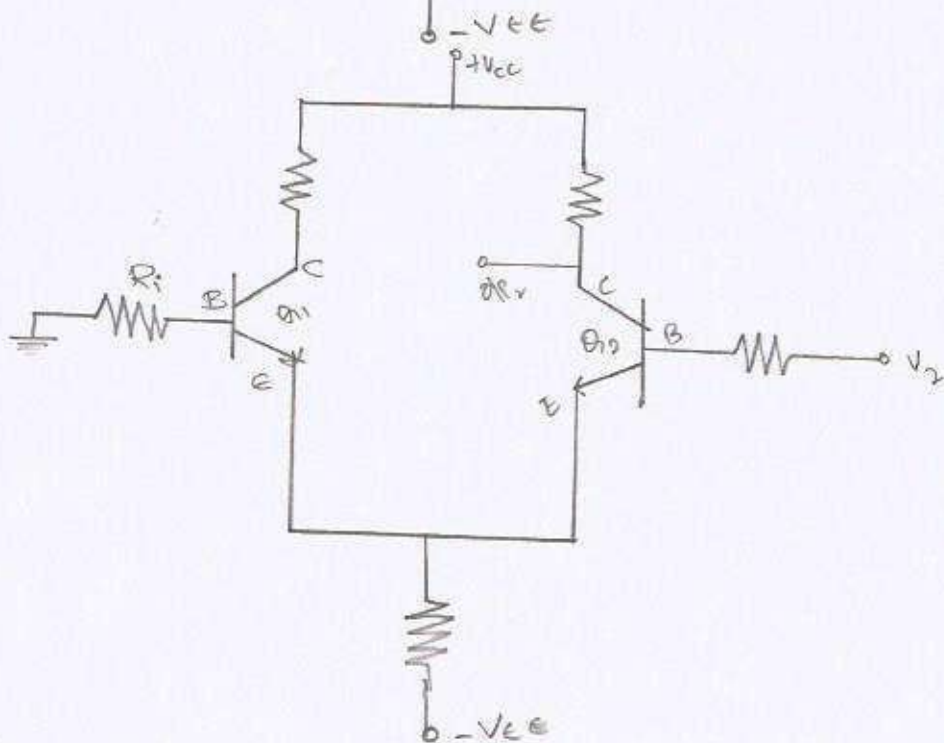
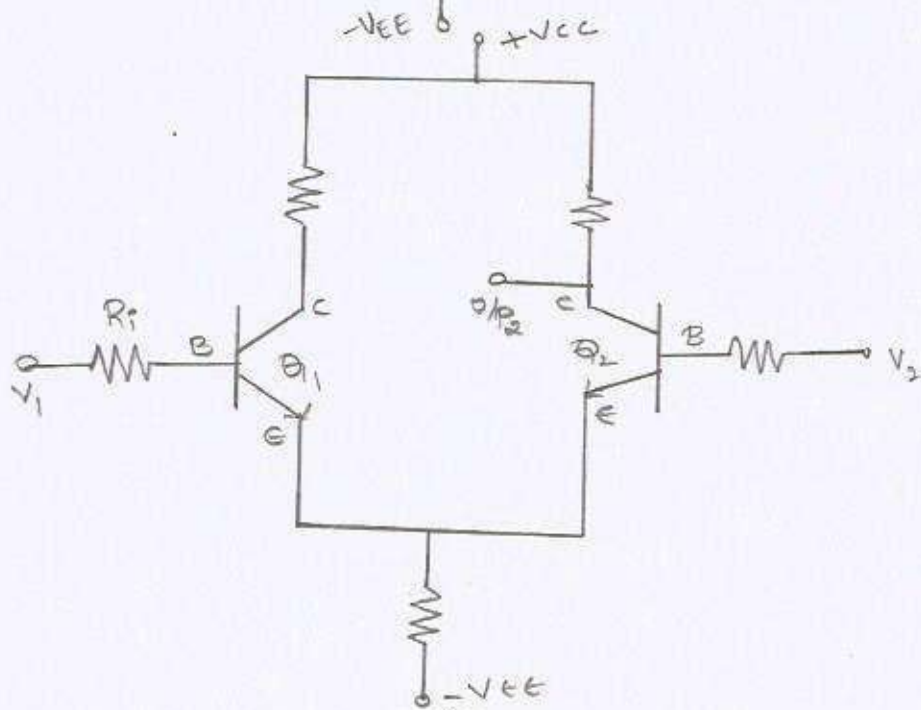
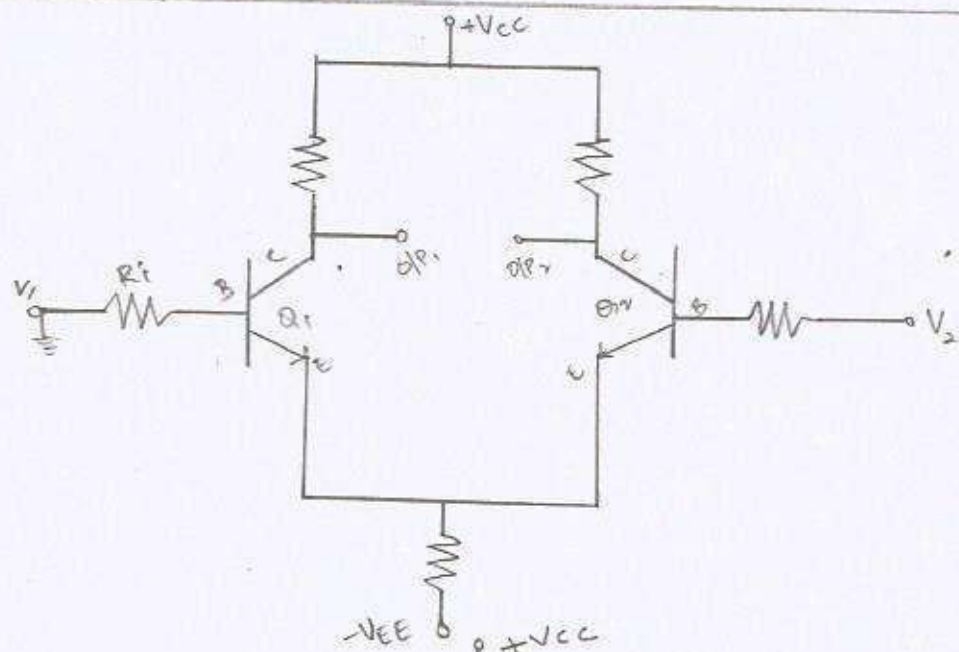
The symbol of an IC is commonly used as a amplifier
(or) Operational amplifier.



Differential amplifier is an device which is used to amplifies the difference of two input signals. It has 4 configurations.

1. Dual i/p, balanced o/p Differential Amplifier
2. Dual i/p, unbalanced o/p Differential Amplifier
3. Single i/p, balanced o/p Differential Amplifier
4. Single i/p, unbalanced o/p Differential Amplifier





* Basic Information of Op-Amp :-

Op-Amp is a operational Amplifier. Op-Amp is an integrated circuit that operates as a voltage amplifier. An Op-amp has a differential input. The symbol for an op-amp along with its various terminals is shown in below fig.

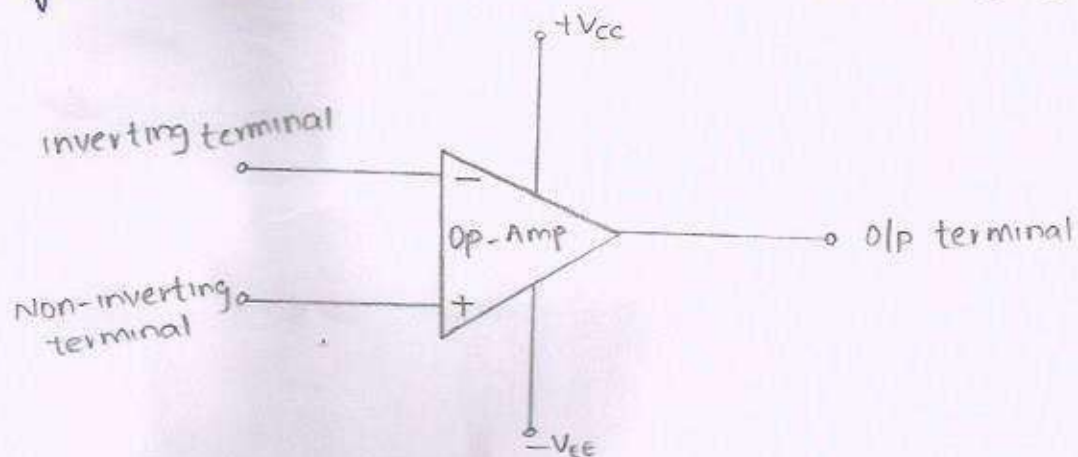


fig :- Symbol of an Op-Amp

The op-amp is indicated by a triangle with points in the direction of the signal flow.

→ Op-amp has 2 inputs of opposite polarities and it has single op and has 2 power supplies.

→ These amplifiers are called Operation Amplifiers because they were initially designed as an effective device for performing arithmetic operations (+, -, x, %) in an analog circuit.

→ Almost all the op-amp have atleast 5 terminals

- The positive supply voltage terminal $+V_{cc}$
- Negative supply voltage terminal $-V_{ee}$
- Output terminal
- Inverting input terminal (-)
- Non-inverting input terminal (+).

- The i/p at inverting terminal is positive voltages the o/p is -ve voltage and vice versa.
- While the i/p at non-inverting terminal results is the same polarity output signal at the o/p terminal. This is shown in below fig:

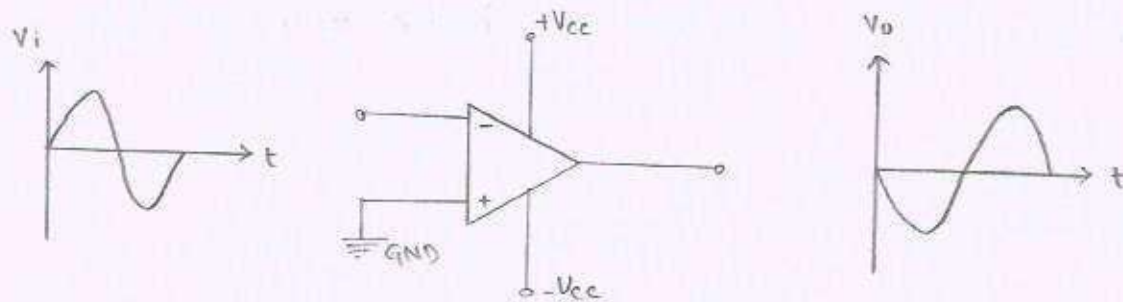


fig: input is applied to the inverting terminal

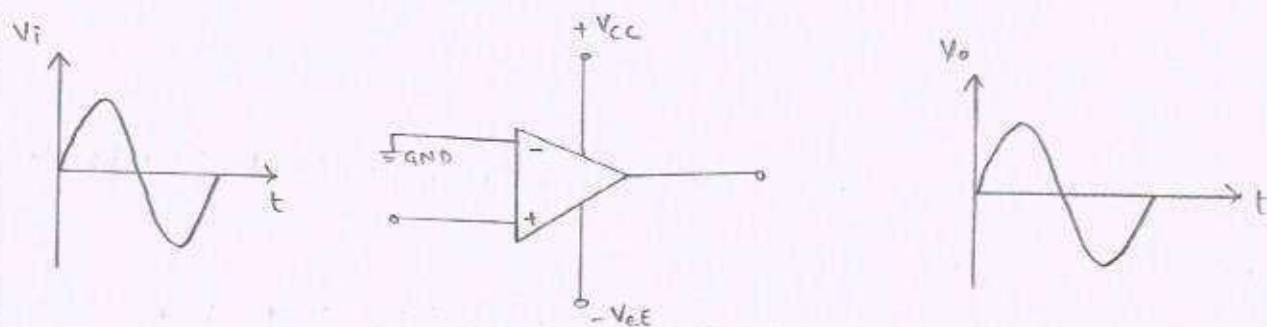
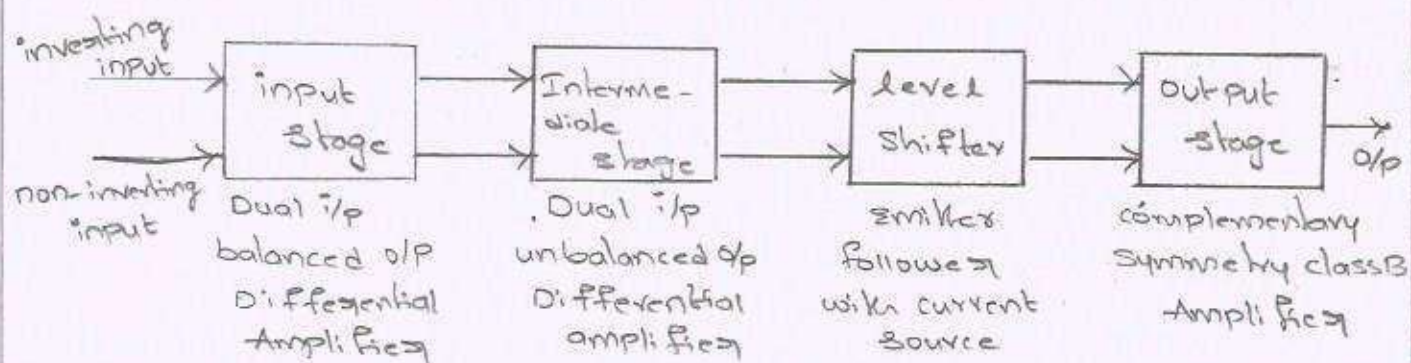


fig: input is applied to the Non-inverting terminal

- The Op-amp works on dual power supply.
- The dual power supply is generally balanced i.e., the voltage of the +ve supply $+V_{cc}$ and -ve supply $-V_{ee}$ are in same magnitude. The typically used power supply voltages are $\pm 15V$.
- But if the 2 voltage magnitudes are not equal in a dual supply it is called as unbalanced power supply.
- But almost we use the balanced dual power supply for Op-amp in practically.

* Block Diagram of Op-Amp :-



The fig. shows the block diagram of Op-amp. It consists of 4 cascaded blocks.

- Input stage
- Intermediate stage
- Level shifter
- Output stage

1. Input stage :-

The output input stage requires high i/p impedance to avoid loading on the sources. It requires 2 i/p terminals & also it requires low o/p impedance.

- All such requirements are achieved by using dual i/p balanced o/p differential amplifier at the i/p stage.
- This stage provides most of the voltage gain of the amplifier & also establishes the i/p resistance of the amplifier.

2. Intermediate Stage :-

The o/p of the i/p stage drives the next stage which is an intermediate stage. This is another differential amplifier with dual i/p unbalanced o/p i.e., single ended o/p.

→ The overall gain of requirement of the op-amp is very high.

→ In most of the amplifier an intermediate stage is a dual i/p unbalanced o/p differential amplifier. This stage increases voltage gain of the amplifier.

3. Level shifting stage :-

The level shifting stage is used after the intermediate stage to shift the dc level at the o/p of the intermediate stage downward to zero volts wrt ground.

→ Here coupling capacitors are not used to couple the amplifiers in the intermediate state. Dc biasing voltage level propagates through the amplifier. Due to this a significant dc level appears at the o/p along with ac o/p.

→ Due to this effect o/p gets distorted & limits the maximum o/p voltage. This is shown in below fig.

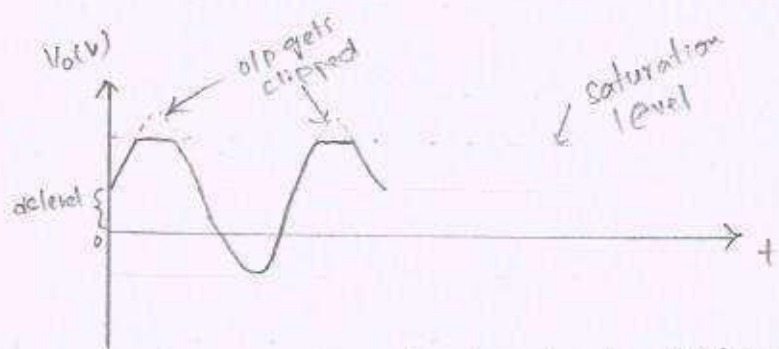
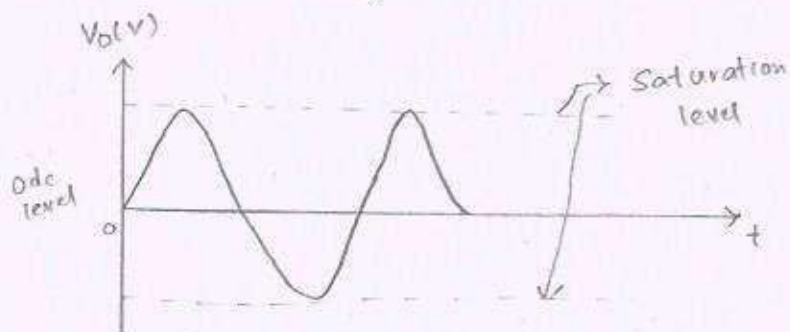


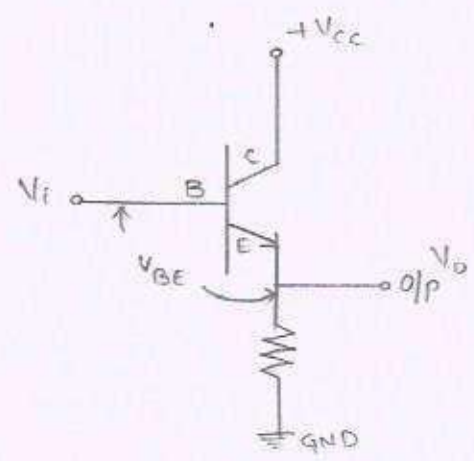
fig: Distorted o/p due to Additional level.

→ So the main purpose of the level shifting stage is to shift the o/p 'Q' point dc level towards the ground with

minimum change in the ac signal.

→ This also satisfies that the o/p should have equal voltage level of ov for '0' i/p signal.

Eq: 1 How to vary o/p vtg by giving i/p



Applying KVL to the i/p side

$$V_i - V_{GS} - V_o = 0$$

$$V_o = V_i - V_{GS}$$

By varying i/p vtg, the o/p is decreasing.

Proof:- Let us assume that

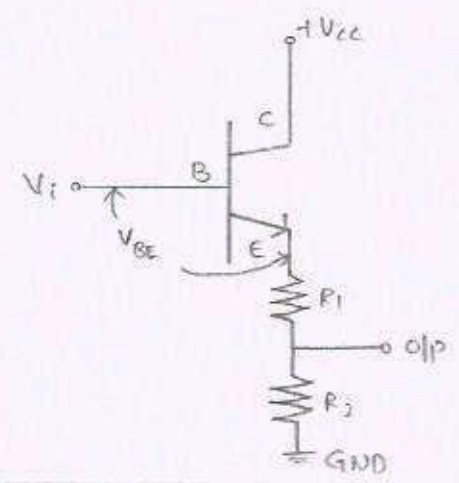
$$V_i = 5V, V_{GS} = V_{BE} = 0.7V$$

$$V_o = V_i - V_{GS}$$

$$= 5 - 0.7$$

$$V_o = 4.3V$$

Eq: 2



Applying KVL to the circuit

$$V_i - V_{BE} - I(R_1 + R_2)$$

$$I(R_1 + R_2) = V_i - V_{BE}$$

$$I = \frac{V_i - V_{BE}}{R_1 + R_2}$$

$$\frac{V_o}{R_2} = \frac{V_i - V_{BE}}{R_1 + R_2}$$

$$V_o = \frac{V_i - V_{BE}}{R_1 + R_2} \times R_2$$

proof :- Let us assume

$$V_o = \frac{5 - 0.7}{10 + 4} \times 4$$

$$= \frac{4.3 \times 4}{14}$$

$$= \frac{17.2}{14}$$

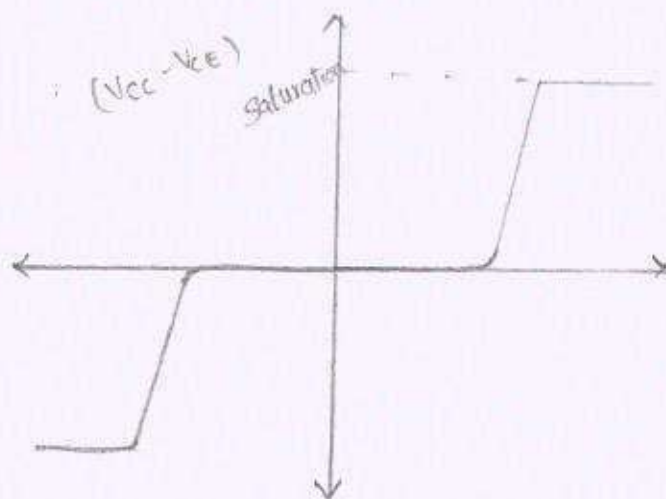
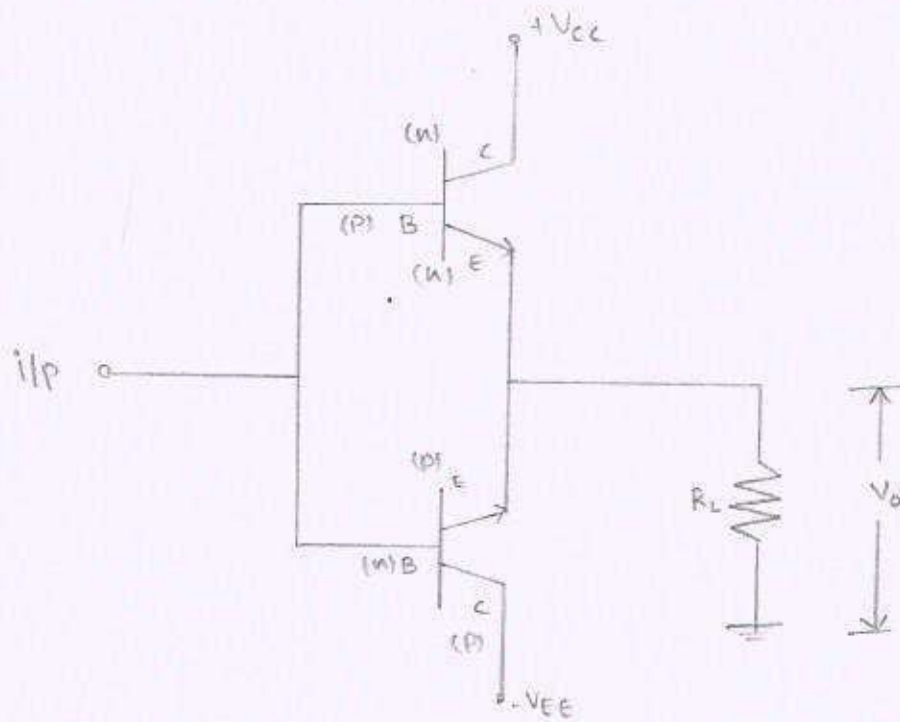
$$V_o = 1.22 \quad V_o \downarrow$$

4. Output Stage :-

The last stage is a complimentary Class B pushpull amplifier. The basic requirements of an o/p stage are low o/p impedance.

1. large o/p voltage
2. large o/p current
3. low o/p impedance
4. low power dissipation
5. Short Circuit protection.

A pushpull amplifier satisfies the above requirements & hence commonly used in the o/p stage of an Op-amp.



* Packages and Pinouts :-

The op-amp is fabricated on a very small silicon chip and is packaged in a suitable case.

The Op-amp is generally available in 2 packages.

1. Metal can
2. DIP (Dual in line package)

- Metal cans are available with 8, 10 or 12 pins.
- DIP packages are having 8 (or) 14 pins.
- DIP package is most widely used.

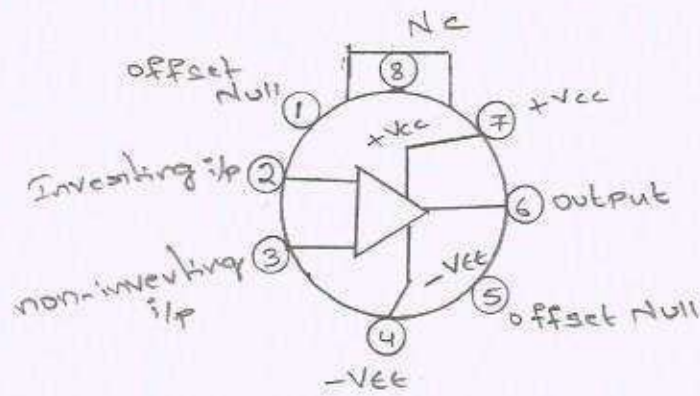


fig: Metal Can Package

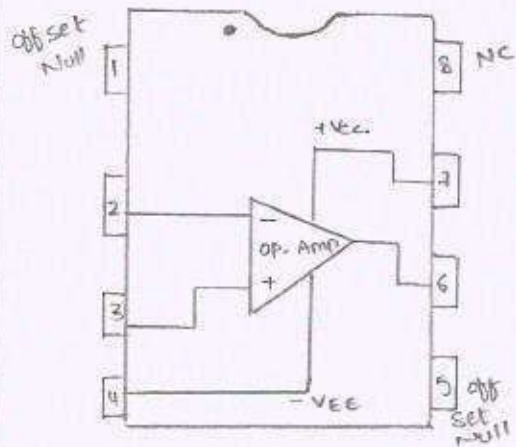


fig: 8-pin DIP package

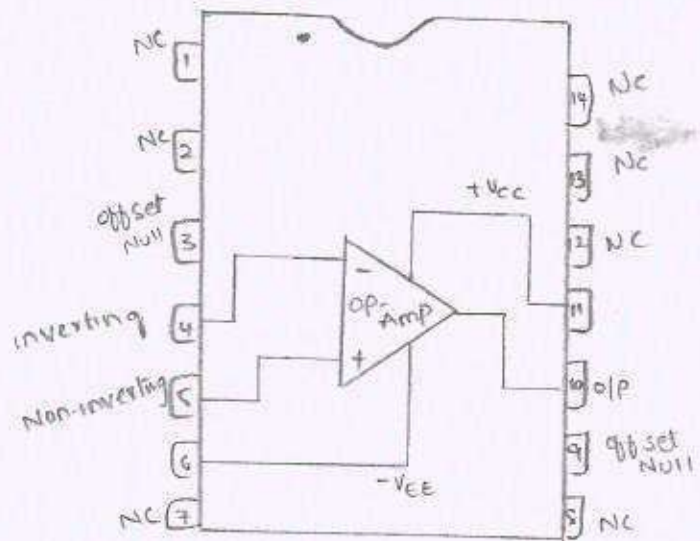
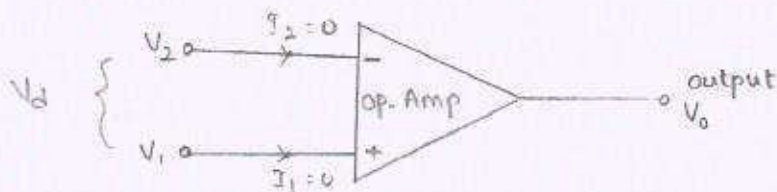


fig: 14-pin DIP package

* Ideal Op-Amp :-



The above fig. shows an ideal op-amp. It has two i/p signals V_1 & V_2 applied to non-inverting and inverting terminals respectively.

The Op-amp amplifies the difference b/w the voltages applied at the non-inverting i/p & inverting i/p.

→ V_1 is the voltage applied at the non-inverting terminal and V_2 is the voltage applied at the inverting terminal. The difference between the 2 voltages ($V_1 - V_2$) can be acts as an input to the op-amp. It is denoted by V_d .

$$V_d = V_1 - V_2$$

→ If the gain of the op-amp is 'A', then

$$A = \frac{V_{out}}{V_d}$$

$$V_{out} = A \times V_d$$

→ The above expression says that the o/p voltage is directly proportional to the algebraic difference b/w the 2 i/p voltages.

→ Hence the op-amp amplifies the difference b/w the 2 i/p voltages.

→ A ideal op-amp draws no current at the i/p terminals i.e., $I_1 = I_2 = 0$. Hence its i/p impedance is infinity ($Z_i = \infty$). This means that any source can drive it & there is no loading effect on the drivers stage.

→ The gain of an ideal op-amp is infinity, hence the differential i/p $V_d = V_1 - V_2$ is essentially zero for the finding o/p voltage V_{out} .

→ The o/p voltage V_{out} is independent of current drawn from the o/p terminals thus its o/p impedance is zero.

→ Hence output can drive an infinite of other circuits.

* Characteristics of an Ideal Op-Amp :-

1. Infinite input Resistance :

It is denoted by R_i and it is infinite for an ideal op-amp. This ensures that no current can flow into an ideal op-amp.

2. Infinite Voltage Gain :

It is denoted by A_{OL} (or) A . It is infinite for an ideal op-amp.

3. Zero op impedance :

It is denoted by R_o . It is infinite for an ideal op-amp.

4. Zero offset voltage :

The presence of the small op voltage $V_1 = V_2 = 0$ is called as an offset voltage. It is zero for an ideal op-amp.

5. Infinite Band width :

The band width of an ideal op-amp is infinite. This means that the operating frequency range is from 0 to ∞ . This ensures that the gain of the op-amp remains constant over the frequency range from dc to infinite frequency. Therefore an op-amp can amplify dc as well as ac signals.

6. Infinite CMRR :

It is defined as the ratio of differential gain and common mode gain. It is infinite for an ideal op-amp.

$$CMRR = \frac{A_D}{A_C}$$

7. Slew Rate :

It is defined as the maximum rate of change of op voltage with respect to time. It is infinite for an ideal op-amp.

It is denoted by 's'.

$$s = \frac{dV_o}{dt}$$

* Practical Op-Amp :-

The characteristics of an ideal op-amp can be approximated closely enough, for many practical op-amp characteristics are little bit different than the ideal op-amp characteristics.

1. Input Resistance :

It is denoted by R_i . It has large value in practical op-amp. The typical value of op-amp is $2\text{M}\Omega$.

2. Open Loop Gain :

It is the voltage gain of an op-amp when no feedback is applied, practically it is large.

3. Output Impedance :

It is denoted by R_o . It has very small value. The typical value of o/p resistance is few ohms i.e., 1Ω or 2Ω etc.

4. Band Width :

The band width of a practical op-amp is very small but if we apply -ve feedback it can be increased to a desired value.

* Virtual Ground :-

It is the situation in which the inverting input of an op-amp is at ground potential even though it is not connected directly to ground.

Assuming that the op-amp is ideal and it is producing some finite o/p. Then the open loop gain will be finite.

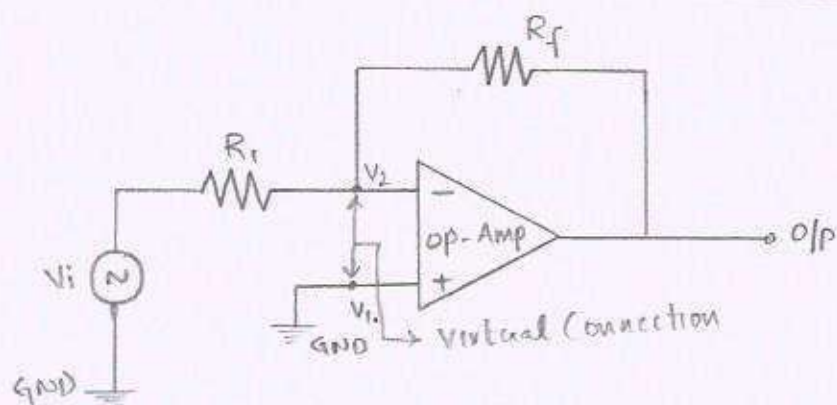


fig: Practical Inverting Op-Amp.

For an op-amp, we know that

$$A = \frac{V_{out}}{V_d}$$

$$V_d = V_1 - V_2$$

$$A = \frac{V_{out}}{V_1 - V_2}$$

$$V_1 - V_2 = \frac{V_{out}}{A}$$

$$V_1 - V_2 = \frac{V_{out}}{\infty} = 0$$

$$V_1 - V_2 = 0$$

$$\boxed{V_1 = V_2}$$

→ From above eqⁿ it is observed that the practical potential difference b/w 2 terminals is zero. We can say that virtual short circuit exists b/w the 2 i/p terminals.

→ Here, the word virtual is used to clear that actually we are not shorting the i/p terminals.

→ A virtual short circuit means that whatever voltage is at non-inverting terminal, it will automatically appear at the inverting terminal.

→ Here in fig. $V_1 = 0$, so we have $V_2 = 0$. Therefore potential at inverting terminal is zero and it is called virtual ground.

→ Virtual ground means that the terminal is not connected to the ground actually even then the voltage at the terminal is zero.

Temperature Ranges :-

There are 3 different temperature grades based on which the op-amp IC's are classified. These temperature ranges are ;

1. Military Temperature Range : -55°C to $+125^{\circ}\text{C}$ (or) -55°C to $+85^{\circ}\text{C}$.
2. Industrial Temperature Range : -20°C to $+85^{\circ}\text{C}$ (or) -40°C to $+85^{\circ}\text{C}$.
3. Commercial Temperature Range : 0° to $+70^{\circ}\text{C}$ (or) 0°C to $+75^{\circ}\text{C}$.

* DC characteristics :-

We have four different DC characteristics. They are ;

1. input bias current.
2. input offset current.
3. input offset voltage.
4. Thermal Drift.

1. Input Bias Current :-

The average value of 2 currents flowing into the op-amp input terminals is called input bias currents. It is denoted by I_B . This is shown in below fig.

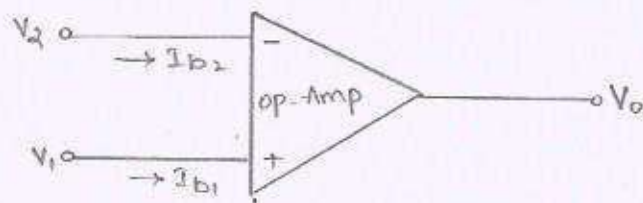


fig: input bias currents

Mathematically, it is expressed as

$$\bar{I}_B = \frac{I_{b1} + I_{b2}}{2}$$

→ Ideally it should be zero, practically it should be $\bar{I}_B = 200\text{nA}$.

→ Consider basic inverting amplifier as shown in fig. ②

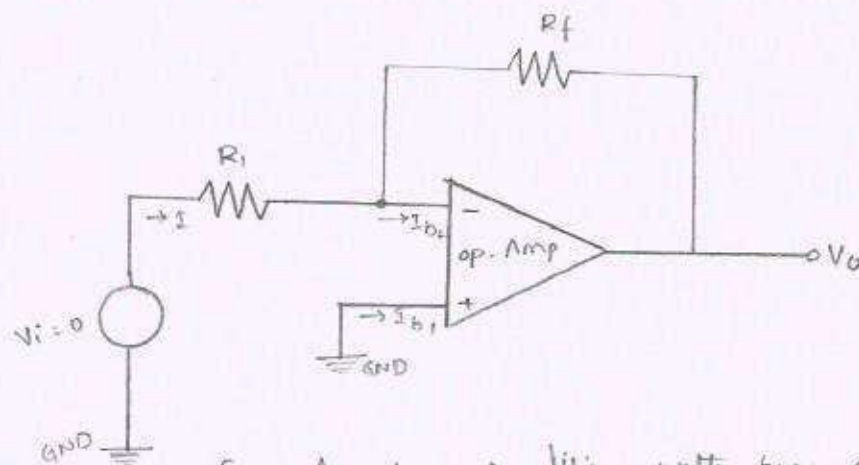


fig: Inverting Amplifier with bias currents

→ If i/p voltage V_i is said to zero volts, the o/p voltage V_o should also be zero volt.

→ o/p voltage V_o is given that $V_o = I_b R_f$

for a op-amp have $1\text{M}\Omega$ feedback resistor

$$V_o = 200\text{nA} \times 1\text{M}\Omega$$

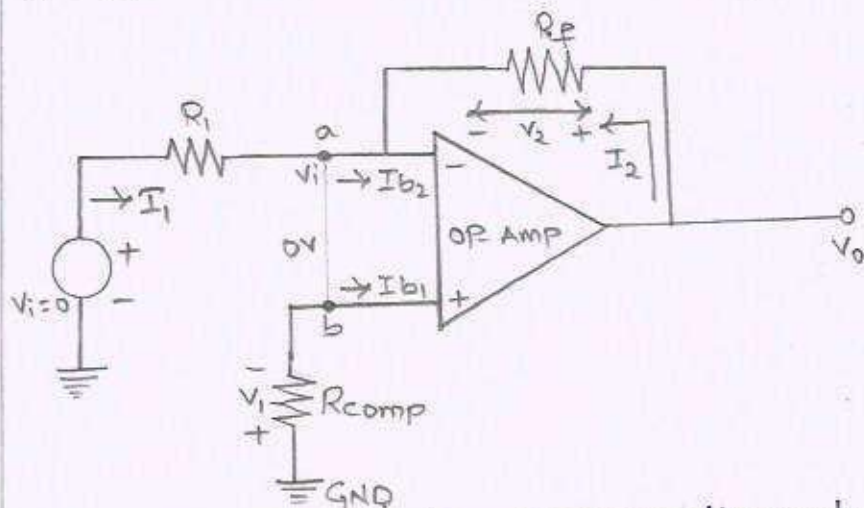
$$V_o = 200\text{mV}$$

→ The o/p is driven to 200mV with zero i/p because of the bias currents.

→ In applications where signal levels are measured in mV ,

this is totally unacceptable.

→ This effect can be compensated by a compensation resistor $[R_{comp}]$ has been added between the non-inverting terminal and ground. It is shown in below fig.



→ Where current I_{b1} flowing through the compensating resistor $[R_{comp}]$ and V_1 voltage drop across it.

Applying KVL, we get

$$-V_1 + 0V + V_2 - V_0 = 0$$

$$V_0 = V_2 - V_1 \rightarrow (1)$$

$$V_2 = V_1$$

→ By selecting proper value of R_{comp} , V_2 can be cancelled with V_1 & o/p will be zero

→ The value of R_{comp} is derived as

$$I_{b1} = \frac{V_1}{R_{comp}} \rightarrow (2)$$

[dropping vtg across R_{comp}
 $V_1 = I_{b1} R_{comp}$]

→ The node 'a' is the voltage V_1 because the voltage at non-inverting terminal is V_1 . so we get

$$I_1 = \frac{V_1}{R_1} \rightarrow (3)$$

$$I_2 = \frac{V_2}{R_f}$$

from eq(1)

$V_1 = V_2$, so we get

$$I_2 = \frac{V_1}{R_f}$$

Applying KCL at node 'a' gives

$$I_{b2} = I_1 + I_2$$

$$= \frac{V_1}{R_1} + \frac{V_1}{R_f}$$

$$= V_1 \left[\frac{1}{R_1} + \frac{1}{R_f} \right]$$

$$= V_1 \left[\frac{R_f + R_1}{R_1 R_f} \right]$$

let us consider $I_{b1} = I_{b2}$

$$\Rightarrow \frac{V_1}{R_{comp}} = V_1 \left[\frac{R_1 + R_f}{R_1 R_f} \right]$$

$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$$

$$(\because R_{comp} = R_1 \parallel R_f)$$

i.e., to compensate for bias currents, the compensation resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting i/p terminal.

2. Input offset current :

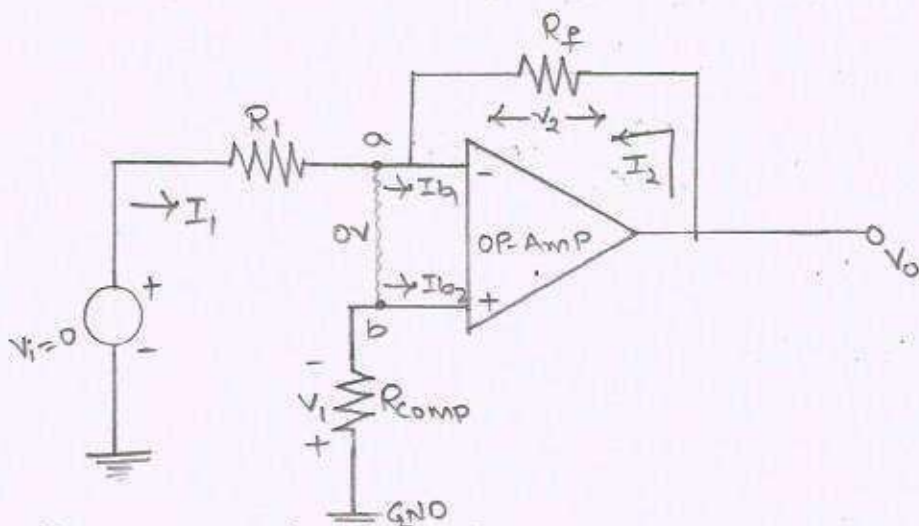
It is defined as the algebraic difference between the currents flowing into the 2 i/p terminals of the op-amp. It is denoted by I_{ios} .

Mathematically it is given by

$$I_{ios} = I_{b1} - I_{b2}$$

Effect of i/p offset current on o/p voltage :

Let us consider the op-amp used in the closed loop configuration with R_{comp} as shown in below fig.



From fig. $V_1 = I_{b1} R_{comp}$

$$I_{b1} = \frac{V_1}{R_{comp}}$$

But $V_1 = \frac{V_i}{R_1}$

$$= \frac{I_{b1} R_{comp}}{R_1}$$

Now, $I_{b2} = I_1 + I_2$

$$I_2 = I_{b2} - I_1$$

So we get $I_2 = I_{b2} - \frac{I_{b1} R_{comp}}{R_1}$

We know that, $V_o = V_2 - V_1$

from fig. $V_2 = I_2 R_f$

So, $V_o = I_2 R_f - I_{b1} R_{comp}$

$$= \left[I_{b2} - \frac{I_{b1} R_{comp}}{R_1} \right] R_f - I_{b1} R_{comp}$$

$$= \frac{[I_{b2} R_1 - I_{b1} R_{comp}] R_f}{R_1} - I_{b1} R_{comp}$$

$$= \frac{I_{b2} R_1 R_f - I_{b1} R_{comp} R_f - I_{b1} R_1 R_{comp}}{R_1}$$

$$\begin{aligned}
 &= \frac{I_{b2} R_1 R_f - I_{b1} R_{comp} (R_1 + R_f)}{R_1} \\
 &= \frac{I_{b2} R_1 R_f - I_{b1} \left[\frac{R_1 R_f}{R_1 + R_f} \right] (R_1 + R_f)}{R_1} \\
 &= \frac{R_1 R_f (I_{b2} - I_{b1})}{R_1} \\
 &= R_f (I_{b2} - I_{b1})
 \end{aligned}$$

$$V_o = R_f I_{ios}$$

→ The o/p voltage exists by the i/p offset current.

3. Input offset Voltage:

The differential voltage must be applied b/w the 2 i/p terminals of an op-amp, to make the o/p voltage zero is called as input offset voltage. It is denoted by V_{ios} .

→ Whenever both the i/p terminals of the op-amp are grounded ideally the o/p voltage should be zero. However, in this condition the practical op-amp shows a small non-zero o/p voltage. This is due to mis-matching present in the internal circuit of an op-amp. Such a voltage can cause error in the practical applications, for which op-amp is used.

→ To make such a voltage to zero, it is necessary to apply small difference voltage b/w the 2 i/p terminals of an op-amp. This voltage is called i/p offset voltage.

→ For an IC op-amp i/p offset voltage is 6mV.

→ Let us see the effect of V_{ios} on the o/p of non-inverting & inverting op-amp amplifiers shown in below figures.

Internal Circuit of op-amp:



- AV_1 is the thevenin's equivalent voltage source.
 - R_0 is the thevenin's equivalent resistance.
 - R_1 is input resistance.
- i.e. V_{id} is the difference of input voltage and it's

$$\text{i.e. } V_{id} = V_1 - V_2$$

= Non-inverting i/p terminal - inverting i/p terminal

V_{out} is Output voltage and it is

$$\text{i.e. } V_o = A V_{id}$$

$$= A(V_1 - V_2)$$

$\therefore$ The output voltage V_{out} is directly proportional to the difference between two input voltages

IMP

Ideal Voltage Transfer Characteristic:

- The Ideal Op-amp produces the output voltage V_{out} proportional to the difference between the two input voltages

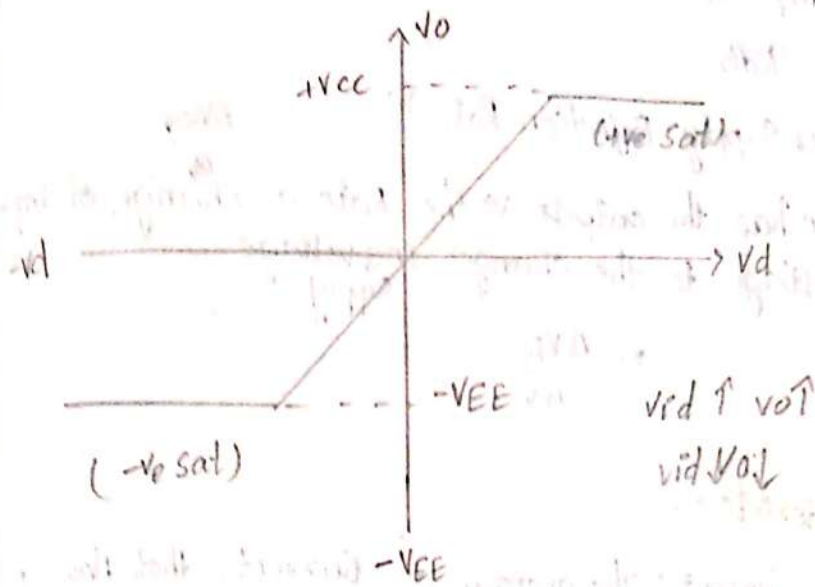
$$V_{out} = A \cdot V_{id}$$

$$= A(V_1 - V_2)$$

where A is Constant

The graphical Representation of the statement gives the Voltage transfer Curve.

- It is the graph of Output voltage V_{out} plotted against the input voltage V_{id} assuming the gain Constant.
- these graph is called transfer characteristics of the op-amp



Note:

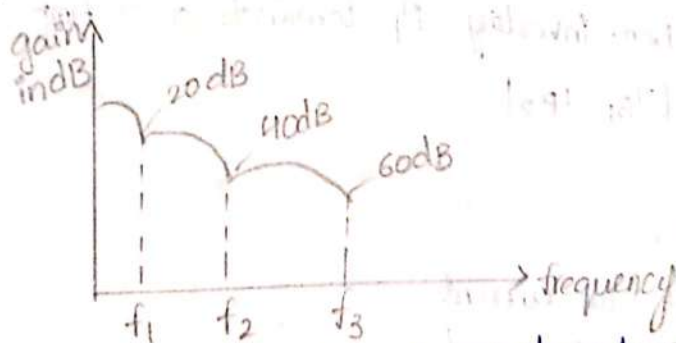
i) op-amp output voltage get saturated at the $+V_{CC}$ and $-V_{EE}$
 ii) op-amp Can not produce output voltage more than $+V_{CC}$ and $-V_{EE}$

iii) practically Saturation Voltage $+V_{sat}$ and $-V_{sat}$ are slightly less than $+V_{CC}$ and $-V_{EE}$

AC & DC characteristics:

AC characteristics:

frequency Response: It is defines graphical Representation of gain providing for input signals of different frequency



Slew Rate: It is defined as the rate of change of output voltage with respect to time.

$$\text{Slew Rate} = \frac{dV_o}{dt} \text{ V}/\mu\text{sec} \quad (\text{practical of } 0.5 \text{ V}/\mu\text{sec})$$

Common Mode Rejection Ratio (CMRR):

It is defined as the Ratio of differential mode gain to the Common mode gain.

$$\text{CMRR} = \frac{A_d}{A_{cm}} \quad (\text{or}) \quad 20 \log \left| \frac{A_d}{A_{cm}} \right| \text{ in dB's}$$

Ideal op-amp = ∞

Practically = 90dB

PSRR (Power Supply Rejection Ratio):

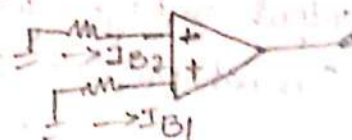
It is defined as the ratio of the change of output voltage to the change in input offset voltage to the change in supply voltage.

$$= \frac{\Delta V_{io}}{\Delta V}$$

DC characteristics:

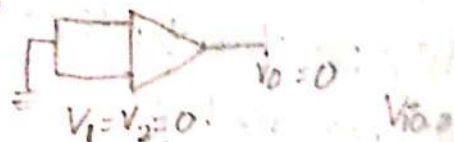
Input Bias Current: The average of currents that flow into the inverting and non-inverting input terminals of op-amp.

$$= \frac{I_{B1} + I_{B2}}{2}$$



Input offset voltage: The algebraic difference

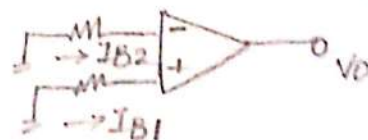
The voltage which applied between two input terminals of an op-amp to nullify the output.



Input offset current:

The algebraic difference between currents entering into the inverting and non-inverting input terminals of op-amp.

$$I_{io} = |I_{B1} - I_{B2}|$$



Thermal Drift:

Change of input bias current and input offset voltage and input offset current.

I_{B} drift $\mu A/^\circ C$
 I_{io} drift $\mu A/^\circ C$

It is defined as the change of input bias current, input offset voltage and input offset current with respect to the temperature.

Features of 741 op-amp:

The op-amp is a popular, general purpose op-amp known as for its versatility and ease to use.

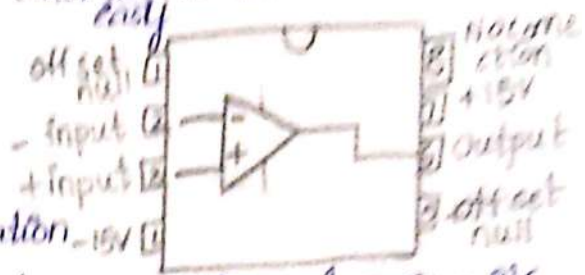
1. High input impedance.

2. Low output impedance.

3. Short Circuit protection.

4. Internal frequency compensation.

It is commonly used in wide range of analog circuits due to its stability and wide frequency Response.



Problem

1. The Output Voltage of certain op-amp circuit changes by 20V in 4 microSec (4 μ sec). What is Slew Rate.

$$\frac{dV_o}{dt} \text{ V}/\mu\text{sec}$$

$$= \frac{d(20V)}{dt(4 \mu\text{sec})} = \frac{d}{dt} \left(\frac{20}{4 \times 10^{-6}} \right)$$

$$= 5 \times 10^6$$

$$= 5V/\mu\text{sec}$$

2. Assume that 741 op-Amp is Connected has unity gain inverting amplifier. Let the input change be 8V. determine the time taken for the output to change by 8V

$$\text{Slew Rate} = \frac{dV_o}{dt} \text{ V}/\mu\text{sec}$$

$$dt = \frac{dV_o}{S}$$

$$= \frac{8V}{0.5V/\mu\text{sec}}$$

$$t = 16 \mu\text{sec}$$

UNIT-II

APPLICATIONS OF OP-AMP

Modes of Operation :

Op-Amp will performs the two modes operation.

1. Open loop mode of Operation
2. Closed Loop mode of Operation.

1. Open Loop Mode of Operation :

It says that no feedback terminal in b/w input and output but op-amp will performs the three basic operation in open loop mode of operation.

1. Inverting Amplifier
2. Non-inverting Amplifier
3. Differential Amplifier

(a) Inverting Amplifier :

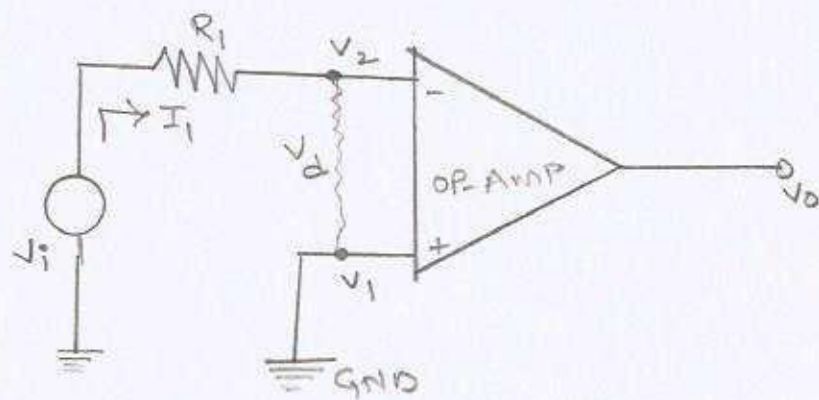


Fig: Inverting Amplifier

→ In this the input is applied at inverting terminal and the non-inverting terminal is grounded.

→ In this the output is out of phase (180° phase shift) with the input.

→ we know that, open loop gain,

$$A = \frac{V_o}{V_d}$$

where, $V_d = V_1 - V_2$

$$\text{So, } A = \frac{V_o}{V_1 - V_2}$$

$$V_o = A(V_1 - V_2)$$

If source resistance R_i is very small, then it is neglected.

$$\therefore V_d = V_i$$

$$V_o = A(V_1 - V_i)$$

from fig. $V_1 = 0$ ($\because$ it is connected to ground)

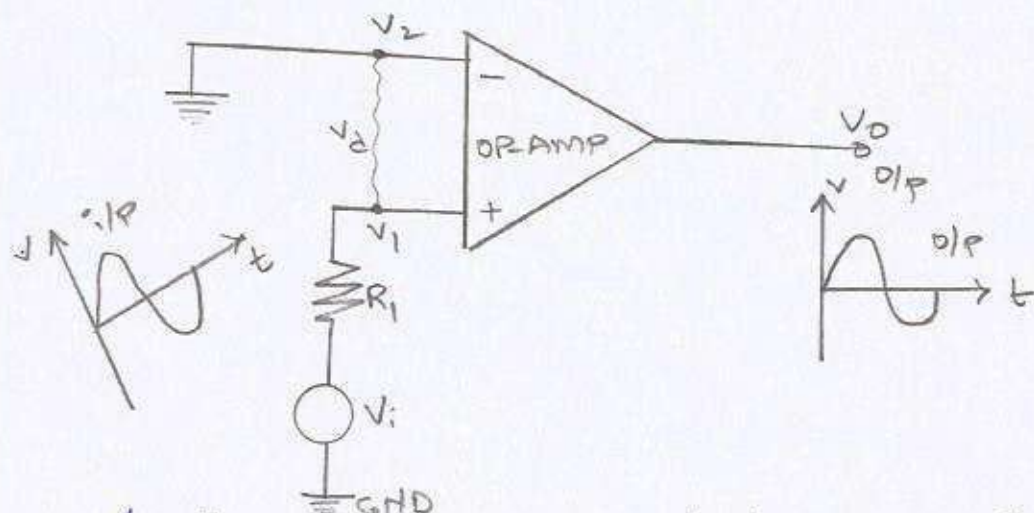
$$V_o = A(0 - V_i)$$

$$V_o = -AV_i$$

where, -ve sign indicates that phase shift provided in b/w input & output.

The above eqⁿ says that the o/p voltage 'A' times larger (or) increased then the input.

(b) Non-inverting Amplifier:



→ In this the i/p is applied at non-inverting terminal and the inverting terminal is grounded.

- In this the output is in phase (0° or 360°) with the i/p.
- we know that open loop gain,

$$A = \frac{V_o}{V_d}$$

where, $V_d = V_1 - V_2$

So, $A = \frac{V_o}{V_1 - V_2}$

$$V_o = A(V_1 - V_2)$$

- If source resistance R_i is very small, then it is neglected.

$$\therefore V_1 = V_i$$

$$V_o = A(V_i - V_2)$$

from fig. $V_2 = 0$ ($\because$ it is grounded)

$$V_o = A(V_i - 0)$$

$$V_o = AV_i$$

where, +ve sign indicates that phase shift is Zero provided in input and output.

(c) Differential Amplifier:

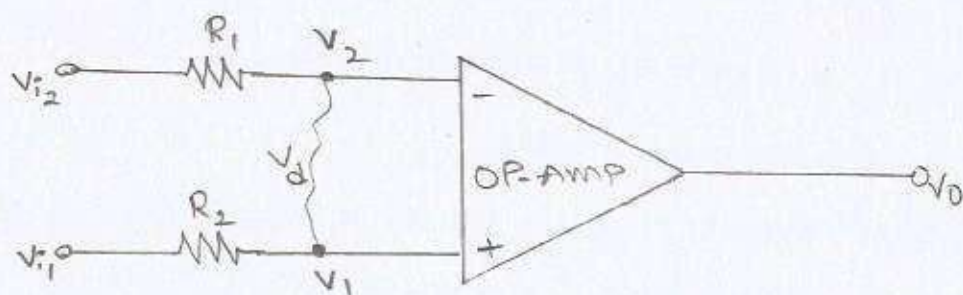


fig: Differential Amplifier

→ In these inputs are applied at both the inverting and non-inverting terminals. Since the difference b/w two input signals is amplified which is called Differential Amplifier.

→ We know that open loop gain,

$$A = \frac{V_o}{V_d}$$

Where, $V_d = V_1 - V_2$

$$\text{So, } A = V_o / V_d$$

$$A = \frac{V_o}{V_1 - V_2}$$

$$V_o = A(V_1 - V_2)$$

→ If source resistance R_i is very small, then it is neglected.

$$V_{i1} = V_1 \quad ; \quad V_{i2} = V_2$$

$$\text{So, } V_o = A(V_1 - V_2)$$

$$\boxed{V_o = A(V_{i1} - V_{i2})}$$

2. Closed Loop Mode of Operation:

In this feedback exist, in b/w input & output.

These feedback is a negative feedback.

→ Due to this negative feedback if resistance increases, output resistance decreases and noise is reduced, band width is increases and gain is decreases.

→ But op-amp will performs three basic operation in closed loop mode of operation.

1. Inverting Amplifier
2. Non-inverting Amplifier
3. Differential Amplifier.

(a) Inverting Amplifier:

In this inverting ^{ip} is applied at the inverting terminal and non-inverting terminal is grounded.

- In this op signal is out of phase with the input signal.
- The op voltage V_o is fed back to the inverting input terminals through $R_f - R_i$ network.

Where, R_f = feedback resistor

- The inverting amplifier circuit shown in below figure.

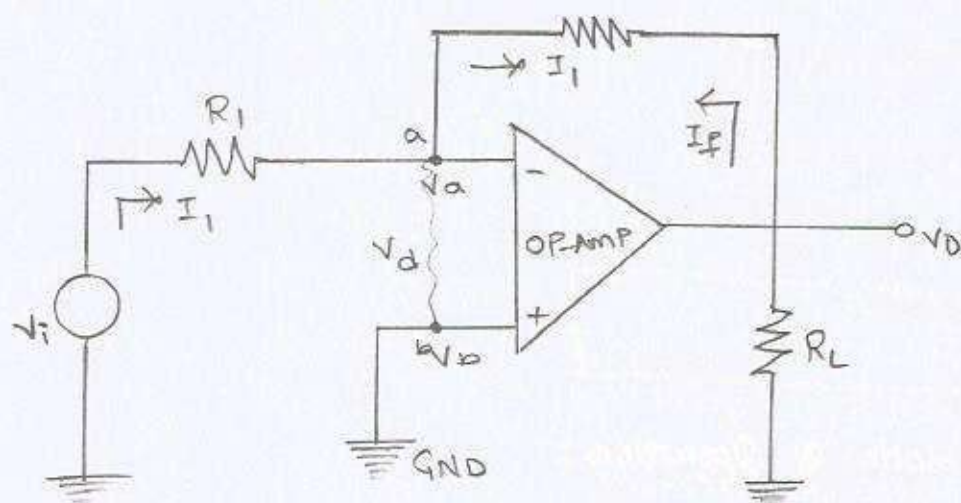


fig.

Analysis:

- Let us assume an ideal op-amp $V_d = 0$ and node A is at ground potential (virtual ground potential) then and I_i current flows through R_i resistor.

$$\text{So, } I_i = \frac{V_A}{R_i} \rightarrow (1)$$

→ Since op-amp draws no current, all the current flowing with R_i must flow through R_f resistors. The o/p voltage V_o is given by

$$V_o = -I_i R_f \rightarrow (2)$$

Since on sub_g, eq(1) & (2), we get

$$V_o = -\frac{V_i}{R_i} \times R_f$$

$$\boxed{\frac{V_o}{V_i} = -\frac{R_f}{R_i}}$$

Hence the closed loop gain of the inverting amplifier is given by A_{CL}

$$A_{CL} = V_o/V_i$$

So, $\boxed{A_{CL} = -\frac{R_f}{R_i}}$

Method - II :

According to nodal eqⁿ at node A,

$$I_i = I$$

$$\text{so, } \frac{V_i - V_a}{R_i} = \frac{V_a - V_o}{R_f}$$

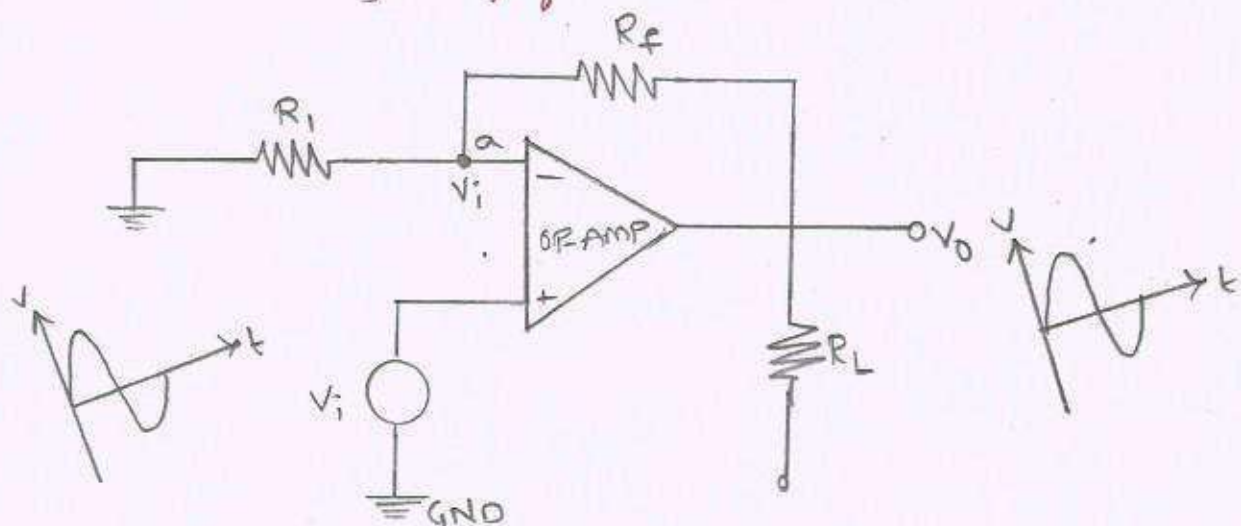
But $V_a = 0$; (because V_a is virtually grounded)

$$\frac{V_i}{R_i} = -\frac{V_o}{R_f}$$

$$\boxed{\frac{V_o}{V_i} = -\frac{R_f}{R_i}}$$

where, -ve sign indicates that the 180° phase shift provided in b/w input & output.

(b) Non-Inverting Amplifier:



- If a signal is applied to the non-inverting input terminal then it is called as non-inverting amplifier.
- If a signal is applied to the non-inverting terminal and feedback is connected from output to input as shown in above figure.
- It may be noted that it is also a -ve feedback system as output is being fed back to the inverting input terminal.
- As a differential voltage V_d at the input terminal of op-amp is zero, the voltage at node 'A' is V_i , same as the input voltage applied to non-inverting input terminal.
- In circuit R_f and R_1 forms a potential divider. Hence, according to potential divider theorem,

$$V_i = \frac{R_1 V_o}{R_1 + R_f}$$

$$V_o = \frac{R_1 + R_f}{R_1} \times V_i$$

$$V_o = 1 + \frac{R_f}{R_1} \times V_i$$

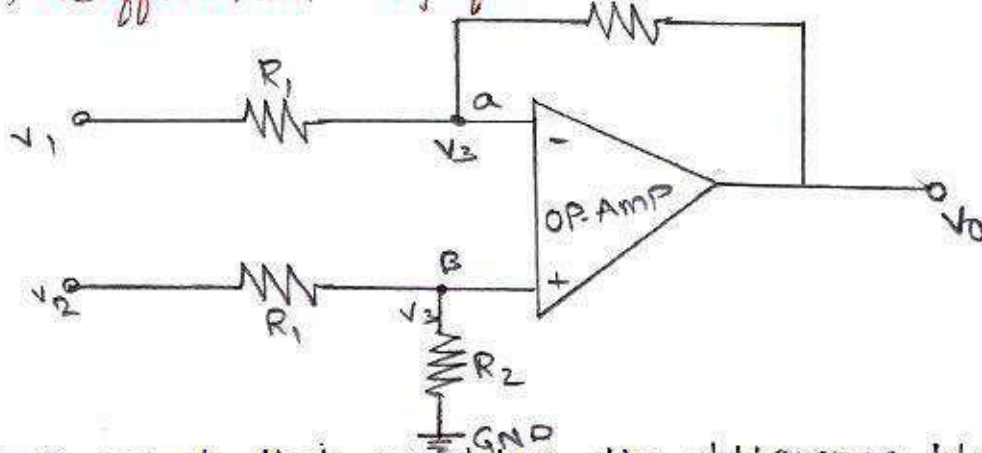
$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

We know that,

$$A_{CL} = \frac{V_o}{V_i}$$

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

(c) **Differential Amplifier:** $R_f \text{ (or) } R_2$



→ A circuit that amplifies the difference b/w two input signals is called as difference amplifier (or) Differential amplifier.

→ The differential amplifier circuit is shown in above figure.

→ Since the differential voltage at the input terminal of the op-amp is zero.

→ Node A and Node B are at the same potential i.e., V_s .

→ The nodal eqn at node A is,

$$\frac{V_2 - V_3}{R_1} = \frac{V_s - V_o}{R_2}$$

$$\frac{V_3 - V_2}{R_1} + \frac{V_s - V_o}{R_2} = 0$$

$$V_s \left[\frac{1}{R_1} + \frac{1}{R_2} \right] - \frac{V_2}{R_1} - \frac{V_o}{R_2} = 0 \rightarrow (1)$$

The nodal eqn at node B is

$$\frac{V_1 - V_3}{R_1} = \frac{V_3}{R_2}$$

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0$$

$$V_3 \left[\frac{1}{R_1} + \frac{1}{R_2} \right] - \frac{V_1}{R_1} = 0 \rightarrow (2)$$

subtracting the above two equations, we get

$$V_3 \left[\cancel{\frac{1}{R_1}} + \cancel{\frac{1}{R_2}} \right] - \frac{V_2}{R_1} - \frac{V_0}{R_2} - V_3 \left[\cancel{\frac{1}{R_1}} + \cancel{\frac{1}{R_2}} \right] + \frac{V_1}{R_1} = 0$$

$$\frac{V_1}{R_1} - \frac{V_2}{R_1} - \frac{V_0}{R_2} = 0$$

$$\frac{1}{R_1} [V_1 - V_2] = \frac{V_0}{R_2}$$

$$\frac{V_0}{V_1 - V_2} = \frac{R_2}{R_1}$$

$$V_0 = \frac{R_2}{R_1} (V_1 - V_2)$$

Differential Mode Gain :

We know that,

$$V_0 = A_d (V_1 - V_2)$$

$$V_0 = A_d \times V_d$$

where, A_d is the differential gain

→ The differential gain is the gain in which differential amplifier amplifies the difference b/w two input signals. Hence it is called as differential gain of the differential amplifier.

→ The difference b/w the two inputs ($V_1 - V_2$) is generally called as difference voltage that is represented by V_d .

$$\text{So, } V_0 = A_d \times V_d$$

$$A_d = \frac{V_o}{V_d}$$

→ The gain is represented by decibals and it is given by $20 \log A_d$.

Common Mode Gain:

→ The gain in which it amplifies the common mode signals (to same signals) to produce the output is called as Common mode gain of the differential amplifier. It is denoted by A_c .

→ If we apply two input voltages which are applied (or) equal in all the respects to the differential amplifier then ideally output voltage must be zero.

$$\text{i.e., } V_o = V_1 - V_2$$

If we know that, $V_1 = V_2$

$$\text{we get, } \boxed{V_o = 0}$$

→ But the o/p voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs.

→ Such an average level of two input signals is called common mode signal, it is denoted as V_c .

$$\text{i.e., } V_c = \frac{V_1 + V_2}{2}$$

→ The o/p voltage is given by, when common input signal is consider.

$$\boxed{V_o = A_c \times V_c}$$

→ Thus there exists some finite o/p. so the total o/p of any differential amplifier can be expressed as

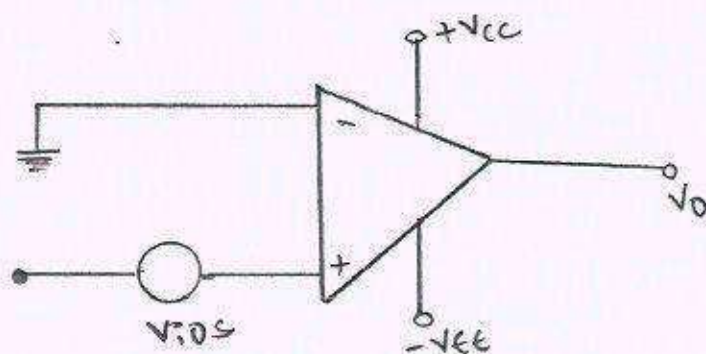
$$V_o = V_d A_d + A_c V_c$$

Note :

→ In op-amp differential mode gain is infinity and common mode gain is zero.

PSRR :

It is defined as the change in i/p offset voltage due to change in any one power supply, remaining power supply must be constant is called as "Power Supply Rejection Ratio". It is also called as power supply sensitivity (PSS).



→ If $V_{ee} = \text{constant}$ & due to certain change in V_{cc} , there is change in i/p offset voltage, then

$$PSRR = \left. \frac{\Delta V_{ios}}{\Delta V_{cc}} \right|_{V_{ee} = \text{constant}}$$

→ If $V_{cc} = \text{constant}$ & due to certain change in V_{ee} , there is change in i/p offset voltage, then

$$PSRR = \left. \frac{\Delta V_{ios}}{\Delta V_{ee}} \right|_{V_{cc} = \text{constant}}$$

Basic Applications of Op-Amp :

A op-amp is a basic building block of linear & non-linear analog systems. In linear circuits (such as adder,

subtractor, differentiator, integrator, voltage to current, I-v convertor, instrumentation amplifier etc.), the o/p signal varies directly or linearly with the i/p signal.

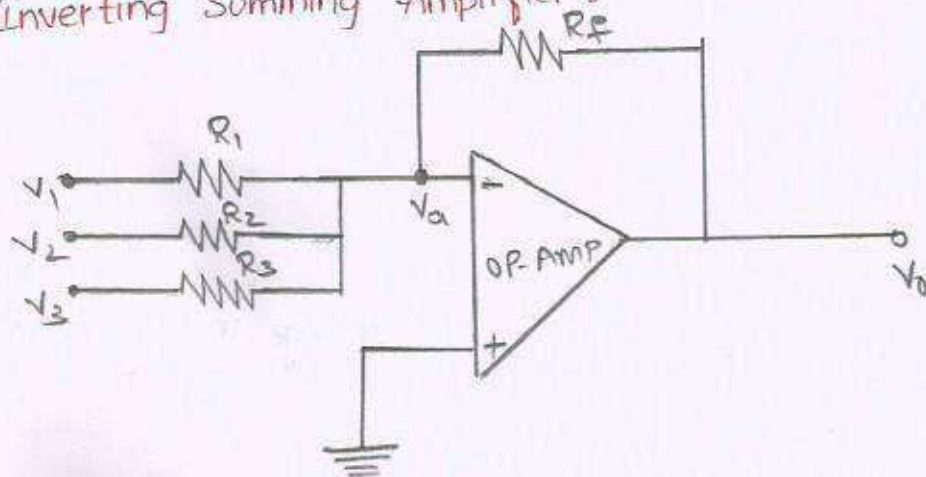
Summing Amplifier :

Op-amp may be used to design the circuit whose o/p is the sum of several i/p signals. Such a circuit is called Summing Amplifier (or) Summer.

→ The summing amplifier are classified into two types.

1. Inverting summing amplifier
2. Non-inverting summing amplifier.

1. Inverting Summing Amplifier :



→ A typical summing amplifier with 3 i/p voltages V_1, V_2, V_3 & three i/p resistors R_1, R_2, R_3 & one feedback resistor R_f shown in above fig.

→ The voltage at node 'a' is zero ($V_a = 0$) because the non-inverting terminal is grounded.

The nodal eqⁿ at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = \frac{V_a - V_0}{R_f}$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_0}{R_f}$$

$$\frac{V_0}{R_f} = - \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

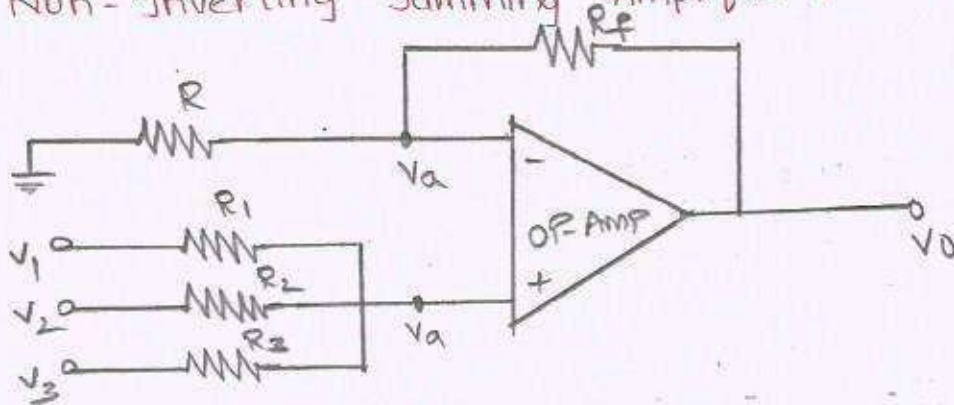
$$V_0 = - \left[V_1 \frac{R_f}{R_1} + V_2 \frac{R_f}{R_2} + V_3 \frac{R_f}{R_3} \right]$$

$$\text{Let } R_1 = R_2 = R_3 = R_f$$

$$V_0 = - [V_1 + V_2 + V_3]$$

where "-ve" sign indicates that phase difference b/w i/p & o/p.
So it is called as inverting summing amplifier.

R. Non-Inverting Summing Amplifier :



- The non-inverting summing amplifier shown in above fig.
- The i/p voltages V_1, V_2, V_3 is fed to the non-inverting terminal. The voltage at non-inverting i/p terminal is V_a .
- The voltage at the inverting i/p terminal will also be V_a , because they are ~~virtually~~ grounded.
- i.e., the voltage across the inverting terminal is same as that of the non-inverting terminal.

The nodal eqⁿ at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$\frac{V_1}{R_1} - \frac{V_a}{R_1} + \frac{V_2}{R_2} - \frac{V_a}{R_2} + \frac{V_3}{R_3} - \frac{R V_a}{R_3} = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = V_a \left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right]$$

$$V_a = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3}$$

w.k.T gain of non-inverting amplifier is

$$A = \frac{V_o}{V_d} = 1 + \frac{R_f}{R_1}$$

But Here $V_d = V_a$

$$V_o = \left[1 + \frac{R_f}{R} \right] V_a$$

sub. V_a in above eqn

$$V_o = \left[1 + \frac{R_f}{R} \right] \left[\frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3} \right]$$

Let $R_1 = R_2 = R_3 = R = R_f/2$

$$V_o = \left[1 + \frac{R_f}{R_f/2} \right] \left[\frac{2V_1/R_f + 2V_2/R_f + 2V_3/R_f}{2/R_f + 2/R_f + 2/R_f} \right]$$

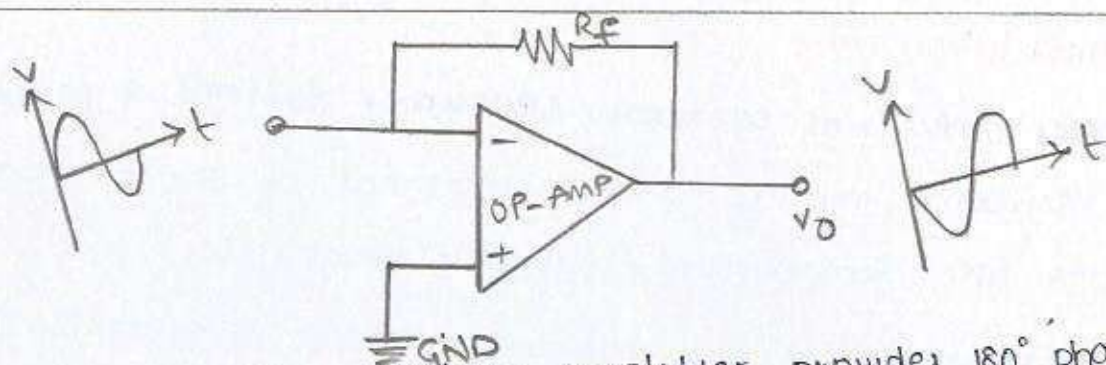
$$= 3 \times \frac{2(V_1 + V_2 + V_3)}{6}$$

$$V_o = V_1 + V_2 + V_3$$

→ Here the o/p voltage is in phase with sum of the i/p voltages. So it is called as non-inverting summing amplifier.

Inverter :

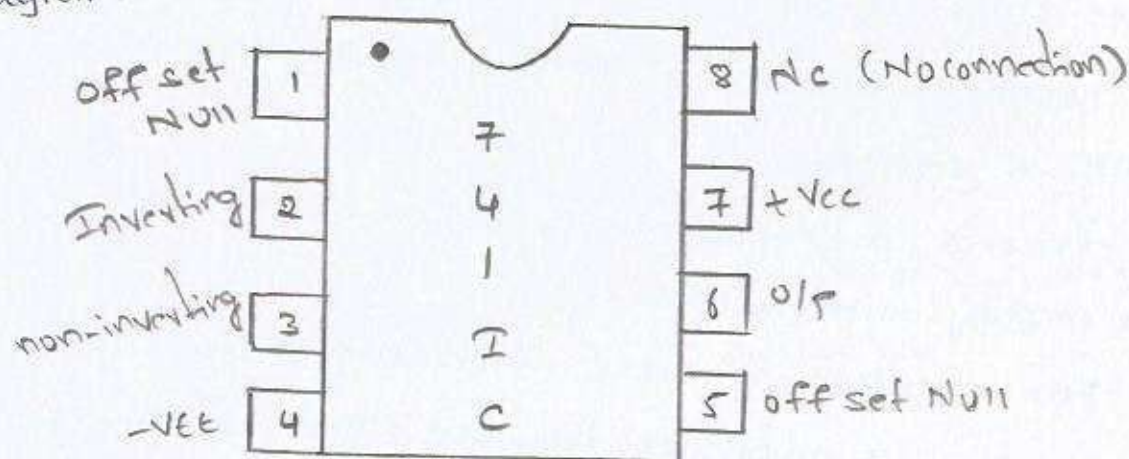
Inverter is defined as o/p is the complement of i/p. For example, let us consider an inverting amplifier as shown in below fig.



→ From fig. the inverting amplifier provides 180° phase shift b/w o/p & i/p. so the op-amp can also be acts as inverter.

741 op-amp and its features:

741 op-amp is a monolithic IC. It is available in 4 pin, 8 pin, 16 pin packages. Let us consider 8 pin package pin diagram.



Features:

1. No frequency compensation required.
2. short circuit protection provided.
3. offset voltage null capability.
4. Common mode & differential voltage range is large.
5. No latch-up.

Instrumentation Amplifier :

Many industrial systems, consumer systems & process control systems require a measurement of the physical quantities like temperature, humidity, weight etc.

→ The measurement of the physical quantities is generally carried out with the help of a device called "Transducer."

→ A transducer is a device which converts one form of energy into another form of energy. Eg: microphone.

→ But most of the transducer o/p are generally very low level signals. Such low level signals are not sufficient to drive the next stage of the op-amp. Hence, before the next stage it is necessary to amplify the level of such signal, rejecting the noise & interference.

→ However, a general amplifier like CE amplifier is not suitable to amplify such signals.

→ For rejection of noise, such amplifiers must have high CMRR. But CE amplifier has low CMRR. So it is not useful. Therefore a special amplifier is used to amplify such signals.

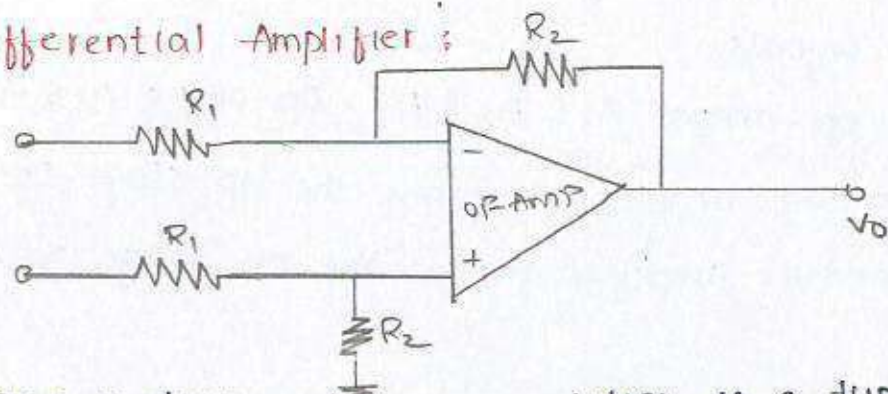
→ A special amplifier which is used for such a low level amplification with high CMRR, high i/p impedance, low o/p impedance, low power consumption is known as instrumentation amplifier. It is also called as Data Amplifier.

→ The requirements of an good instrumentation amplifier is given by :

- (a) High i/p impedance
- (b) Low o/p impedance
- (c) High CMRR

- (d) Low power consumption
- (e) Easier gain adjustment
- (f) High Slew rate.
- (g) Gain is high (or) finite stable gain.

Differential Amplifier:



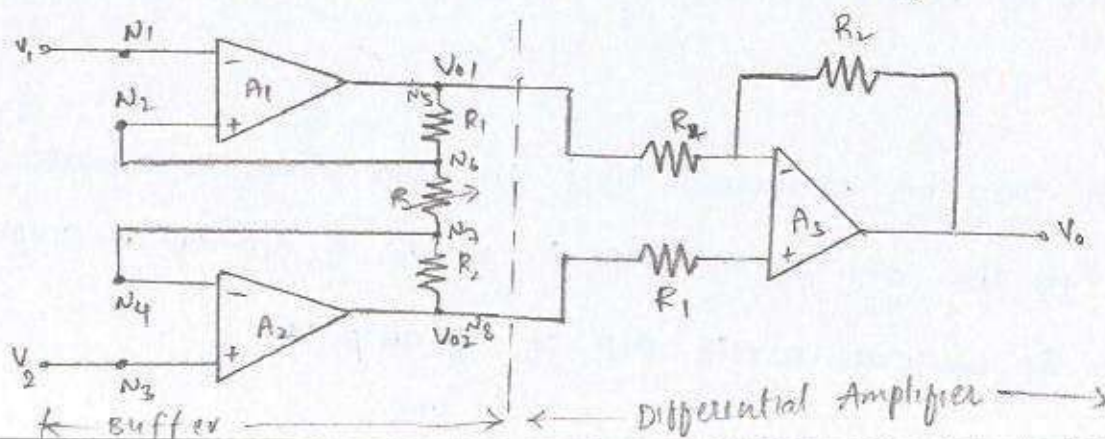
→ The instrumentation amplifier is a type of differential amplifier. Hence differential amplifier is shown in above fig.

From fig.

$$V_0 = \frac{R_2}{R_1} (V_2 - V_1)$$

→ The instrumentation amplifier is a type of D.A i.e., the D.A using op-amp can be used as instrumentation amplifier. But the main problem in using it as an instrumentation amplifier is its i/p impedance.

→ The i/p impedance of D.A is low while the I.A needs very high i/p impedance. To get very high i/p impedance, the D.A can be modified by using Buffer (or) voltage follower circuits at the i/p. It is shown in below fig.



- The gain of the voltage follower circuit is unity. While its i/p impedance is very high. Hence the circuit provides same voltage gain as provided by the op-amp differential amplifier.
- The above ckt provides high i/p impedance for accurate measurement of signals.
- It consists of op-amps A_1 & A_2 & A_3 . Op-amps A_1 & A_2 are the non-inverting amplifiers forms the i/p stage. Op-amp A_3 is the differential amplifier forms the o/p stage of the amplifier.
- One variable resistor R_v is inserted b/w the o/p's of A_1 & A_2 op-amps with the help of this resistor gain can be varied.
- Gain depends on the external resistances & hence can be adjusted accurately.
- The i/p impedance depends on the i/p impedance of the non-inverting amplifier which is very high.
- The o/p impedance is the o/p impedance of the op-amp A_3 which is very low.
- The CMRR of the op-amp A_3 is very high. Thus the circuit satisfies all the requirements of a good instrumentation amplifier & hence commonly used in practical applications.

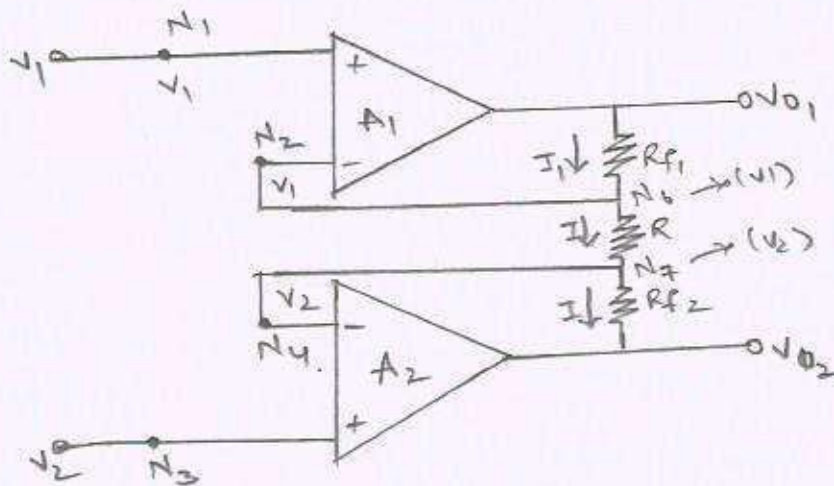
Analysis :

It may be observed that the o/p stage is a basic D.A. Hence if the o/p of op-amp A_1 is V_{o1} & o/p of op-amp A_2 is V_{o2} . So we can write o/p of op-amp is

$$V_0 = \frac{R_2}{R_1} (V_{02} - V_{01}) \rightarrow (1)$$

→ Let us find out the expression for V_{02} & V_{01} in terms of $V_1, V_2, R_{f1}, R_{f2}, R$.

→ Let us consider the first stage of an I.A shown in fig.



→ The node N_1 voltage of op-amp A_1 is V_1 . So that will be appeared at the node N_2 by virtual connection. So the voltage at node N_6 is V_1 .

→ The node N_3 voltage of op-amp A_2 is V_2 . So that will be appeared at the node N_4 by virtual connection. So the voltage at node N_7 is V_2 .

→ The i/p current of op-amp A_1 & A_2 both are zero. Hence current I remains same through R_{f1}, R, R_{f2} .

→ Applying ohms law b/w the nodes N_5 & N_8 , we get

$$I = \frac{V_{01} - V_{02}}{R_{f1} + R + R_{f2}}$$

let, $R_{f1} = R_{f2} = R_f$

$$\text{So } I = \frac{V_{01} - V_{02}}{2R_f + R} \rightarrow (2)$$

Now at the nodes N_6 & N_7

$$\boxed{I = \frac{V_1 - V_2}{R}} \rightarrow (3)$$

Equate eq(2) & eq(3), we get

$$\frac{V_{O1} - V_{O2}}{2R_f + R} = \frac{V_1 - V_2}{R}$$

multiply '-' on b/s, we get

$$\frac{V_{O2} - V_{O1}}{2R_f + R} = \frac{V_2 - V_1}{R}$$

$$V_{O2} - V_{O1} = \frac{V_2 - V_1}{R} (2R_f + R)$$

$$= V_2 - V_1 \left(\frac{2R_f}{R} + \frac{R}{R} \right)$$

$$\boxed{V_{O2} - V_{O1} = V_2 - V_1 \left(1 + \frac{2R_f}{R} \right)} \rightarrow (4)$$

sub. eq(4) in eq(1), we get

$$\boxed{V_O = \frac{R_2}{R_1} \left(1 + \frac{2R_f}{R} \right) (V_2 - V_1)}$$

This is the overall voltage gain of the I.A.

where R is the variable resistor.

$\therefore$ The gain is depends on the R .

Applications :

1. Temperature controller
2. Light intensity meter
3. Analog weight scale
4. Measure the pressure, weight & humidity.

AC Amplifier :

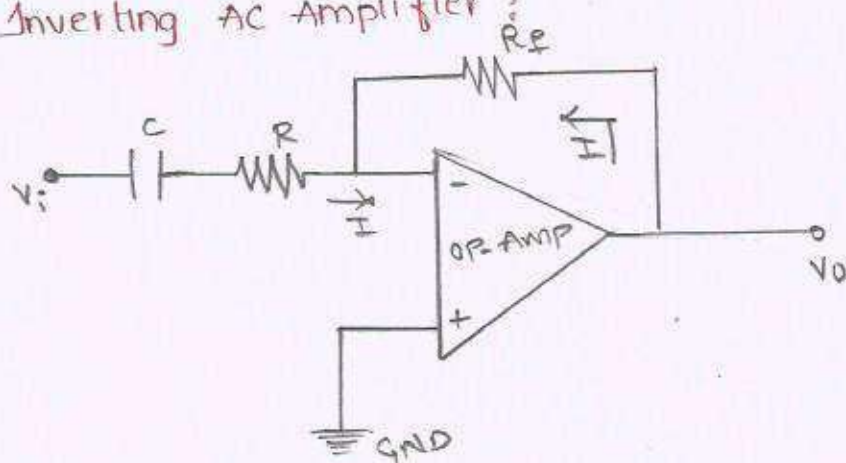
→ The op-amp can amplify both the types of signals i.e., DC to AC. The op-amp responding to AC signal then it is called as AC amplifier.

→ If the AC signal is superimposed with the DC signal, to restrict the amplification of such DC signals, the coupling capacitors must be used at the input of the AC amplifier.

→ There are 2 types of AC amplifiers.

1. Inverting AC amplifier
2. Non-inverting AC amplifier

1. Inverting AC Amplifier :



→ The above circuit shows the inverting AC amplifier because the AC signal is fed to the inverting terminal.

→ The capacitor 'C' blocks the DC components and resistor 'R' sets the lower 3dB frequency of the amplifier.

→ Since node 'a' is at ground potential by the virtual connection. The output voltage V_o is given by

$$V_o = -I R_f$$

from fig.
$$I = \frac{V_i}{R + \frac{1}{j\omega C}}$$

According to laplace transform

$$\text{let } j\omega = s$$

$$\text{So, } \boxed{I = \frac{V_i}{R + \frac{1}{sc}}} \rightarrow (2)$$

Sub. eq(2) in eq(1)

$$V_o = - \left[\frac{V_i}{R + \frac{1}{sc}} \right] \times R_f \rightarrow (3)$$

w.k.T closed loop gain

$$A_{cl} = \frac{V_o}{V_i} \rightarrow (4)$$

Sub. eq(3) in eq(4)

$$A_{cl} = \frac{- \left(\frac{V_i}{R + \frac{1}{sc}} \right) R_f}{V_i}$$

$$= - \frac{1}{R + \frac{1}{sc}} \times R_f$$

$$= - \frac{R_f}{R} \left[\frac{1}{1 + \frac{1}{sCR}} \right]$$

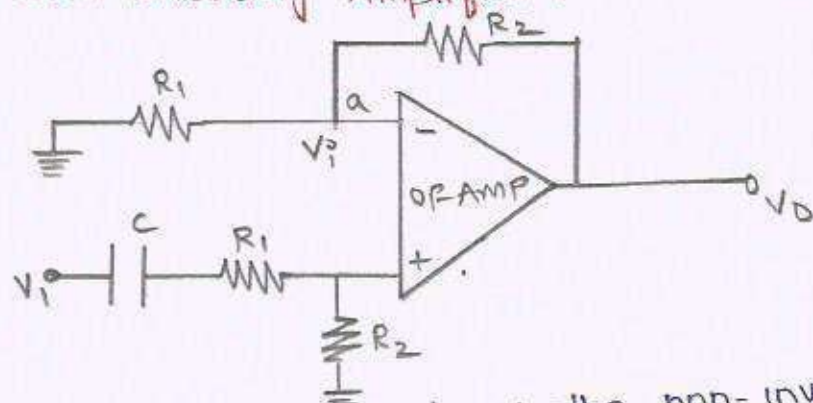
$$= - \frac{R_f}{R} \left[\frac{1}{\frac{1}{s} (1 + \frac{1}{RC})} \right]$$

$$\boxed{A_{cl} = - \frac{R_f}{R} \left[\frac{s}{s + \frac{1}{RC}} \right]}$$

The capacitor 'c' is short circuited for mid frequencies
So the 2nd term in the above eqn becomes unity.

$$\boxed{\therefore A_{cl} = - \frac{R_f}{R}}$$

2. Non-inverting Amplifier :



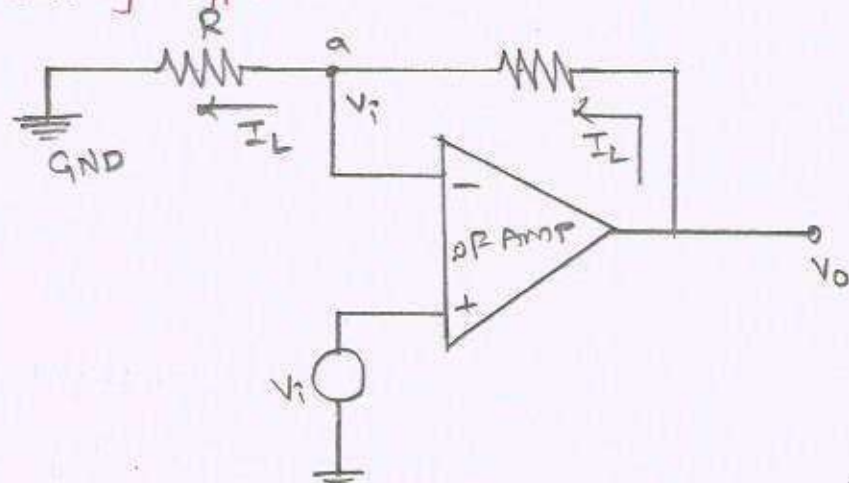
The above fig. shows the non-inverting AC amplifier because the i/p AC signal is fed to the non-inverting terminal. The o/p voltage V_o is given by.

$$V_o = 1 + \frac{R_2}{R_1}$$

Voltage - Current Converter :

- In v-I converter the o/p load current is proportional to the i/p voltage.
- According to connection of load there are 2 types
 1. Floating type v-I converter
 2. Grounded type v-I converter
- In floating type v-I converter, the load resistor R_L is not connected to the ground.
- In grounded type v-I converter, the load resistor R_L is directly connected to the ground.
- This circuit is also called as voltage controlled current source (VCCS) because here the i/p voltage controls the o/p current (or) o/p current is controlled by the input voltage.

1. Floating Type V-I convertor :



→ The above fig. shows the v-i convertor. Here the load resistor R_L is not connected to the ground.

Since the voltage at node 'a' is $V_i = I_L R$

$$\therefore I_L = \frac{V_i}{R}$$

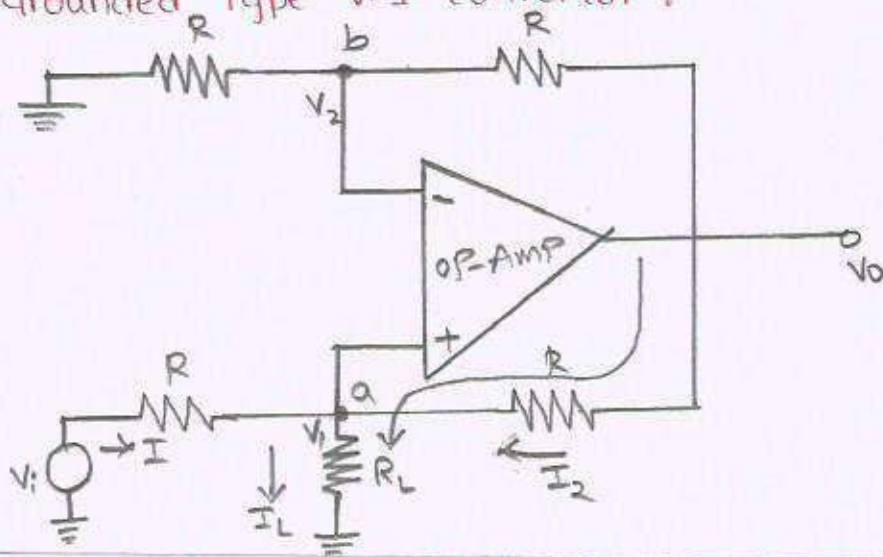
→ Thus the load current is directly proportional to the i/p voltage and it is given by

$$I_L \propto V_i$$

i.e., the i/p voltage V_i is converted into an o/p current I_L .

Here we observed that the proportionally constant is generally $1/R$. Therefore this circuit is called Transconductance amplifier.

2. Grounded Type V-I convertor :



→ A V-I convertor with grounded load is shown in above fig.

→ Let V_1 be the voltage at node 'a'. applying KCL at node 'a' we get

$$\boxed{I_1 + I_2 = I_L} \rightarrow (1)$$

From fig. $I_1 = \frac{V_i - V_1}{R_f} \rightarrow (2)$

$$I_2 = \frac{V_o - V_1}{R} \rightarrow (3)$$

Sub. eq(2) & eq(3) in eq(1)

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = I_L$$

$$V_i - V_1 + V_o - V_1 = I_L R$$

$$V_i - 2V_1 + V_o = I_L R$$

$$\boxed{V_1 = \frac{V_i + V_o - I_L R}{2}} \rightarrow (4)$$

W.K.T, $A = \frac{V_o}{V_i} = 1 + \frac{R_f}{R}$

But Here we have $R_f = R$

$$\frac{V_o}{V_i} = 1 + \frac{R}{R}$$

$$= 2$$

$$\boxed{V_o = 2V_i} \rightarrow (5)$$

Sub. eq(4) in eq(5)

$$V_o = \frac{2(V_i + V_o - I_L R)}{2}$$

$$V_o = V_i + V_o - I_L R$$

$$V_i = I_L R$$

$$\therefore I_L = \frac{V_i}{R}$$

→ From the above expression, we can say that the load current I_L depends on the i/p voltage V_i .

$$\therefore I_L \propto V_i$$

Applications :

1. Low voltage to dc voltage convertor
2. Diode tester
3. Zener Diode tester.

Current - Voltage Convertor :

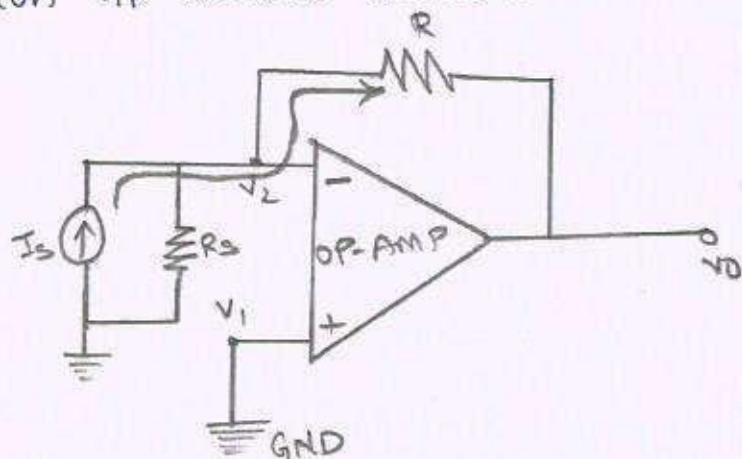
→ In I-v convertor the o/p voltage is directly proportional to the i/p current.

$$V_o \propto I_s$$

where, V_o = o/p voltage

I_s = i/p current

→ This circuit is also called as current controlled voltage source (CCVS) because the o/p voltage is controlled by i/p current (or) i/p current controls the o/p voltage.



→ The above fig. shows the current to voltage converter because of virtual ground the voltage $V_2 = 0$.

Applying KCL at node 'a'.

$$I_S = \frac{V_2 - V_0}{R}$$

$$V_2 = 0$$

$$I_S = \frac{-V_0}{R}$$

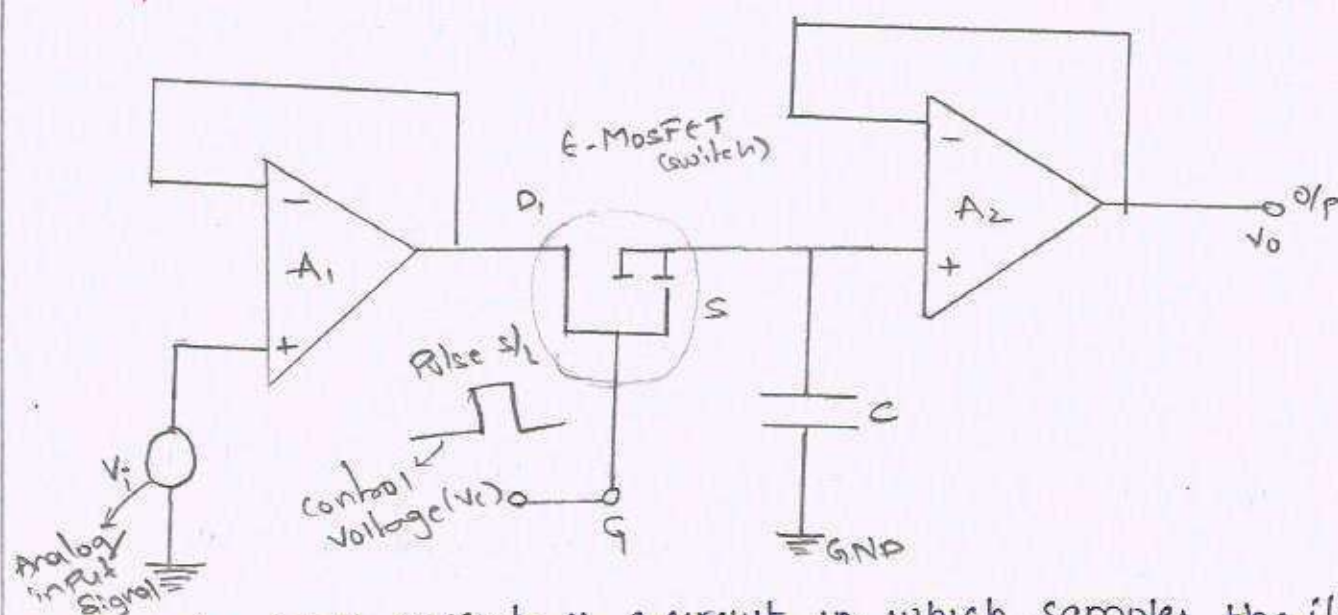
$$V_0 = -I_S R$$

→ Thus the o/p voltage is proportional to the i/p current so the circuit works as current to voltage converter. It is also called as Trans resistance amplifier.

Applications:

1. Photo diode detectors
2. Photo Fet detector.

Sample And Hold Circuits :



→ Sample hold circuit is a circuit in which samples the i/p signal and holds on to its last sampled value until the o/p is sampled again.

→ This type of circuit is very useful in analog to digital convertors & digital communications etc.

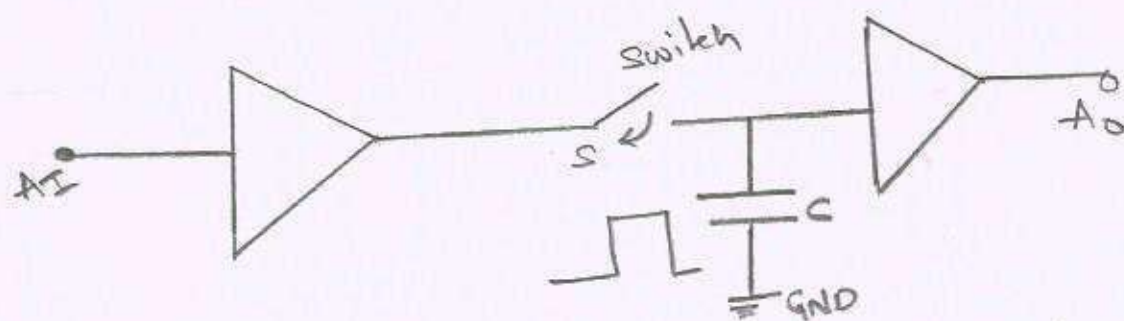
→ The above fig. E-MOSFET acts as switch & is controlled by the control voltage V_c & Capacitor 'C' stores the charge.

→ The analog signal V_i to be sampled is applied at the non-inverting terminal of A_1 op-amp & the same ~~app~~ V_i appeared at the drain terminal of E-MOSFET. When the control voltage V_c is applied to its gate, the +ve half cycle is going, the MOSFET is ON which acts as a closed switch & the capacitor 'C' charged by the i/p voltage V_i and the same voltage appears at the o/p of the op-amp.

→ When -ve half cycle is going the MOSFET is switched OFF & only discharge path for capacitor C through non-inverting i/p of the op-amp.

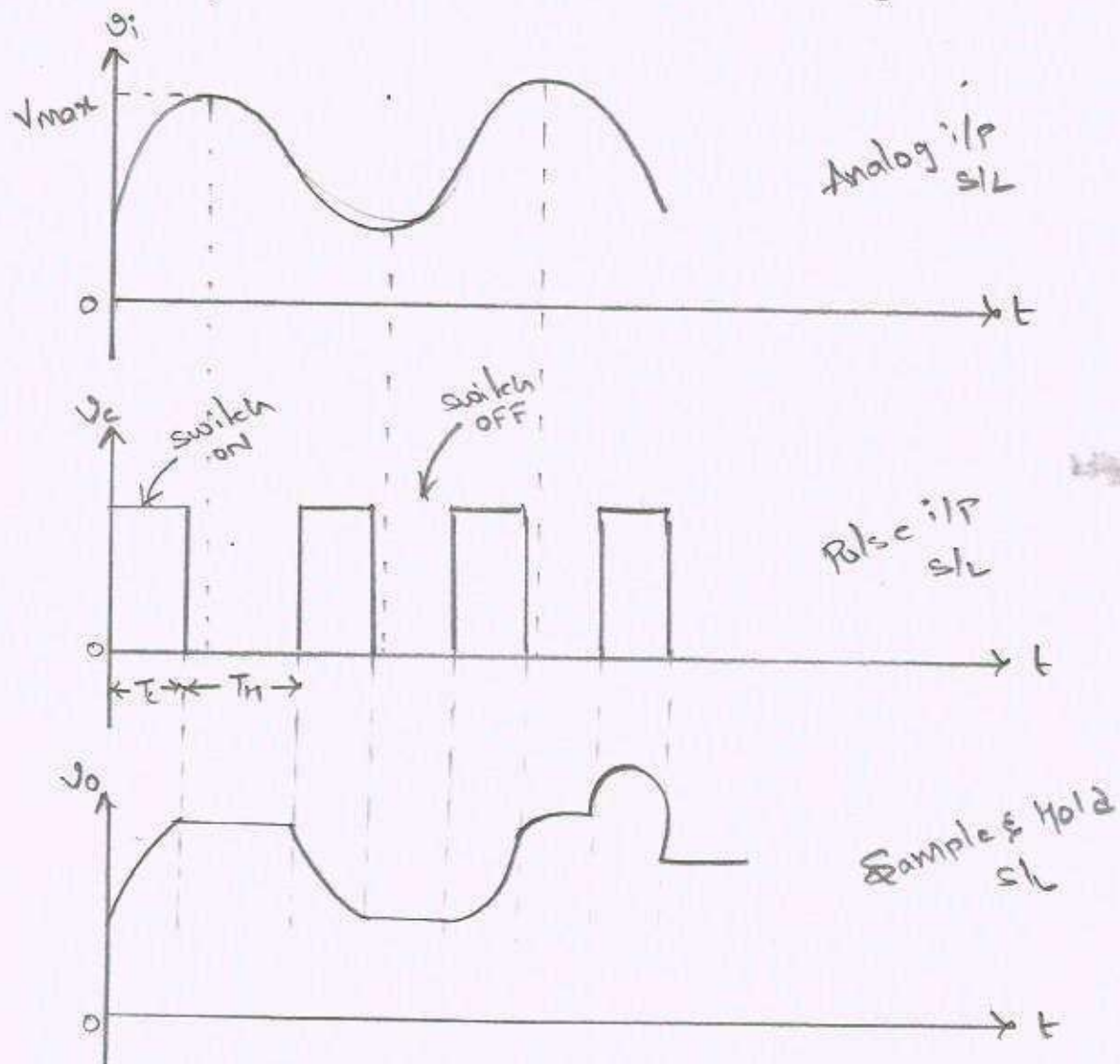
→ Since the i/p impedance of the op-amp is high, the voltage V_i is retained & it is appears at the o/p of the op-amp.

→ The i/p & o/p waveforms of the circuit shown in below fig.



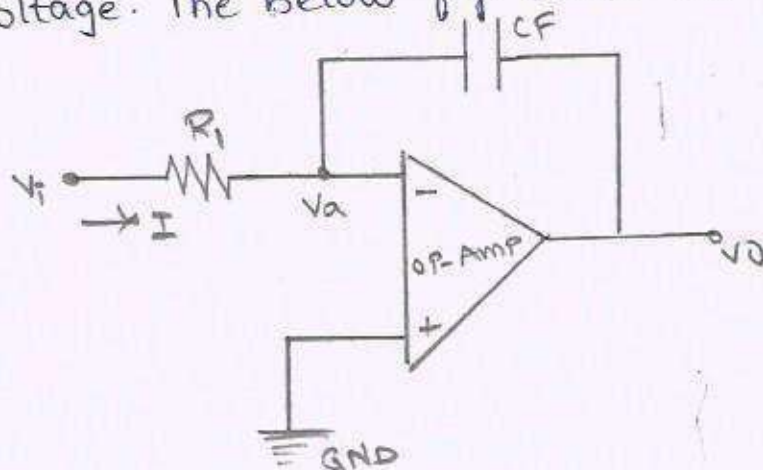
→ The time period of the signal during which the voltage across the capacitor (V_c) is equal to V_i is called sample period (T_s) (or) on time (or) charging time.

→ The time period of the signal during which the voltage across the capacitor V_c is held constant are called Hold period (T_H) (or) OFF time (or) Discharging time.



Integrator :

Integrator is a circuit in which op voltage is integral of i/p voltage. The below fig. shows the ideal integrator circuit.



→ The i/p voltage V_i is applied to the inverting i/p terminal through

R_1 resistor.

→ The capacitor current I is given by $I = C_f \frac{dv}{dt}$.

→ Since o/p current of Op-amp is zero, the entire current I flowing through R_1 & C_f .

Applying KCL at node 'a'

$$\text{For i/p side } I = \frac{V_i - V_a}{R_1}$$

where $V_a = 0V$; because virtual connection

$$I = \frac{V_i}{R_1} \rightarrow (1)$$

$$\text{At o/p side ; } I = C_f \frac{d(V_a - V_o)}{dt}$$

$$I = -C_f \frac{dV_o}{dt} \rightarrow (2)$$

equating eq(1) & eq(2)

$$\frac{V_i}{R_1} = -C_f \frac{dV_o}{dt}$$

$$dV_o = - \frac{V_i dt}{R_1 C_f}$$

integrating on b.s, we get

$$\int_0^t dV_o = - \frac{1}{R_1 C_f} \int_0^t V_i dt$$

$$V_o(t) - V_o(0) = - \frac{1}{R_1 C_f} \int_0^t V_i(t) dt$$

$$V_o(t) = - \frac{1}{R_1 C_f} \int_0^t V_i(t) dt + V_o(0)$$

Where, $R_1 C_f = \tau$ = Time constant of integrator

$V_o(0)$ is the initial o/p voltage

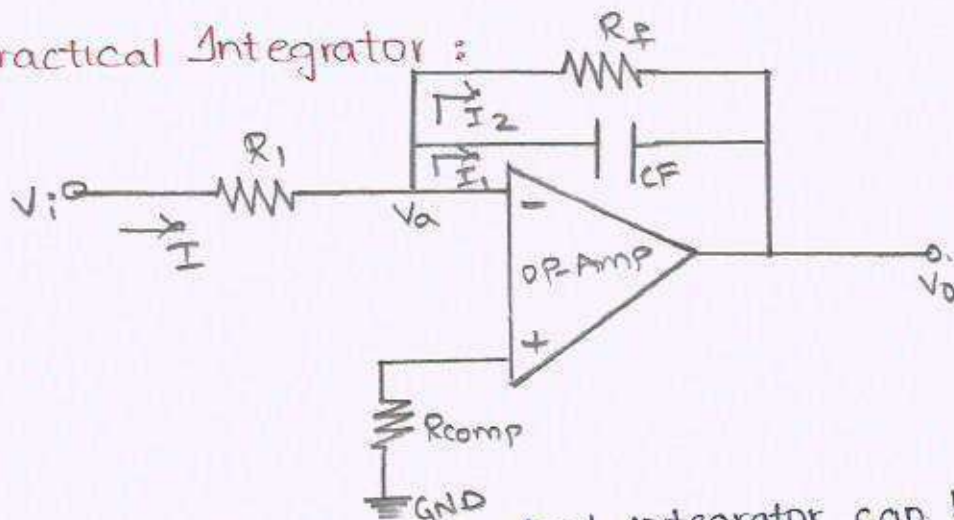
→ The above eqn shows that the o/p is $-\frac{1}{R_1 C_f}$ times the integral of i/p.

Drawbacks :

1. Without giving any i/p, we get some voltage at the o/p so we can treat that as error signal.
2. Capacitor gets charging & discharging due to bias currents & add its effects on o/p error voltage. After sometime o/p of op-amp may achieve its saturation level.
3. Band width is very small for ideal integrator. Hence ideal integrator can be used for very small frequency range of i/p's only.

→ Because of all the above drawbacks the ideal integrator is not used in practically. Some additional components are used along with basic integrator circuit to reduce the effect of an error voltage in practically such an integrator is called as practical integrator circuit.

Practical Integrator :



→ The drawbacks of an ideal integrator can be minimised in the practical integrator circuit, which consists of resistance R_F in parallel with the capacitance C_F .

→ The practical integrator circuit shown in above fig.

→ The resistance R_{comp} is used to overcome the errors due to the bias currents.

→ The resistance R_f reduces the low frequency gain of the Op-amp.

→ The parallel combination of R_f & C_f behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason this circuit is also called as "Lossy integrator."

→ Since i/p current of op-amp is zero, from the concept of virtual ground $V_a = 0$.

Applying KCL at node 'a',

$$I = I_1 + I_2 \rightarrow (1)$$

But
$$I = \frac{V_i - V_a}{R_i}$$

$$I = \frac{V_i}{R_i} \rightarrow (2)$$

$$I_1 = -C_f \frac{dV_o}{dt} \rightarrow (3)$$

$$I_2 = \frac{-V_o}{R_f} \rightarrow (4)$$

Sub. eq(2), (3) & (4) in eq(1)

$$\frac{V_i}{R_i} = -C_f \frac{dV_o}{dt} - \frac{V_o}{R_f}$$

Apply L.T on b.s, we get

$$\frac{V_i(s)}{R_i} = -sC_f V_o(s) - \frac{V_o(s)}{R_f}$$

$$\frac{V_i(s)}{R_i} = -V_o(s) \left[sC_f + \frac{1}{R_f} \right]$$

$$V_o(s) = \frac{-V_i(s)}{R_i \left[sC_f + \frac{1}{R_f} \right]}$$

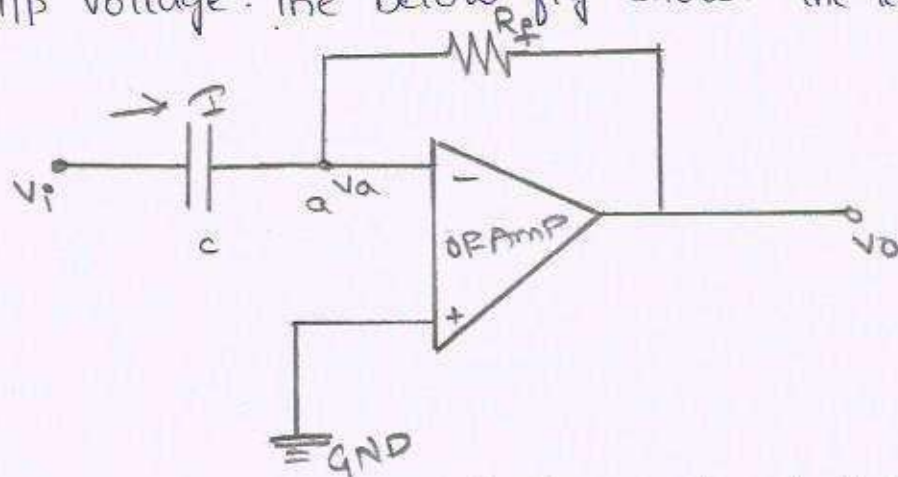
$$V_o(s) = \frac{-V_i(s)}{sCR_i + R_i/R_f}$$

Applications :-

1. It is used in Analog computers
2. It is used in analog to digital convertors
3. It is used in solving differential equations
4. It is used in wave shapping circuits.

Differentiator :-

Differentiator is a circuit in which o/p voltage is differentiate of i/p voltage. The below fig. shows the ideal differentiator.



The node 'a' is at virtual ground potential i.e., $V_a = 0$.

→ The current I flowing through the capacitor is

$$I = C \frac{dv}{dt}$$

→ Apply KCL at node 'a'

$$I = C \frac{d(V_i - V_a)}{dt}$$

Due to virtual connection $V_a = 0$

$$I = C \frac{dV_i}{dt} \rightarrow (1)$$

Similarly at the o/p side

$$I = \frac{V_a - V_o}{R_f}$$

$$I = \frac{-V_o}{R_f} \rightarrow (2)$$

Equating above 2 equs

$$C \frac{dV_i}{dt} = \frac{-V_o}{R_f}$$

$$V_o = -R_f C \frac{dV_i}{dt}$$

where, $R_f \cdot C$ = Time constant.

→ Thus the o/p voltage V_o is constant ($-R_f \cdot C$) times the derivative of the i/p voltage.

Drawbacks :

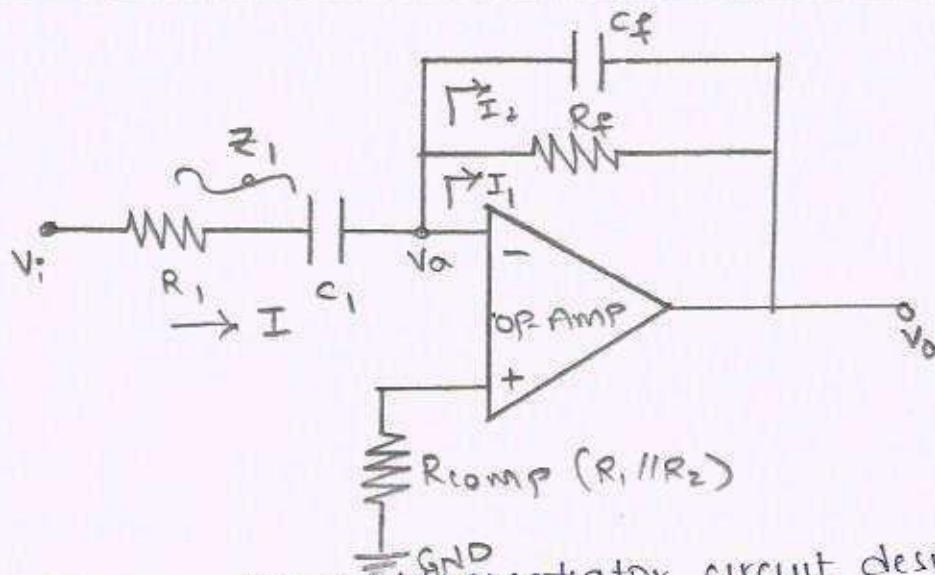
1. The gain of the differentiator increases at frequency increases. Thus at some high frequency the differentiator may become unstable & break into the oscillations.
2. The i/p impedance $X_{ci} = \frac{1}{2\pi f C}$, if frequency increases impedance decreases. This makes the circuit very much sensitive to the noise.
3. This noise may completely overwrite the o/p of the differentiator.

Hence the differentiator circuit ~~satisfies~~ suffers from the stability & noise problem at high frequencies.

→ These problems can be overcome by adding additional components.

Practical Differentiator :

→ The differentiator circuit suffers from the stability & noise problems at high frequencies. These problems can be eliminated by practical differentiator.



→ The practical differentiator circuit designed by using resistance R_1 is in series with C_1 & capacitor C_f is in parallel with resistance R_f .

→ The resistance R_{comp} is used for bias compensations.

Analysis :

→ The current I flowing through the R_1 & C_1 components. But the series combination of R_1 & C_1 is denoted by impedance Z_1 .

$$\text{So, } I = \frac{V_i}{Z_1}$$

According to L.T

$$I = \frac{V_i(s)}{Z_1} \rightarrow (1)$$

$$\text{N.K.T, } Z_1 = R_1 + \frac{1}{j\omega C_1}$$

$$= R_1 + \frac{1}{sC_1}$$

$$Z_1 = \frac{R_1 s C_1 + 1}{s C_1}$$

Sub. Z_1 in eq(1)

$$I = \frac{V_i(s) s C_1}{1 + R_1 s C_1}$$

Similarly $I_1 = \frac{-V_o}{R_f}$

$$I_1 = \frac{-V_o(s)}{R_f}$$

$$I_2 = -C_f \frac{dV_o}{dt}$$

$$I_2 = -sC_f V_o(s)$$

Apply KCL at node 'a'

$$I = I_1 + I_2$$

$$\frac{V_i(s) sC_1}{1 + R_1 sC_1} = \frac{-V_o(s)}{R_f} - sC_f V_o(s)$$

$$= \frac{-V_o(s)}{R_f} - V_o(s) \left[\frac{1}{R_f} + sC_f \right]$$

$$= -V_o(s) \left[\frac{1 + sC_f R_f}{R_f} \right]$$

$$V_o(s) = - \frac{V_i(s) sC_1 R_f}{(1 + sC_1 R_1)(1 + sC_f R_f)}$$

Let us assume $R_f C_f = R_1 C_1$

$$V_o(s) = - \frac{V_i(s) sC_1 R_f}{(1 + sC_f R_f)^2}$$

If $R_f C_1 \gg C_f R_f$, then the denominator can be neglected

$$\therefore V_o(s) = -V_i(s) sC_1 R_f$$

By applying inverse L.T to the above eqn, we get

$$\therefore V_o(t) = -R_f C_1 \frac{dV_i(t)}{dt}$$

Applications :

1. It is used in wave shaping circuits
2. It is used in convertors i.e., analog to digital.

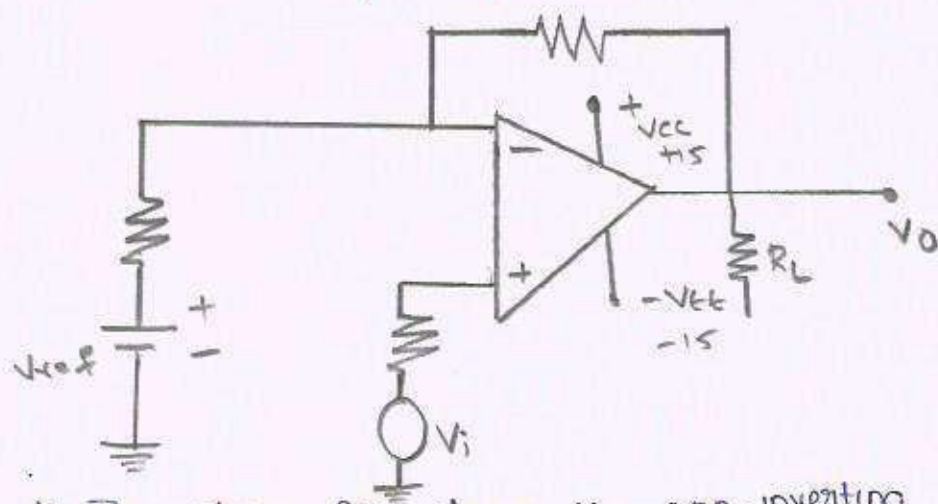
Comparator :

→ Comparator is a circuit in which compares the signal voltage at one i/p terminal of an op-amp with a known reference voltage at another i/p terminal of an op-amp.

→ Basically comparators are of 2 types.

1. Non-Inverting Comparator
2. Inverting Comparator.

1. Non-Inverting Comparator :



→ The above fig. shows the non-inverting comparator.

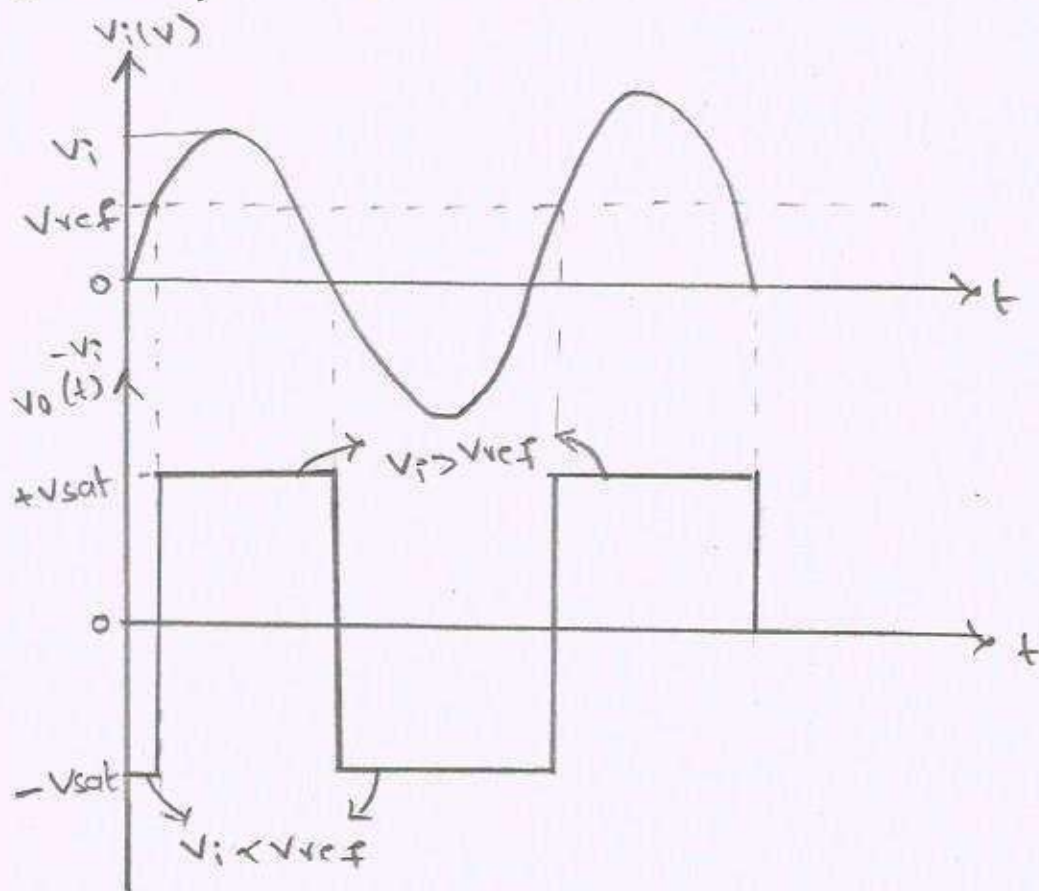
→ A fixed reference voltage V_{ref} is applied to the inverting i/p terminal & signal voltage V_i is applied to the non-inverting i/p terminal.

→ Because of this arrangement the circuit is called non-inverting comparator.

→ When $V_i < V_{ref}$, the o/p voltage V_o is at $-V_{sat}$ ($\cong -V_{EE}$) because the voltage at the inverting i/p terminal (-ve i/p terminal) is higher than that of non-inverting i/p terminal (+ve i/p terminal).

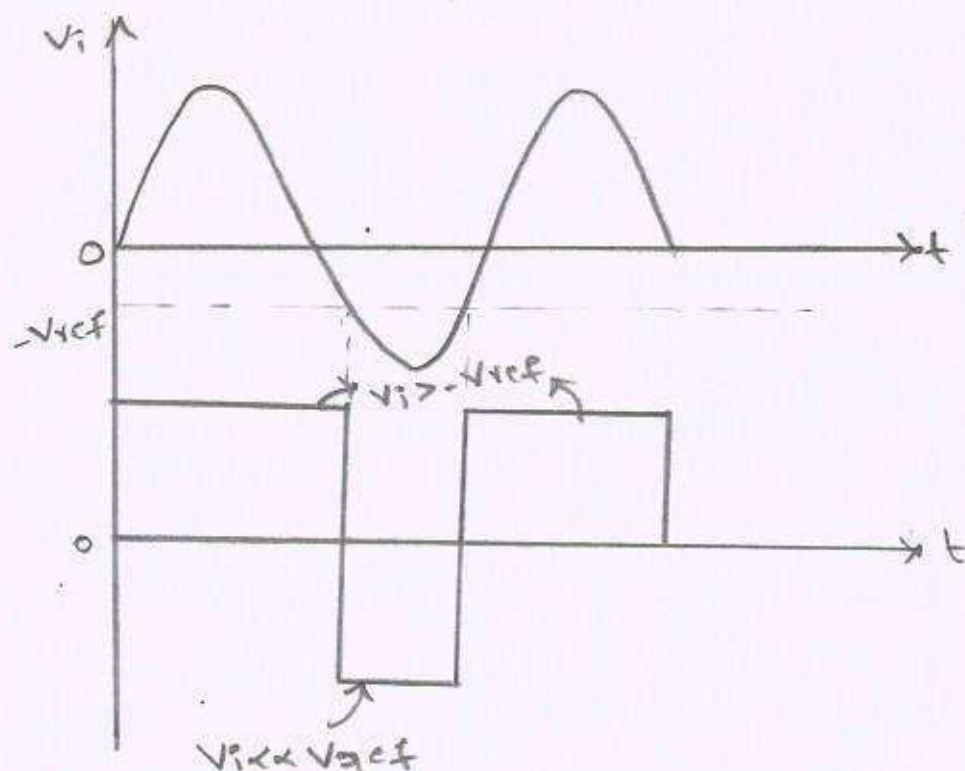
→ Similarly when $V_i > V_{ref}$, the +ve i/p voltage is greater than the -ve i/p voltage. so o/p voltage V_o goes to $+V_{sat}$ ($\cong +V_{CC}$).

→ Thus o/p voltage V_o changes from one saturation level to another saturation level whenever $V_i = V_{ref}$, the corresponding i/p & o/p waveforms for +ve reference v/tg is shown in fig.

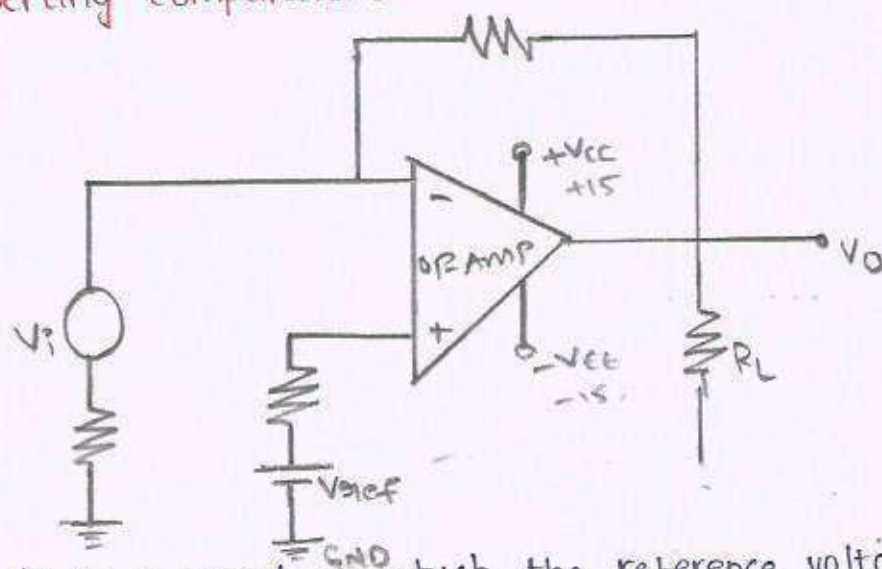


→ if the reference voltage V_{ref} is -ve with respect ground with the signal applied to the +ve terminal.

→ The corresponding waveforms are shown below.



Inverting Comparator:

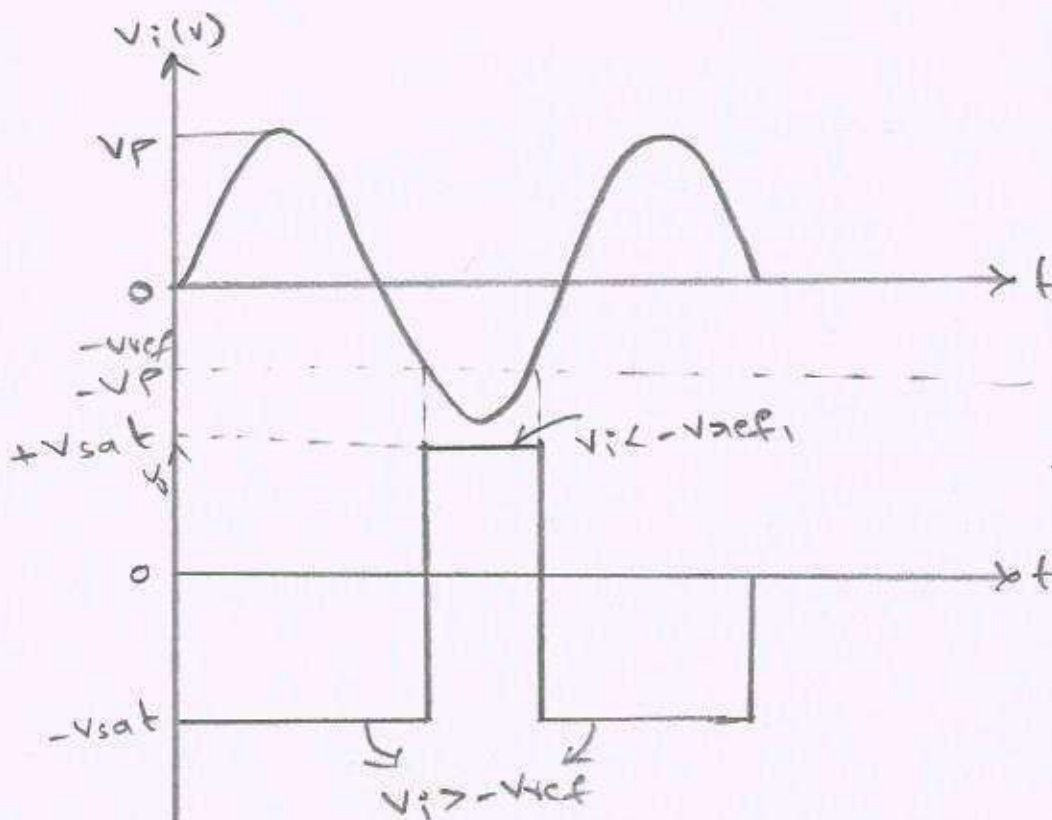
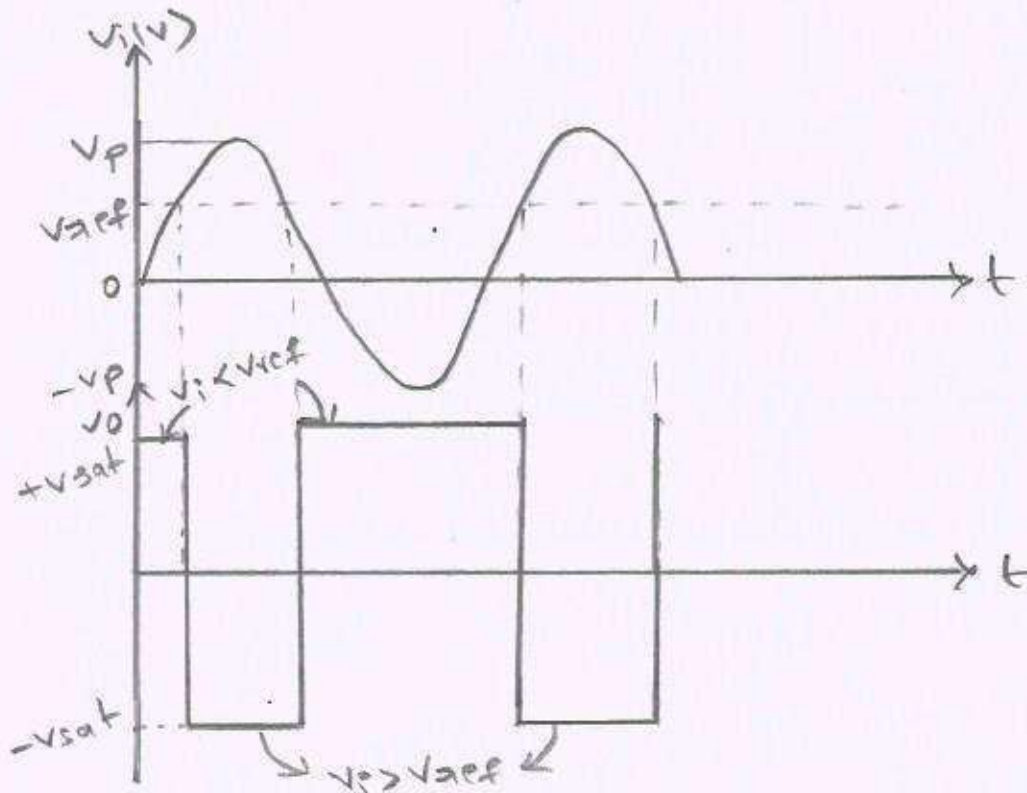


→ It is a circuit in which the reference voltage V_{ref} is applied to non-inverting terminal & signal voltage is applied to the inverting terminal.

→ When $V_i < V_{ref}$, the o/p voltage V_o is at $+V_{sat}$ ($+V_{CC}$), because the voltage at the inverting input is less than that the non-inverting i/p voltage.

→ Similarly when $V_i > V_{ref}$, the non-inverting i/p is less than the inverting i/p then V_o goes to $-V_{sat}$ ($-V_{EE}$).

→ The corresponding waveforms is shown in below fig.



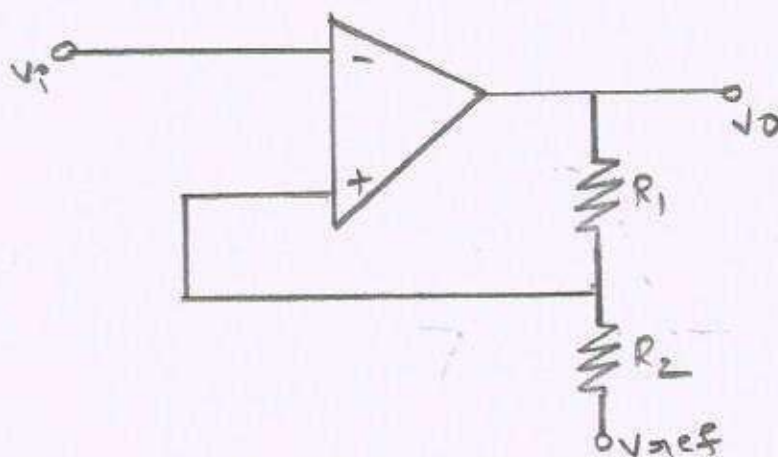
Applications :

1. Zero crossing detector

2. Schmitt trigger (regenerative comparator)

Schmitt Trigger :

- In basic comparator circuit f/b is not used & op-amp is used in open loop mode.
- In open loop op-amp gain is large. At any cost where small noise voltages can cause triggering of the comparator. Such unwanted noise cause the o/p to jump b/w high & low state.
- The comparator circuit used to avoid such unwanted triggering (change) is called regenerative comparator (or) schmitt trigger which basically uses +ve f/b.
- A comparator circuit with +ve f/b is known as schmitt trigger (or) regenerative comparator.



- A +ve f/b comparator with signal is applied at -ve i/p is shown in above fig.
- The i/p voltage V_i triggers the o/p voltage V_o everytime it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) & lower threshold voltage (V_{LT})
- The difference b/w these voltages are called hysteresis voltage (V_H)

$$\therefore V_H = V_{UT} - V_{LT}$$

→ The threshold voltages are calculated as follows.

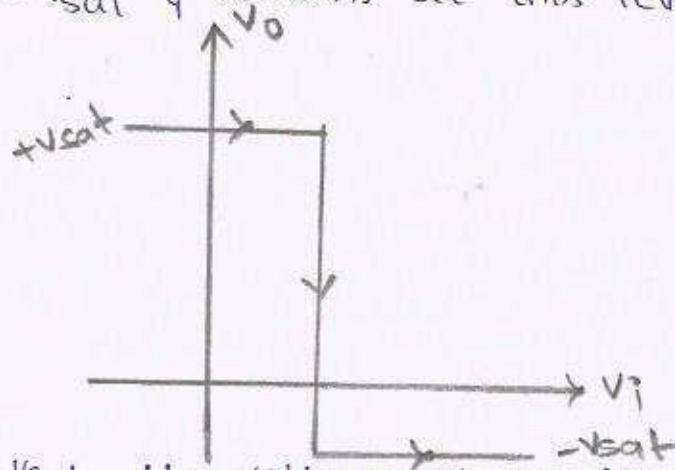
(a) Suppose o/p voltage $V_o = +V_{sat}$, the voltage at +ve i/p terminal can be obtained by using super position theorem.

$$V_{UT} = \frac{V_{ref} \cdot R_1}{R_1 + R_2} + \frac{V_{sat} R_2}{R_1 + R_2}$$

This voltage is called upper threshold voltage (V_{UT}).

(b) If $V_i < V_{UT}$, the o/p V_o remains constant at $+V_{sat}$.

(c) When V_i is just greater than V_{UT} , the o/p regeneratively switches to $-V_{sat}$ & remains at this level until $V_i > V_{UT}$.



(d) For $V_o = -V_{sat}$, the voltage at +ve i/p terminal is

$$V_{LT} = \frac{V_{ref} \cdot R_1}{R_1 + R_2} - \frac{V_{sat} R_2}{R_1 + R_2}$$

This voltage is called lower threshold voltage.

(e) The i/p voltage is V_i must become lesser than V_{LT} in order to cause V_o to switch from $-V_{sat}$ to $+V_{sat}$.

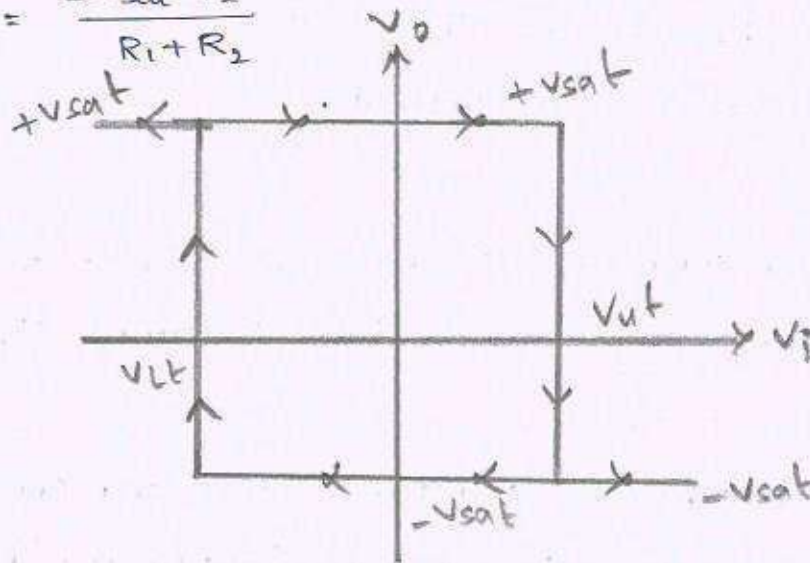
(f) A regenerative transition takes place & o/p V_o returns from $-V_{sat}$ to $+V_{sat}$, shown in below fig.

(g) The difference b/w 2 threshold voltage called as hysteresis voltage V_H

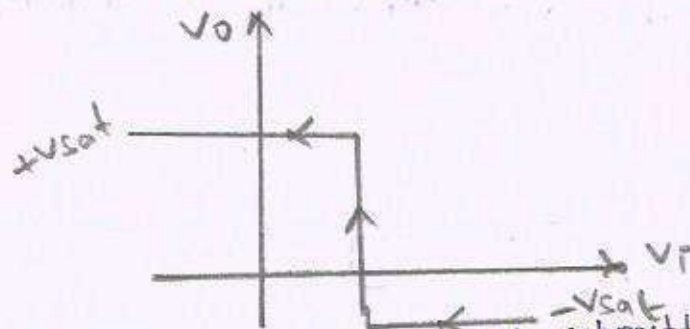
$$V_H = V_{UT} - V_{LT}$$

$$= \frac{V_{ref} \cdot R_1}{R_1 + R_2} + \frac{V_{sat} \cdot R_2}{R_1 + R_2} - \frac{V_{ref} \cdot R_1}{R_1 + R_2} + \frac{V_{sat} \cdot R_2}{R_1 + R_2}$$

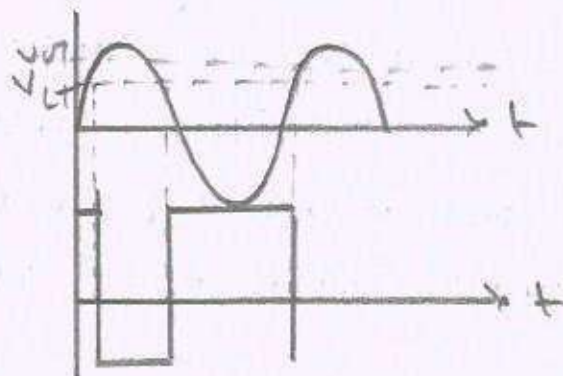
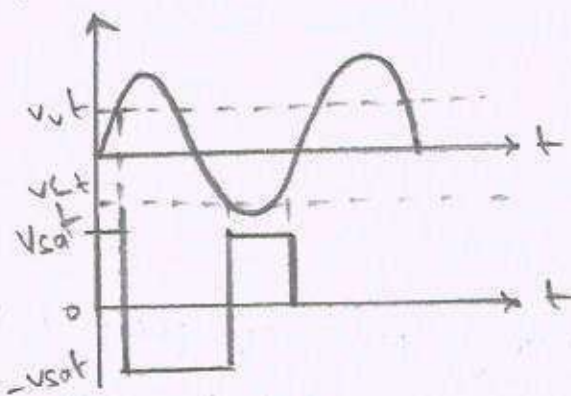
$$V_H = \frac{2 V_{sat} \cdot R_2}{R_1 + R_2}$$



(h) The hysteresis curve is shown in below fig.



→ Corresponding i/p & o/p waveform, of schmitt trigger shown in fig.



Multivibrators:

Multivibrators is used to generate non-sinusoidal signals, multivibrators are regenerative circuits.

Basically multivibrators are three types.

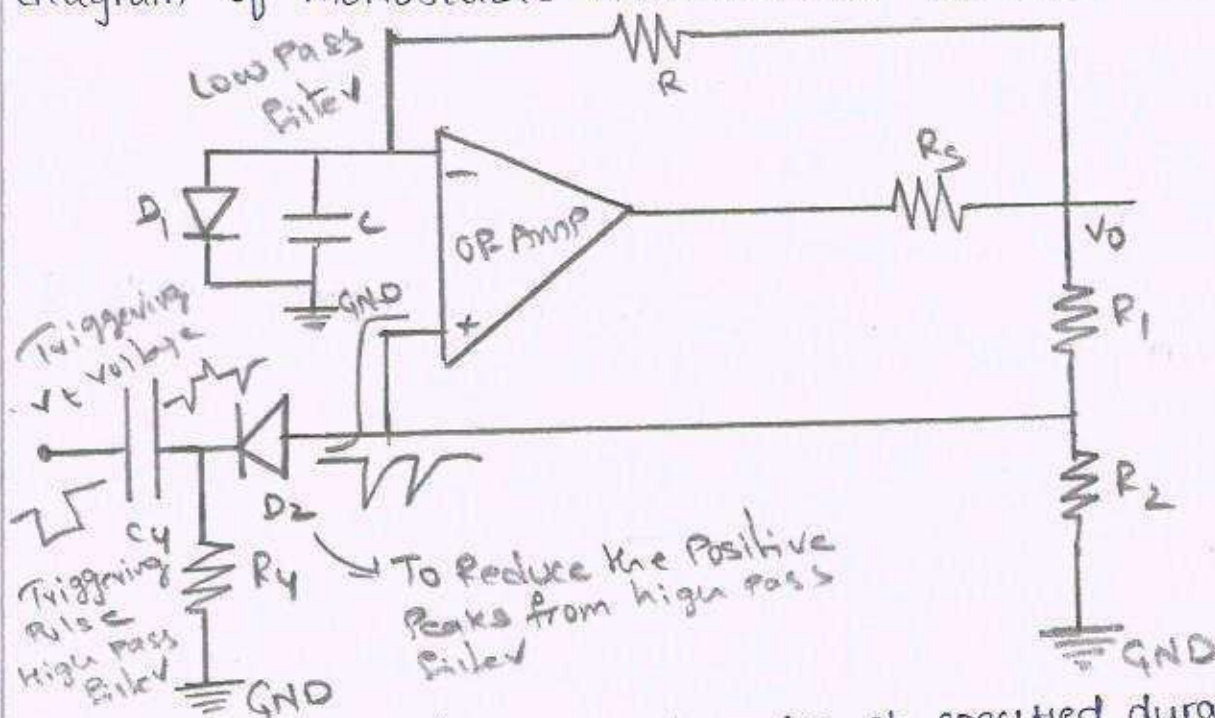
1. Bistable
2. Astable
3. Monostable

(a) Bistable Multivibrator:

In Bistable multivibrator has two stable states we use two triggering pulse to change stable state to quasi stable state.

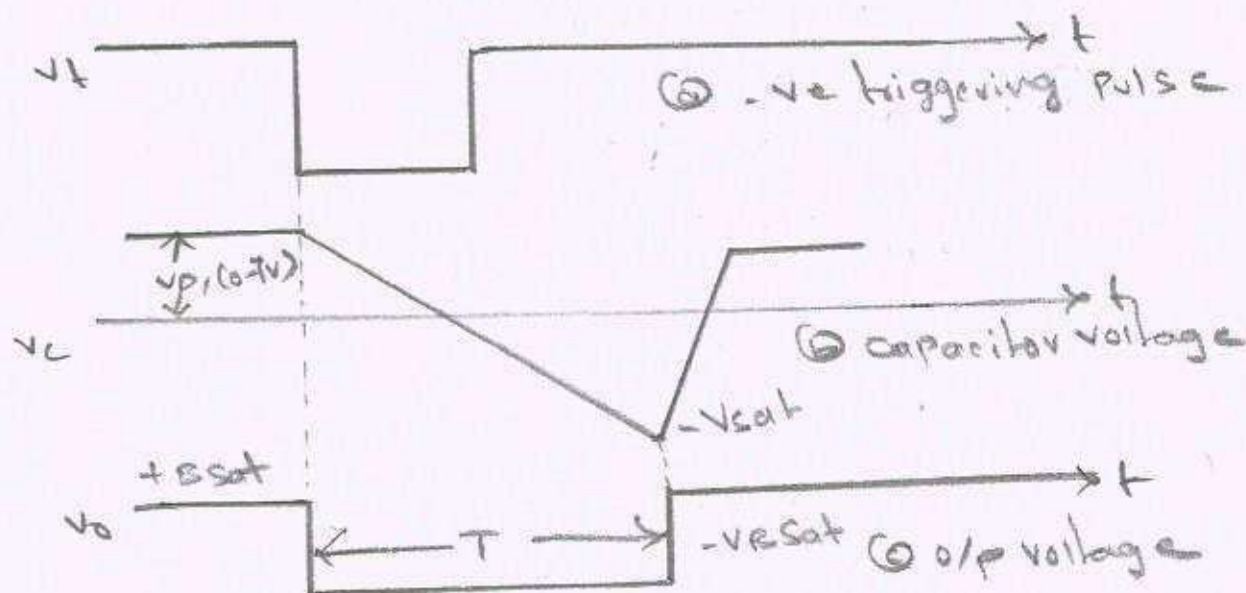
(b) Monostable Multivibrator:

Monostable multivibrators are stable state and one quasi stable state. It is also called as one shot multivibrator. The circuit diagram of monostable multivibrator are shown in below fig.



- The circuit produces a single pulse of specified duration in response to each external trigger signal for such circuit produces one stable state. When external trigger is applied, the op changes its stable state into state is called "quasi stable state".
- The diode D_1 clamping diode is connected across capacitance C_1 .
- The diode clamps the capacitor voltage to $0.7V$ when the op is at $+V_{sat}$.

- A negative going pulse signal V_t passing through the high pass filter R_4C_4 and diode D_2 produces negative going triggering pulse and it is applied to the non-inverting terminal.
- To understand the operation let us assume that the o/p V_o is at $+V_{sat}$ that is in its stable state.
- The diode D_1 conducts and the voltage across the capacitor is clamped at $0.7V$.
- The voltage at the non-inverting i/p terminal is controlled by potentiometric divider R_1, R_2 to βV_{sat} .
- Now, if a negative triggering pulse applied to non-inverting terminal, so that the effective voltage at this terminal is less than $0.7V$ because $\beta V_{sat} - V_t < 0.7V$.
- Then o/p changes its state from $+V_{sat}$ to $-V_{sat}$.
- The diode will now get reverse bias and capacitor starts discharging through resistance R .
- The voltage at the non-inverting i/p terminal is now $-\beta V_{sat}$.
- When capacitor voltage V_c becomes just slightly more -ve than $-\beta V_{sat}$, then o/p of the op-amp changes from $-V_{sat}$ to $+V_{sat}$ again capacitance gets charging $+V_{sat}$ through resistance R until capacitor voltage reaches $0.7V$.



Derivation of pulse width (P):

For low pass filter a general expression is given by

$$V_o = V_f + (V_i - V_f) e^{-t/RC}$$

where, V_f = final value of voltage

V_i = initial value of voltage

From the monostable vibrators are discussed about the values of V_f and V_i .

$$V_f = -V_{sat}$$

$$V_i = V_{D1}$$

where, V_o = o/p capacitor voltage (V_c)

$$\text{so, } V_c = -V_{sat} + (V_{D1} - (-V_{sat})) e^{-t/RC}$$

$$\text{At, } t = T, V_c = -\beta V_{sat}$$

$$-\beta V_{sat} = -V_{sat} + (V_{D1} + V_{sat}) e^{-T/RC}$$

$$V_{sat}(1-\beta) = (V_{D1} + V_{sat}) e^{-T/RC}$$

$$e^{-T/RC} = \frac{V_{sat}(1-\beta)}{V_{D1} + V_{sat}}$$

Apply log on b.s

$$-T/RC = \ln \left[\frac{V_{sat}(1-\beta)}{V_{D1} + V_{sat}} \right]$$

$$T/RC = \ln \left[\frac{V_{D1} + V_{sat}}{V_{sat}(1-\beta)} \right]$$

$$= \ln \left[\frac{V_{D1} + V_{sat}}{V_{sat}} \times \frac{1}{1-\beta} \right]$$

$$= \ln \left[\frac{1 + \frac{V_{D1}}{V_{sat}}}{1-\beta} \right]$$

$$= RC \ln \left[\frac{1 + V_{D1}/V_{sat}}{1-\beta} \right]$$

$$\text{If } V_D \ll V_{sat} \text{ , } R_1 = R_2 \text{ , } \beta = 0.5$$

$$T = RC \ln \left[\frac{1}{1-0.5} \right]$$

$$= RC \ln(2)$$

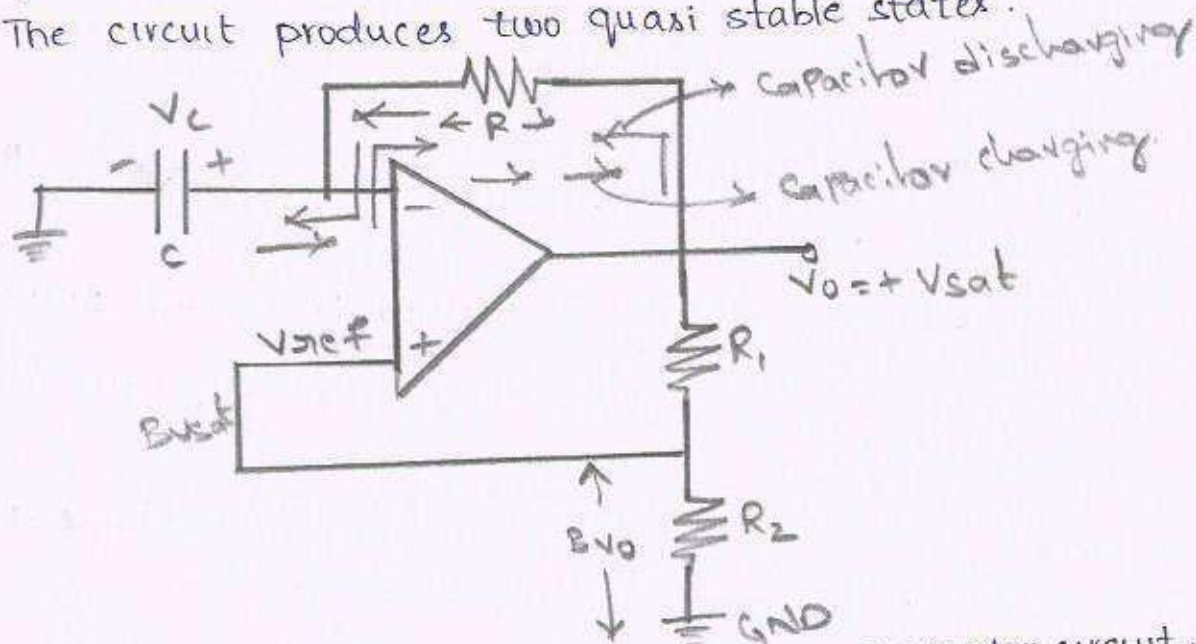
$$T = 0.69 RC$$

(c) Astable Multivibrator :

→ Astable multivibrator has two quasi stable states. So, no need to give the triggering pulse to change the state.

→ It is also called as free running multivibrator. It is used to generate the square waves.

→ The circuit produces two quasi stable states.



→ The above fig. shows the square wave generator circuit.

→ The reference voltage βV_0 is fed back to the non-inverting terminal, where

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$V_0 = +V_{sat} \text{ to } -V_{sat} \text{ (or)}$$

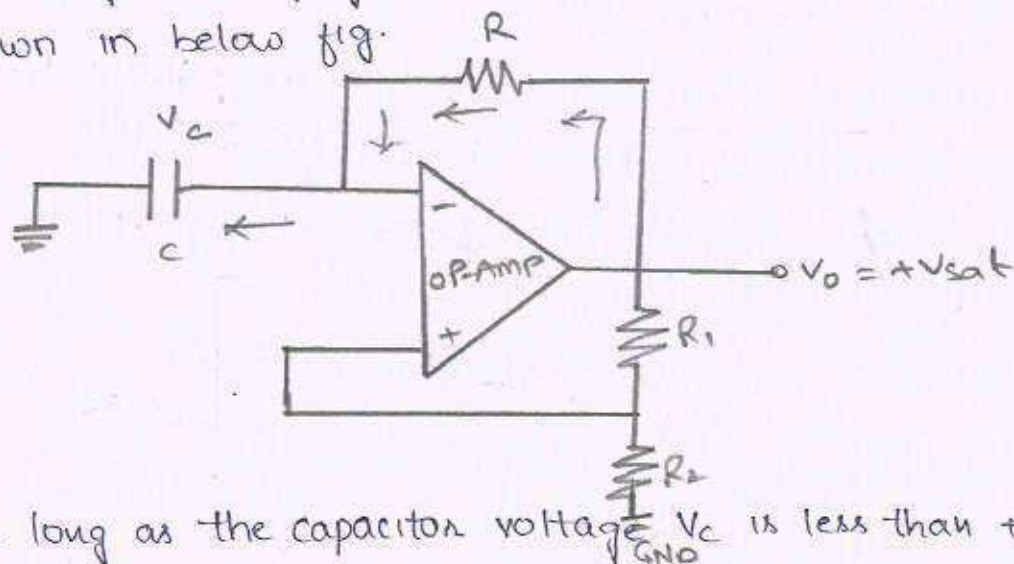
$$-V_{sat} \text{ to } +V_{sat}$$

→ The o/p is also fed back to the inverting terminal through R_c combination (low pass filter).

→ Whenever i_{lp} at the inverting terminal exceeds V_{ref} , changing takes place in the o/p then it produces square wave.

→ In astable multivibrator, both the states are quasi stable state.

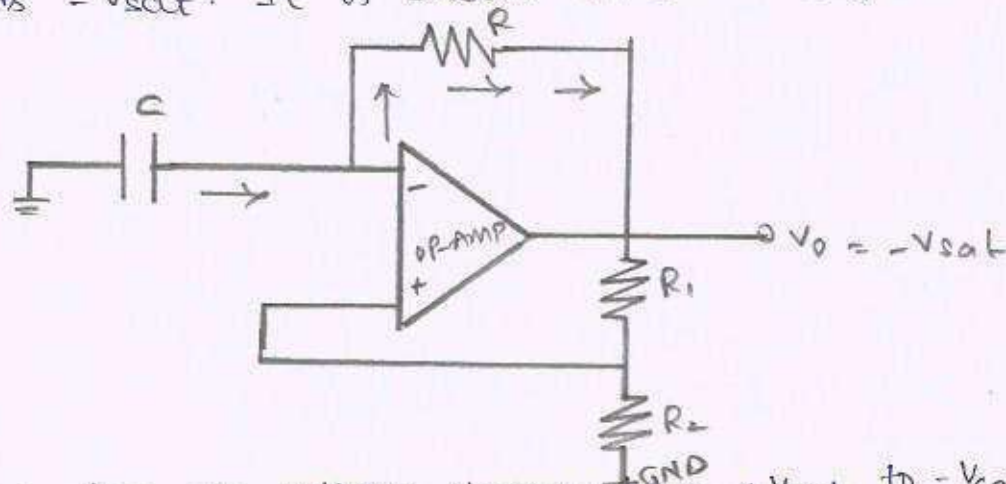
→ To understand the operation let us consider $V_o = +V_{sat}$ now capacitor gets charging towards $+V_{sat}$ through resistance R . This is shown in below fig.



→ As long as the capacitor voltage V_c is less than $+\beta V_{sat}$ the o/p voltage remains at $+V_{sat}$.

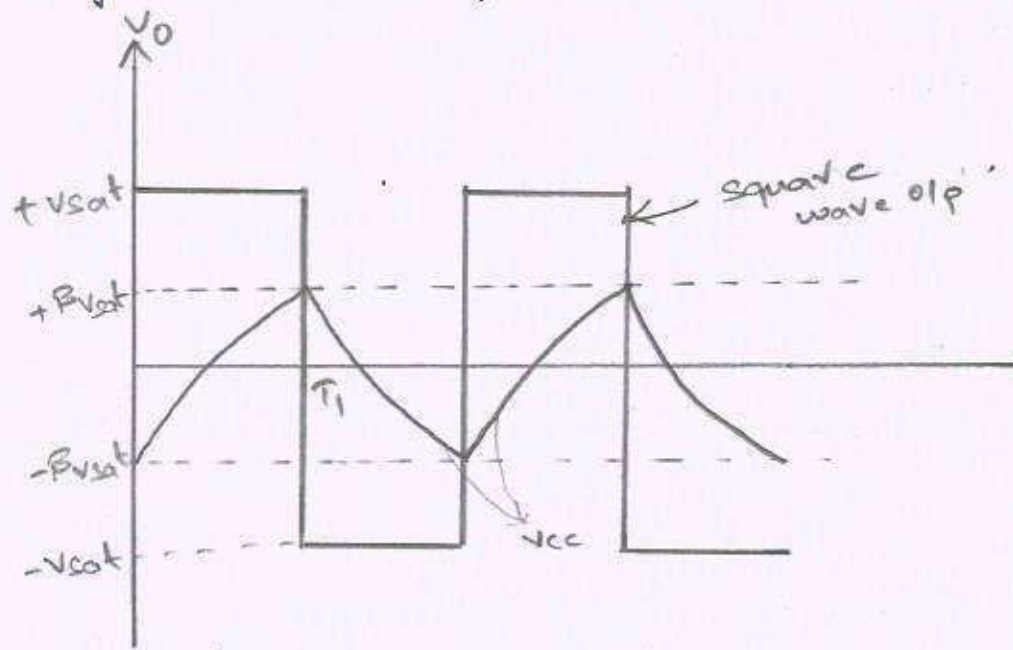
→ As soon as capacitor voltage V_c charged to a value slightly greater than $+\beta V_{sat}$, then the o/p voltage changes from $+V_{sat}$ to $-V_{sat}$.

→ Now the capacitor gets discharging through resistance R towards $-V_{sat}$. It is shown in below fig.



→ When the o/p voltage changes from $+V_{sat}$ to $-V_{sat}$ the capacitor charges more & more negatively until its voltage just exceeds $-\beta V_{sat}$.

→ The o/p changes back to $+V_{sat}$. The cycle repeats itself. Corresponding i/p & o/p waveforms shown in below fig.



Derivation of frequency of Oscillations:

The general expression of Low pass filter is given by

$$V_o = V_f + (V_i - V_f) e^{-t/RC}$$

Where, V_i = initial value of voltage

V_f = final value of voltage

So, $V_i = -\beta V_{sat}$; $V_f = V_{sat}$

Where, V_o = o/p capacitor voltage V_c .

At, $t = T$

$$V_c(t) = \beta V_{sat}$$

$$\beta V_{sat} = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-T/RC}$$

$$\beta V_{sat} = V_{sat} - V_{sat} (1 + \beta) e^{-T/RC}$$

$$V_{sat} (1 + \beta) e^{-T/RC} = V_{sat} - \beta V_{sat}$$

$$V_{sat} (1 + \beta) e^{-T/RC} = V_{sat} (1 - \beta)$$

$$e^{-T/RC} = \frac{V_{sat} (1 - \beta)}{V_{sat} (1 + \beta)}$$

$$= \frac{1-\beta}{1+\beta}$$

Apply log on b.s

$$T/RC = \ln \left[\frac{1-\beta}{1+\beta} \right]$$

$$T = RC \ln \left[\frac{1+\beta}{1-\beta} \right]$$

So $T = 2T$

$$\begin{aligned} T/2 &= RC \ln \left[\frac{1+\beta}{1-\beta} \right] \\ &= RC \ln \left[\frac{1+0.5}{1-0.5} \right] \\ &= RC \ln(3) \end{aligned}$$

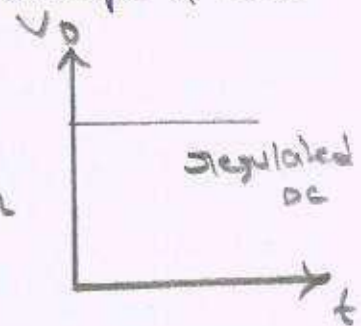
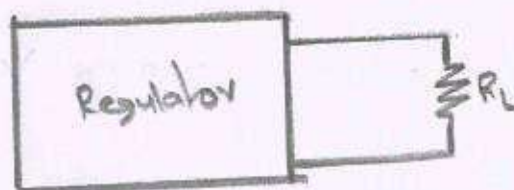
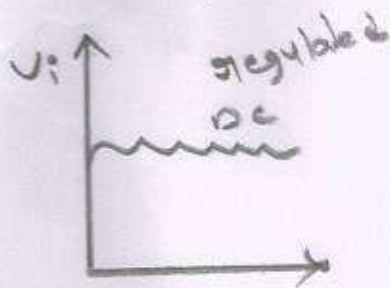
$$T = 2RC$$

$$\therefore f = 1/T$$

$$f = \frac{1}{2RC}$$

Voltage Regulators :

→ Voltage regulator is an electronic circuit that gives constant o/p dc voltage irrespective of variation in i/p voltage & load.



These are of 3 types :-

1. Series voltage regulator
2. Switching voltage regulator
3. Shunt voltage regulator

Series Voltage Regulator :

1. In series regulator, we use power transistor (control element) connected in series in b/w i/p & load.
2. The o/p voltage is controlled by the continuous voltage drop

taking place across the series pass transistor.

3. Since the transistor conducts in the active (or) linear region so these regulators are also called as linear regulators.

4. Series regulators (or) linear regulators may have fixed & variable voltage regulators & it should be +ve (or) -ve voltages.

Fixed Voltage Regulators:

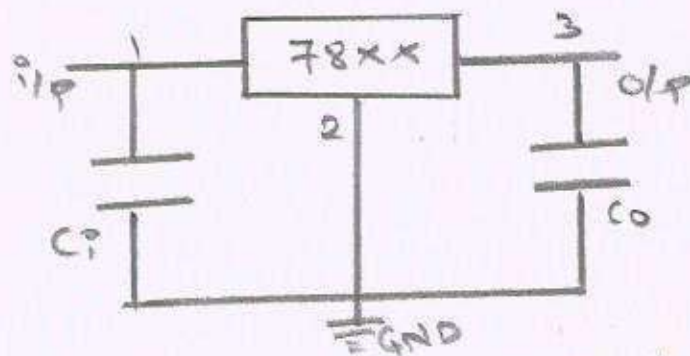
1. It provides a fixed constant o/p voltage as designed by the manufacturer. These are classified as 2 types.

(a) +ve fixed voltage regulator

(b) -ve fixed voltage regulator

(a) +ve fixed voltage regulator:

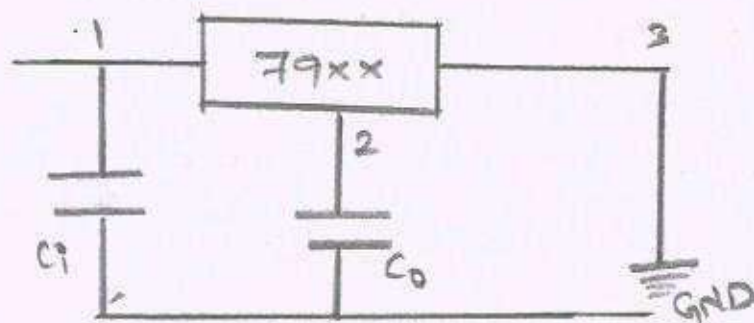
1. 78xx series regulators are +ve voltage regulators. It has 3 terminals. 1st terminal acts as i/p & 2nd as grounded & 3rd as o/p terminal.
2. The last 2 digits of 78xx series indicates the o/p voltage of regulator. For eg: 7805
3. It indicates +ve 5 volts produced by the circuit.
4. The 78xx has different o/p voltage options they are 5v, 7v, 9v, 12v, 15v, 18v, 24v.
5. The standard representation of 78xx series is shown in below fig.



6. Here pin 1 is the i/p pin, pin 2 is grounded, pin 3 is the o/p.
7. The i/p capacitor C_i is used to remove the fluctuation in given i/p signal & o/p capacitor C_o is used to improve transient response.

(b) -ve fixed voltage regulator:

1. 79xx series is a -ve voltage regulators. It is a 3 terminal device. 1st pin acts as i/p, 2nd pin acts as o/p, 3rd pin acts as grounded terminal.
2. The last 2 digits of 79xx series indicates the -ve o/p voltage of regulator. for eg: 7905
it indicates -ve 5 volts produced by circuit.
3. 79xx has different o/p voltage options. They are -5V, -9V, -12V, -15V, -18V, -24V.
4. The standard representation of 79 series is shown below.



Variable Voltage Regulator:

1. It is a kind of regulator whose regulated o/p voltage can be varied over the range.
2. It has 2 types. (a) +ve variable regulator
(b) -ve variable regulator.

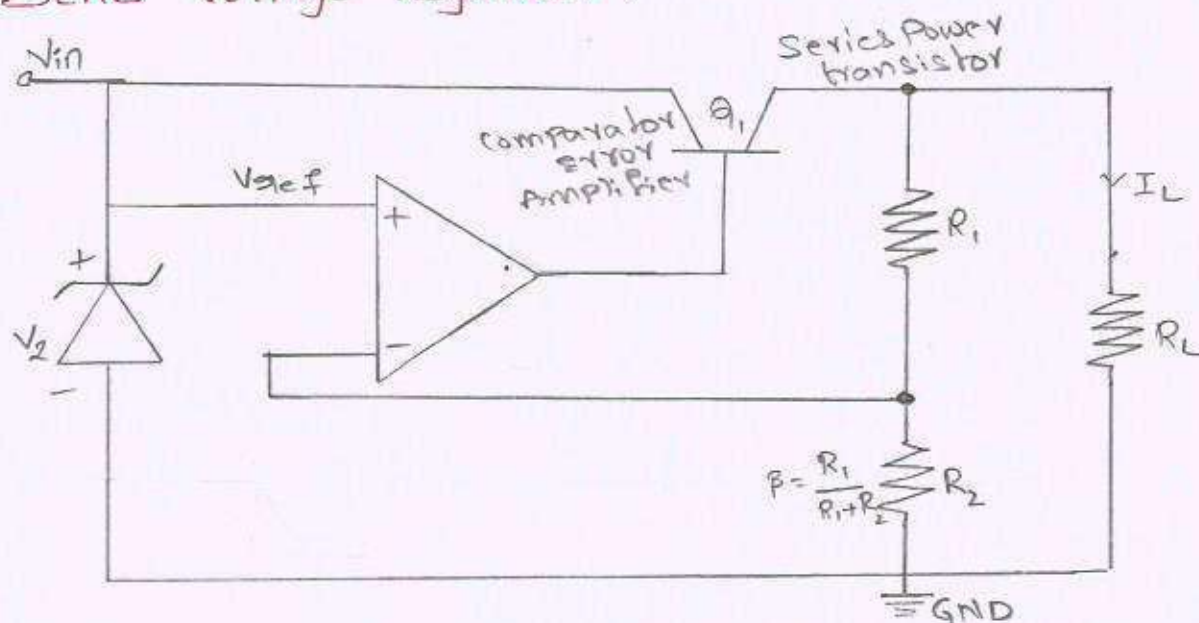
(a) +ve variable regulator:

LM317 is a +ve adjustable voltage regulator whose o/p voltage can be varied over a range of 1.2V to 57V.

(b) -ve variable regulator:

LM337 is a -ve adjustable regulator whose o/p voltage can be varied over a range of -1.2V to -57V.

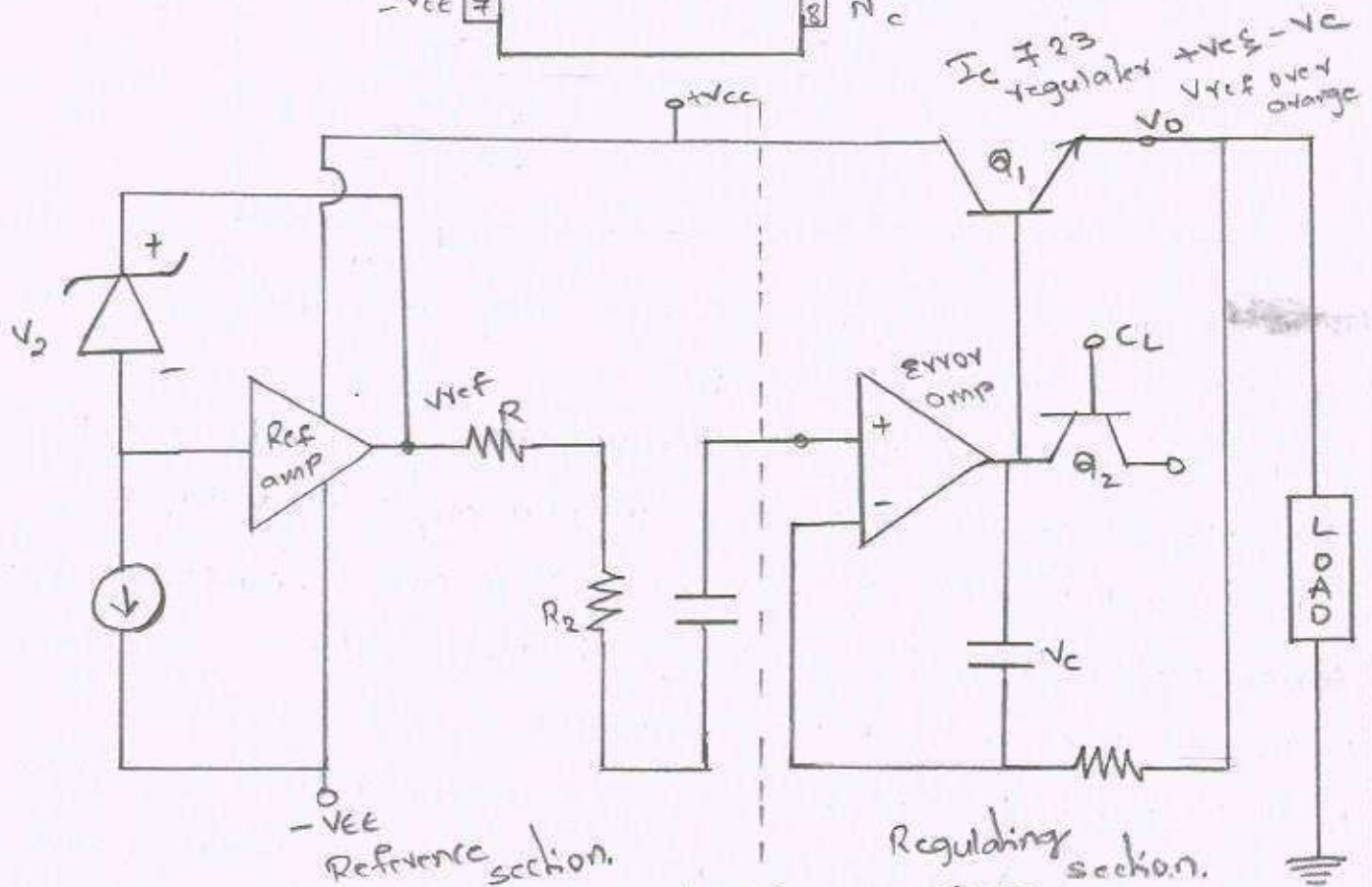
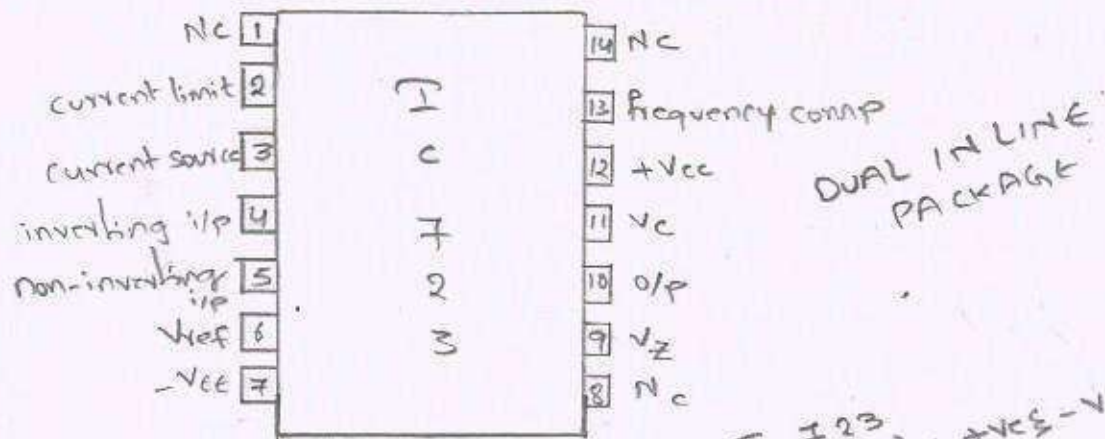
Series Voltage Regulator:



1. Regulator is a circuit in which o/p voltage is constant irrespective of changes in load & i/p voltage.
2. The above circuit shows series voltage regulator because power transistor is connected in series in b/w o/p & i/p voltages.
3. The circuit consists of reference voltage circuit, comparator, series power transistor & voltage divider circuit.
4. The op-amp is used as comparator.
5. It compares the part of o/p voltage obtained from the potential divider circuit as a f/b [sampled voltage] with the reference voltage generated by Zener diode.
6. The o/p of op-amp drives the transistor Q_1 .
7. If there is any changes in o/p voltage, the control signal from op-amp controls the conduction of transistor Q_1 .
8. Thus, the o/p voltage is maintained at constant level.

General Purpose Regulator [IC 723]:

1. General purpose regulator are used to obtain both +ve & -ve voltage over a wide range.
2. IC 723 is a general purpose regulator.



3. It is available in 14 pin dual line package.
4. Its o/p current is only in milliamps & can increased upto 5 amps.
5. IC 723 has 2 functional blocks. (a) Reference Section
(b) Regulating Section.

(a) Reference Section :

1. It produces reference voltage of $\approx 7V$ by the Zener diode.
2. It consists of Zener diode, current source & reference amplifier.
3. This Section provides a reference voltage to the regulating section.

(b) Regulating Section :

1. It consists of error amplifier, transistor Q_1 & current limiting transistor Q_2 .
2. The error amplifier (or) comparator compares the reference voltage from reference section at non-inverting terminal with a part of o/p voltage at inverting terminal.
3. Based on the compared o/p voltage drives the transistor Q_1 .
4. If any changes in o/p voltage, the control signal from op-amp controls the conduction of transistor Q_1 .

Features :

1. input voltage 40V maximum.
2. output voltage adjustable from 2V to 37V
3. 150mA o/p current without external pass transistor.
4. o/p currents in excess of 10amps possible by adding external transistor.
5. It can be used as either a linear (or) switching (or) shunt regulator.
6. o/p & i/p short circuit protection is provided.
7. Low temperatures & high ripple regulators.
8. Low stand by current drain.
9. Small size.
10. Lower cost.

UNIT-II

TIMERS, PHASE LOCKED LOOP & D-A & A-D CONVERTORS

Introduction:

555 Timer:

- 555 timer is a timing circuit that can produce accurate & high stable time delays (or) oscillations.
- 555 timer is available in 8 pin DIP & 14 pin DIP packages.
- It can be used with supply voltages range in b/w +5V to +18V.
- The below fig. shows the pin diagram of 8 pin DIP package.

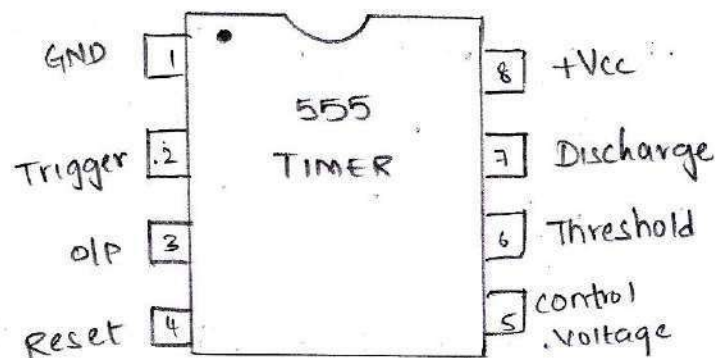


Fig: 555 Timer

Features:

1. It can be used with supply voltages over a range in b/w +5V to +18V.
2. It is easy to use.
3. It can drive the load upto 200 mA.
4. It is compatible with TTL (Transistor transistor logic) & CMOS (complementary ^{metal oxide} semiconductor).
5. It is used in various applications such as square wave generator, ramp & pulse wave generator, astable & monostable multivibrators.

Functional Diagram:

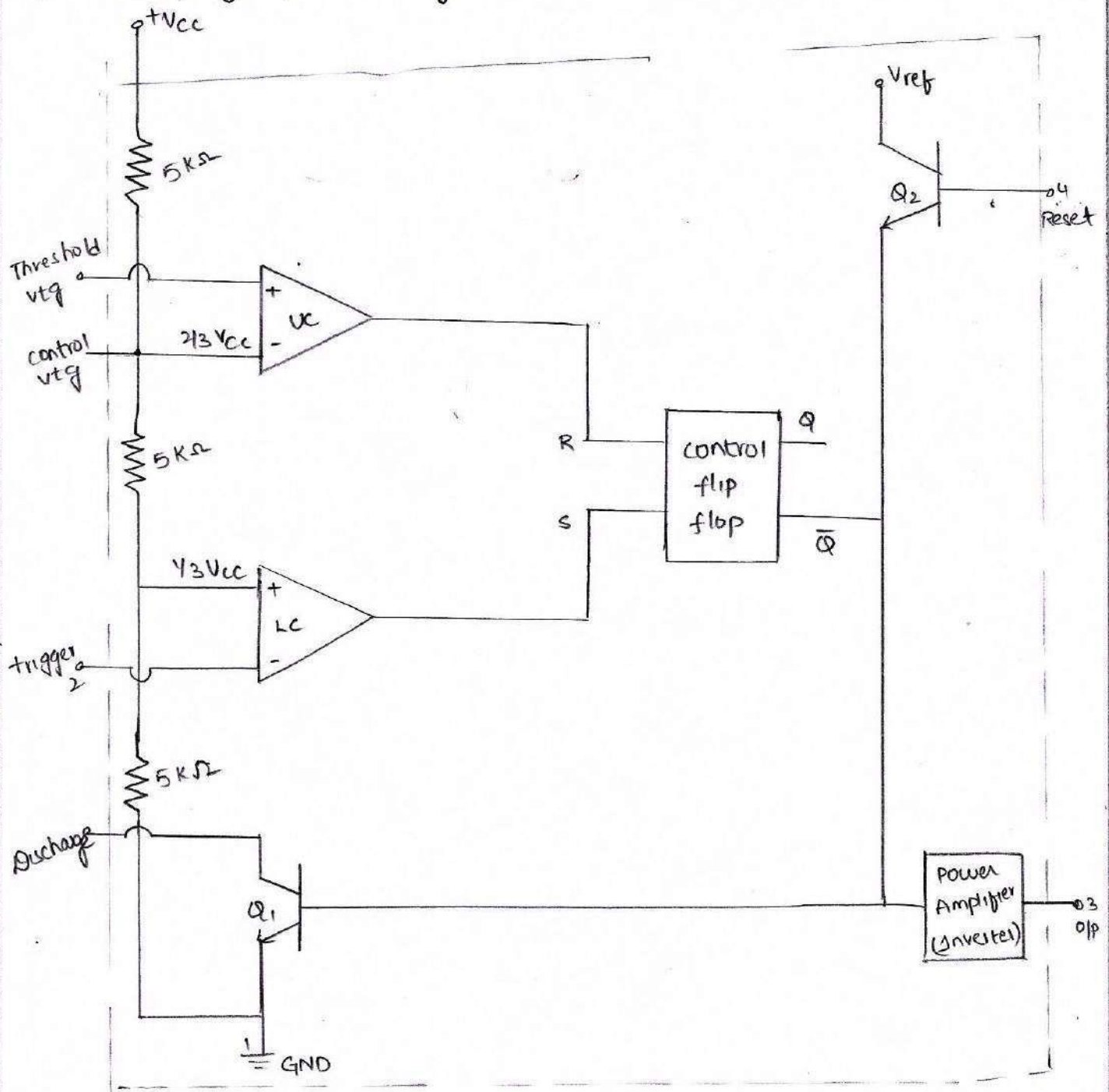
- It consists of 2 comparators namely upper comparator & lower comparator that can drive set (S) & reset (R) terminals of a flip flop.

- These flipflops can control the ON & OFF cycles of the discharge transistor Q_1 .
- It has $3.5k\Omega$ resistors which acts as potential divider, providing biasing voltages of $\frac{2}{3}V_{CC}$ to the upper comparator & $\frac{1}{3}V_{CC}$ to the lower comparator where V_{CC} = supply voltage.
- These voltages are called as reference voltages. These are required to control the timing.
- The timing can be controlled by externally applying voltage to the control voltage terminal.
- If no such control voltage is required then the control voltage terminal can be bypassed by a capacitor to ground.
- Typically the capacitor value is chosen of about $0.1\mu F$.

Operation:

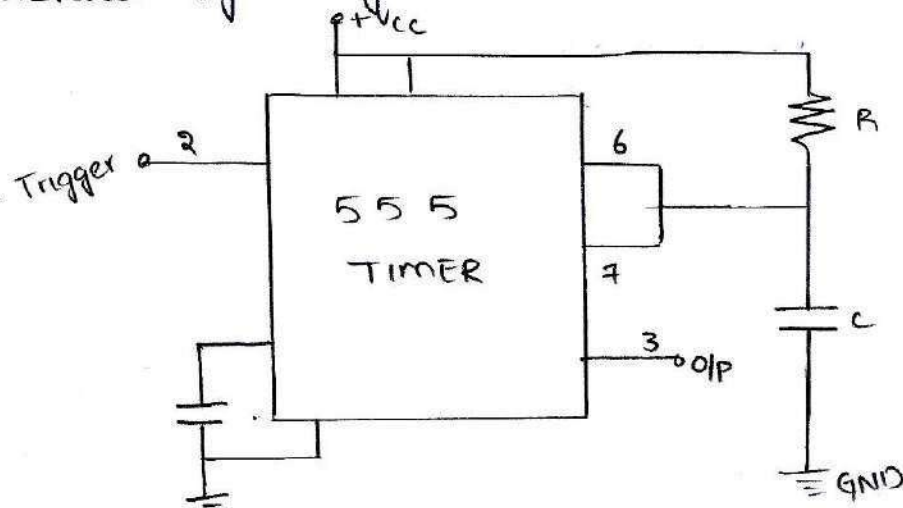
- In the stand by state (stable state), the o/p $\bar{Q}$ of the control flipflop is high ($\bar{Q}=1$; $Q=0$). This makes o/p low because of power amplifier can be acts as a inverter.
- A -ve triggering pulse passes through $\frac{V_{CC}}{3}$, the o/p of the lower comparator goes high & sets the flipflop ($Q=1$; $\bar{Q}=0$)
- When the threshold voltage at pin 6 passes through $\frac{2}{3}V_{CC}$ the o/p of upper comparator goes high & resets the flipflop ($Q=0$; $\bar{Q}=1$)
- A separate reset terminal is produced to reset the flipflop externally.
- Normally the reset terminal is not used, if we need it should be connected to +ve supply voltage V_{CC} .
- The transistor Q_2 acts as buffer to isolate the reset i/p from the flipflop & the transistor Q_1 .

- The transistor Q_2 is driven by an internal ~~reference~~ reference voltage V_{ref} obtained from supply voltage V_{CC} .
- If $\bar{Q}$ is high, the transistor Q_1 is ON due to this it become s/c in blw discharge pin to ground. Similarly $\bar{Q}$ is low, the transistor Q_1 is OFF & it becomes open circuit in blw discharge pin to ground.

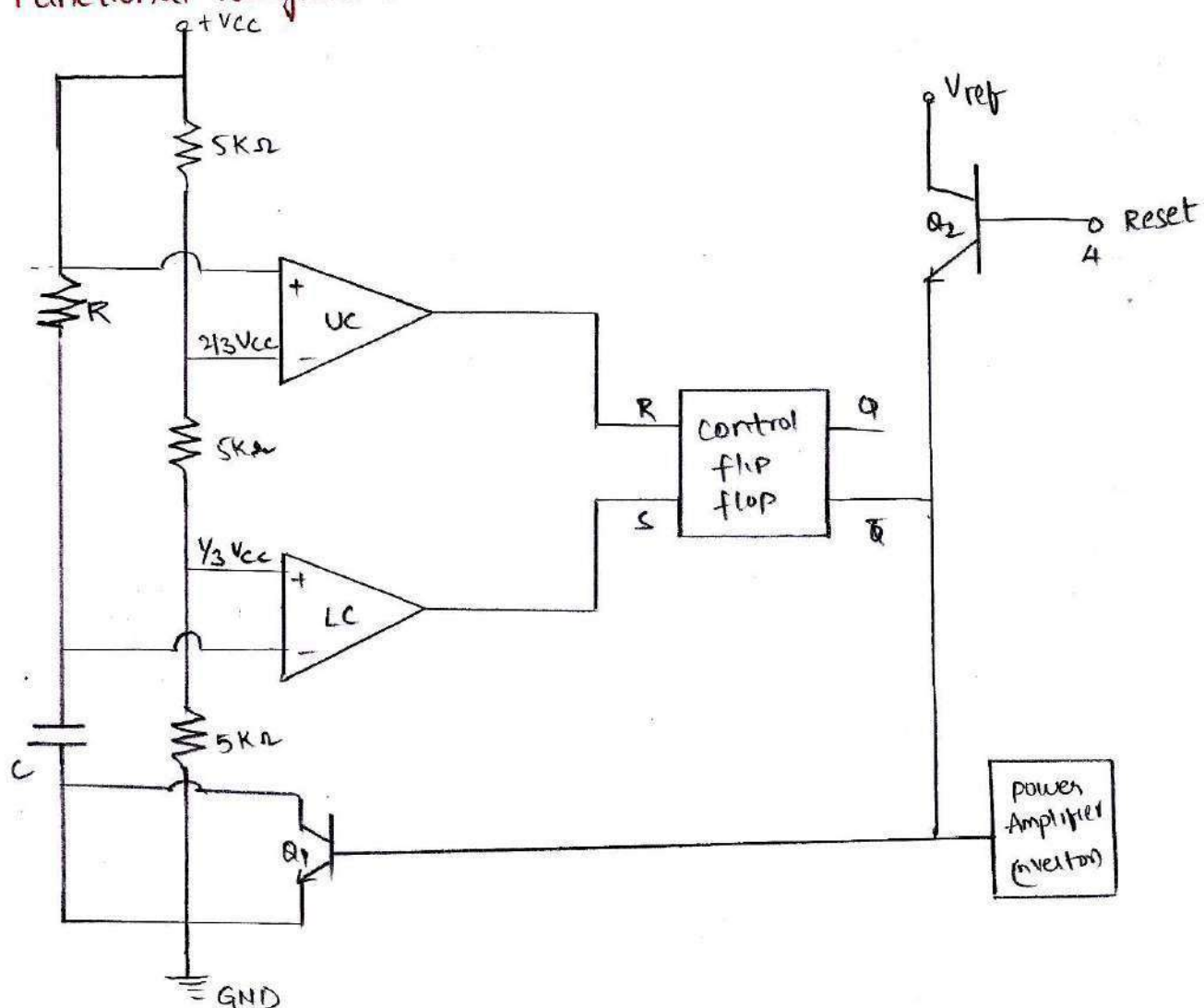


Monostable Multivibrator :-

Monostable multivibrator is a circuit which generates the non-sinusoidal signals. It has one stable state and one quasi stable state. The below fig. shows the monostable multivibrator by using 555 timer.

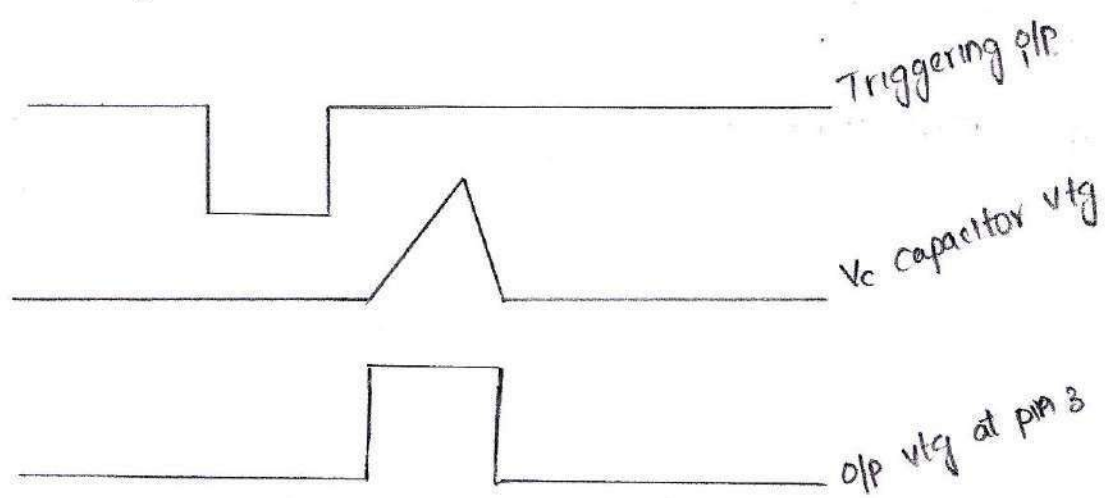


Functional Diagram :-



The above fig. shows the functional block diagram of monostable multivibrator.

1. In the stand by state [stable state] $Q = 0$, $\bar{Q} = 1$. So o/p is low. Under this condition transistor is ON i.e., it becomes short circuit through capacitor, 'C' to the ground.
2. Now the triggering passes through $V_{cc}/3$ at 2nd pin, due to this lower comparator o/p is high. So $Q = 1$, $\bar{Q} = 0$. This makes transistor Q_1 OFF & it becomes a open circuit across the capacitor. So o/p is high.
3. Now, the capacitor takes charging by V_{cc} .
4. After a time period T , the capacitor voltage is just greater than $2/3 V_{cc}$ and upper comparator o/p is high. So $Q = 0$, $\bar{Q} = 1$.
5. Under this condition, o/p is low & transistor Q_1 goes on there by discharging capacitor 'C' rapidly to ground.
6. The corresponding o/p waveforms of monostable multivibrator is shown in fig.



Analysis of Time Constant :

The capacitor voltage across the capacitor is given by

$$V_c = V_{cc} (1 - e^{-t/RC}) \rightarrow (1)$$

At $t = T$, the capacitor charges by $V_c = 2/3 V_{cc} \rightarrow (2)$

sub. eq(2) in eq(1)

$$2/3 V_{cc} = V_{cc} - V_{cc} e^{-t/RC}$$

$$2/3 V_{cc} + V_{cc} e^{-T/RC} = V_{cc}$$

$$e^{-T/RC} = \frac{V_{cc} - 2/3 V_{cc}}{V_{cc}}$$

Apply log on b.s

$$\ln[a/b] = -\ln[b/a]$$

$$\ln[e^{-T/RC}] = \ln\left[\frac{V_{cc} - 2/3 V_{cc}}{V_{cc}}\right]$$

$$-\frac{T}{RC} = \ln\left[\frac{V_{cc}}{V_{cc} - 2/3 V_{cc}}\right]$$

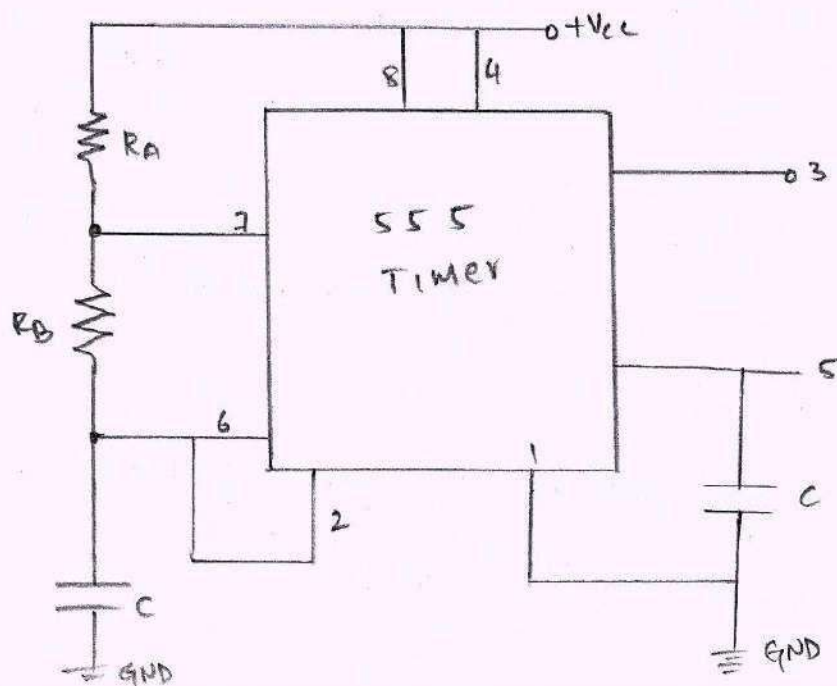
$$T = \ln RC(3)$$

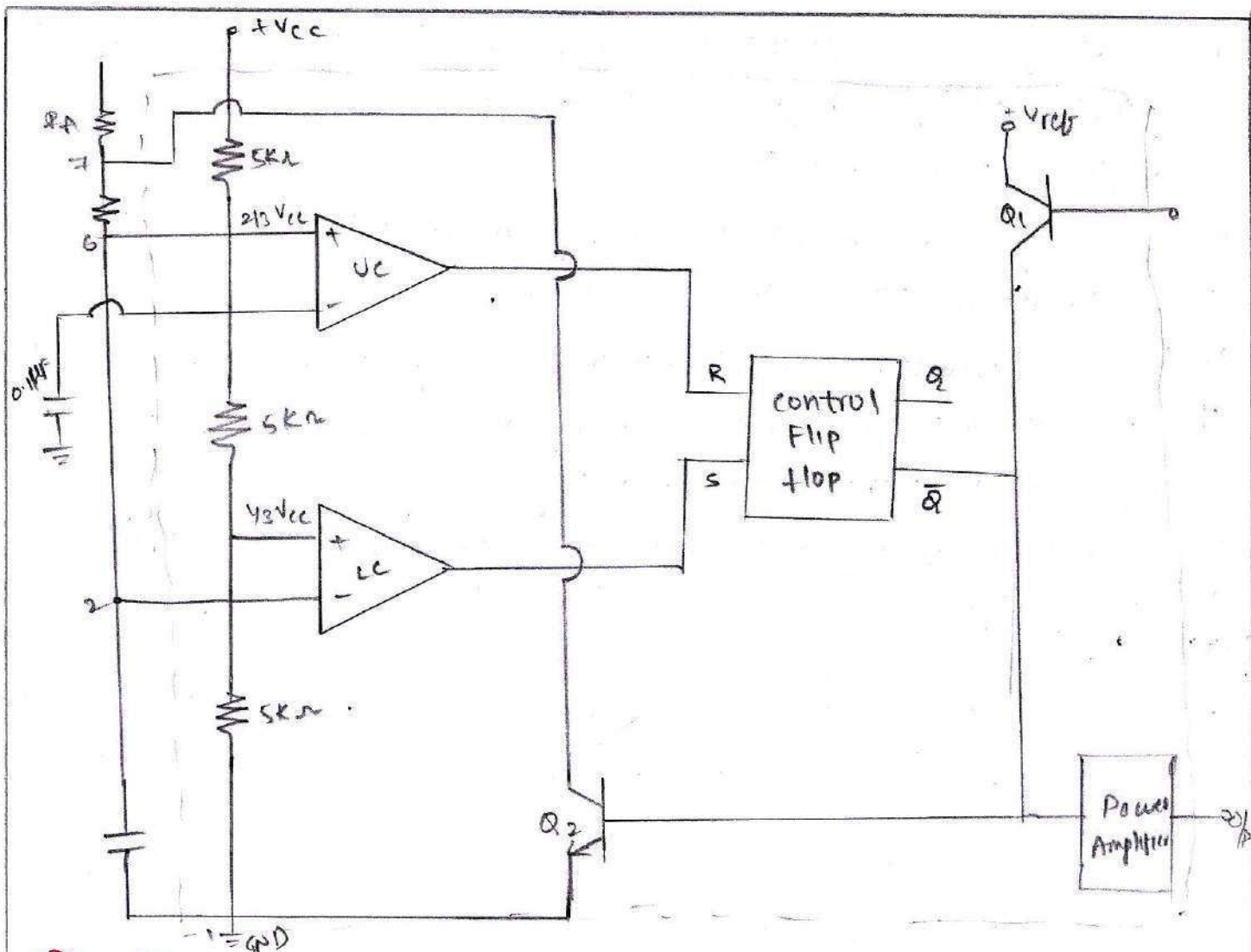
$$\therefore T = 1.1 RC$$

Applications :

1. Pulse width generator
2. Water level control.

Asstable Multivibrator :

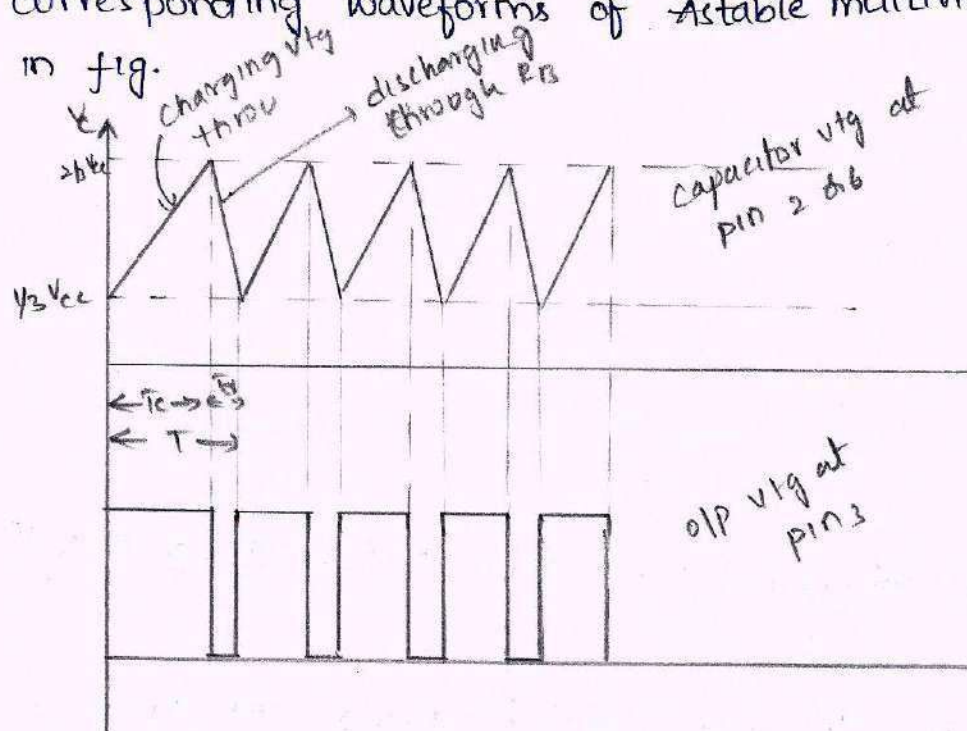




Operation :

1. Astable multivibrator has no stable states. It has 2 quasi stable states.
2. The astable multivibrator circuit by using 555 timer is shown in above fig.
3. Comparing with monostable multivibrator, the timing resistor is now split into 2 sections i.e., R_A & R_B .
4. The discharging transistor Q_1 is connected in b/w R_A & R_B .
5. When supply voltage is connected, the external capacitor gets charging through R_A & R_B resistors.
6. When the charging voltage reaches the $\frac{1}{3} V_{cc}$ voltage then lower comparator goes high. Due to this $R=0$; $S=1$; $\bar{Q}=0$; $Q=1$ and therefore o/p is high.

7. Similarly when charging voltage reaches $\frac{2}{3} V_{CC}$ then upper comparator o/p goes high. Due to this $R=1$; $S=0$; $\bar{Q}=1$; $Q=0$ and the o/p becomes low.
8. When $\bar{Q}=1$, the discharging transistor Q_2 is ON & it makes short circuited across the capacitor.
9. So the capacitor gets discharging through R_B resistor towards the ground. The capacitor discharging voltage reaches $\frac{1}{3} V_{CC}$ & again lower comparator o/p goes high.
10. The corresponding waveforms of Astable multivibrator is shown in fig.



Analysis of time constant :-

$$V_C = V_{CC}(1 - e^{-t/RC}) \rightarrow (1)$$

at $t = t_1$, $V_C = \frac{1}{3} V_{CC}$

$$\frac{1}{3} V_{CC} = V_{CC} - V_{CC} e^{-t_1/RC}$$

$$V_{CC} e^{-t_1/RC} = V_{CC} - \frac{1}{3} V_{CC}$$

$$e^{-t_1/RC} = \frac{V_{CC} - \frac{1}{3} V_{CC}}{V_{CC}}$$

Taking log on b/s

$$-\frac{t_1}{RC} = \ln \left[\frac{V_{CC} - \frac{1}{3}V_{CC}}{V_{CC}} \right]$$

$$-\frac{t_1}{RC} = -\ln \left[\frac{V_{CC}}{V_{CC} - \frac{1}{3}V_{CC}} \right]$$

$$t_1 = RC \ln \left[\frac{1}{1 - \frac{1}{3}} \right]$$

$$t_1 = RC \ln(1.5)$$

$$\therefore t_1 = 0.405 RC$$

→ When the capacitor charges from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$.

at $t = t_2$; $V_{CC} = \frac{2}{3}V_{CC}$

$$\frac{2}{3}V_{CC} = V_{CC} - V_{CC} e^{-t_2/RC}$$

$$V_{CC} e^{-t_2/RC} = V_{CC} - \frac{2}{3}V_{CC}$$

$$e^{-t_2/RC} = \frac{V_{CC} - \frac{2}{3}V_{CC}}{V_{CC}}$$

Taking log on b/s

$$-t_2/RC = \ln \left[\frac{V_{CC} - \frac{2}{3}V_{CC}}{V_{CC}} \right]$$

$$t_2 = \ln RC \left[\frac{V_{CC}}{V_{CC} - \frac{2}{3}V_{CC}} \right]$$

$$t_2 = RC \ln(3)$$

$$\therefore t_2 = 1.1 RC$$

$$T_C = t_2 - t_1$$

$$= 1.1 - 0.405$$

$$= 0.695 RC$$

$$\therefore T_C = 0.695 (R_A + R_B) C$$

→ The capacitor takes discharging from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$

$$\frac{1}{3}V_{CC} = \frac{2}{3}V_{CC} e^{-t/RC}$$

$$e^{-t/RC} = \frac{\frac{1}{3}V_{CC}}{\frac{2}{3}V_{CC}}$$

$$e^{-t/RC} = \frac{1}{2}$$

$$e^{-t/RC} = \ln\left(\frac{1}{2}\right)$$

$$t/RC = \ln(2)$$

$$t = RC \ln(2)$$

$$\therefore T_d = 0.69 R_B C$$

→ Total time constant $T = T_C + T_D$

$$= 0.69(R_A + R_B)C + 0.69 R_B C$$

$$= 0.69 R_A C + 0.69 R_B C + 0.69 R_B C$$

$$\therefore T = 0.69 (R_A + 2R_B)C$$

$$f = \frac{1}{T}$$

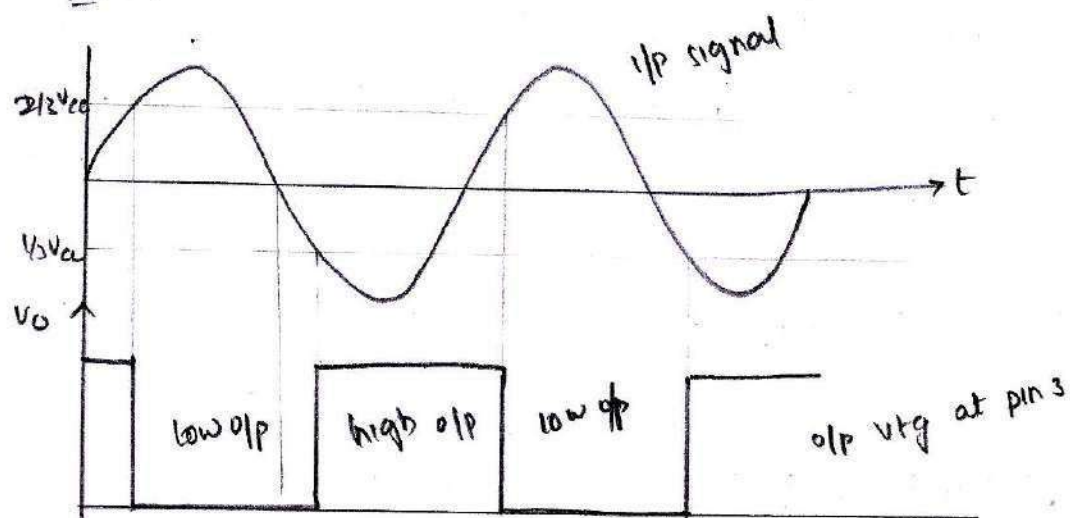
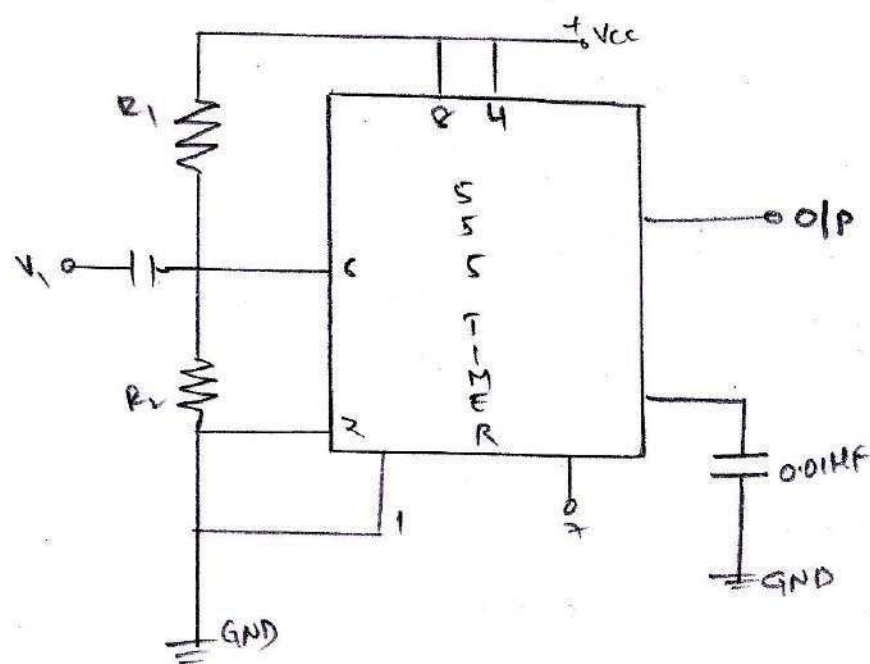
$$= \frac{1}{0.69 (R_A + 2R_B)C}$$

$$\therefore f = \frac{1.449}{(R_A + 2R_B)C}$$

Applications :-

1. Frequency shift key (FSK)
2. Pulse position modulator

Schmitt Trigger :-



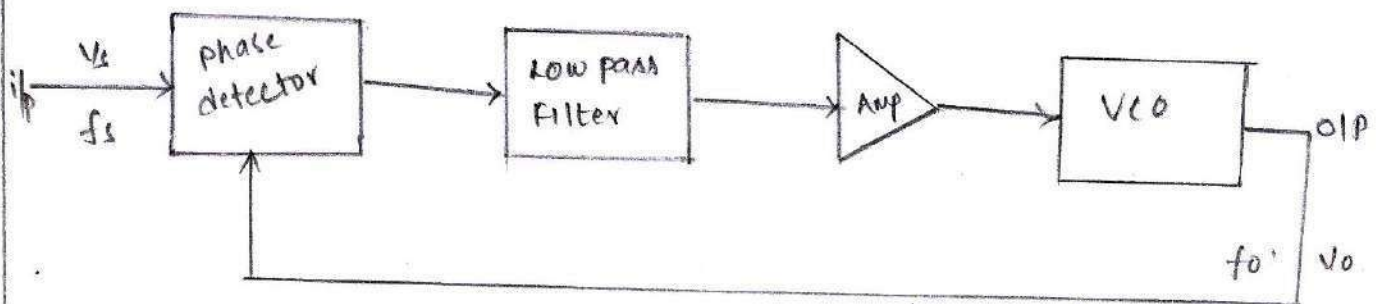
- Here 2 internal comparators are connected together and externally biased through R_1 & R_2 resistors.
- Since upper comparator will be ON (or) o/p is high when the given ip signal reaches the $\frac{2}{3}V_{CC}$.
- Similarly lower comparator o/p is high when the given ip signal reaches the $\frac{1}{3}V_{CC}$.
- Due to this the o/p of the circuit is changing from one state to another state. i.e., When V_C is high, o/p is low. When V_C is high, o/p is high ($R=0$; $S=1$; $\phi=1$; $\bar{\phi}=0$).

Phase Locked Loop :-

Introduction :

1. PLL is a phase locked loop. It is a closed loop circuit & its o/p frequency & o/p phase (ϕ) to be locked.
2. The PLL is an important building block of linear systems.
3. The PLL was used in 1930. At the time PLL has many features. so PLL circuits was very costly.
4. However, after the development of integrated technology, the cost of PLL has reduced.
5. Hence we observed that PLL has become one of the fundamental building block in electronic technology.
6. The PLL principle is used in FM demodulation, FSK demodulation, motor speed control, frequency multiplication & division etc.
7. The PLL is available in single package. The example of PLL is 565 IC.

Block Diagram of PLL :



It consists of 4 blocks ; 1. phase detector / comparator

2. Low pass filter

3. Amplifier

4. VCO (voltage controlled oscillator)

1. Phase Detector/comparator :

1. When i/p signal V_s at frequency f_s is applied to the phase detector & it compares the phase or frequency of incoming signal to that of the o/p of VCO.

2. The phase detector compares the 2 i/p signals & produce an voltage.

3. Phase detector basically acts as an multiplier, so it produces the sum $(f_s + f_o)$ & difference $(f_s - f_o)$ components at its o/p.

2. Low pass Filter :

The low pass filter used to remove high frequency signals i.e., coming from phase detector. It passes only low frequency signals i.e., the difference of two i/p signal $(f_s - f_o)$.

3. Amplifier :

The amplifier is used to amplifies the difference of frequency signal & the amplified signal is given to the voltage controlled oscillator.

4. Voltage Controlled Oscillator :

1. VCO is a frequency running multivibrator and operates at a set frequency f_o called free running frequency.

2. This frequency is determined by an external timing capacitor and an external resistor.

3. It can be shifted to either side by applying a dc control voltage V_c .

4. The frequency derivation is directly proportional to the dc ~~current~~ control voltage and it is called VCO.

5. The vco frequency f_o is compared with the i/p frequency f_i by the phase detector and it is adjusted continuously until it is equal to the i/p frequency f_s .

$$f_o = f_s$$

6. The signal V_c shifts the vco frequency in a direction to reduce the frequency difference b/w f_s and f_o .

7. Once this action starts, we say that the signal is in the capture range.

8. The circuit is then said to be locked. Once locked, the o/p frequency f_o of vco is identical (same) to f_s except for a finite phase ϕ . Thus, a PLL goes through 3 stages.

1. Free Running state :

In this state, there is no control on vco o/p frequency f_o .

2. Lock Range :

In this state when f_o is exactly equal to f_i , the PLL is said to be phase locked. Once locked $f_o = f_i$ except for a finite ϕ .

3. Capture Range :

In this state, the comparison of f_o and f_i begins. The control voltage V_c starts adjusting f_o to bring it closer to f_i . The LPF controls the capture range.

Basic DAC Techniques :

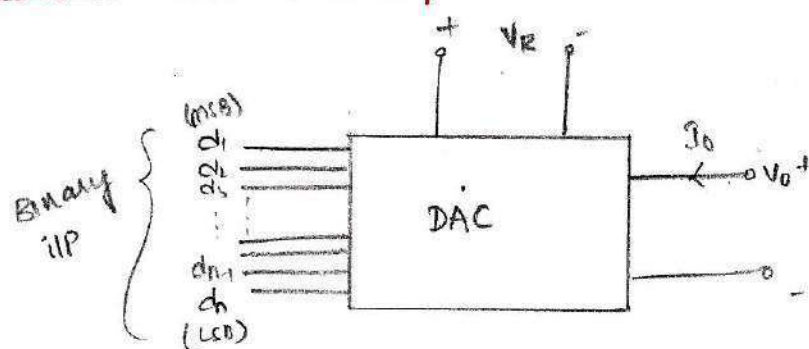


fig. Schematic of DAC

1. The i/p is an n -bit binary word D and is combined with a reference voltage V_R to give an analog o/p signal.
2. The o/p of a DAC can be either of a voltage or Current.
3. For a voltage o/p DAC, the D/A converter is mathematically described as

$$V_0 = K V_{FS} (d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n)$$

where, V_0 = o/p voltage

V_{FS} = full scale o/p voltage

K = scaling factor = unity

$d_1 \dots d_n$ = n bit binary fractional word with the decimal point located at the left

d_1 = MSB bit

d_n = LSB bit

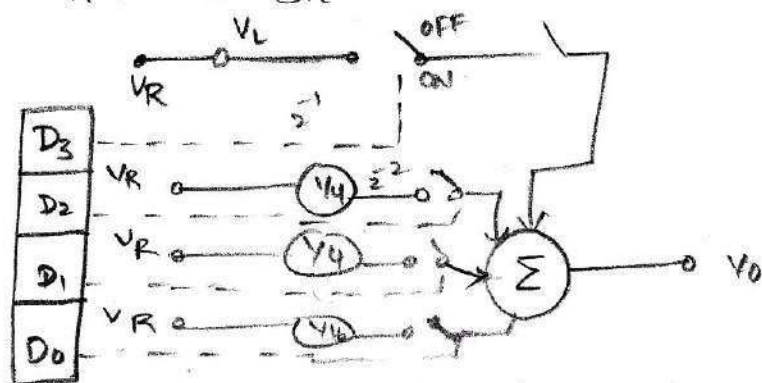


fig. Digital to Analog Conversion

→ Fig. shows explanation of DAC. Here V_R is fixed reference voltage.

→ The digital signal is contained in the register ~~on the~~ on the left.

→ Each flipflop in the register controls an analog switch as shown in the dotted lines.

$$V_0 = [D_3 2^{-1} + D_2 2^{-2} + D_1 2^{-3} + D_0 2^{-4}] V_R$$

If $D_3 D_2 D_1 D_0 = 1001$

$$V_0 = 1 \times \left[\frac{V_R}{2} + 0 \frac{V_R}{4} + 0 \frac{V_R}{8} + \frac{1 V_R}{16} \right]$$

$$V_0 = \frac{9V_R}{16}$$

→ There are 2 types of DAC converters

1. Weighted - resistor DAC converter
2. R-2R ladder DAC converter.

1. **Weighted - Resistor DAC converter :**

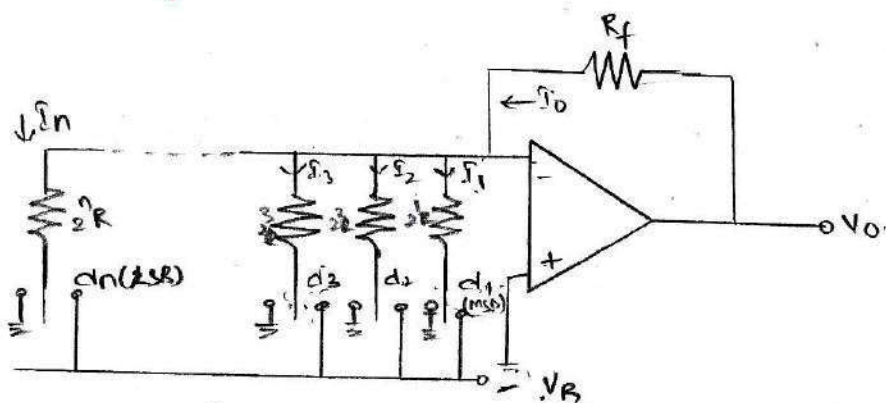


Fig = A simple weighted Resistor DAC

→ One of the simplest ckt uses a summing amplifier with a binary weighted resistor N/w. It has n-electronic switches $d_1, d_2, \dots, d_n$ controlled by binary ip word.

→ These switches are SPDT (single pole double throw) type switch.

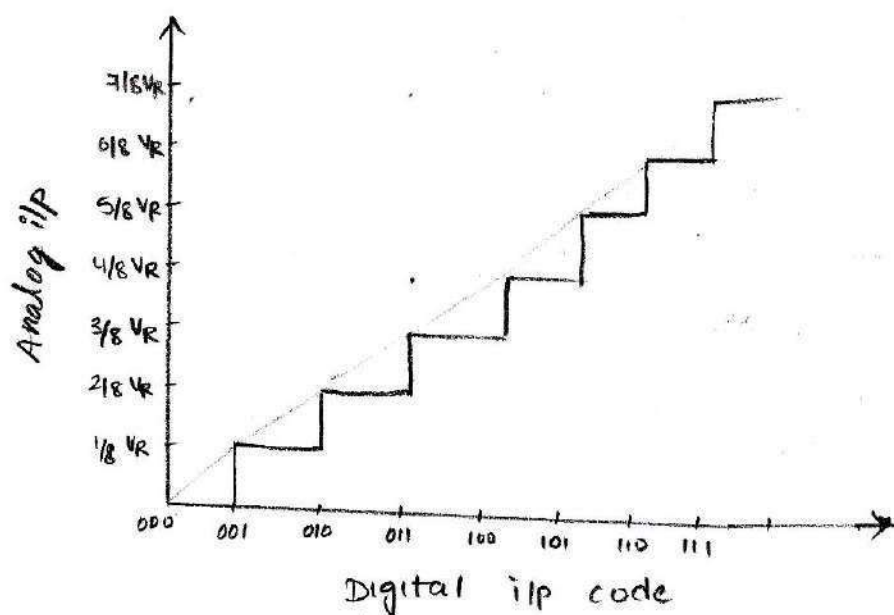


fig: Transfer char'n of a 3bit DAC

eg. If the binary i/p to a particular switch is 1. It connects the resistance to the reference voltage ($-V_R$).

→ The binary weighted resistor DAC uses an op-amp to sum of 'n' binary weighted currents derived from a reference voltage V_R via current scaling resistors $2R, 4R, 8R \dots 2^n R$ as shown in the fig.

Working:

In fig. switch positions are controlled by the digital i/p's. When digital i/p logic 1. it connects the corresponding resistance to the reference voltage V_R otherwise it leaves resistor open.

$$\therefore \text{for ON switch } I = \frac{-V_R}{R}$$

$$\text{for OFF Switch } I = 0$$

Here op-amp is used as a summing amplifier. Due to high i/p impedance of op-amp, summing current will flow through R_f . Hence the total current through R_f can be given as.

$$I_0 = I_1 + I_2 + I_3 + \dots + I_n$$

The o/p voltage is the voltage across R_f and it is given as

$$\text{so } V_0 = -I_0 R_f$$

$$V_0 = -[I_1 + I_2 + I_3 + \dots + I_n] R_f$$

$$V_0 = \left[D_1 \frac{V_R}{2R} + D_2 \frac{V_R}{4R} + D_3 \frac{V_R}{8R} + \dots + D_n \frac{V_R}{2^n R} \right] V_f$$

$$= \frac{V_R}{R} R_f \left[D_1 2^{-1} + D_2 2^{-2} + \dots + D_n 2^{-n} \right]$$

When $R_f = R$

$$V_0 = V_R \left[D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} + \dots + D_n 2^{-n} \right]$$

→ The above eqn indicates that the analog o/p voltage is proportional to the i/p digital word.

Drawbacks :

1. Wide range of resistor values are required.

For 8 bit DAC, the resistor required are $2^1 R$, $2^2 R$, $2^3 R$, ... and $2^8 R$. Therefore, the largest resistor is 128 times the smallest one.

This wide range of resistor values has restriction on both higher & lower ends.

The finite resistance of the switches disturbs the binary weighted relationship among the various currents, particularly in the MSB positions, where the current setting resistances are smaller.

R-2R Ladder DAC :

→ In this type, reference voltage is applied to one of the switch positions and other switch position is connected to ground. It is shown in below figure.

→ Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only 2 values of resistors are required.

→ The typical value of R ranges from $2.5\text{ K}\Omega$ to $10\text{ K}\Omega$.

→ For simplicity let us consider a 3-bit DAC, where the switch position $D_1 D_2 D_3$ corresponds to the binary word 100.

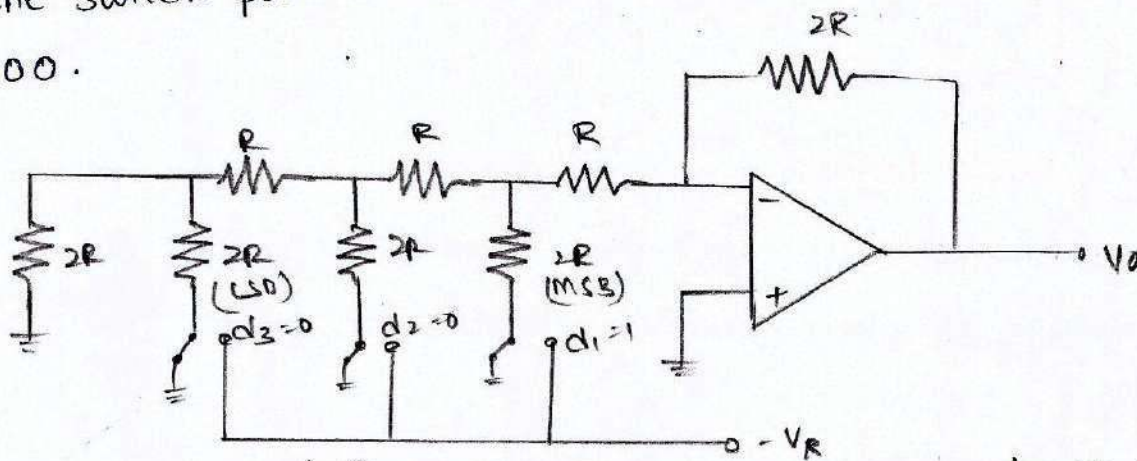


fig (a)

→ The equivalent circuit can be simplified as shown in below

fig.

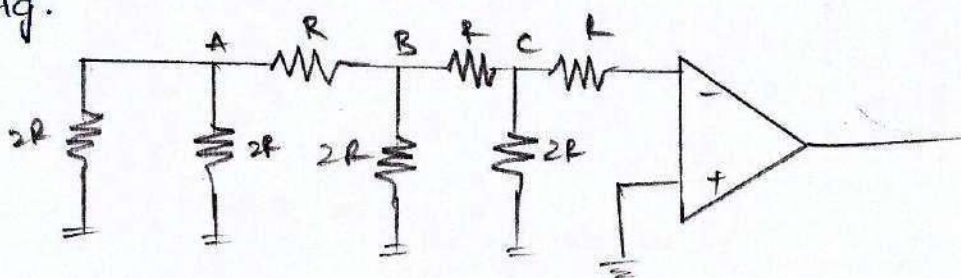
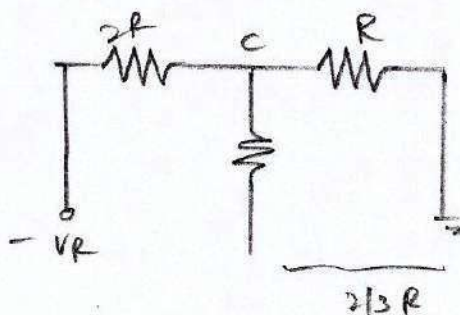


fig (b) Equivalent CRT of fig (a)



equivalent CRT of fig (b)

→ Then voltage at node c can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R \left(\frac{2}{3}R \right)}{2R + \frac{2}{3}R} = \frac{-V_R}{4}$$

The o/p voltage is

$$V_o = -\frac{2R}{R} \left(\frac{-V_R}{4} \right)$$

$$= \frac{V_R}{2}$$

$$V_o = \frac{V_{FS}}{2}$$

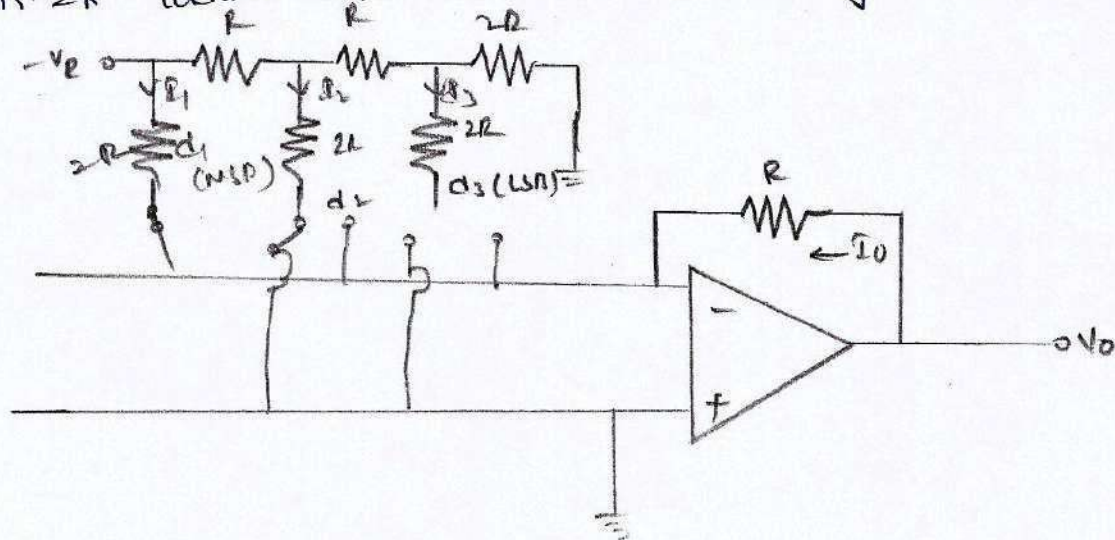
3. Inverted R-2R ladder :

→ In weighted resistor type DAC and R-2R ladder type DAC current flowing in the resistors changes as the i/p data changes.

→ more power dissipation causes heating.

→ this problem can be avoided completely in inverted R-2R ladder type DAC.

→ R-2R ladder D/A converter uses only 2 resistors values.



→ Here each bit of binary word converts the corresponding switch either to ground (or) to the inverting i/p terminal of the op-amp which is at the virtual ground.

→ Since both the positions of switch are at ground potential, the current flowing through resistances is constant and it is independent of switch position.

→ These current can be given as

$$I_1 = \frac{V_R}{R}$$

$$I_2 = \frac{V_R/2}{2R}$$

$$= \frac{V_R}{4R}$$

$$I_2 = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R}$$

$$= \frac{V_R}{8R}$$

$$I_3 = \frac{I_1}{4}$$

We know that ,

$$V_0 = -I_0 R_f$$

$$= -R_f (I_1 + I_2 + I_3)$$

$$V_0 = -R_f \left[D_1 \cdot \frac{V_R}{2R} + D_2 \frac{V_R}{4R} + D_3 \frac{V_R}{8R} \right]$$

$$= -\frac{V_R R_f}{R} \left[D_1 \bar{2}^1 + D_2 \bar{2}^2 + D_3 \bar{2}^3 \right]$$

$$\text{If } R_f = R = V_0 = -V_R (D_1 \bar{2}^1 + D_2 \bar{2}^2 + D_3 \bar{2}^3)$$

Let us consider 3-bit i/p with binary 011.

Here the o/p voltage is given as

$$V_o = -V_R [0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}]$$

$$= -V_R \left[0 + \frac{1}{4} + \frac{1}{8} \right]$$

$$= -V_R [0.25 + 0.125]$$

$$= -V_R [0.375]$$

Let $V_R = 5V$

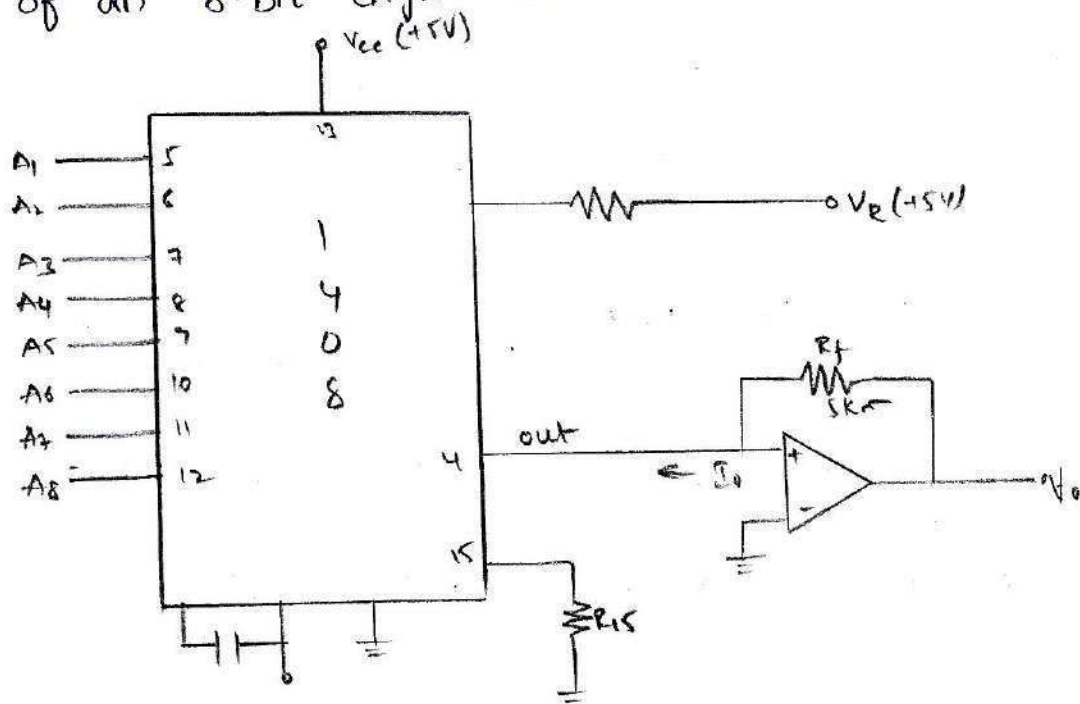
$$= -5 \times 0.375$$

$$V_o = -1.875V$$

IC 1408 DAC :

→ The 1408 is an 8-bit R-2R ladder type D/A Converter compatible with TTL and CMOS logic.

→ It is designed to use where the o/p current is linear product of an 8-bit digital word.



- The IC 1408 consists of a reference current amplifier, an R/2R ladder and 8-bit high speed current switch.
- It has 8 i/p data lines as A_1 (MSB) through A_8 (LSB) which controls the positions of current switches.
- It requires 2mA reference current for full scale i/p & 2 power supplies $V_{CC} = +5V$ and $V_{EE} = -5V$.
- The voltage V_R and resistor R_{14} determines the total reference current source.

$$\text{i.e., Current } I = \frac{V_R}{R_{14}}$$

$$= \frac{5}{2.5K\Omega} = 2mA$$

- R_{15} is generally equal to R_{14} to match the i/p impedance of the current amplifier.
- The below fig. shows a typical 8-bit DAC 1408 compatible with TTL and CMOS logic.
- If settling time is around 300ms.

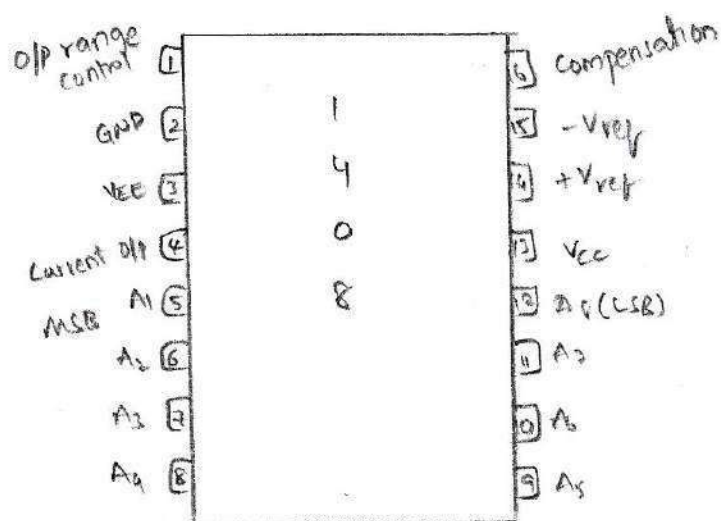


fig : pin diagram

- It consists of 8 i/p data lines A_1 (MSB) to A_8 (LSB).
- It needs 2mA reference current for full scale i/p.
- The two power supplies $V_{CC} = 5V$ & $V_{EE} = -5V$.
- The resistance R_{15} is equal to R_{14} . Hence match the i/p impedance of the reference source.

The o/p current I_0 is given by

$$I_0 = \frac{V_R}{R_{14}} \left[\sum_{i=1}^n A_i 2^{-i} \right]$$

$$A_1 = 0 \text{ (or) } 1$$

The total reference current is equal to

$$\frac{V_R}{R_{14}} = 5V / 2.5K\Omega = 2mA.$$

for full scale i/p

$$I_0 = \frac{5}{2.5K} \left[\sum_{i=1}^8 A_i \times 2^{-i} \right]$$

$$= 1.992 \text{ mA}$$

The o/p voltage V_0 for full scale i/p is

$$V_0 = 2mA \left[\frac{255}{256} \right] \times 5 \times 10^3$$

$$= 9.91 \text{ V.}$$

The o/p voltage eqn

$$V_0 = \frac{V_R}{R_{14}} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \dots + \frac{d_8}{256} \right]$$

- for the bipolar range from -5V to 5V the 1408 DAC can be calibrated by adding R_B b/w V_R and o/p voltage pin 4

as indicator in the following fig.

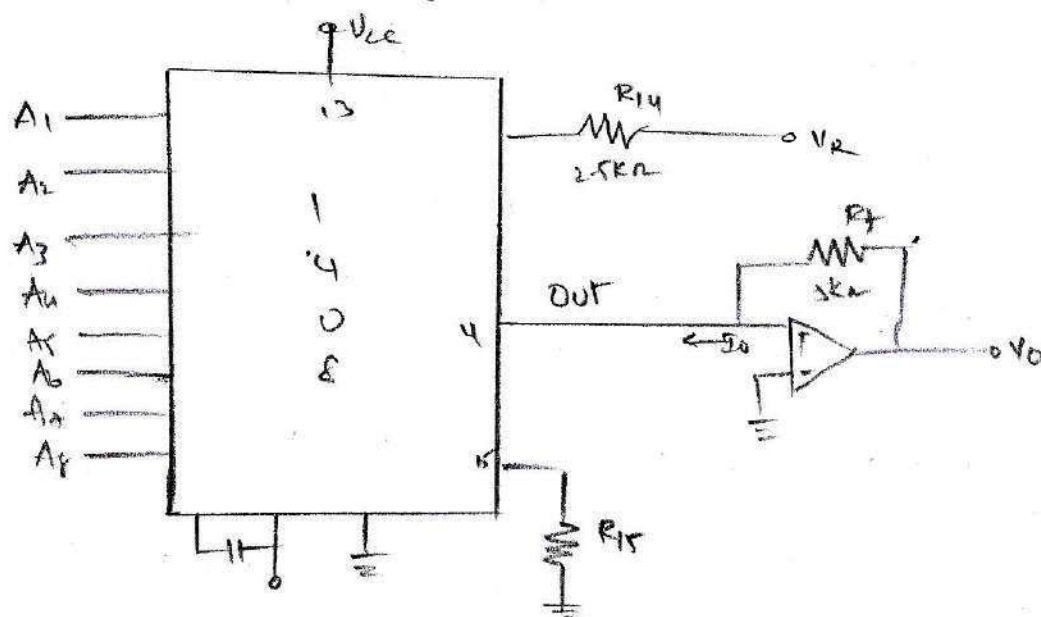


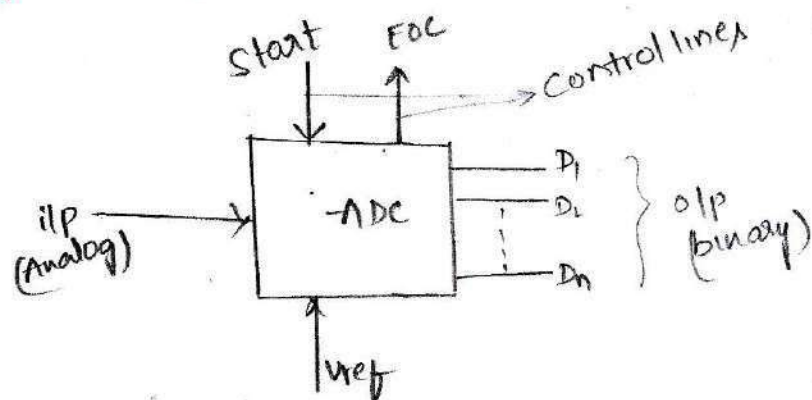
fig: 1408 D/A Converter voltage o/p range in unipolar Range

→ The resistor R_B gives 1mA current to the o/p.

The o/p current for the bipolar operation I_0' is

$$I_0' = I_0 - \left[\frac{V_R}{R_{14}} \right] \left[\sum_{i=1}^8 d_i 2^{-i} \right] - \left(\frac{V_B}{R_B} \right)$$

Analog to Digital Converters :



EOC = end of conversion

→ The ADC is a circuit in which analog i/p combines with reference voltage to give the digital o/p. The schematic representation of ADC is shown in above fig.

→ ADC is a opposite version of DAC. ADC also uses the reference voltage to give an o/p.

The o/p eqn is

$$D = d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n.$$

where $d_1 = \text{MSB}$; $d_n = \text{LSB}$

→ ADC consists of 2 control lines i.e., start & EOC.

start : It is a i/p control line to tell the ADC to start the conversion.

EOC : It is a o/p control line to announce when the conversion is completed.

→ Depending upon the type of application ADC are designed for micro processor.

→ ADC are classified into 2 types. 1. Direct type ADC
2. Integrating type ADC.

1. Direct type ADC :

It compares the given analog signal with the internally generated equivalent signal. These are classified into 3 types.

(a) Parallel Comparator type ADC

(b) Counter type ADC

(c) Successive Approximation type ADC.

2. Integrating Type ADC :

It performs conversion in indirect manner by first changing the analog i/p signal to a linear function of time & then to a digital bits. These are classified into 2 types.

(a) Dual Slope type ADC

(b) Charge Balance type ADC.

218 V_R to 318 V_R	1	1	1	0	0	0	0	0	1	0
318 to 418	1	1	1	1	0	0	0	0	1	1
418 to 518	1	1	1	1	1	0	0	1	0	0
518 to 618	1	1	1	1	1	1	0	1	0	1
618 to 718	1	1	1	1	1	1	1	1	1	0

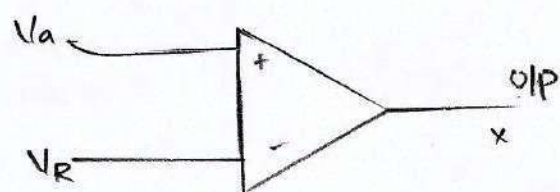
→ One i/p of each comparator is connected to the i/p signal V_a & other i/p is connected to the reference signal V_R generated by the resistive divider n/w.

→ At each node of the resistive divider equal voltage is available.

→ Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided b/w V_R & GND.

→ The purpose of the circuit is to compare the analog i/p V_a with each of the node voltages. Corresponding truth table is shown in above fig.

→ The individual comparator truth table is shown in below fig.



i/p's	o/p
$V_a > V_R$	$x = 1$
$V_a < V_R$	$x = 0$
$V_a = V_R$	previous o/p

→ It is also called as Flash type A/D comparator.

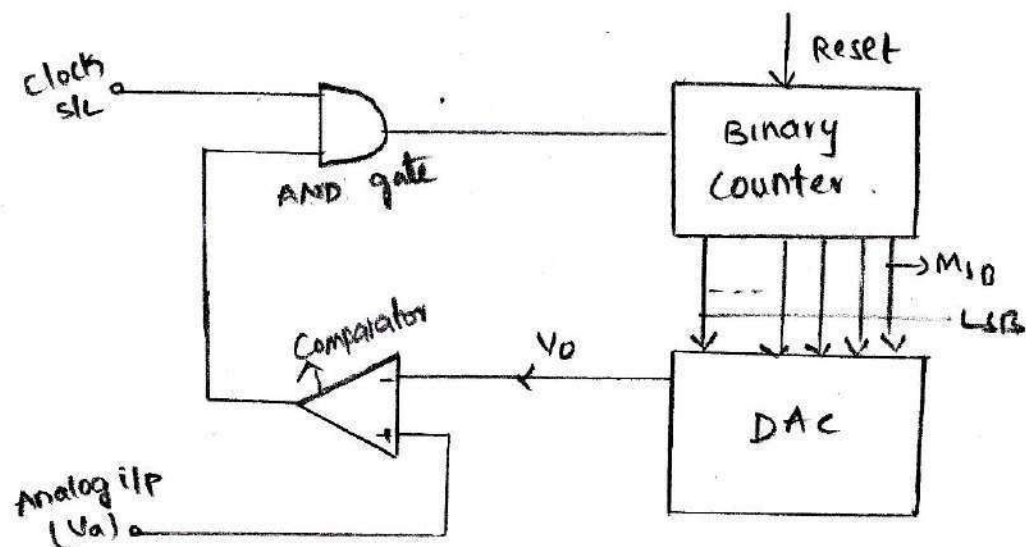
(b) Counter type ADC :

It is one type of analog to digital converter.

→ Here the o/p of DAC is continuously compared with the i/p analog signal.

→ When the o/p of DAC is greater than analog i/p then only the o/p of comparator is high.

- The block diagram of counter type ADC is shown in fig.
- It consists of a binary counter, DAC, comparator & AND gate.



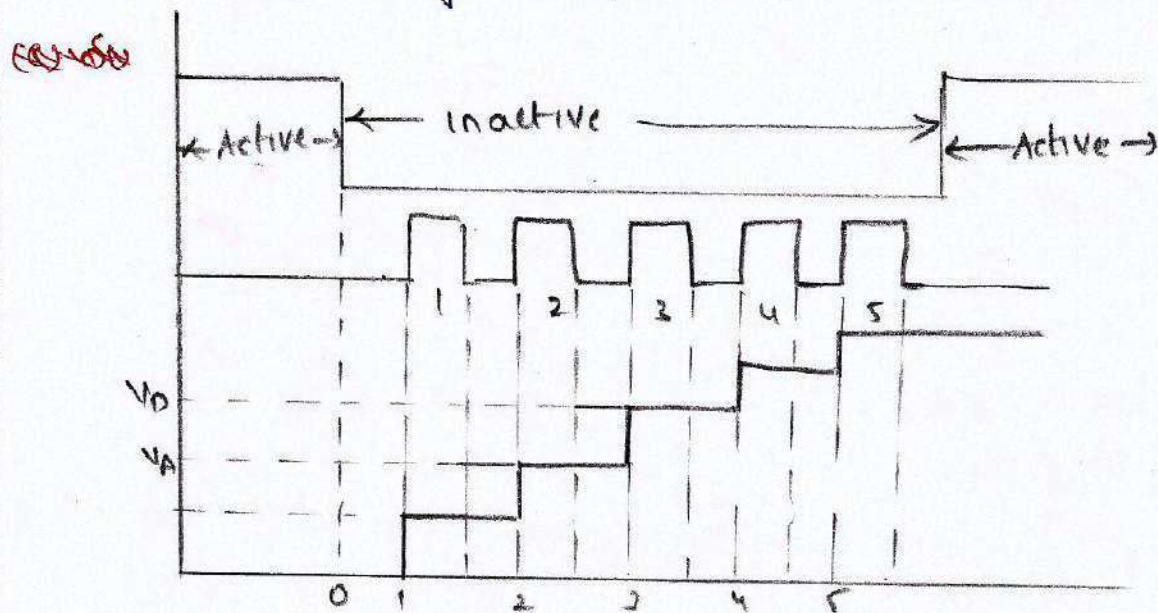
Working :

1. Initially the counter is reset i.e., its o/p is set to zero by applying a reset pulse.
2. The o/p of counter is given as digital i/p to DAC. Since i/p to DAC is zero, its o/p is zero.
3. When the analog i/p is applied to comparator, it becomes greater than V_0 .
4. Here V_A is applied to the non-inverting terminal of the comparator & V_0 is applied to the inverting terminal of the comparator. When $V_A > V_0$, the comparator o/p goes high.
5. For an "AND" gate one i/p is clock pulse applied & another i/p is the o/p of the comparator.
6. When comparator o/p is high then the AND gate is able to allow the clock pulses & it is given to the binary counter.
7. The counter starts counting these clock pulses according to the clock pulses goes on increasing. This increases the o/p of the DAC.

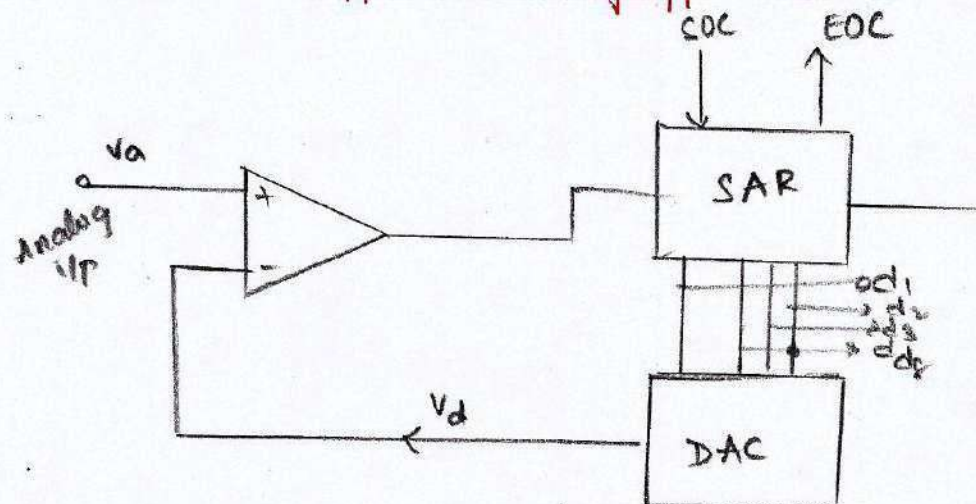
The above steps are repeated till $V_A < V_D$. when V_A is less than V_D the o/p of comparator goes low due to this 'and' gate disables i.e., AND gate is not allow the clock pulses so the counting process of counter is stopped.

→ For next A/D conversion the i/p voltage V_A changes. The binary counter is cleared by applying second reset pulse.

→ The corresponding waveforms shown in below figure.



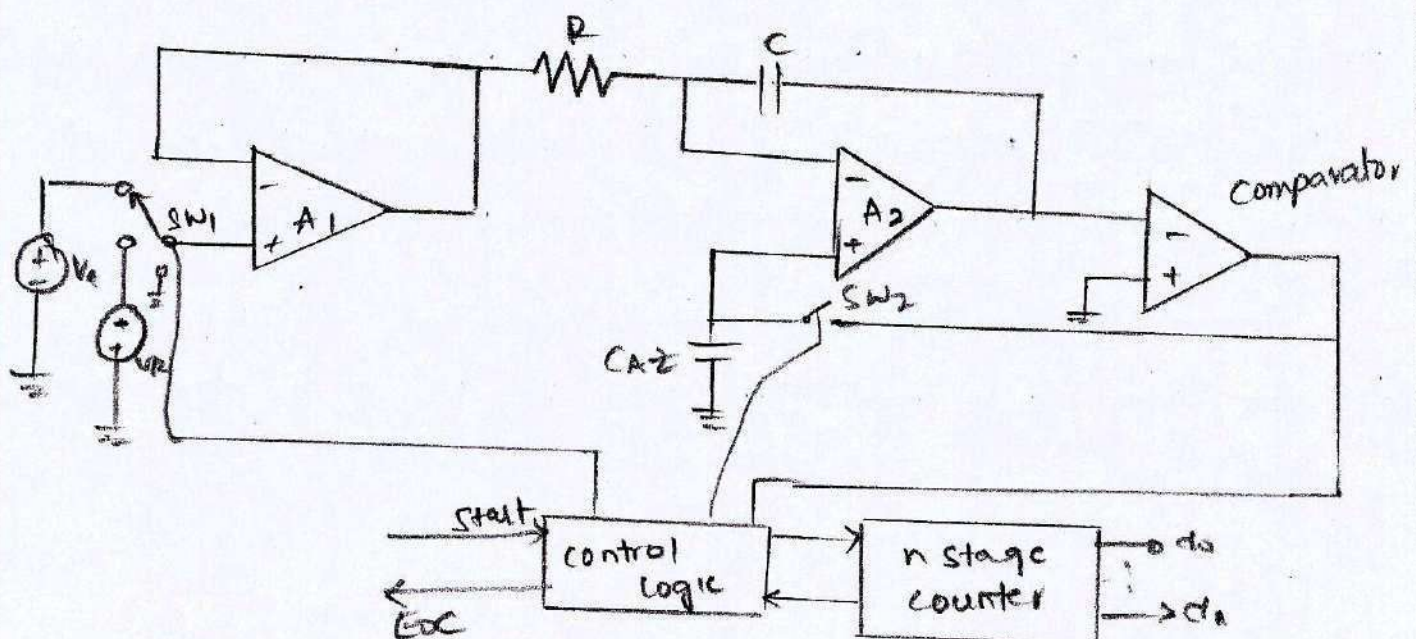
(c) Successive Approximating type ADC :



→ It is one of the most popular A/D convertor. The block diagram of successive approximation type ADC shown in above figure.

- It consists of SAR (Successive Approximation register), SOC, EOC and DAC, comparator.
- The successive approximation method uses ~~proce~~ process for to search binary bits, it completes the searching process for n -bit conversion in ' n ' clock ~~pe~~ cycles.
- The external clock signal is used to set the internal timing parameters.
- The control signal SOC is used to start the conversion and EOC is used to end the conversion.
- The analog i/p signal V_a is applied at one i/p of the comparator before slot the SOC the o/p should be zero.
- After initializing the SOC, the SAR sets the four bit binary code as an input of DAC. i.e., it sets the MSB bit $d_1 = 1$, while all other bits to zeros. So that the trial code is 1000.
- Now the o/p of DAC is compared with the analog i/p signal V_a .
- If $V_a > V_d$, the o/p of comparator is one then the MSB bit (or) SAR sets the MSB bit is left 1 and next LSB bit is made one and further tested.
- However if $V_a < V_d$, the o/p of comparator is zero then SAR sets the MSB bit zero and next LSB bit is made one.
- This process repeated for all subsequent bits, one at a time until all bit positions have been tested.
- Whenever the DAC o/p crosses V_a , the comparator changes the state and this can be taken as the EOC control signal.

Dual Slope Type ADC :



- The above figure shows the dual slope type ADC.
- It consists of high input impedance buffer A_1 , integrator A_2 and voltage comparator, control logic & n -stage counter.
- The converter first integrates the analog i/p signal V_a for a fixed duration of 2^n clock periods.
- Then it integrates an reference voltage V_R of opposite polarity until the integrator o/p is zero.
- The number of N of clock cycles required to return the integrated to zero is proportional to the value of V_a average over the integration period.
- Before the start signal switch sw_1 is connected to ground and switch sw_2 is closed.
- So, any ~~effect~~ offset voltage present in the A_1 & A_2 , it appears across the capacitor in CA_2 till the threshold of the comparator is achieved. Thus the capacitor CA_2 provides the input offset voltage of all the 3 amplifiers.
- Later when sw_2 opens CA_2 acts as memory device to store the energy levels (or) voltage.
- After START signal initiates the at $t = t_1$, the control logic open sw_2 switch and sw_1 switch connects to the V_a and enables the counter starting from zero.
- Here n stage ripple counter is used so the counter resets to zero after counting 2^n clock cycles (or) pulses.
- If the clock period is t_1 , the integration takes place for a time $t_1 = 2^n T$ and the o/p is a ramp going downward shown in below figure.

→ The counter resets itself to zero at the end of the interval T and the switch Sw_1 is connected to the reference voltage $-V_R$.

→ Now, the o/p voltage V_o will have positive slope.

→ However when V_o becomes just zero at a time $t = t_3$ the control logic issues an end of conversion signal. So no further clock pulses enter the counter.

→ It can be shown that the reading of the counter at t_3 is proportional to the analog i/p voltage V_a .

$$T = t_2 - t_1$$

$$= 2^n \cdot \frac{\text{clock period}}{\text{clock pulses}}$$

$$t_3 - t_2 = n \frac{\text{clock cycles}}{\text{clock period}}$$

for an integrator

$$\frac{\Delta V_o}{\Delta V_t} = -\frac{1}{RC}$$

$$\Delta V_o = -\frac{1}{RC} \Delta V_t$$

The voltages V_o will be equal to V_i at the instant t_2 and it can be written as

$$V_i = -\frac{1}{RC} V_a (t_2 - t_1)$$

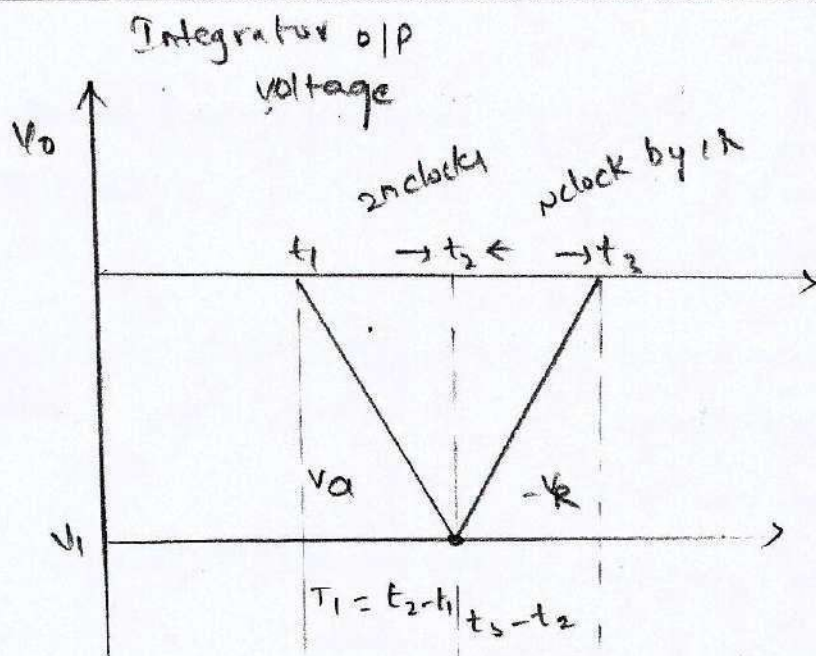
it can be also written as

$$V_i = -\frac{1}{RC} V_R (t_3 - t_2)$$

$$V_a (t_2 - t_1) = -V_R (t_3 - t_2)$$

$$V_a (2^n) = -V_R (N)$$

$$V_a = \frac{-V_R (N)}{2^n}$$



Specifications of A/D and D/A converter :

1. Resolution
2. Linearity
3. Accuracy
4. Settling time
5. Stability

Both A/D & D/A converter are available with ~~with~~ wide range of specifications.

→ The various important specifications of converter generally specified by the manufacture are analysing.

Resolution :

The resolution of a converter is the smallest change in voltage which may be produced at the o/p of the converter.

Linearity :

Linearity specification of converters. It is an important measure of accuracy and tells us how close the converter o/p is to its ideal transfer characteristics.

Accuracy :

It is a maximum deviation b/w the ~~load~~ actual convertor and practical convertor o/p to the ideal convertor o/p.

Settling Time :

It represents the time it takes for the o/p of settle with in a specified band of its final value following a code change at the input.

Settling ranges from 100 ns to 10 ms depending upon word length and type of circuit used.

Stability :

Stability shows the performance of the convertor. The performance of convertor changes with temperature, age of components, power supply variations.

ACTIVE FILTERS & OSCILLATORS

Introduction :

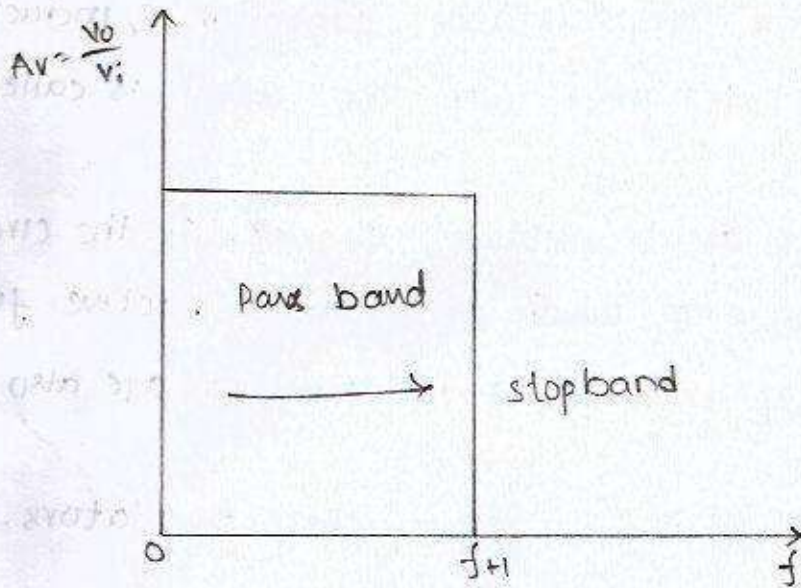
- Filter is a frequency selective device. It is a circuit which is used for selecting a particular band of frequency.
- Filter can be designed which passive and as well as the active components.
- Passive elements are resistance, capacitor & inductor.
- If the circuit designed with RLC which is called passive filter.
- Active elements are transistors, OP-amps. If the circuit is designed with op-amp which is called as active filter.
- In active filter resistors and capacitors are also be used to design circuit.
- RC filters are used for low frequency oscillators. LC filters are used for high frequency oscillators.

Advantages of Active (or) Passive filters :

1. Gain and frequency adjustment flexibility.
2. No loading effect.
3. It is cheap (It is the cost is very low)
4. The most commonly used filters are
 - (a) Low pass filter (LPF)
 - (b) High pass filter (HPF)
 - (c) Band pass filter (BPF)
 - (d) Band Reject filter (BRF)
 - (e) All Pass filter

Low Pass Filter :

In ideal low pass filter, the input signal frequency at the lower range of the band are allowed to pass and its completely stops after designed cutoff frequency (f_H).



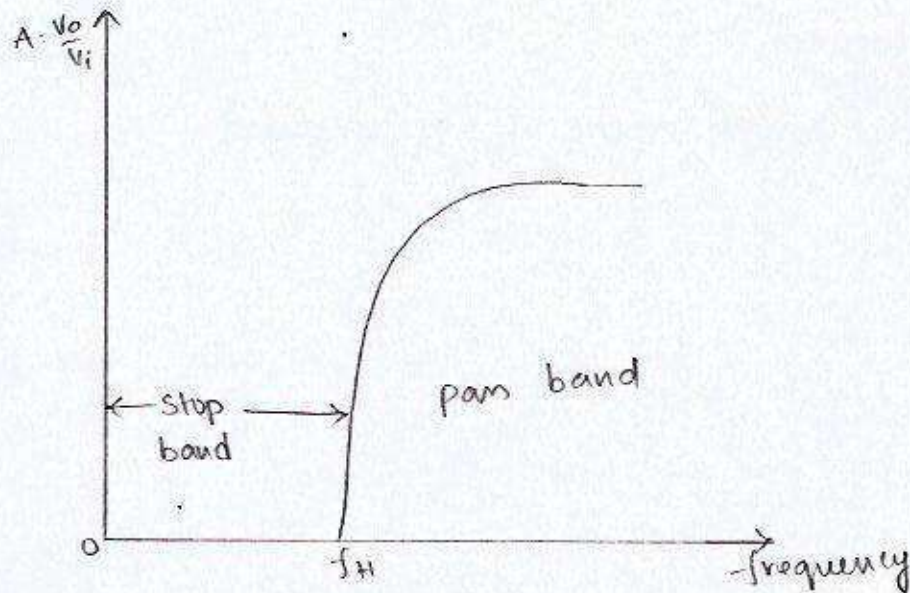
- The low pass filter allows frequency for lower range of frequency upto f_H . and beyond f_H which is the cutoff frequencies, a higher cutoff frequency is totally stopped.
- If we plot the gain V_i frequency of an ideal low pass filter we should get such type of characteristics.
- The region or over the frequency band in which the signal is allow to pass i.e., called pass band.
- The frequencies beyond f_H is called stop band.

High Pass filter :

In high pass filter the higher band of frequency will

14
be allowed and lower band of frequencies will not be allowed.

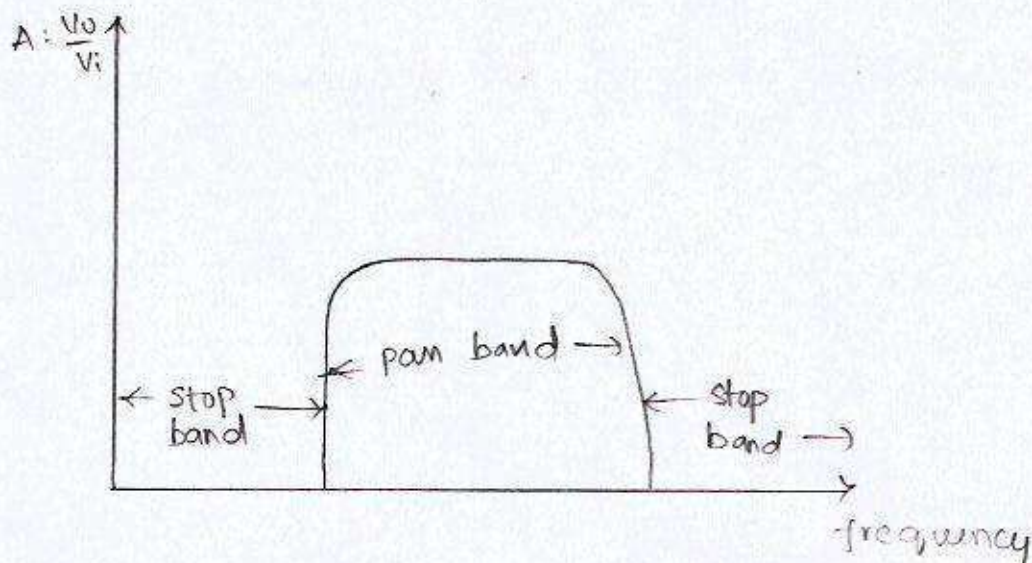
→ If we plot the gain V_o/V_i frequencies.



Band Pass Filter :

The signal is passed with in a particular band which is called pass band.

→ Here between f_L and f_H band of frequencies is allowed but below f_L after f_H it is totally stopped.

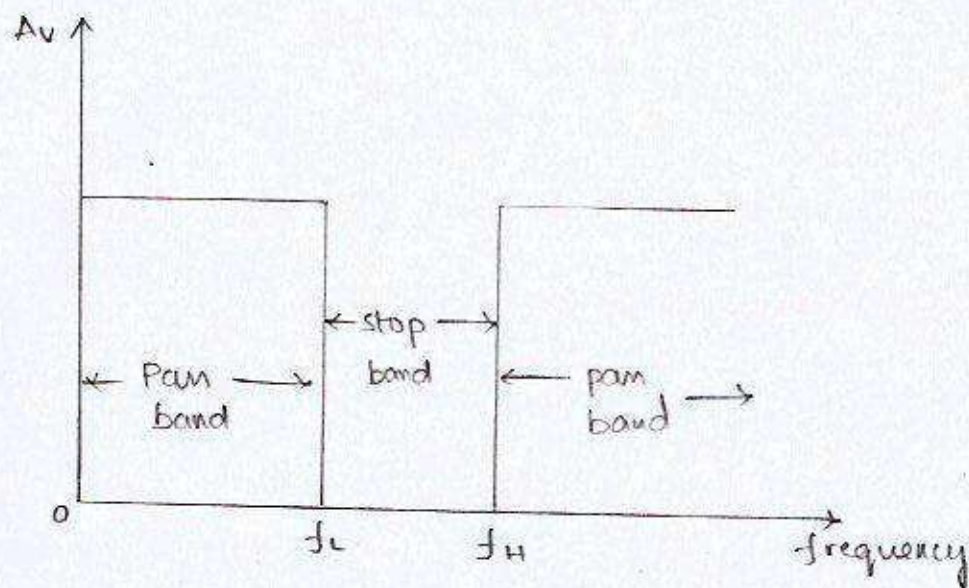


→ Basically band pass filter is a combination of high pass and low pass filters.

Band Reject Filter :

In band reject filter below the frequency band f_L is allow and above f_L and below f_H and frequency band is stopped.

→ Frequency band above f_H is allowed

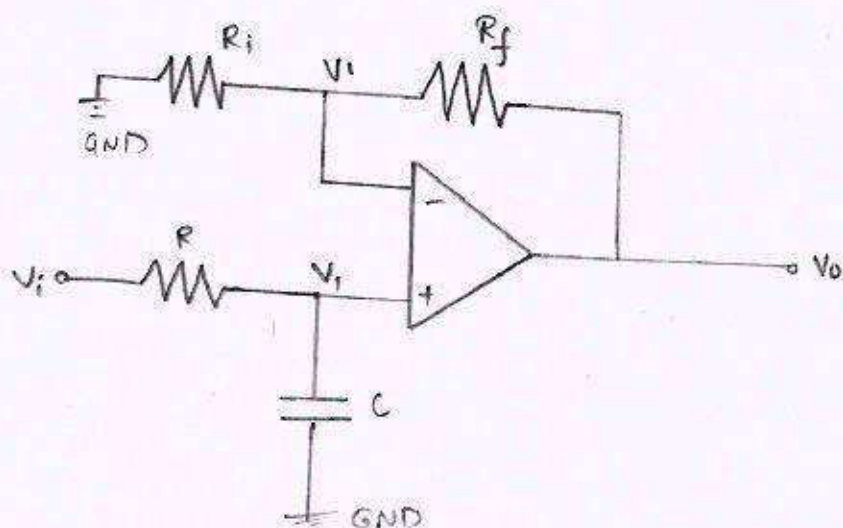


All pass Filter :

It will be allowing all frequencies to pass through it.

First Order LPF :

- First order filter consists of a single RC network connected to the non-inverting input terminal of op-amp.
- First order LPF shown in below figure.



- Resistors R_f & R_i determines the gain of the filter.
- The resistor R & capacitance C determines the cut off frequencies of the filter.
- Since the op-amp is used in the non-inverting configuration, so the closed loop gain of the filter is given by

$$A_{VF} = 1 + \frac{R_f}{R_i}$$

Analysis :

- We have to obtain the expression for v_1 , which is the voltage across the capacitor C .
- The resistor R & capacitor C forms a voltage divider network across the i/p voltage V_i .
- Therefore voltage V_1 at non-inverting terminal is given by according to potential divider theorem,

$$V_i = \frac{V_i \cdot \frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}$$

$$= \frac{V_i \cdot \frac{1}{j\omega C}}{\frac{j\omega RC + 1}{j\omega C}}$$

$$V_i = \frac{V_i}{1 + j\omega RC}$$

We know that, $A_{Vf} = 1 + \frac{R_f}{R_i}$

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_i$$

$$= \left(1 + \frac{R_f}{R_i}\right) \frac{V_i}{1 + j\omega RC}$$

$$\frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_i}\right) \frac{1}{1 + j\omega RC}$$

$$= A_{Vf} \cdot \frac{1}{1 + j\omega RC}$$

But $\omega = 2\pi f$

$$\frac{V_o}{V_i} = A_{Vf} \frac{1}{1 + j2\pi f RC}$$

$$= A_{Vf} \frac{1}{1 + j \frac{f}{f_c} 2\pi RC}$$

$$= A_{Vf} \frac{1}{1 + j(f/f_c)}$$

$$\left[\because f_c = \frac{1}{2\pi RC} \right]$$

$$\left| \frac{V_o}{V_i} \right| = \frac{A_{V_F}}{\sqrt{1 + (f/f_h)^2}}$$

The first order LPF can be verified from the above eqn as under 3 conditions.

1. At very low frequencies i.e., $f \ll f_h$

$$\left| \frac{V_o}{V_i} \right| \approx A_{V_F}$$

Thus at very Low frequencies, the filter gain is constant.

2. At $f = f_h$

$$\left| \frac{V_o}{V_i} \right| = \frac{A_{V_F}}{\sqrt{1 + (1)^2}}$$

$$= \frac{A_{V_F}}{\sqrt{2}}$$

$$\left| \frac{V_o}{V_i} \right| = 0.707 A_{V_F}$$

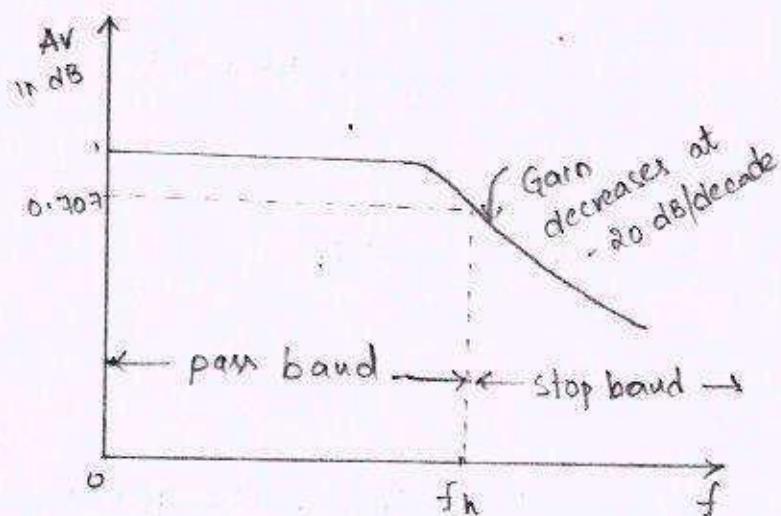
Thus at $f = f_h$, the filter gain reduces by 3 dB, as the dB value of 0.707.

3. At very high frequencies i.e., $f \gg f_h$.

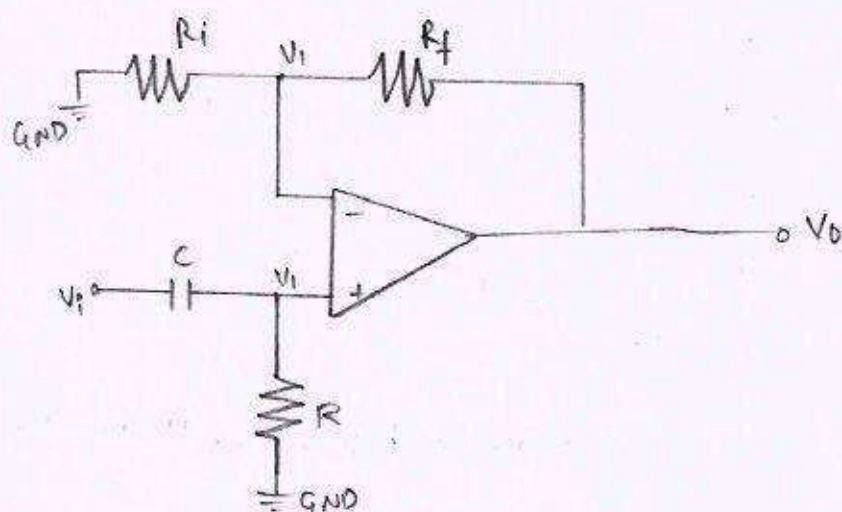
$$\left| \frac{V_o}{V_i} \right| < A_{V_F}$$

Thus the filter gain will keep decreasing with increasing frequency. This decrease takes place at a constant rate of -20 dB/decade. Here "decade" means 10 times & the gain is expressed in dB. & -ve sign indicates that gain is decreasing.

→ Hence, frequency response of first order LPF is shown in below fig.



First Order HPF :



Analysis :

- We obtain voltage across resistor i.e., V_1 .
- According to potential divider rule,

$$V_1 = V_i \cdot \frac{R}{R + \frac{1}{j\omega C}}$$

$$V_1 = V_i \cdot \frac{j\omega RC}{1 + j\omega RC}$$

W.K.T $A_{vf} = 1 + \frac{R_f}{R_i}$

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_i$$

$$= \left(1 + \frac{R_f}{R_i}\right) \times V_i \frac{j\omega RC}{1 + j\omega RC}$$

$$\frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_i}\right) \times \frac{j\omega RC}{1 + j\omega RC}$$

But $\omega = 2\pi f$

$$= \left(1 + \frac{R_f}{R_i}\right) \times \frac{j2\pi f RC}{1 + j2\pi f RC}$$

$$= \left(1 + \frac{R_f}{R_i}\right) \times \frac{j f / \frac{1}{2\pi RC}}{1 + j f / \frac{1}{2\pi RC}}$$

$$\frac{V_o}{V_i} = A_{VF} \times \frac{j f / f_L}{1 + j f / f_L}$$

$$\left| \frac{V_o}{V_i} \right| = \frac{A_{VF} \times (f / f_L)}{\sqrt{1 + (f / f_L)^2}}$$

$$= \frac{A_{VF}}{\sqrt{\frac{1 + (f / f_L)^2}{(f / f_L)^2}}}$$

$$\boxed{\left| \frac{V_o}{V_i} \right| = \frac{A_{VF}}{\sqrt{1 + (f / f_L)^2}}}$$

→ The first order HPF can be verified from the above eqⁿ under 3 conditions.

1. At very low frequencies i.e. $f \ll f_L$

$$\left| \frac{V_o}{V_i} \right| < A_{VF}$$

Thus at very low frequencies, gain is Low, with increase in frequency, gain also increases.

2. At $f = f_L$

$$\left| \frac{V_o}{V_i} \right| = \frac{A_{VF}}{\sqrt{2}}$$
$$= 0.707 A_{VF}$$

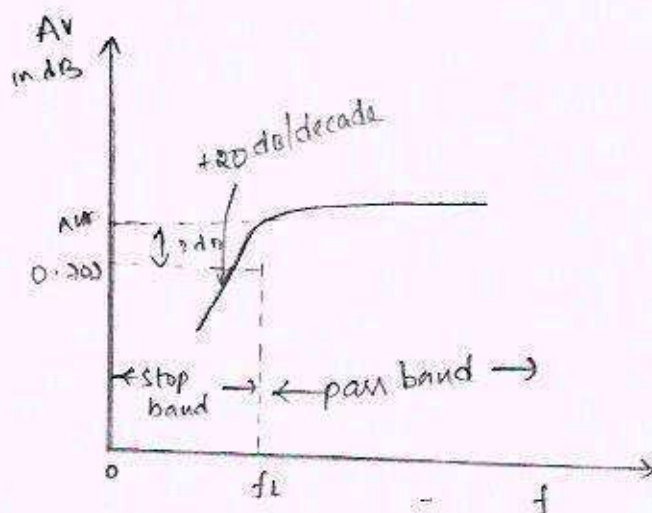
Thus at $f = f_L$ the filter gain increases by 3 dB.

3. At very high frequencies i.e., $f \gg f_L$.

$$\left| \frac{V_o}{V_i} \right| \approx A_{VF}$$

→ Thus at very high frequencies the filter gain is constant.

→ Hence the frequency response of first order HPF shown in below figure.



Band Pass Filter:

→ A band pass filter has a pass band b/w two cut-off frequencies f_H & f_L . i.e., it passes the frequencies f_H & f_L . Outside of this pass band will stop the frequencies.

There are two types of band pass filter, which are classified as per the quality factor.

(a) wide band pass filter

(b) Narrow band

→ If the quality factor is less than 10 ($Q < 10$) then the filter is called as wide band pass filter.

→ If the quality factor is greater than 10 ($Q > 10$) then the filter is called as Narrow band pass filter.

Quality factor:

→ Quality factor Q is the measure of selectivity of filter. The value of Q is given by

$$Q = \frac{f_c}{f_H - f_L}$$

where, $f_H - f_L$ = Bandwidth, so

$$Q = \frac{f_c}{B.W}$$

where $f_c = \sqrt{f_H f_L}$

f_H = upper cut-off frequency

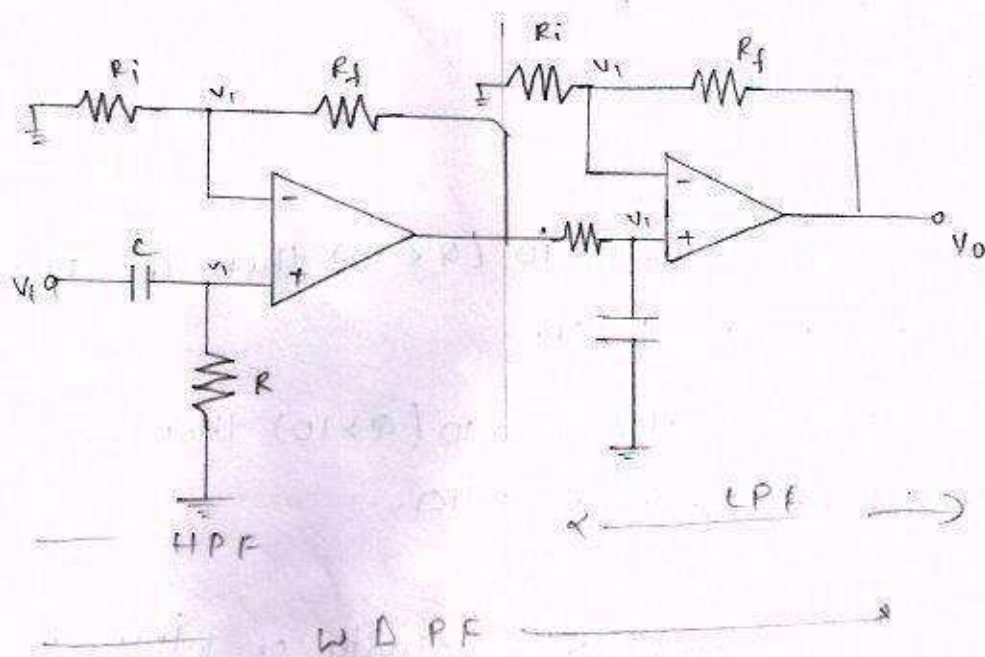
f_L = lower cut-off frequency

(a) Wide Band pass filter:

→ A wide band pass filter is implemented by cascading a first order HPF & first order LPF.

→ It has more band width b/w the two frequencies.

→ The circuit diagram of wide band pass filter shown in below figure.



→ Let us consider individual voltage gains of HPF & LPF is AV_{F1} & AV_{F2} .

→ The overall voltage gain of the wide band pass filter is AV_F .

→ Then AV_F is the product of individual voltage gains.

$$\text{i.e., } \boxed{AV_F = AV_{F1} \times AV_{F2}}$$

→ The magnitude voltage gain of first order HPF is given by

$$\left| \frac{V_0}{V_i} \right| = \frac{AV_{F1}}{\sqrt{1 + (f_L/f)^2}}$$

→ The magnitude voltage gain of first order LPF is given by

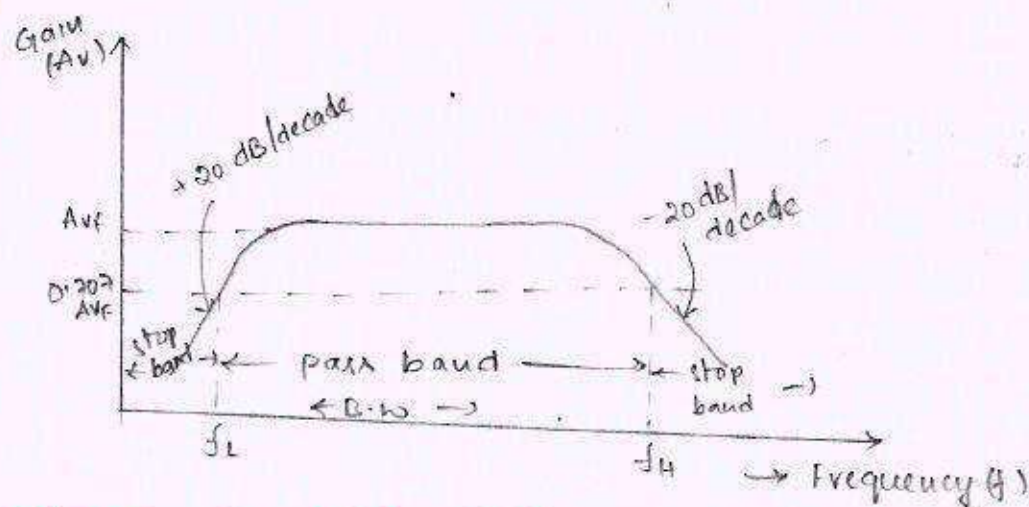
$$\left| \frac{V_0}{V_i} \right| = \frac{AV_{F2}}{\sqrt{1 + (f/f_H)^2}}$$

→ Now, the magnitude voltage gain of wide band pass filter is the product of first order HPF & LPF.

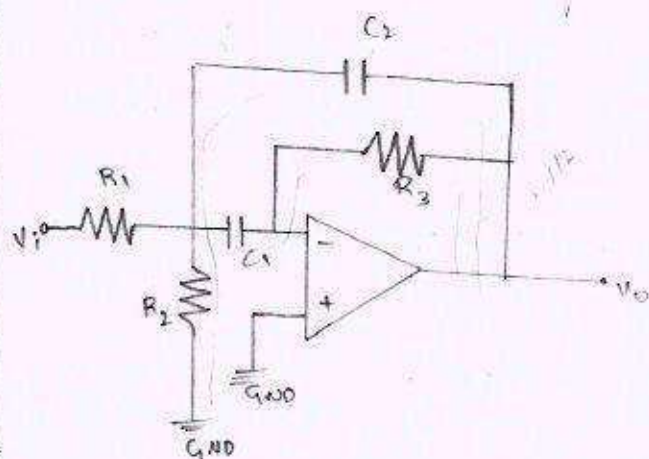
$$\left| \frac{V_0}{V_i} \right| = \frac{AV_F}{\left[\sqrt{1 + (f_L/f)^2} \right] \left[\sqrt{1 + (f/f_H)^2} \right]}$$

Where, $A_{VF} = A_{VF1} \times A_{VF2}$

→ The frequency response of wide band ^{pass} filter is shown in below fig.

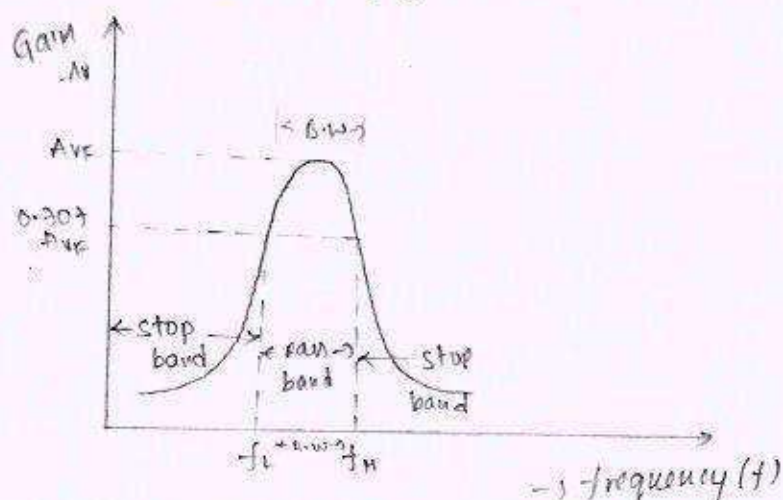


(b) Narrow Band Pass Filter:



→ The narrow band pass filter shown in below fig.

→ The narrow band pass filter is a band pass filter with a small band width shown in below fig.



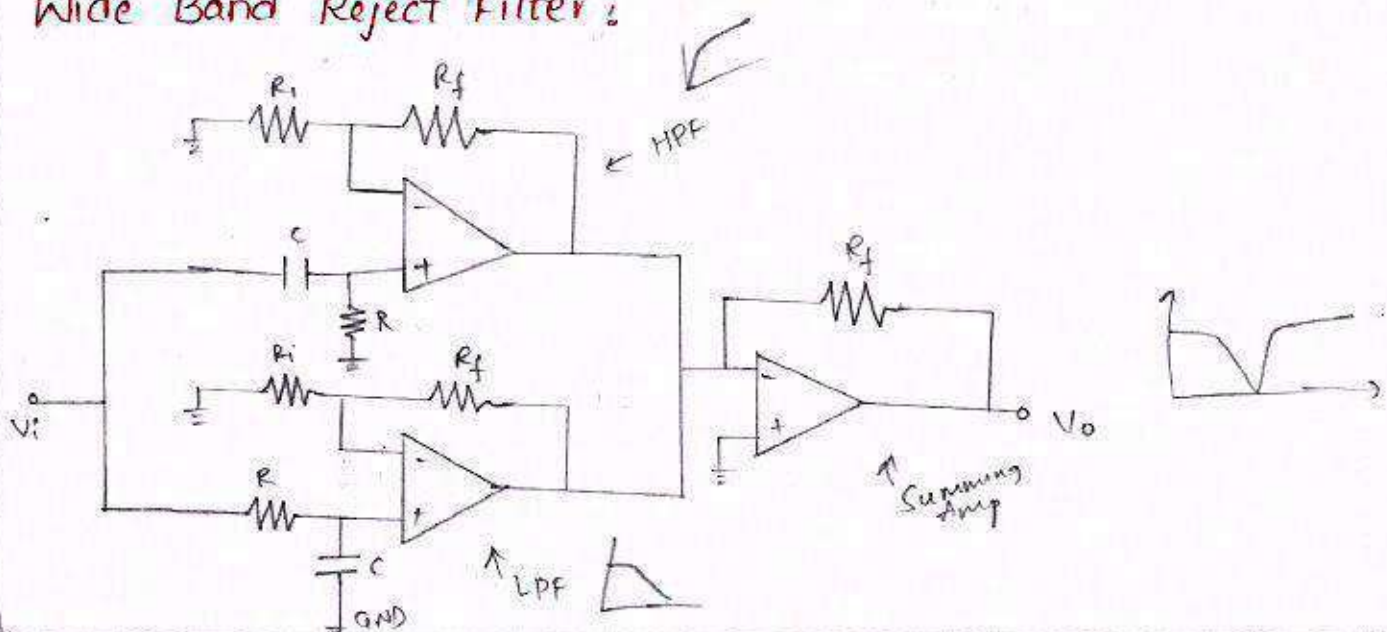
- The frequency response of narrow band pass filter is sharper than that of a wide band pass filter.
- The quality factor of this filter is high than that of wide band pass filter.
- The main features of this filter is
 - It has only one op-amp
 - It has two f/b paths. Hence it is called as multipath f/b filter.
 - Here the op-amp is inverting mode.
 - Here the Band width is small compared to WBPF.

Band Reject Filter :

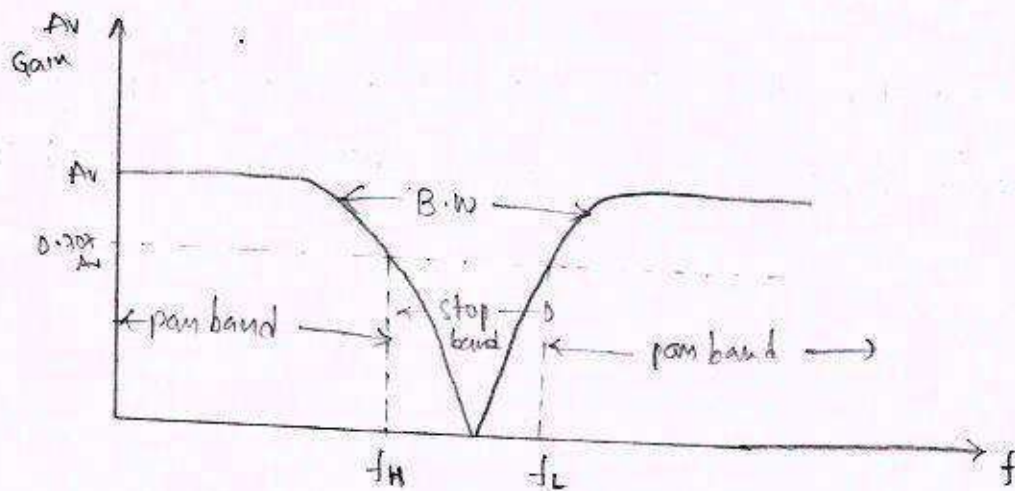
- Band reject filter is a filter in which stop the frequencies in stop band & passes all the frequencies outside the stop band.
- It is also called as Band stop filter (or) Band elimination filter.
- The band reject filter operation is exactly opposite to the band pass filter.
- Band reject filter are classified into 2 types.

- Wide Band reject filter
- Narrow band reject filter

Wide Band Reject Filter :

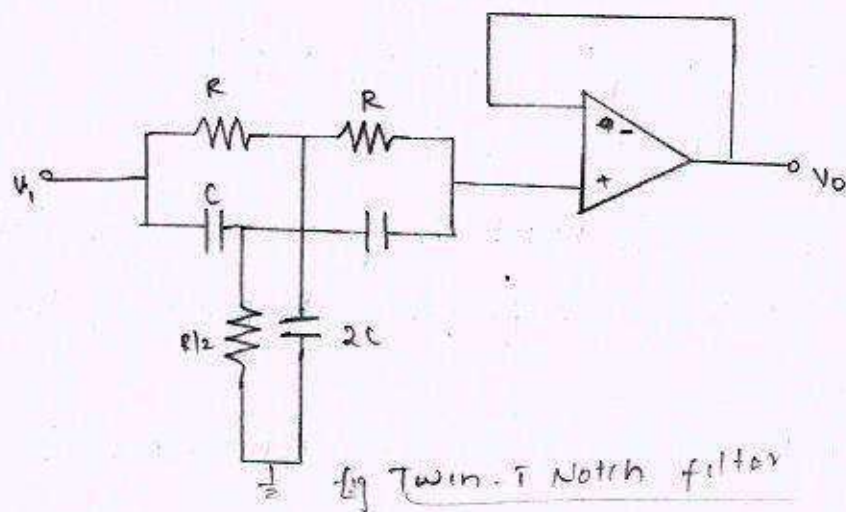


- Like WBPF, this filter also consists of a first order HPF & LPF sections. Additionally it consists of a summing amplifier.
- Here stops the all frequencies b/w f_H & f_L .
- The lower cut-off frequency f_L must be greater than the higher cut-off frequency f_H . It is shown in frequency response of the filter. Shown in below fig.
- The pass band gain of both high pass & low pass sections must be equal.
- Hence the frequency response of the filter is shown in below fig.

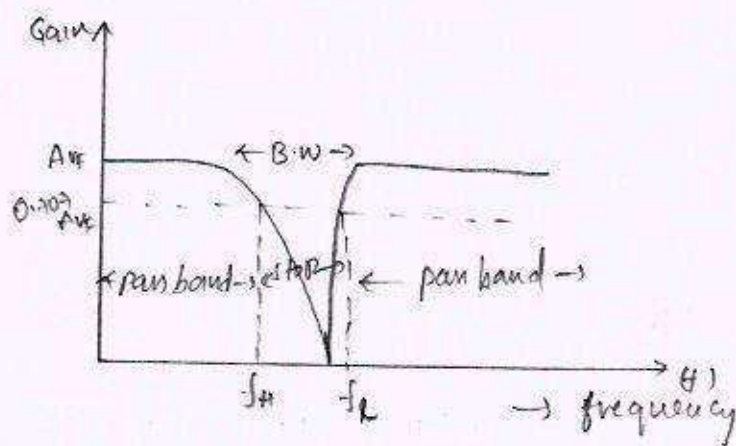


Narrow Band Reject Filter :

- Narrow band reject filter is also called as the notch filter. The quality factor Q of such filters is higher than that of the WBPF.
- Narrow band reject filter have a very sharp frequency response characteristics.
- These are used for rejecting a single frequency such as 50 Hz power line frequency hum.
- Notch filter is the Twin-T n/w shown in below fig.



- The ckt consists of two T-networks. One consist of 2 resistors & 1 capacitor while other consist of 2 capacitor & 1 resistor.
- To design a Notch filter to reject the particular frequency.
- The frequency response of this Notch filter shown in below fig.

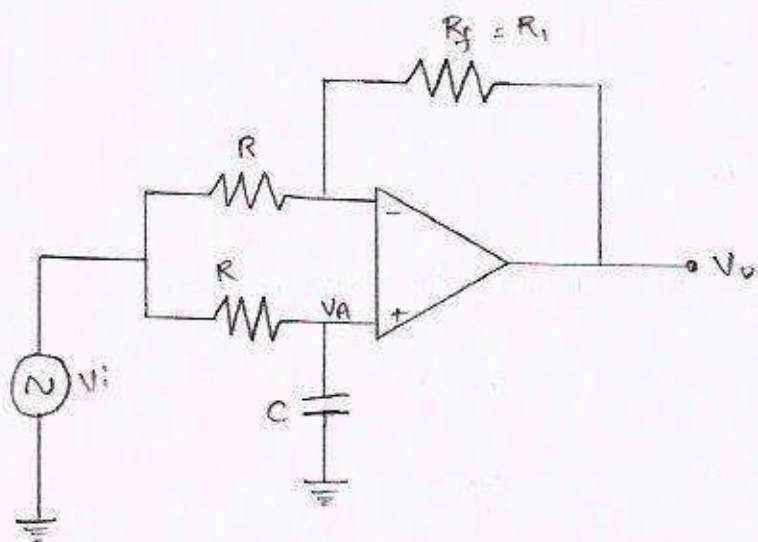


Applications :-

1. Communication circuits
2. Biomedical instruments in order to eliminate the particular frequency.

All Pass Filter :

- APF passes all frequency components of the i/p signal without any attenuation but it provides 90° phase shift for different frequencies of the i/p signal.
- Its magnitude of the gain is 1 (unity) for all the frequencies.
- When signals are transmitted over the transmission lines there is change in their phase.
- Hence all pass filters are also called as delay equalizer because circuit takes some delay to o/p signal.



- Let us use super position principle to obtain the o/p V_o .
- Assume i/p to the non-inverting terminal is zero. so ckt act as an inverting amplifier.
- Therefore, voltage gain of inverting terminal

$$A_{vf} = -\frac{R_f}{R_1}$$

$$\frac{V_{o1}}{V_i} = -\frac{R_f}{R_1}$$

$$V_{O1} = -\frac{R_f}{R_i} \times V_i$$

$$\text{as } R_f = R_i$$

$$V_{O1} = -V_i \rightarrow (1)$$

→ Similarly, let us assume i/p to the inverting terminal is '0'. So the circuit acts as a non-inverting amplifier.

$$\therefore A_{VF2} = 1 + \frac{R_f}{R_i}$$

$$\frac{V_{O2}}{V_A} = 1 + \frac{R_f}{R_i}$$

$$V_{O2} = \left[1 + \frac{R_f}{R_i} \right] V_A$$

$$\text{as } R_f = R_i$$

$$V_{O2} = 2V_A \rightarrow (2)$$

→ The o/p voltage of the circuit is given by,

$$V_O = V_{O1} + V_{O2} \rightarrow (3)$$

Sub. (1) & (2) in eq (3), we get

$$\boxed{V_O = -V_i + 2V_A} \rightarrow (4)$$

→ By potential divider rule, the voltage V_A can be obtained as

$$\begin{aligned} V_A &= \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \times V_i \\ &= \frac{\frac{1}{j2\pi f C}}{j2\pi f C R + 1} \times V_i \end{aligned}$$

$$V_A = \frac{1}{1+j2\pi fRC} \times V_i \rightarrow (5)$$

sub. eq (5) in eq (4)

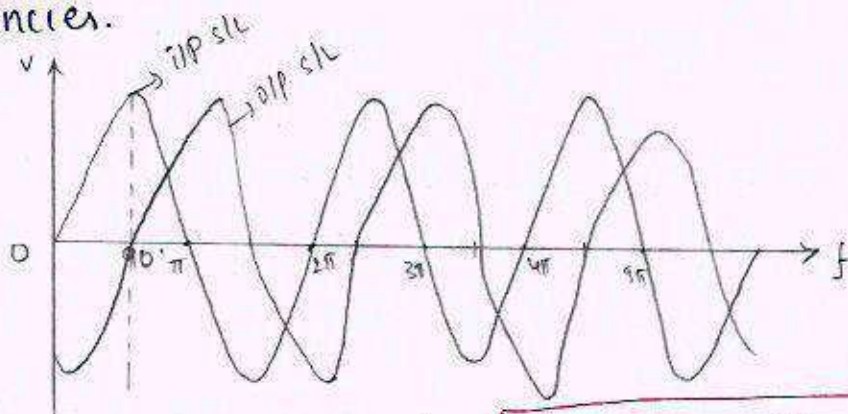
$$\begin{aligned} V_o &= -V_i + 2V_i \left[\frac{1}{1+j2\pi fRC} \right] \\ &= V_i \left[-1 + \frac{2}{1+j2\pi fRC} \right] \end{aligned}$$

$$\frac{V_o}{V_i} = \frac{1-j2\pi fRC}{1+j2\pi fRC}$$

$$\left| \frac{V_o}{V_i} \right| = \frac{\sqrt{1+(2\pi fRC)^2}}{\sqrt{1+(2\pi fRC)^2}}$$

$$\left| \frac{V_o}{V_i} \right| = 1$$

→ The above expression says that the magnitude voltage gain is always 1. for all pass filter and it can pass the range of frequencies.



phase angle is given by $\phi = -2\tan^{-1}(2\pi fRC)$

→ This is the phase angle in degrees which indicates there is a phase shift of angle ϕ° b/w i/p & o/p signal.

Barkhausen Criterion:

It states that

1. The total phase shift around a loop should be 0° or 360° .
2. The magnitude of the product of open loop gain of the op-amp and feedback factor (β) is unity.

i.e., $|A\beta| = 1$

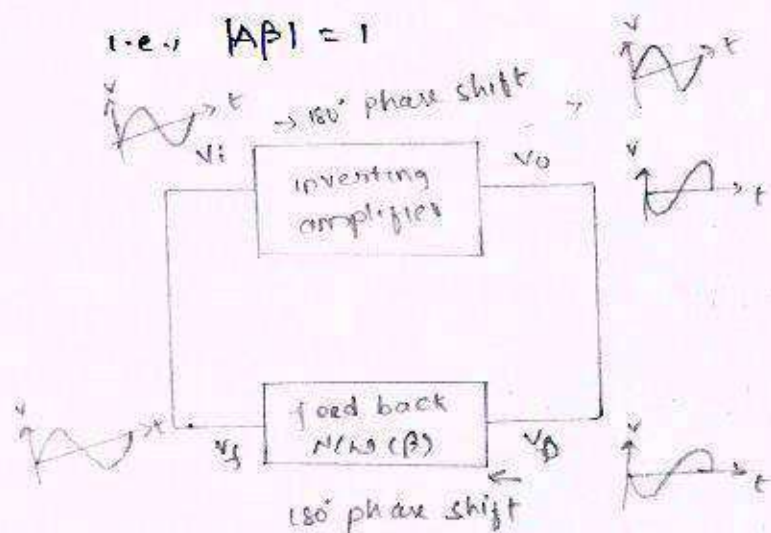


Fig. Block Diagram of oscillator circuit

→ The f/b n/w i/p is V_o , then the feedback n/w produces 180° phase shift.

→ This feedback signal is given to the i/p of the inverting amplifier then again 180° phase shift is provided by the inverting amplifier. so total phase shift around a loop is 0° (or) 360° .

→ Let input voltage of the feedback n/w is V_o i.e. o/p voltage of the inverting amplifier. It is given by

$$V_o = A \cdot V_i \quad \left[\because A = \frac{V_o}{V_i} \right]$$

→ The feedback n/w β provides 180° phase shift i.e., given by

$$V_f = -\beta V_o$$

$$\beta = V_f / V_o$$

$$V_f = \beta V_o$$

where, -ve sign indicates that 180° phase shift provided by the f/b network.

→ For the oscillator, V_f must act as an i/p voltage V_i . So

$$V_i = -\beta V_o$$

we know that, $V_o = AV_i$

$$V_i = -\beta AV_i$$

$$-\beta A = 1$$

let us take magnitude on b.s

$$\therefore |A\beta| = 1$$

→ The above condition is called as Barkhausen criterion.

→ The phase of V_f must be as i/p voltage V_i i.e., feedback n/w introduces 180° phase shift. In addition to 180° phase shift introduced by the amplifier. so total phase shift around a loop is 360° . In this condition feedback voltage V_f drives the circuit without external i/p. so the circuit acts as an oscillator.

→ Similarly the magnitude of product of open loop gain & feedback factor is unity. It is also called as Barkhausen Criterion.

→ The above 2 conditions are required to satisfy the circuit works as an oscillator producing sustained oscillations of constant frequency & amplitude.

→ Let us see the effect of magnitude of product of gain & f/b factor $|A\beta|$ on the nature of the oscillations.

(i) $|A\beta| > 1$:

When the total phase shift around a loop is 0° or 360° and $|A\beta| > 1$ then the oscillations are growing type i.e., the amplitude of the oscillations goes on increasing. it is shown in fig.

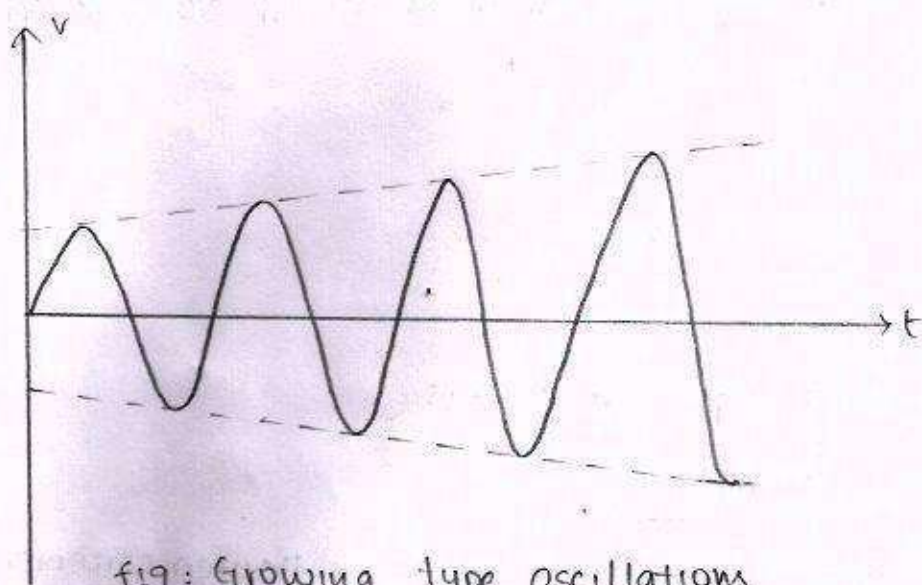


fig: Growing type oscillations

(iii) $|A\beta| = 1$:

When the total phase shift around a loop is 0° or 360° & $|A\beta| = 1$, then the oscillations are with constant frequency & amplitude, it is called as sustained oscillations. It is shown in below fig.

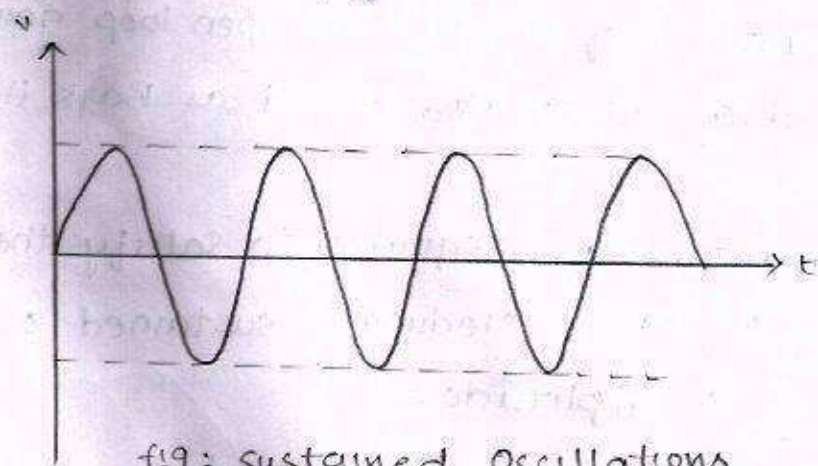


fig: sustained Oscillations

(iii) $|A\beta| < 1$:

When the total phase shift around a loop is 0° or 360° & $|A\beta| < 1$ then the oscillations are decaying type i.e., the amplitude of the oscillations decreases exponentially. It is shown in below fig.

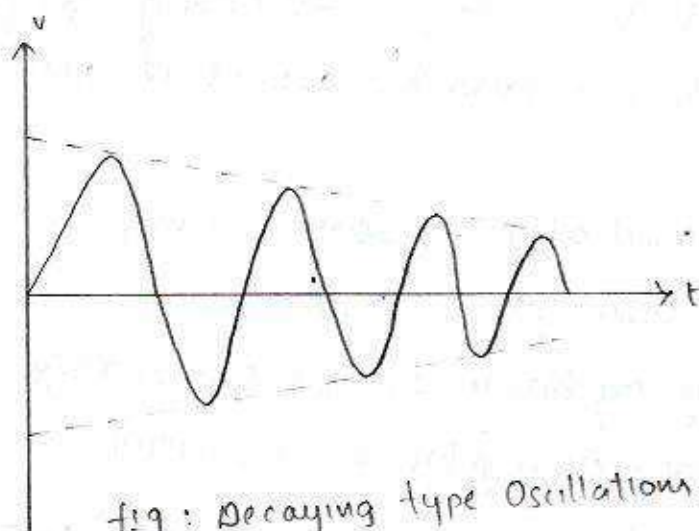


fig: Decaying type Oscillations:

Classification of Oscillations:

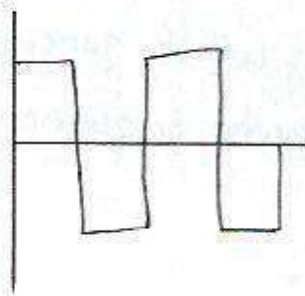
Oscillators are classified into different ways

- (1) According to waveform
- (2) According to frequency range
- (3) According to RLC components.

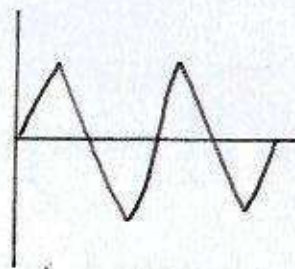
(1) **According to waveform:** According to waveform the oscillator can be classified into 2 types.

(a) **sinusoidal oscillator:** A sinusoidal oscillator generates the sinusoidal signals only.

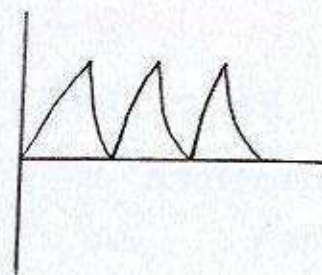
(b) **Non-sinusoidal oscillator:** it generates the non-sinusoidal signals like square, triangular & sawtooth.



Square wave form



Triangular wave form



Sawtooth wave form

(2) According to frequency range : According to frequency range the oscillator can also be classified into different types.

(a) Audio frequency oscillator :- $20\text{ Hz} - 20\text{ kHz}$

(b) Radio frequency oscillator :- $> 20\text{ kHz}$

(c) Very high frequency oscillator :- $30\text{ MHz} - 300\text{ MHz}$

(d) Micro wave frequency oscillator :- $> 300\text{ MHz}$

(3) According to RLC components : According to RLC components the oscillator can be classified into different ways.

(a) RC oscillators : The oscillator using the components R & C are called as RC oscillators. It can be used to generate the low frequency signals in audio range.

(b) LC oscillators : The oscillator using the components L & C are called as LC oscillators. It can be used to generate the high frequency signals.

(c) Crystal Oscillators : The oscillator using the crystal is called as crystal oscillator. It can be used to generate the very high frequency signals.

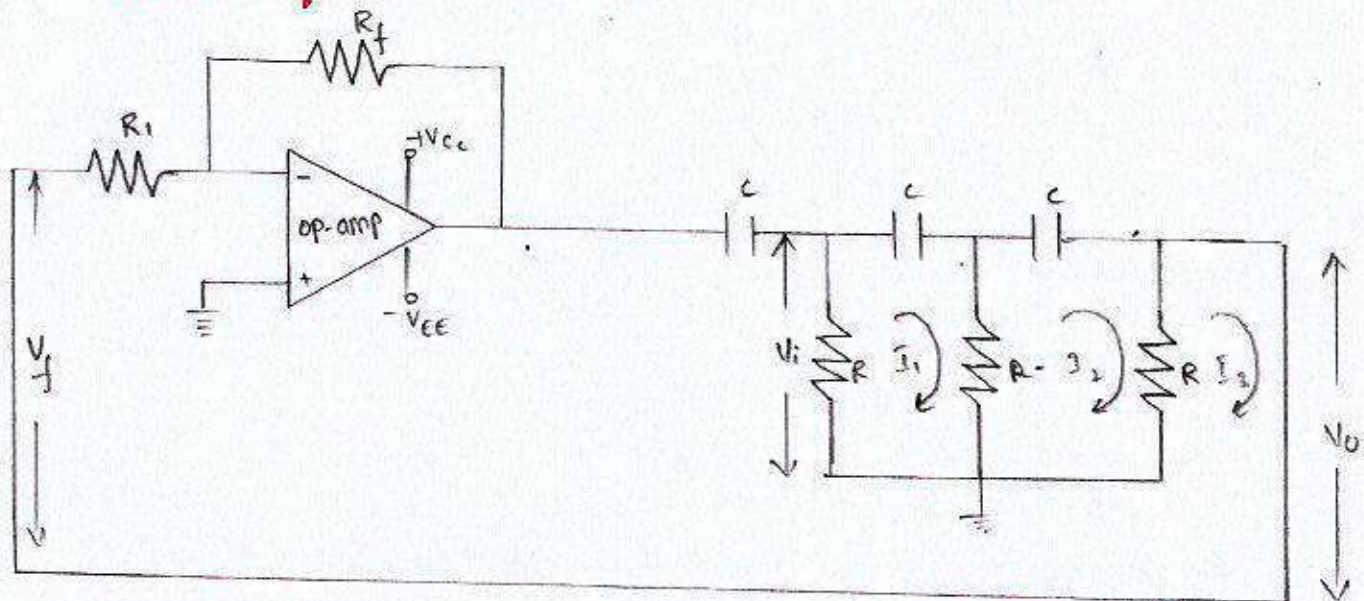
RC Oscillator :

RC oscillator is a one type of oscillator which generates oscillations in the low frequency range (audio frequency range).

→ RC oscillators can be classified into 2 types.

1. RC phase shift oscillator
2. Wein bridge oscillator

RC Phase Shift Oscillator :



- It consists of CE amplifier followed by a 3 sections of RC phase shift network. In the RC phase shift n/w RC oscillator can be used as a feedback path.
- In oscillator, amplifier produces 180° phase shift & feedback must introduced 180° phase shift to obtain a total phase shift around a loop is 360° .
- One RC network produces phase shift of $\phi = 60^\circ$.
- Here 3 RC networks are available to produce phase shift is 180° ($60^\circ + 60^\circ + 60^\circ$). The feedback network is also called as ladder network.
- In this network all the resistances & capacitances values are same. so that for a particular frequency each section of RC produces a phase shift is 60° . The o/p of RC phase shift n/w is connected to the input of CE amplifier through RC feedback network.
- To make 3 RC sections are identical (similar), R_3 should be choosen as

$$R_1^l = R_1 + R_3$$

$$R_1 = R_1^l - R_3$$

$$R_3 = R_1^l - R_1$$

→ The phase shift ϕ produced by the RC section is

$$\phi = \tan^{-1} \left[\frac{1}{\omega RC} \right]$$

$$= \tan^{-1} \left[\frac{1}{2\pi f RC} \right]$$

Let us assume $R = 1K\Omega$, $C = 0.1\mu F$, $F = 1KHz$

$$\phi = \tan^{-1} \left[\frac{1}{2\pi \times 1 \times 10^3 \times 1 \times 10^3 \times 0.1 \times 10^{-6}} \right]$$

$$\phi = 57.85 \approx 60^\circ$$

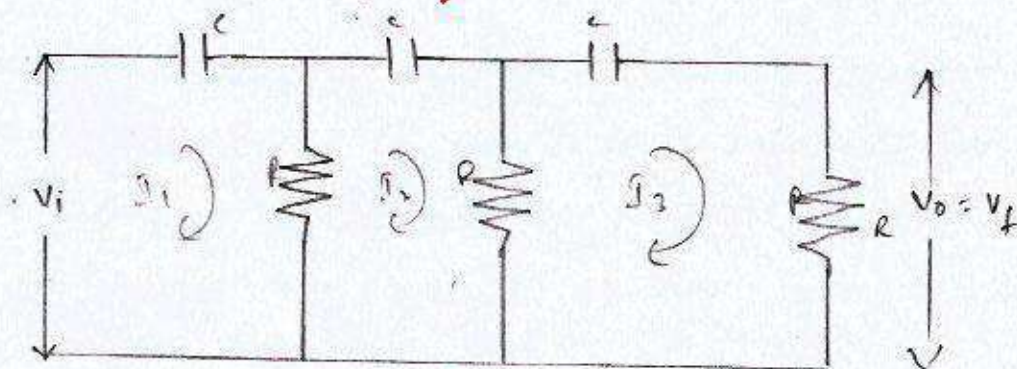
→ If all the resistors & capacitors are same in 3 sections then each section can produce a phase shift of 60° . So, the ladder network produce 180° phase shift in between o/p & i/p voltages.

→ The total phase shift from the base of the op-amp around the circuit will be exactly 360° . So there by satisfying Barkhausen Criterion for Oscillations.

→ The frequency generated by the RC phase shift oscillator is

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

Derivation for frequency of Oscillations:



Apply KVL for 1st, 2nd and 3rd loop

$$\text{loop (I)} :- V_i = I_1 \left(\frac{1}{j\omega C} \right) + R(I_1 - I_2)$$

$$= I_1 \left[\frac{1}{j\omega C} + R \right] - R I_2 \rightarrow (1)$$

loop (2): $0 = I_2 \left(\frac{1}{j\omega C} \right) + R(I_2 - I_1) + R(I_2 - I_3)$

$$= I_2 \left(\frac{1}{j\omega C} + 2R \right) - R I_1 - R I_3$$

$$0 = -R I_1 + I_2 \left(\frac{1}{j\omega C} + 2R \right) - R I_3 \rightarrow (2)$$

loop (3): $V_0 = I_3 \left(\frac{1}{j\omega C} \right) + R(I_3 - I_2) + R I_3$

$$= I_3 \left(\frac{1}{j\omega C} + 2R \right) - R I_2$$

$$V_0 = -R I_2 + I_3 \left(\frac{1}{j\omega C} + 2R \right) \rightarrow (3)$$

By solving the 3 eqns, we get

$$I_3 = \frac{V_i}{R} \left[\frac{1}{(1-5\alpha^2) + j\alpha(\alpha^2-6)} \right]$$

$$\alpha = \frac{1}{\omega RC} \quad (\text{or}) \quad \alpha = \frac{1}{2\pi f RC}$$

W.K.T ; $V_0 = I_3 R$

$$V_0 = V_i \left[\frac{1}{(1-5\alpha^2) + j\alpha(\alpha^2-6)} \right]$$

for determining the frequency of an oscillator the imaginary part must be equal to zero

$$\text{i.e., } \alpha(\alpha^2-6) = 0$$

$$\alpha^2 - 6 = 0$$

$$\alpha^2 = 6$$

$$\alpha = \pm \sqrt{6}$$

W.K.T, $\alpha = \frac{1}{\omega RC}$

$$\frac{1}{\omega RC} = \sqrt{6}$$

$$\frac{1}{2\pi f RC} = \sqrt{6}$$

$$f = \frac{1}{2\pi f RC \sqrt{6}}$$

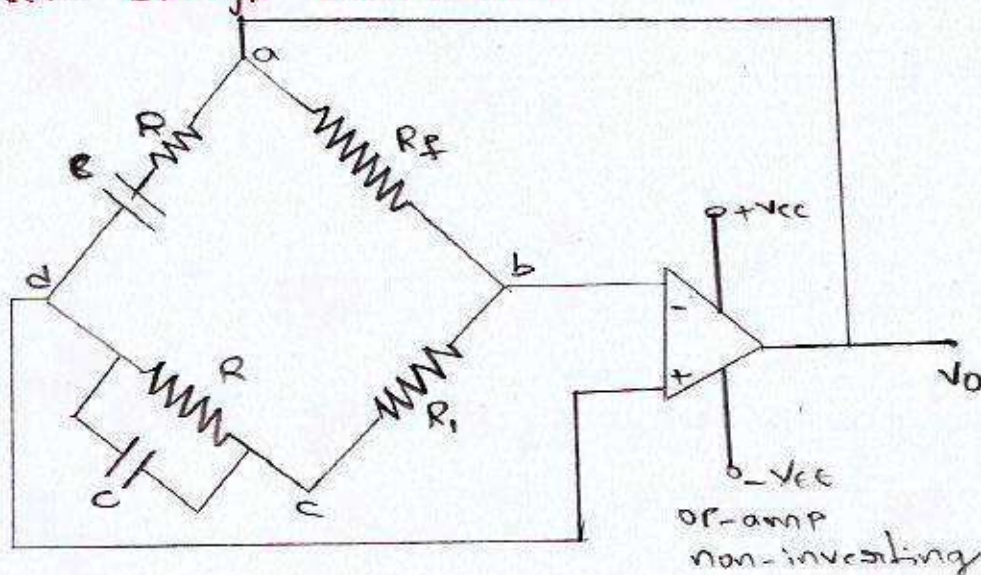
Advantages :

1. The circuit is simple to design.
2. It is suitable to produce o/p waveform for audio frequencies only.
3. It produces sinusoidal o/p voltages.
4. It is able to generate the low frequency signals.

Disadvantages :

1. By changing the values of R & C , the frequency of oscillator can be changed.
2. It is unable to generate the high frequency signals.

(2) Wein Bridge Oscillator :



- Generally in an oscillator the amplifier stages introduces 180° phase shift and feed back network introduces another 180° phase shift. To obtain a phase shift of 360° around a loop.
- But wein-bridge oscillator consist of non-inverting amplifier & hence does not provide any phase shift during amplifier stage.
- As the total phase shift required is 360° in wein bridge, because no phase shift is necessary.
- The o/p of amplifier is connected b/w terminals a & c which is i/p.

→ While the amplifier i/p is connected b/w terminals b & d which is o/p.

→ The bridge n/w consists of 2 arms namely $R_1 C_1$ in series & $R_2 C_2$ in parallel. These arms are called frequency sensitive arms which decides the frequency.

→ The frequency of wein bridge oscillator

$$f = \frac{1}{2\pi RC}$$

→ This is also called as lead lag n/w because at low frequency signals the voltage leads current.

$$Z_1 = R_1 + \frac{1}{j\omega C_1}$$

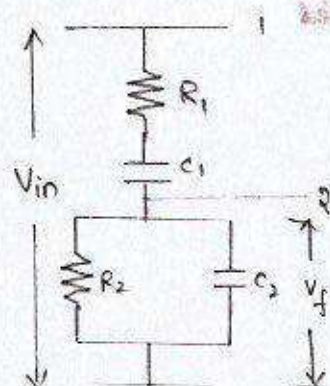
$$= \frac{j\omega R_1 C_1 + 1}{j\omega C_1}$$

$$Z_2 = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}}$$

$$= \frac{R_2 / j\omega C_2}{\frac{j\omega C_2 R_2 + 1}{j\omega C_2}}$$

$$= \frac{R_2}{1 + j\omega C_2 R_2}$$

$$Z_1 = \frac{1 + sR_1 C_1}{sC_1}, \quad Z_2 = \frac{R_2}{1 + sC_2 R_2}$$



From fig. $I = \frac{V_{in}}{Z_1 + Z_2}$ i.e., $V_f = I \times Z_2$

$$V_f = \frac{V_{in} \times Z_2}{Z_1 + Z_2}$$

We know that, $\beta = \frac{V_f}{V_{in}}$

$$= \frac{V_{in} \times Z_2}{Z_1 + Z_2}$$

$$= \frac{Z_2}{Z_1 + Z_2}$$

$$\beta = \frac{SC_1 R_2}{1 + SC_1 R_1 (1 + SC_2 R_2) + SC_1 R_2}$$

$$= \frac{SC_1 R_2}{1 + SC_2 R_2 + SC_1 R_1 + S^2 C_1 R_1 C_2 R_2 + SC_1 R_2}$$

$$= \frac{SC_1 R_2}{1 + S(C_2 R_2 + C_1 R_1 + C_1 R_2) + S^2 C_1 C_2 R_1 R_2}$$

$$= \frac{j\omega C_1 R_2}{1 + j\omega(C_2 R_2 + C_1 R_1 + C_1 R_2) - \omega^2 C_1 C_2 R_1 R_2}$$

$$= \frac{R_2 / SC_2 R_2 + 1}{(1 + SC_1 R_1)(1 + SC_2 R_2) + R_2 SC_1}$$

$$= \frac{SC_1(1 + SC_2 R_2)}{SC_1(1 + SC_2 R_2)}$$

$$= \frac{R_2 SC_1}{(1 + SC_1 R_1)(1 + SC_2 R_2) + R_2 SC_1}$$

$$= \frac{SC_1 R_2}{1 + S(R_1 C_1 + R_2 C_2) + S^2 R_1 R_2 C_1 C_2 + SC_1 R_2}$$

$$\beta = \frac{j\omega C_1 R_2}{1 + j\omega(R_1 C_1 + R_2 C_2) - \omega^2 R_1 R_2 C_1 C_2 + j\omega C_1 R_2}$$

$$= \frac{j\omega C_1 R_2}{j\omega(R_1 C_1 + R_2 C_2 + C_1 R_2) - (\omega^2 R_1 R_2 C_1 C_2 - 1)}$$

Rationalising with expression

Then

$$\beta = \frac{\omega^2 C_1 R_2 (R_1 C_1 + R_2 C_2 + C_1 R_2) + j\omega C_1 R_2 (1 - \omega^2 R_1 R_2 C_1 C_2)}{(1 - \omega^2 R_1 R_2 C_1 C_2) + \omega^2 (R_1 C_1 + R_2 C_2 + R_2 C_1)}$$

$$\Rightarrow \omega (1 - \omega^2 R_1 R_2 C_1 C_2) = 0$$

$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\text{let } R_1 = R_2 = R$$

$$C_1 = C_2 = C$$

$$\omega^2 = \frac{1}{RC}$$

$$2\pi f = \frac{1}{RC}$$

$$f = \frac{1}{2\pi RC}$$

$$\text{Here } \beta = 1/3$$

$$|A| \times 1/3 \geq 1$$

$$|A| \geq 3$$

Without any phase shift, gain of amplifier

Advantages:

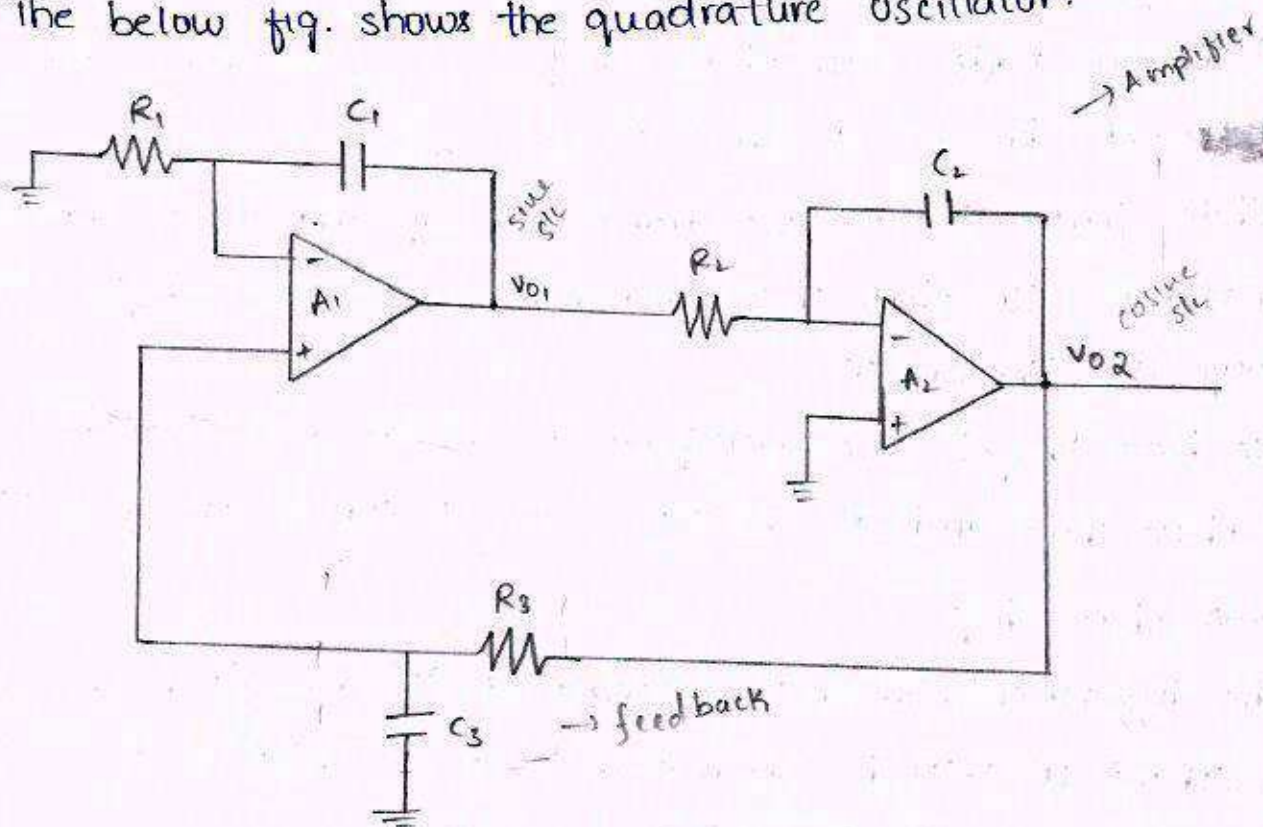
1. Different frequency ranges can be obtained by varying the capacitor values.
2. Perfect sine wave is possible.
3. It is useful for audio frequency range.

Disadvantages :

1. Poor frequency stability

Quadrature Type Oscillator:

- If the phase shift b/w the two signals is exactly 90° then it is called as quadrature.
- But the 2 signals having same frequency.
- For example, sine & cosine signals are said to be in quadrature.
- Thus oscillator which generates the ² signals sine & cosine which are in quadrature is called quadrature oscillator.
- The below fig. shows the quadrature oscillator.



- It consists of two op-amps which is called amplifier circuit and one feed back n/w.
- Let one op-amp is A_1 and other op-amp is A_2 .
- It is required to operate A_1 as an non-inverting integrator while A_2 as pure inverting integrator.
- Thus $R_1 C_1$ combination is used for op-amp A_1 and $R_2 C_2$ is used for op-amp A_2 .
- The o/p of op-amp A_2 is connected to feed back n/w ($R_3 C_3$)

and voltage across C_3 is given as feedback to the non-inverting i/p of A_1 .

→ The op-amp A_1 & A_2 forms amplifier stage of the oscillator while R_3C_3 forms a feedback stage of the oscillator.

Operation :

1. Here op-amp A_2 is an inverting integrator. Due to inverting nature it adds -180° phase shift & due to integrating nature it adds -90° phase shift. So total phase shift introduced due to op-amp A_2 is -270° .
2. While feedback n/w R_3C_3 along with op-amp A_1 contributes remaining -90° phase shift and hence total phase shift around a loop is -360° (or) 0° .
3. We have to get sine waveform at the o/p of A_1 which is 360° phase shift and at the o/p of A_2 is cosine waveform which is -270° phase shift.
4. The difference b/w these 2 signals is 90° phase shift. Hence this circuit is called Quadrature type oscillator. Due to this it satisfies the Barkhausen conditions.
5. The frequency f_o produces sine & cosine waveforms is given by

$$f = \frac{1}{2\pi RC}$$

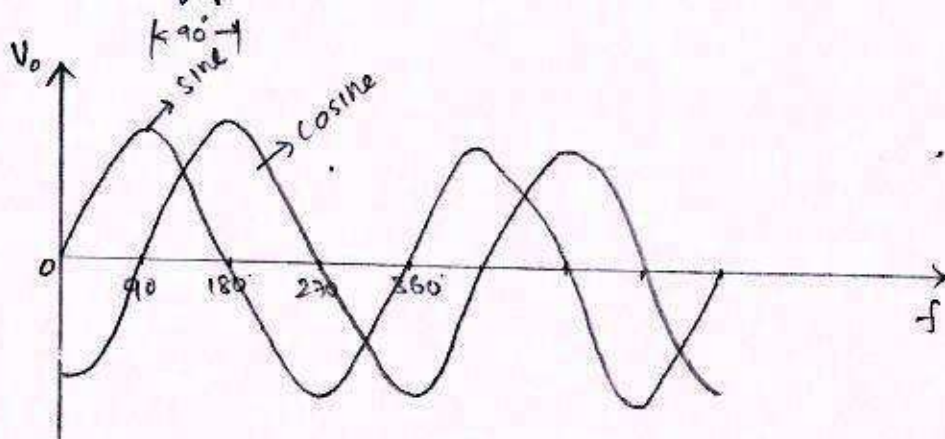
where, $R = R_1 = R_2 = R_3$

$C = C_1 = C_2 = C_3$

Applications :

→ Communication Circuits

→ The corresponding waveforms of quadrature type oscillator is shown in below fig.



Waveform Generators :

→ Generator is a circuit which generates the different types of sinusoidal & non-sinusoidal signals.

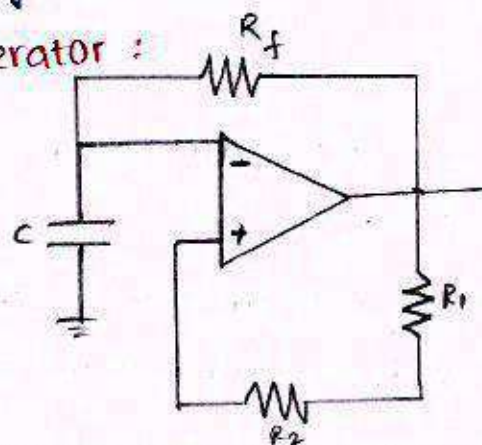
→ If circuit generates the sinusoidal signals then it is called as sinusoidal generator.

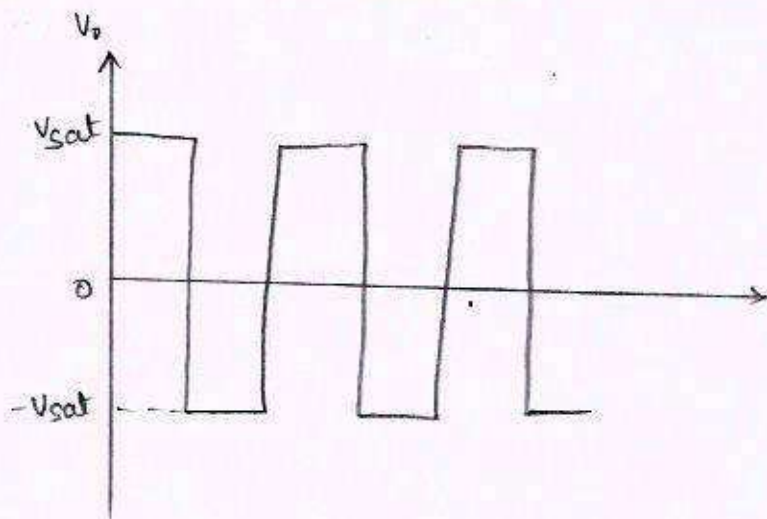
→ If the circuit generates non-sinusoidal signals (square, triangle, sawtooth) then it is called as non-sinusoidal waveform generators.

→ According to definition of non-sinusoidal waveform generators there are different types of generators.

1. Square wave generator
2. Triangular wave generator
3. Sawtooth wave generator

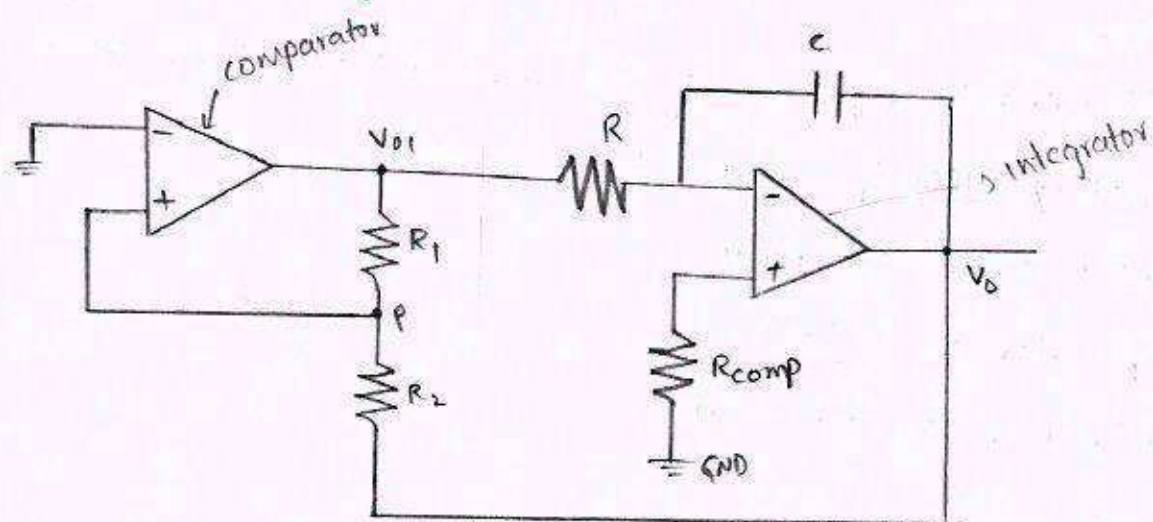
1. Square Wave generator :





- To understand the operation of circuit $+V_{sat}$ is available at the o/p. Due to this the capacitor gets charging.
- The same voltage ($+V_{sat}$) flows through the potential divider n/w due to this some voltage dropped. The dropping voltage appeared at the non-inverting terminal of the comparator.
- If compare the non-inverting voltage than the inverting voltage which is low. So the comparator can change from $+V_{sat}$ to $-V_{sat}$.

R. Triangular Wave generator :



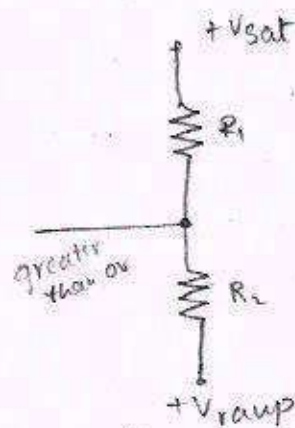
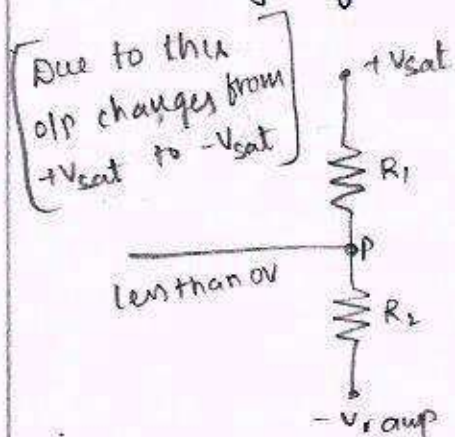
- Generally integrator o/p waveform will be triangular if the i/p to it is a square wave. So, the
- So, the triangular wave generator can be implemented by cascading an integrator and a square wave generator. It is shown

in above fig.

→ It consists of two op-amps. First op-amp acts as comparator & second op-amp acts as integrator.

Operation:

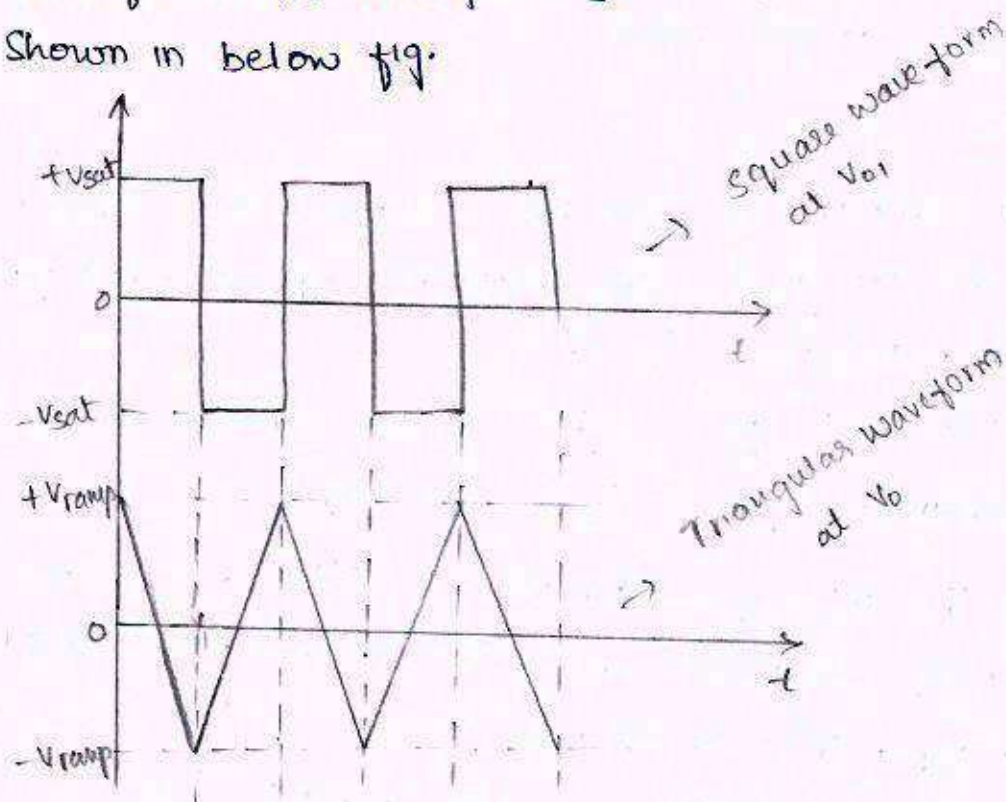
1. The comparator compares the voltage at a point 'P' continuously with respect to the voltage at the inverting i/p of comparator, which is at ground potential (0V).
2. When the voltage at 'P' goes slightly below 0V, the o/p of comparator will change from $+V_{sat}$ to $-V_{sat}$.
3. Let us consider the o/p of comparator is $+V_{sat}$, since this voltage is the i/p of integrator then its o/p will be $(-V_{ramp})$ negative going ramp. Thus one end of the potential divider R_1, R_2 is at $+V_{sat}$ & other end is at -ve going ramp $(-V_{ramp})$.
4. When the -ve going ramp attains a value say $-V_{ramp}$ the effective voltage at P becomes slightly less than 0V. Then o/p will change from $+V_{sat}$ to $-V_{sat}$.



Due to this o/p changes from $-V_{sat}$ to $+V_{sat}$.

5. During this time integrating o/p will be +ve going ramp. When the value of +ve going ramp attains $+V_{ramp}$, voltage at 'P' becomes slightly greater than 0V. Due to this o/p of comparator changes from $-V_{sat}$ to $+V_{sat}$ which is shown in fig (ii)

6. This cycle repeats continuously and generates triangular wave forms. The corresponding triangular waveform generator shown in below fig.



Sawtooth Wave generator :

- Sawtooth wave form is a type of linear non-sinusoidal waveform with a triangular shape in which the raise & fall time are different.
- A ~~pure~~ pure triangular waveform is also linear non-sinusoidal with a triangular shape but it has equal raise & fall time.
- The sawtooth wave form & triangular waveform graphical representation shown in below fig. Here T_1 is the rise & T_2 is the fall time.

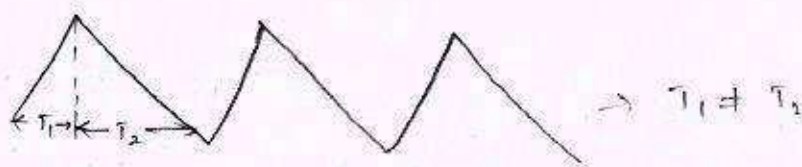


fig: sawtooth wave form

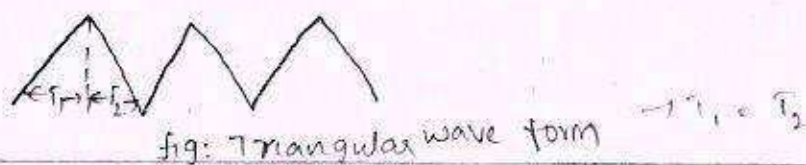
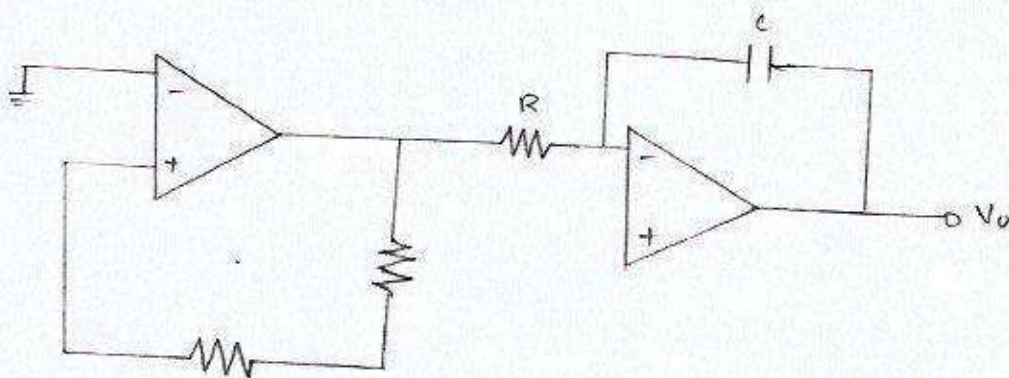


fig: Triangular wave form

→ The sawtooth generator can be designed by doing little modifications in the triangular wave generator circuit.

→ In this circuit, the non-inverting terminal of op-amp is grounded, to get sawtooth generate we just need to add a potentiometer & variable resistor at the non-inverting terminal of 2nd op-amp.



→ The circuit consists of comparator, integrator & potentiometer.

→ The potentiometer is used to set the raising time & falling time at the op of integrator.

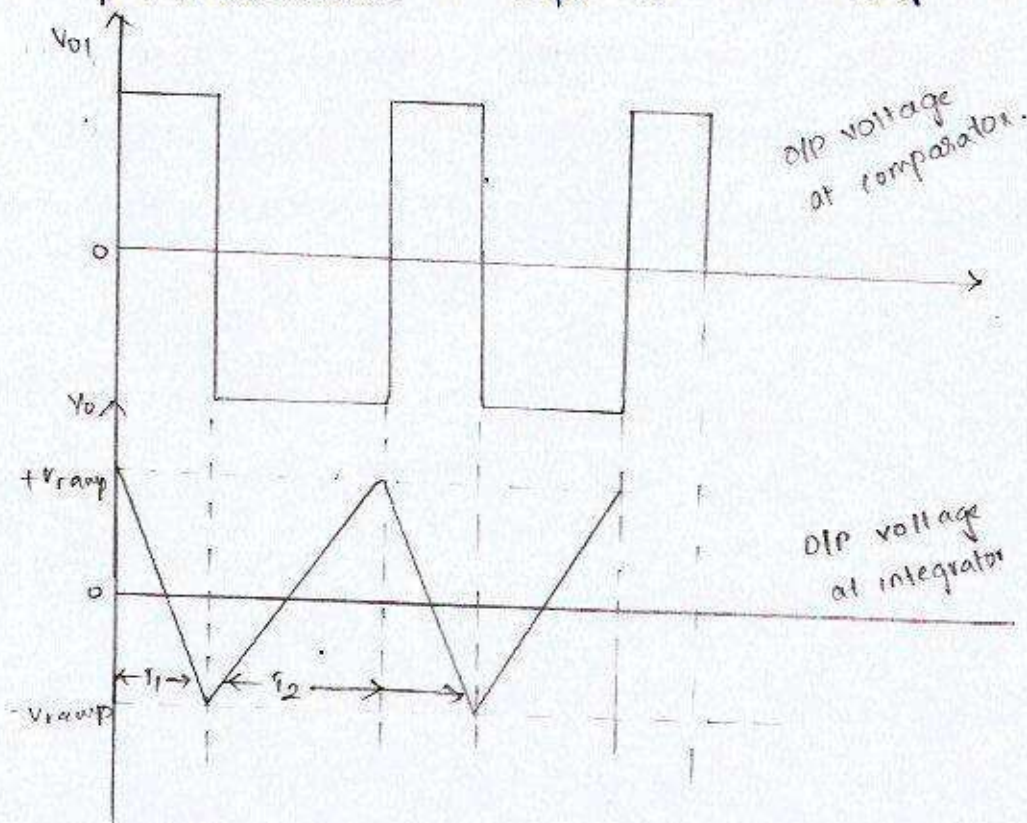
→ If the potentiometer moves towards -ve supply ($-V_{EE}$), the raise time of the sawtooth becomes larger than the fall time because when potentiometer kept at the -ve supply voltage, the -ve voltage adds at the inverting terminal of op-amp (2).

→ Due to that, the fall time suddenly downs than the raise time.

→ When the potentiometer moves towards +ve supply ($+V_{CC}$), the fall time becomes larger than the raise time because when potentiometer kept at the +ve supply voltage, the +ve voltage adds at the investing terminal of 2nd op-amp.

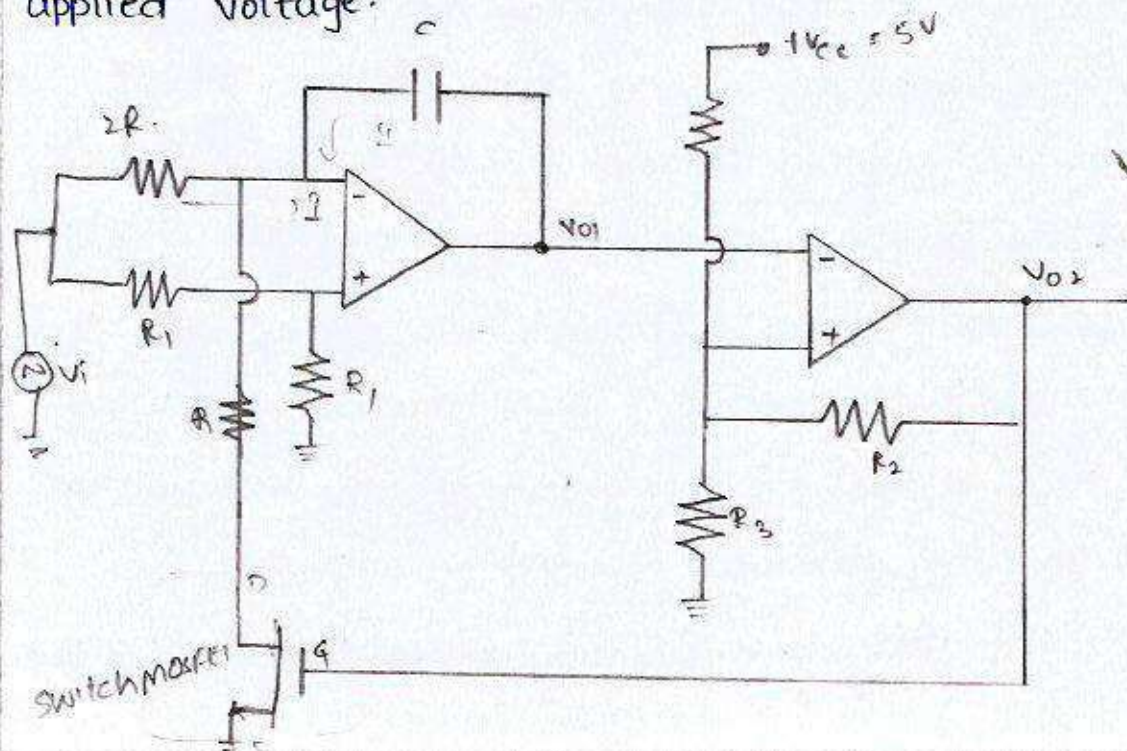
→ Due to that, the raise time suddenly raises than the fall time.

→ The corresponding sawtooth wave generator is shown below when potentiometer is kept at -ve supply voltage.



VCO:

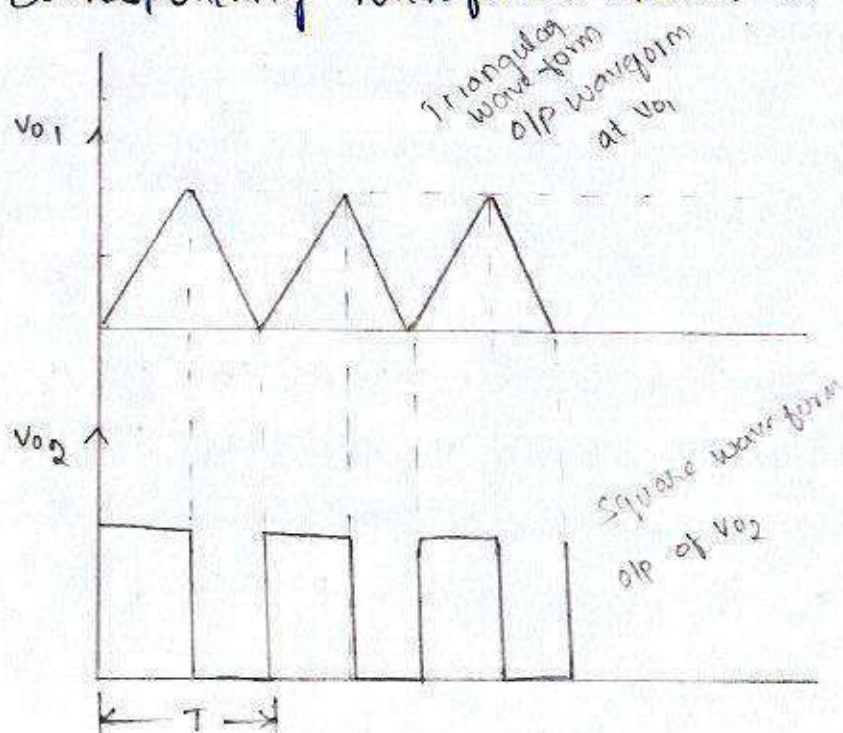
→ VCO is a voltage controlled oscillator. VCO is a circuit in which frequency of oscillations can be controlled by an externally applied voltage.



- VCO provides the linear relationship b/w the applied voltage and the oscillator frequency.
- Here applied voltage is called as control voltage.
- Practically vco is used to produce square & triangular waveforms whose frequency is controlled by control voltage.
- VCO oscillator circuit is shown in above fig.
- It consists of two op-amps & one MOSFET switch.
- First Op-amp can be acts as an integrator and other one acts as a comparator.
- MOSFET can be acts as a switch which is connected b/w the o/p of comparator & i/p of integrator.
- Here comparator o/p is square wave & integrator o/p is triangular waveform.
- For getting triangular & square waveform, capacitor must charge & discharge. So current I direction through capacitor must keep on alternating.
- The direction of current I through the capacitor is controlled by the MOSFET switch.
- But ON & OFF MOSFET switch is controlled by the o/p of comparator. i.e., when o/p of comparator is high, switch is going to ON & o/p of comparator is low, switch is going to OFF.
- To understand the operation let us assume the o/p of comparator is low. Therefore switch is OFF. Hence entire current I has to pass through the capacitor 'C' & the voltage v_{o1} starts to decreasing due to polarity of voltage across the capacitor.

Hence V_{O1} ramps down.

- When V_{O1} becomes zero, then comparator changes its state & o/p V_{O2} becomes high.
- Due to this, switch becomes ON & the resistance R gets connected to the ground. So now the total current $2I$ i.e., one current I supplied by input & remaining current I must supplied by capacitor flows through the ground.
- Thus the direction of current through the capacitor gets reversed. Therefore V_{O1} voltage starts ramping up i.e., starts increasing.
- It may be noted that capacitor current I gets maintained at same magnitude only its direction reversed. Therefore triangular waveform available at V_{O1} .
- As soon as V_{O1} reaches the level of V_{O2} , the comparator changes its state making switch is off.
- Thus the current I through the capacitor again reverse its direction & V_{O1} ramps down. Thus the cycle continuous.
- Corresponding waveforms shown in below fig.



555 TIMER AND PHASE LOCKED LOOPS (PLLs)

<u>Syllabus Contents:</u>
Active Filters: Introduction, Butterworth Filters – 1 st order, 2 nd order Low pass and High Pass Filters, Band Pass, Band Reject and All Pass Filters.
Timer and Phase Locked Loops (PLLs): Introduction to IC 555 Timer, description of functional diagram, monostable and astable operations and applications, Schmitt Trigger, PLL-Introduction, basic principle, Phase detector/Comparator, Voltage controlled oscillator (IC 566).

ACTIVE FILTERS

Electrical Filter:

An Electrical Filter is a circuit that passes signals of specified frequencies and attenuates (rejects) signals of frequencies outside this band. Based on processing techniques, electrical filters are classified as analog filters and digital filters. Based on the type of elements used analog filters are classified as passive and active filters.

Passive Filters: (RC filters and LC filters)

They use passive components (R, L and C). LC filters (also called crystal filters) have high quality factor 'Q'. So, they produce stable operation at high frequencies.

LC filters are not preferred at audio and low frequencies. It is because

- Inductors are bulky (large in size and heavy)
- They are costly.
- Stray magnetic fields are present due to magnetic coupling.

Thus, **RC filters** are used at audio and low frequencies.

Active Filters: They use opamps, resistors and capacitors. Here opamps are active components and R & C are passive components.

Advantages of active filters over passive filters:

- Opamps provide large gain. So, i/p signal is not attenuated as in passive filters.
- Opamps provide high i/p impedance and low o/p impedance. So, they do not cause loading of source and load.

- Because of high i/p impedance, we can use large resistor values. This reduces the need to use large capacitor values. (Large capacitors are bulky and costly).
- Opamps are less expensive and inductors are absent in active filters. So, they are more economical than passive filters.
- Active filters are easier to tune and adjust.

Disadvantages of active filters over passive filters:

- ✓ Opamps need two power supplies
- ✓ High frequency response of active filters is limited by the slew rate of the opamp.
- ✓ High frequency opamps are costly.
- ✓ There is a problem of oscillations in multi stage amplifiers.
- ✓ Since active filters use active devices, they are more susceptible to RF interference.
- ✓ In band pass filters and notch filters, practical considerations limit the value of Q factor to 50.

Types of Active Filters:

1. Low Pass Filters (LPFs):

They allow low frequency signals and attenuate high frequency signals $>$ a cutoff frequency of f_h .

2. High Pass Filters (HPFs):

They allow high frequency signals and attenuate low frequency signals $<$ a cutoff frequency of f_l .

3. Band Pass Filters (BPFs):

They allow a specified range of frequencies and reject frequencies outside this range.

4. Band Reject Filters (BRFs):

They attenuate a particular range of frequencies and allow frequency components outside this range.

Frequency Response of Active Filters:

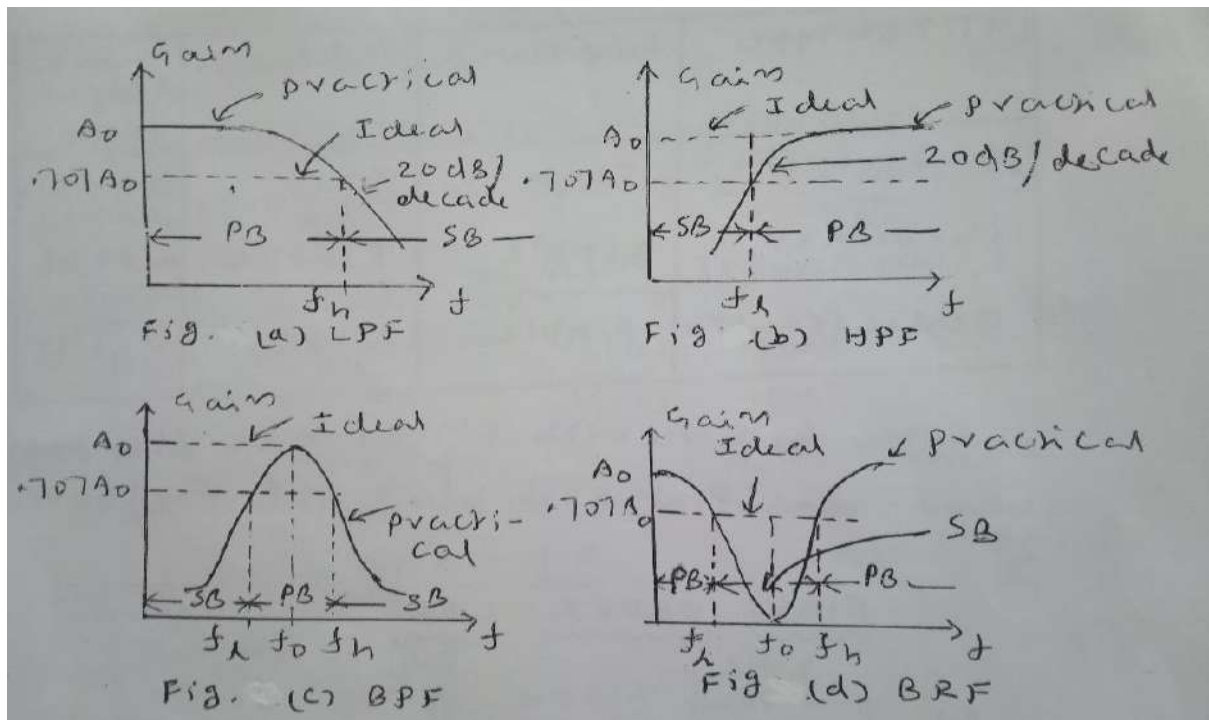


Fig. 1: Frequency Response of Active Filters

Fig. 1 represents the frequency response of the 4 types of active filters. Here frequency (in Hz) is taken on X-axis and gain is taken on Y-axis. Log scale is used for X-axis and linear scale is used for Y-axis.

Based on the design of filters, analog active filters are classified as Butterworth filters, Chebyshev filters and Bessel (Cauer) filters. This classification depends on the Transfer function.

Comparison of filters:

Filter Type	Pass Band	Stop Band	Damping factor
Butterworth	Flat	Flat	$\alpha = 1.44$
Chebyshev	Ripple	Flat	$\alpha = 1.06$
Bessel	Ripple	Ripple	$\alpha = 1.73$

Since Butterworth filter has flat pass band and flat stop band, it is preferred much.

First Order LPF

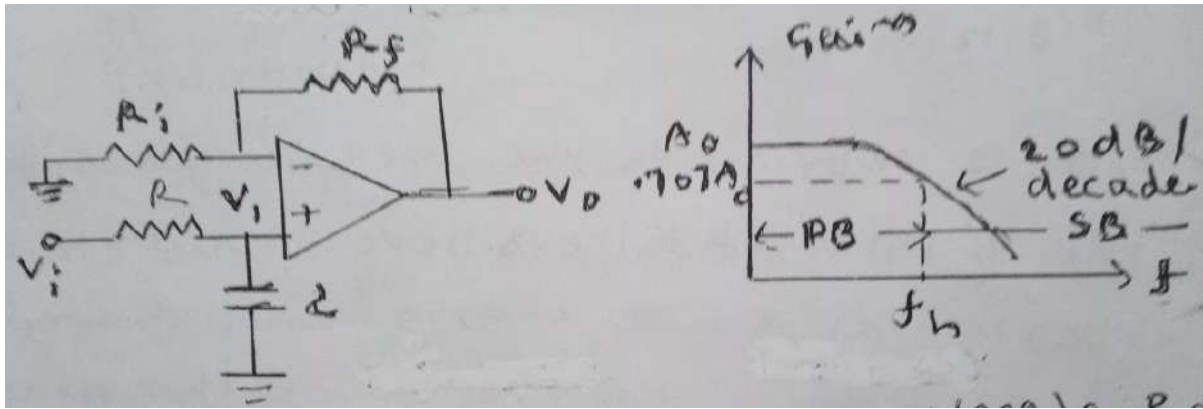


Fig. 2 (a): First Order LPF

Fig. 2(b) Frequency response

A First Order LPF has a single RC network connected to the non-inverting terminal of opamp as shown in Fig. 2(a). Here v_i is the input voltage and v_o is the output.

Here R_i and R_f determine the gain of the filter.

Let v_1 be the voltage at the (+) input terminal of opamp.

$$\therefore v_1(s) = v_i(s) \cdot \frac{\frac{1}{sC}}{R + \frac{1}{sC}} = v_i(s) \cdot \frac{1}{1 + sRC}$$

$$\text{i.e., } \frac{v_1(s)}{v_i(s)} = \frac{1}{1 + sRC} \quad \dots\dots\dots (1)$$

where $v(s)$ is the Laplace Transform of 'v' in time domain.

$$\text{Closed loop gain of opamp} = \frac{v_o(s)}{v_1(s)} = 1 + \frac{R_f}{R_i} \quad \dots\dots\dots (2)$$

Overall Transfer Function is given by

$$\begin{aligned} H(s) &= \frac{v_o(s)}{v_i(s)} = \frac{v_o(s)}{v_1(s)} \cdot \frac{v_1(s)}{v_i(s)} \\ &= \left(1 + \frac{R_f}{R_i}\right) \frac{1}{1 + sRC} \quad \{\text{using eqs. (1) and (2)}\} \\ &= \frac{A_o}{1 + sRC} \quad \text{Where } A_o = 1 + \frac{R_f}{R_i} \quad \dots\dots\dots (3) \end{aligned}$$

Standard form of Transfer Function:

$$\text{Let } \omega_h = \frac{1}{RC}$$

Then from eq. (3), we can write

$$H(s) = \frac{A_o}{1 + sRC} = \frac{A_o}{1 + \frac{s}{\omega_h}} = \frac{A_o \omega_h}{s + \omega_h} \quad \dots\dots\dots (4)$$

Frequency Response:

To determine the frequency response put $s = j\omega$ in eq. (3). Then we get

$$\begin{aligned} H(j\omega) &= \frac{A_o}{1 + j\omega RC} \\ &= \frac{A_o}{1 + j2\pi f RC} \\ &= \frac{A_o}{1 + jf / (1/2\pi RC)} \\ &= \frac{A_o}{1 + jf / f_h} \quad \dots\dots (5) \end{aligned}$$

Where $f_h = \frac{1}{2\pi RC}$ or $\omega_h = \frac{1}{RC}$

Consider eq. (5).

$$\text{When } f \ll f_h, \quad |H(j\omega)| = \frac{A_o}{1 + 0} = A_o$$

$$\text{When } f = f_h, \quad |H(j\omega)| = \frac{A_o}{\sqrt{1^2 + 1^2}} = \frac{A_o}{\sqrt{2}}$$

$$\text{When } f \gg f_h, \quad |H(j\omega)| = \frac{A_o}{1 + \infty} = 0$$

Fig. 2 (b) shows the frequency response of first order LPF.

Important observations in Fig. 2(b):

- i. Maximum gain is A_o at $f = 0$ Hz.
- ii. At f_h , gain falls by $,707A_o$ (or -3 dB below A_o when A_o is expressed in dB).
- iii. Frequency response from 0 to f_h is called pass band.
- iv. When $f > f_h$, gain decreases at a rate of 20 dB/decade.
- v. Range of frequencies where $f > f_h$ is called stop band

FIRST ORDER HPF

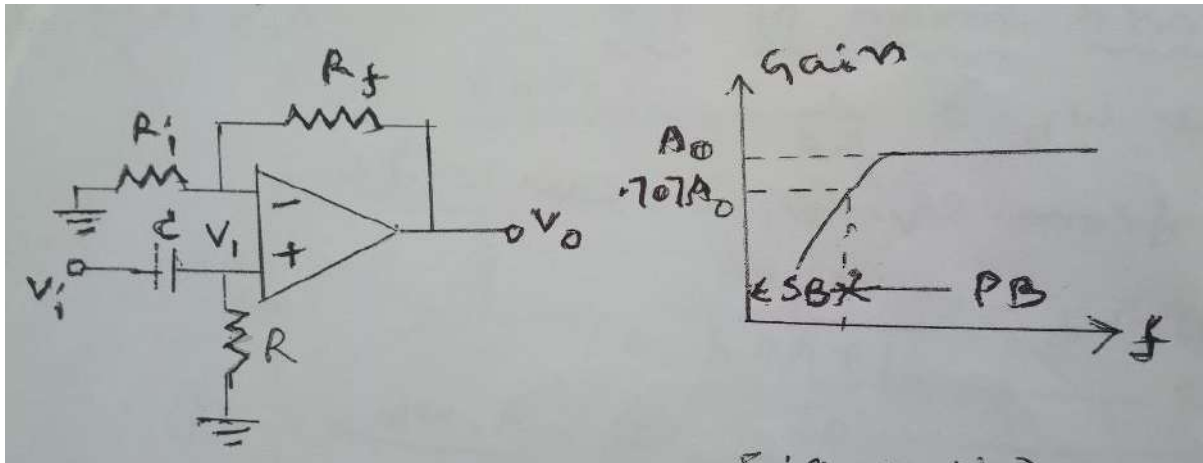


Fig. 3 (a): First Order HPF

Fig. 3 (b) Frequency response

A first order HPF has a single RC network connected to the non-inverting terminal of opamp as shown in Fig. 3 (a). Note that, by interchanging the positions of R and C of a first order LPF, we will get a first order HPF.

Let the minimum frequency allowed by this filter is f_l .

Here R_i and R_f determine the gain of the filter.

Let v_1 be the voltage at the (+) input terminal of opamp.

$$\therefore v_1(s) = v_i(s) \cdot \frac{R}{R + \frac{1}{sC}} = v_i(s) \cdot \frac{sRC}{1 + sRC}$$

$$\text{i.e., } \frac{v_1(s)}{v_i(s)} = \frac{sRC}{1 + sRC} \quad \dots\dots\dots (1)$$

where $v(s)$ is the Laplace Transform of 'v' in time domain.

$$\text{Closed loop gain of opamp} = \frac{v_o(s)}{v_1(s)} = 1 + \frac{R_f}{R_i} \quad \dots\dots\dots (2)$$

Overall Transfer Function is given by

$$\begin{aligned} H(s) &= \frac{v_o(s)}{v_i(s)} = \frac{v_o(s)}{v_1(s)} \cdot \frac{v_1(s)}{v_i(s)} \\ &= \left(1 + \frac{R_f}{R_i}\right) \frac{sRC}{1 + sRC} \quad \{\text{using eqs. (1) and (2)}\} \\ &= \frac{sA_oRC}{1 + sRC} \quad \dots\dots\dots (3) \end{aligned}$$

$$\text{Where } A_o = 1 + \frac{R_f}{R_i}$$

Standard form of Transfer Function:

$$\text{Let } \omega_l = \frac{1}{RC}$$

Then from eq. (3), we can write

$$H(s) = \frac{sA_oRC}{1+sRC} = \frac{\frac{sA_o}{\omega_l}}{\frac{s}{\omega_l}+1} = \frac{A_o s}{s+\omega_l} \dots\dots\dots (4)$$

Frequency Response:

To determine the frequency response put $s = j\omega$ in eq. (3). Then we get

$$\begin{aligned} H(j\omega) &= \frac{A_o}{1+\frac{1}{sRC}} \\ &= \frac{A_o}{1+\frac{1}{j\omega RC}} \\ &= \frac{A_o}{1+\frac{1}{j2\pi f RC}} \quad (\text{Since } \omega = 2\pi f) \\ &= \frac{A_o}{1-\frac{j}{2\pi RC} \cdot \frac{1}{f}} \quad (\text{Since } \frac{1}{j} = -j) \\ &= \frac{A_o}{1-j\frac{f_l}{f}} \dots\dots\dots (5) \end{aligned}$$

Where $f_l = \frac{1}{2\pi RC}$ or $\omega_l = \frac{1}{RC}$

Consider eq. (5).

When $f \gg f_l$, $|H(j\omega)| = \frac{A_o}{1-j.0} = 0$

When $f = f_l$, $|H(j\omega)| = \frac{A_o}{\sqrt{1^2+1^2}} = \frac{A_o}{\sqrt{2}}$

When $f \ll f_l$, $|H(j\omega)| = \frac{A_o}{1-j.\infty} = 0$

Fig. 3(b) shows the frequency response of first order LPF.

Important observations in Fig. 3(b):

- i. Maximum gain is A_o at $f = 0$ Hz.
- ii. At f_l , gain falls by ,707 A_o (or -3 dB below A_o when A_o is expressed in dB).
- iii. Frequency response from 0 to f_l is called stop band.
- iv. When $f < f_l$, gain decreases at a rate of 20 dB/decade.
- v. Range of frequencies $> f_l$ is called pass band

SECOND ORDER LPF AND HPF

In 1st order LPF and HPF, the gain rolls off at a rate of -20 dB/decade. i.e., response is not close to ideal response. For 2nd order LPF and HPF roll off rate is - 40 dB/decade.

Let us consider a general 2nd order filter (it is called Sallen-key filter) as shown in Fig. 4. Let us derive expression for $\frac{v_o}{v_i}$. Then we can substitute appropriate values for Y1, Y2, Y3, and Y4 to get the expression for $\frac{v_o}{v_i}$ for (a) 2nd order LPF (b) 2nd order HPF.

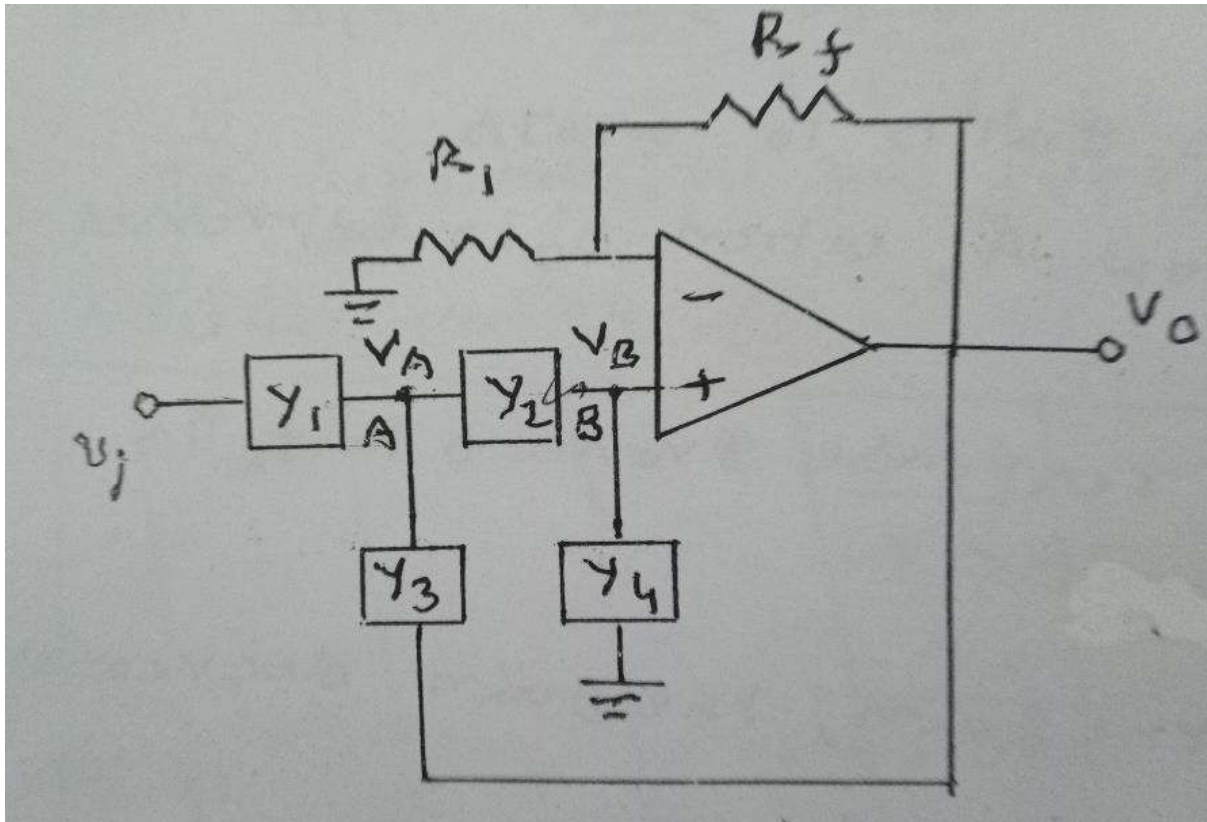


Fig. 4: Sallen-Key Filter

Let v_A be the voltage at node A and v_B be the voltage at node B.

Since opamp is in non-inverting configuration, closed loop gain A_o is given by

$$A_o = \frac{v_o}{v_B} = 1 + \frac{R_f}{R_i} \quad \dots\dots (1)$$

$$\text{i.e., } v_B = \frac{v_o}{A_o} \quad \dots\dots(2)$$

Applying KCL at node A, we get

$$(v_A - v_i)Y_1 + (v_A - v_B)Y_2 + (v_A - v_o)Y_3 = 0$$

$$\text{i.e., } v_A (Y_1 + Y_2 + Y_3) - v_i Y_1 - v_B Y_2 - v_o Y_3 = 0$$

$$\begin{aligned}
\text{i.e., } v_i Y_1 &= v_A (Y_1 + Y_2 + Y_3) - v_B Y_2 - v_o Y_3 \\
&= v_A (Y_1 + Y_2 + Y_3) - \frac{v_o}{A_o} Y_2 - v_o Y_3 \quad \{\text{using eq. (1)}\} \\
&= v_A (Y_1 + Y_2 + Y_3) - \frac{v_o}{A_o} (Y_2 + A_o Y_3) \quad \dots\dots\dots (3)
\end{aligned}$$

Applying KCL at node B, we get

$$(v_B - v_A)Y_2 + (v_B - 0)Y_4 = 0$$

$$\text{i.e., } -v_B Y_2 + v_B (Y_2 + Y_4) = 0$$

$$\begin{aligned}
\text{i.e., } v_A &= \frac{v_B (Y_2 + Y_4)}{Y_2} \\
&= \frac{v_o}{A_o} \frac{Y_2 + Y_4}{Y_2} \quad \dots\dots\dots (4) \quad \{\text{using eq. (2)}\}
\end{aligned}$$

Putting v_A value from eq. (4) into eq. (3), we get

$$\begin{aligned}
v_i Y_1 &= \frac{v_o}{A_o} \left(\frac{Y_2 + Y_4}{Y_2} \right) (Y_1 + Y_2 + Y_3) - \frac{v_o}{A_o} (Y_2 + A_o Y_3) \\
&= \frac{v_o}{A_o Y_2} \{ (Y_2 + Y_4)(Y_1 + Y_2 + Y_3) - Y_2^2 - A_o Y_2 Y_3 \} \\
&= \frac{v_o}{A_o Y_2} \{ Y_1 Y_2 + \cancel{Y_2^2} + Y_2 Y_3 + Y_2 Y_3 + Y_2 Y_3 + Y_2 Y_3 - \cancel{Y_2^2} - A_o Y_2 Y_3 \} \\
&= \frac{v_o}{A_o Y_2} \{ Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o) \}
\end{aligned}$$

$$\therefore \frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)} \quad \dots\dots (5)$$

(a) Second order LPF:

To get second order LPF, choose $Y_1 = Y_2 = \frac{1}{R}$ and $Y_3 = Y_4 = \text{SC}$. Then Fig. 4 becomes Fig. 5.

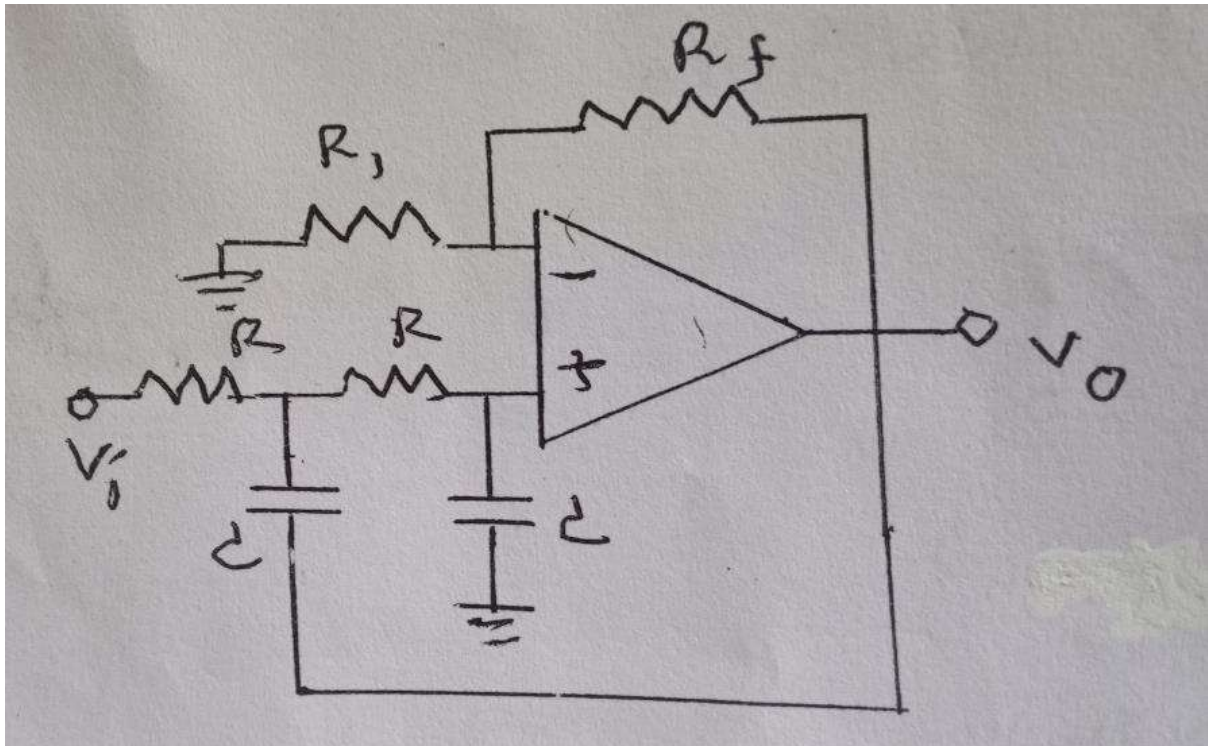


Fig. 5: Second order LPF

Substituting $Y_1 = Y_2 = \frac{1}{R}$ and $Y_3 = Y_4 = sC$ in eq. (5), we get

$$H(s) = \frac{A_o * \frac{1}{R} * \frac{1}{R}}{\frac{1}{R} * \frac{1}{R} + sC \left(\frac{1}{R} + \frac{1}{R} + sC \right) + \frac{1}{R} * sC (1 - A_o)}$$

$$= \frac{A_o / R^2}{\frac{1}{R^2} + \frac{sC}{R} (2 + sRC) + \frac{sC}{R} (1 - A_o)}$$

$$= \frac{\frac{A_o}{R^2}}{\frac{1 + sRC (2 + sRC) + sRC (1 - A_o)}{R^2}}$$

$$= \frac{A_o}{s^2 R^2 C^2 + sRC (3 - A_o) + 1} \dots\dots (6)$$

$$s = 0 \Rightarrow H(s) = A_o$$

$$s = \infty \Rightarrow H(s) = 0$$

So, it is an LPF of 2nd order.

For any second order systems such as electrical, mechanical, hydraulic and chemical system, the Transfer function (TF) is given by

$$H(s) = \frac{A_o \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2} \dots\dots (7)$$

Where α = damping factor or damping coefficient

A_o = Gain of the system

$\omega_h = 2 \pi f_h$, where f_h = Highest cutoff frequency.

Eq. (6) can be written as

$$H(s) = \frac{A_o / R^2 C^2}{s^2 + \frac{sRC}{R^2 C^2}(3 - A_o) + \frac{1}{R^2 C^2}}$$

$$= \frac{A_o / R^2 C^2}{s^2 + \frac{s}{RC}(3 - A_o) + \frac{1}{R^2 C^2}} \dots\dots\dots (8)$$

Comparing eqs. (7) and (8), we get

$$\omega_h = \frac{1}{RC} \text{ and } \alpha = 3 - A_o$$

Where $\alpha = 1.414 = \sqrt{2}$ for Butterworth filter, 1.06 for Chebyshev filter and 1.73 for Bessel filter.

Normalized expression for Transfer function:

Putting $s = j \omega$ in eq. (7), we get

$$H(j\omega) = \frac{A_o \omega_h^2}{(j\omega)^2 + \alpha \omega_h s(j\omega) + \omega_h^2} \text{ Dividing the numerator and denominator of above equation by } \omega_h^2, \text{ we get}$$

$$H(j\omega) = \frac{A_o}{(j\omega/\omega_h)^2 + j \alpha \omega \omega_h / \omega_h^2 + 1}$$

$$= \frac{A_o}{(j\omega/\omega_h)^2 + j \alpha \omega / \omega_h + 1} \dots\dots\dots (9)$$

$$= \frac{A_o}{s_n^2 + j \alpha s_n + 1}$$

Where s_n = normalized frequency = $j \left(\frac{\omega}{\omega_h} \right)$

Expression for magnitude of TF in dB:

Eq. (9) can be written as

$$H(j\omega) = \frac{A_o}{-(\omega/\omega_h)^2 + j \alpha \omega / \omega_h + 1}$$

$$= \frac{A_o}{\left(1 - \frac{\omega^2}{\omega_h^2}\right) + j \alpha \frac{\omega}{\omega_h}}$$

$$\begin{aligned}
 20 \log |H(j\omega)| &= 20 \log \frac{A_o}{\sqrt{\left(1 - \frac{\omega^2}{\omega_h^2}\right)^2 + \alpha^2 \frac{\omega^2}{\omega_h^2}}} \\
 &= 20 \log \frac{A_o}{\sqrt{1 + \frac{\omega^4}{\omega_h^4} - 2\frac{\omega^2}{\omega_h^2} + \alpha^2 \frac{\omega^2}{\omega_h^2}}}
 \end{aligned}$$

Since $\alpha^2 = 2$, last 2 terms in the root get cancelled. So, we get

$$\begin{aligned}
 20 \log |H(j\omega)| &= \frac{A_o}{\sqrt{1 + \frac{\omega^4}{\omega_h^4}}} = \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^4}} \\
 &= \frac{A_o}{\sqrt{1 + \left(\frac{f}{f_h}\right)^4}} \quad (\text{since } \omega = 2\pi f \text{ and } \omega_h = 2\pi f_h)
 \end{aligned}$$

Generalized expression for magnitude of TF for LPF is

$$20 \log |H(j\omega)| = \frac{A_o}{\sqrt{1 + \left(\frac{f}{f_h}\right)^{2n}}}$$

Where 'n' is the order of the filter.

(b) Second order HPF:

Consider the expression for $\frac{v_o}{v_i}$ derived using general second order filter.

$$\frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)} \quad \dots (5)$$

To get second order LPF, choose $Y_1 = Y_2 = sC$ and $Y_3 = Y_4 = \frac{1}{R}$. Then Fig. 4 becomes Fig. 6.

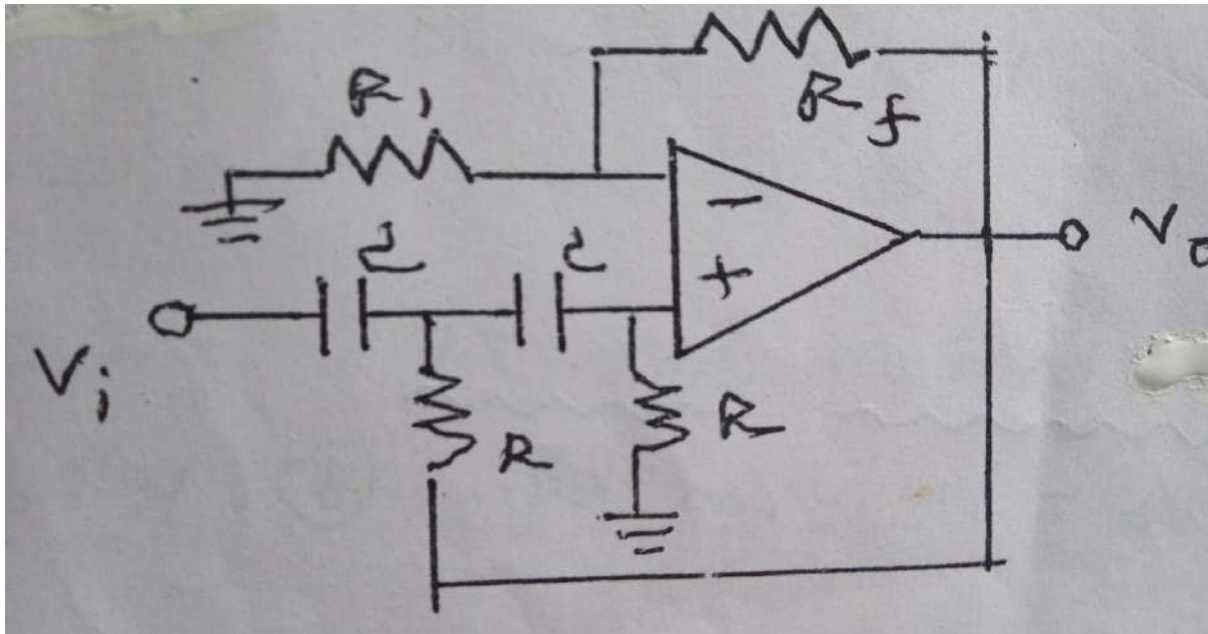


Fig. 6: Second order HPF

Substituting $Y_1 = Y_2 = \frac{1}{R}$ and $Y_3 = Y_4 = sC$ in eq. (5), we get

$$\begin{aligned}
 H(s) &= \frac{A_o * sC * sC}{sC * sC + \frac{1}{R} \left(sC + sC + \frac{1}{R} \right) + \frac{sC}{R} (1 - A_o)} \\
 &= \frac{A_o s^2 C^2}{s^2 C^2 + \frac{sC}{R} \left(2 + \frac{1}{sCR} \right) + \frac{sC}{R} (1 - A_o)} \\
 &= \frac{A_o}{1 + \frac{1}{sRC} \left(2 + \frac{1}{sRC} \right) + \frac{1}{sRC} (1 - A_o)} \\
 &= \frac{A_o}{1 + \frac{1}{sRC} (3 - A_o) + \frac{1}{s^2 R^2 C^2}} \dots\dots (6)
 \end{aligned}$$

For any second order system such as electrical, mechanical, hydraulic and chemical system, the Transfer function (TF) is given by

$$H(s) = \frac{A_o s^2}{s^2 + \alpha \omega_l s + \omega_l^2} \dots\dots (7)$$

Where α = damping factor or damping coefficient

A_o = Gain of the system

$\omega_l = 2 \pi f_l$, where f_l = Lowest cutoff frequency.

Eq. (6) can be written as

$$H(s) = \frac{A_o / R^2 C^2}{s^2 + \frac{sRC}{R^2 C^2} (3 - A_o) + \frac{1}{R^2 C^2}}$$

$$= \frac{A_o}{1 + \frac{\omega_l}{s}(3 - A_o) + \frac{\omega_l^2}{s}} \dots\dots\dots (8)$$

Comparing eqs. (7) and (8), we get

$$\omega_l = \frac{1}{RC} \text{ and } \alpha = 3 - A_o$$

Where $\alpha = 1.414 = \sqrt{2}$ for Butterworth filter, 1.06 for Chebyshev filter and 1.73 for Bessel filter.

Normalized expression for Transfer function:

Putting $s = j \omega$ in eq. (8), we get

$$H(j\omega) = \frac{A_o}{\left(\frac{\omega_l}{j\omega}\right)^2 + \frac{\omega_l}{j\omega}(3 - A_o) + 1} \text{ Dividing the numerator and denominator of above}$$

$$= \frac{A_o}{1 - \frac{j\omega_l}{\omega}(3 - A_o) - \frac{\omega_l^2}{\omega^2}} \dots\dots\dots (9)$$

Normalized expression for Transfer function is

$$= \frac{A_o}{s_n^2 + j \alpha s_n + 1}$$

Where $s_n = \text{normalized frequency} = -\frac{j\omega_l}{\omega}$ and $\alpha = 3 - A_o$

Expression for magnitude of TF in dB:

Eq. (9) can be written as

$$H(j\omega) = \frac{A_o}{1 - \frac{\omega_l^2}{\omega^2} - \frac{j\omega_l}{\omega}(3 - A_o)}$$

$$|H(j\omega)| = \frac{A_o}{\sqrt{\left(1 - \frac{\omega_l^2}{\omega^2}\right)^2 + \alpha^2 \frac{\omega_l^2}{\omega^2}}}$$

$$\begin{aligned} 20 \log |H(j\omega)| &= 20 \log \frac{A_o}{\sqrt{\left(1 - \frac{\omega_l^2}{\omega^2}\right)^2 + \alpha^2 \frac{\omega_l^2}{\omega^2}}} \\ &= 20 \log \frac{A_o}{\sqrt{1 + \frac{\omega_l^4}{\omega^4} - 2 \frac{\omega_l^2}{\omega^2} + \alpha^2 \frac{\omega_l^2}{\omega^2}}} \end{aligned}$$

Since $\alpha^2 = 2$, last 2 terms in the root get cancelled. So, we get

$$20 \log |H(j\omega)| = \frac{A_o}{\sqrt{1 + \frac{\omega_l^4}{\omega^4}}} = \frac{A_o}{\sqrt{1 + \left(\frac{\omega_l}{\omega}\right)^4}}$$

$$= \frac{A_o}{\sqrt{1 + \left(\frac{f_l}{f}\right)^4}} \quad (\text{since } \omega = 2\pi f \text{ and } \omega_l = 2\pi f_l)$$

Generalized expression for magnitude of TF for LPF is

$$20 \log |H(j\omega)| = \frac{A_o}{\sqrt{1 + \left(\frac{f_l}{f}\right)^{2n}}}$$

Where 'n' is the order of the filter.

Design of LPF and HPF:

(a) Design of second order LPF:

Select equal values of R and C in the two RC sections. Then follow the steps given below.

Step1: Choose value of f_h . (e.g.: $f_h = 1000$ Hz)

Step2: Select C Value $\leq 0.1 \mu\text{F}$ (Say $C = 0.1 \mu\text{F}$)

Step3: Calculate R value using the relation

$$f_h = \frac{1}{2\pi RC}$$

Step4: Select R_i and R_f using the relation

$$A_0 = 1 + \frac{R_f}{R_i} = 3 - \alpha$$

Where A_o = Pass band gain

A = Damping factor

= 1.414 for Butterworth filter

= 1.06 for Chebyshev filter

= 1.73 for Bessel filter

(b) Design of second order HPF:

Follow the same procedure given above, where cutoff frequency ' f_h ' is replaced by f_l , where f_l is the lower cutoff frequency of HPF.

Note: Use mylar or tantalum capacitors.

Design of first order LPF and HPF:

Procedure is same as that of second order LPF and HPF. But here there is a single RC section.

Problem1: Design a 2nd order Butterworth LPF having upper cutoff frequency of 1 KHz.

Solution:

Given $f_h = \frac{1}{2\pi RC} = 1 \text{ KHz} = 1000 \text{ Hz}$

i.e., $R = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 1000 \times C}$

Choose $C = 0.1 \mu\text{F} = 10^{-7} \text{ F}$ $\frac{R_f}{R_i}$

$\therefore R = \frac{1}{2\pi \times 1000 \times 10^{-7}}$

We know that $A_o = 3 - \alpha$

For Butter worth filter $\alpha = \sqrt{2} = 1.414$

$\therefore A_o = 3 - 1.414 = 1.586$

But $A_o = 1 + \frac{R_f}{R_i}$

i.e., $1.586 = 1 + \frac{R_f}{R_i}$

or $\frac{R_f}{R_i} = 1.586 - 1 = 0.586$

Let $R_f = 5.86 \text{ K}\Omega$

Then $R_i = \frac{5.86 \text{ K}\Omega}{0.586} = 10 \text{ K}\Omega$

Problem2: Design a 2nd order Butterworth LPF having lower cutoff frequency of 1 KHz.

Solution is same as in Problem1. Answers are also same.

But frequency response formulae are different for LPF and HPF.

Band Pass Filter (BPF)

A BPF allows a particular band of frequencies and rejects frequencies outside that band.

Wide Band Pass Filter:

Let f_l = Lower cutoff frequency

f_h = Higher cutoff frequency

f_o = Center frequency

Q = Quality Factor

Then

$$f_o = \sqrt{f_l f_h}$$

$$\text{Bandwidth} = f_h - f_l$$

$$Q = \frac{f_o}{f_h - f_l}$$

There are two types of BPFs. They are wide BPF and narrow BPF. For wide BPF, $Q < 10$ and for narrow BPF, $Q > 10$.

Wide Band Pass Filter ($Q < 10$)

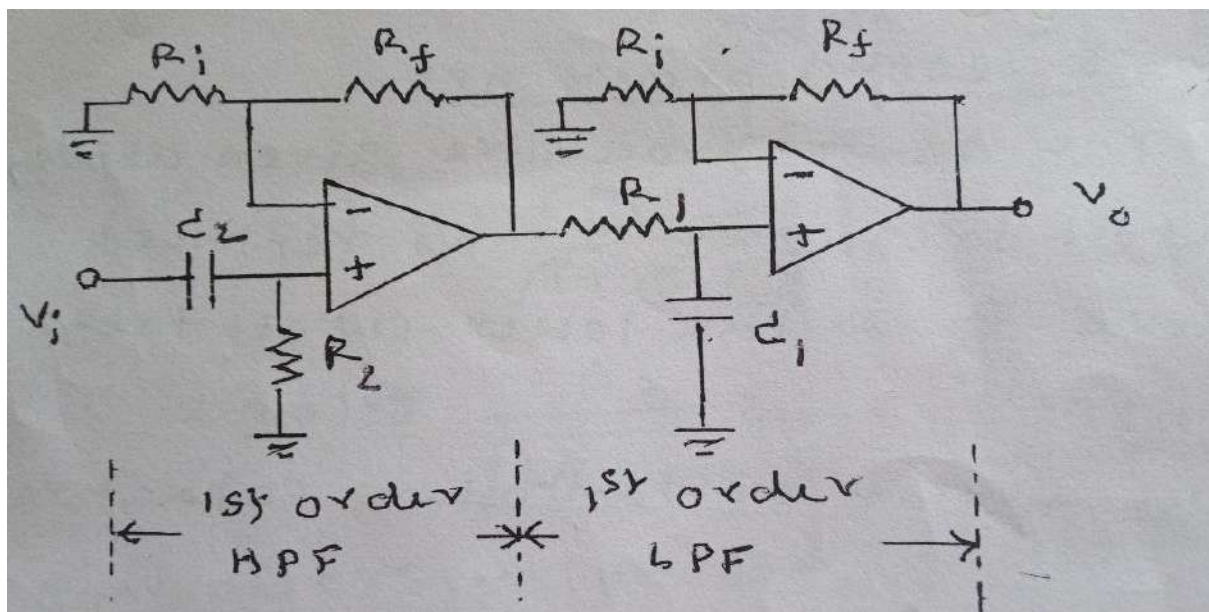


Fig. 7: First order wide BPF

Fig. 7 represents a first order wide BPF. It is obtained by cascading a first order HPF and a first order LPF as shown.

Let A_{o1} = Pass band gain of HPF

Let A_{o2} = Pass band gain of LPF

Then

Magnitude of Transfer Function (TF) of HPF is given by

$$|H_{HP}| = \frac{A_{01}}{\sqrt{1 + \left(\frac{f_l}{f}\right)^2}} \text{ where } f_l = \frac{1}{2\pi R_2 C_2} \quad \dots\dots (1)$$

Magnitude of Transfer Function (TF) of LPF is given by

$$|H_{LP}| = \frac{A_{02}}{\sqrt{1 + \left(\frac{f}{f_h}\right)^2}} \text{ where } f_h = \frac{1}{2\pi R_1 C_1} \quad \dots\dots (2)$$

Magnitude of TF of BPF =

$$|H_{BP}| = |H_{HP}| * |H_{LP}| \quad \dots\dots\dots (3)$$

Eqs. (1), (2) and (3), we write

$$|H_{BP}| = \frac{A_{01}}{\sqrt{1 + \left(\frac{f_l}{f}\right)^2}} \frac{A_{02}}{\sqrt{1 + \left(\frac{f}{f_h}\right)^2}} = \frac{A_0}{\sqrt{1 + \left(\frac{f_l}{f}\right)^2 + \left(\frac{f}{f_h}\right)^2}} \text{ where } A_0 = A_{01} \cdot A_{02} \quad \dots\dots\dots (4)$$

Problem 3: Design a wide band pass filter having $f_l = 400$ Hz and $f_h = 2$ KHz with a pass band gain of 2.

Solution:

For LPF:

$$f_h = 2 \text{ KHz} = 2000 \text{ Hz} = \frac{1}{2\pi R_1 C_1}$$

$$\text{Choose } C_1 = 0.01 \text{ } \mu\text{F} = 0.01 \times 10^{-6} \text{ F}$$

$$\text{Then } R_1 = \frac{1}{2\pi \times 2000 \times 0.01 \times 10^{-6}} = 7.9 \text{ K}\Omega$$

For HPF:

$$f_l = 400 \text{ Hz} = \frac{1}{2\pi R_2 C_2}$$

$$\text{Choose } C_2 = 0.01 \text{ } \mu\text{F} = 0.01 \times 10^{-6} \text{ F}$$

$$\text{Then } R_2 = \frac{1}{2\pi \times 400 \times 0.01 \times 10^{-6}} = 39.8 \text{ K}\Omega$$

Here, the pass band gains of LPF and HPF should be same.

$$\text{Let } A_{o1} = A_{o2} = 2 = 1 + \frac{R_f}{R_i}$$

$$\text{i.e., } R_f = R_i = 10 \text{ K}\Omega \text{ (say)}$$

$$f_o = \sqrt{f_h f_l} = \sqrt{2000 \times 400} = 894.4 \text{ K}\Omega$$

$$Q = \frac{f_o}{BW} = \frac{f_o}{f_h - f_l} = \frac{894.4}{2000 - 400} = 0.56$$

Note that $Q < 10$

Narrow Band Pass Filter:

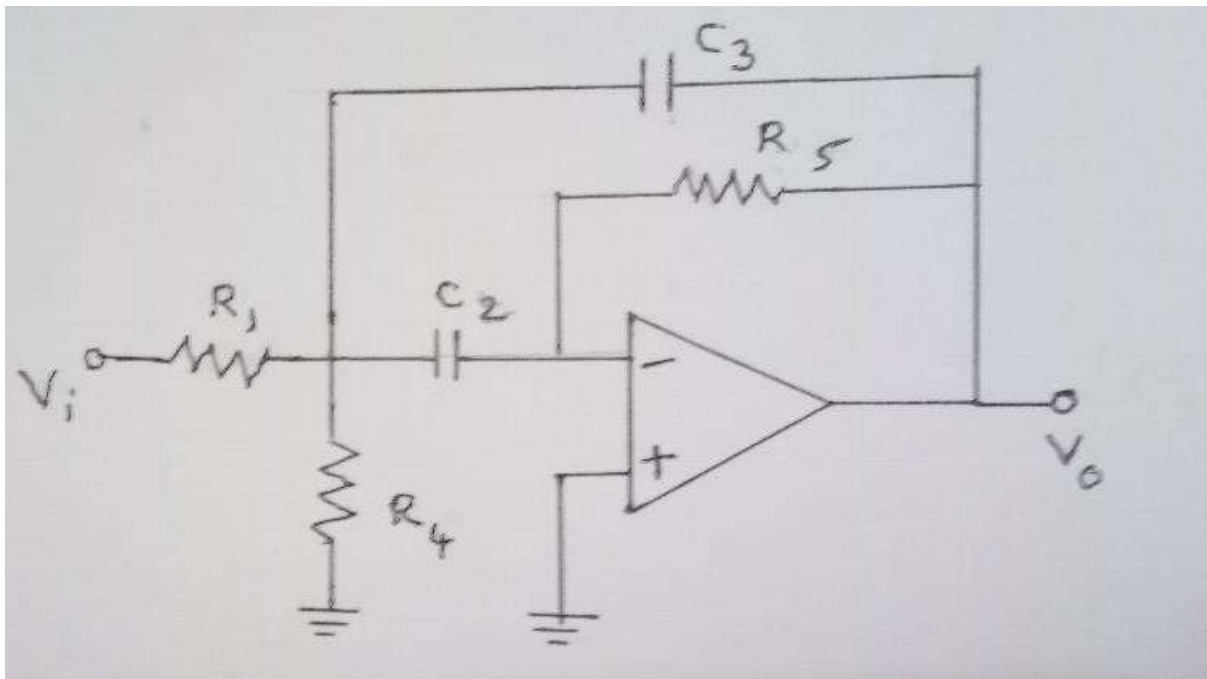


Fig. 8: Second Order narrow Band Pass Filter

Fig. 8 shows a narrow BPF. Here $Q > 10$.

BAND REJECT FILTER (BRF):

A BRF is also called a band stop filter or band elimination filter. It rejects a particular band of frequencies and rejects frequencies outside this band. There are two types of BRF. They are wide BRF and narrow BRF.

Wide Band Reject Filter:

It has a $Q < 10$. It can be made using an LPF, HPF and a summer. Its necessary constraints are (i) The lower cutoff frequency f_l of the HPF $\gg$ the higher cutoff frequency f_h of LPF. (ii) The pass band gains of LPF and HPF should be same.

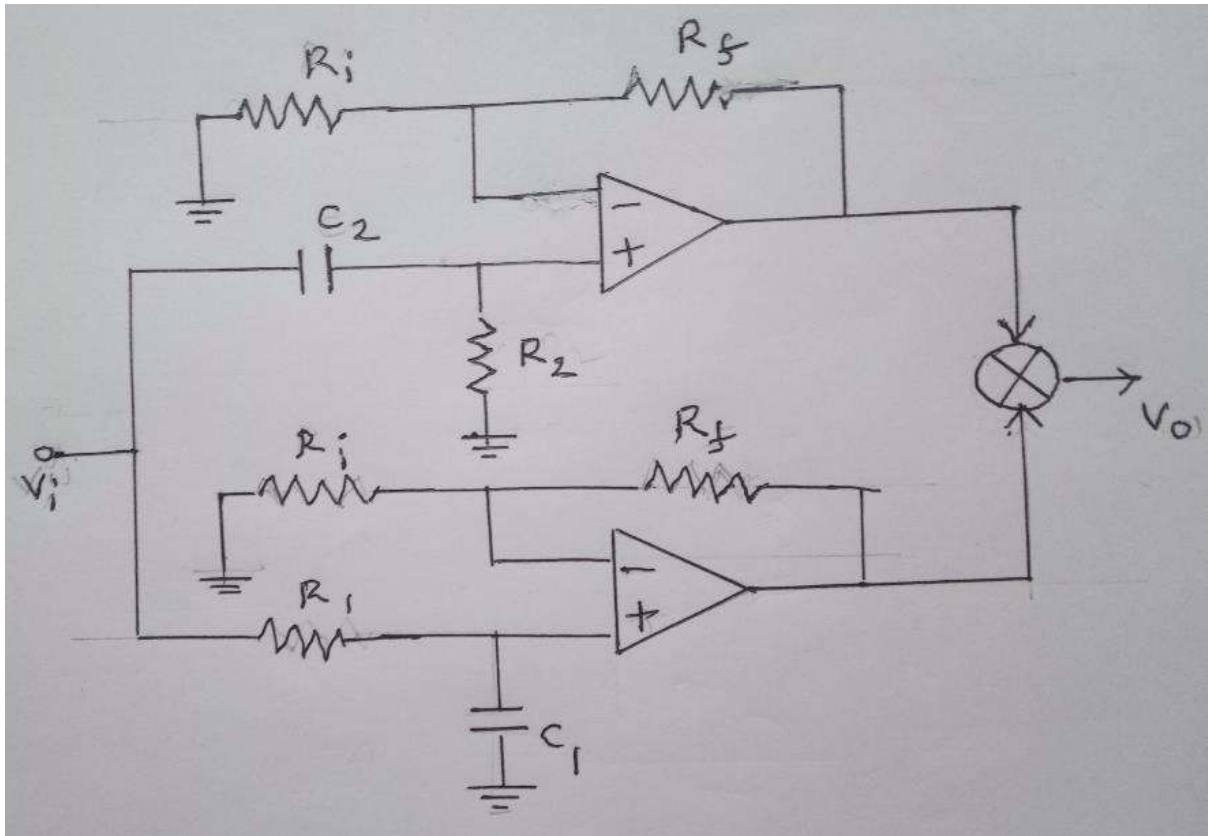


Fig. 9 (a): Wide BRF

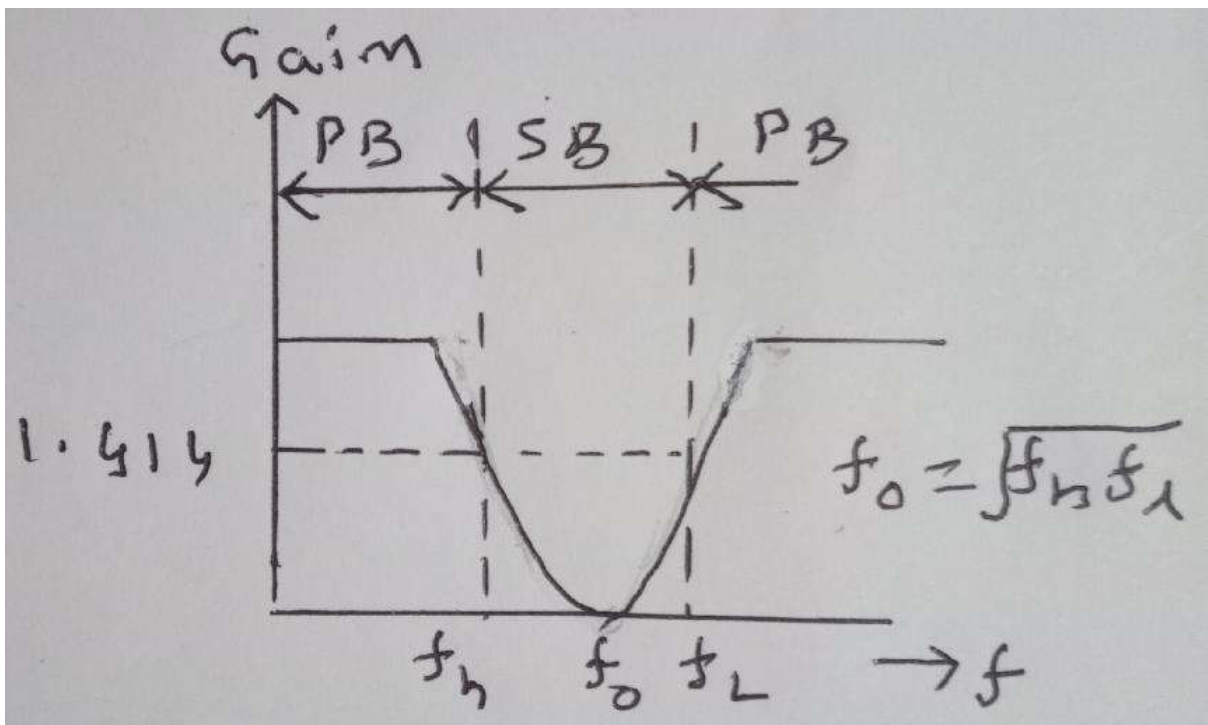


Fig. 9 (b): Frequency response of wide BRF

Fig. 9 (a) shows the circuit diagram of a wide BRF. Fig. 9 (b) shows its frequency response.

Problem 4: Design a wide band reject filter having $f_h = 400$ Hz and $f_l = 2$ KHz with a pass band gain of 2.

Solution:

For HPF:

$$f_l = 2 \text{ KHz} = 2000 \text{ Hz} = \frac{1}{2\pi R_2 C_2}$$

$$\text{Choose } C_2 = 0.1 \text{ } \mu\text{F} = 0.1 \times 10^{-6} \text{ F}$$

$$\text{Then } R_2 = \frac{1}{2\pi \times 2000 \times 0.1 \times 10^{-6}} = 795 \text{ } \Omega \approx 800 \text{ } \Omega$$

For LPF:

$$f_h = 400 \text{ Hz} = \frac{1}{2\pi R_1 C_1}$$

$$\text{Choose } C_1 = 0.1 \text{ } \mu\text{F} = 0.1 \times 10^{-6} \text{ F}$$

$$\text{Then } R_1 = \frac{1}{2\pi \times 400 \times 0.1 \times 10^{-6}} = 3978 \text{ } \Omega \approx 4 \text{ K}\Omega$$

Here, the pass band gains of LPF and HPF should be same.

$$\text{Let } A_{o1} = A_{o2} = 2 = 1 + \frac{R_f}{R_i}$$

$$\text{i.e., } R_f = R_i = 10 \text{ K}\Omega \text{ (say)}$$

Narrow Band Reject Filter:

Narrow BRF is commonly called a **notch filter**. It is useful for the rejection of a single frequency like 50 Hz power line hum.

There are mainly two ways of realizing notch filter

First way of realizing a second order notch filter:

It is achieved by cascading a second order narrow BPF and a summer. It is shown in Fig. 10 (a)

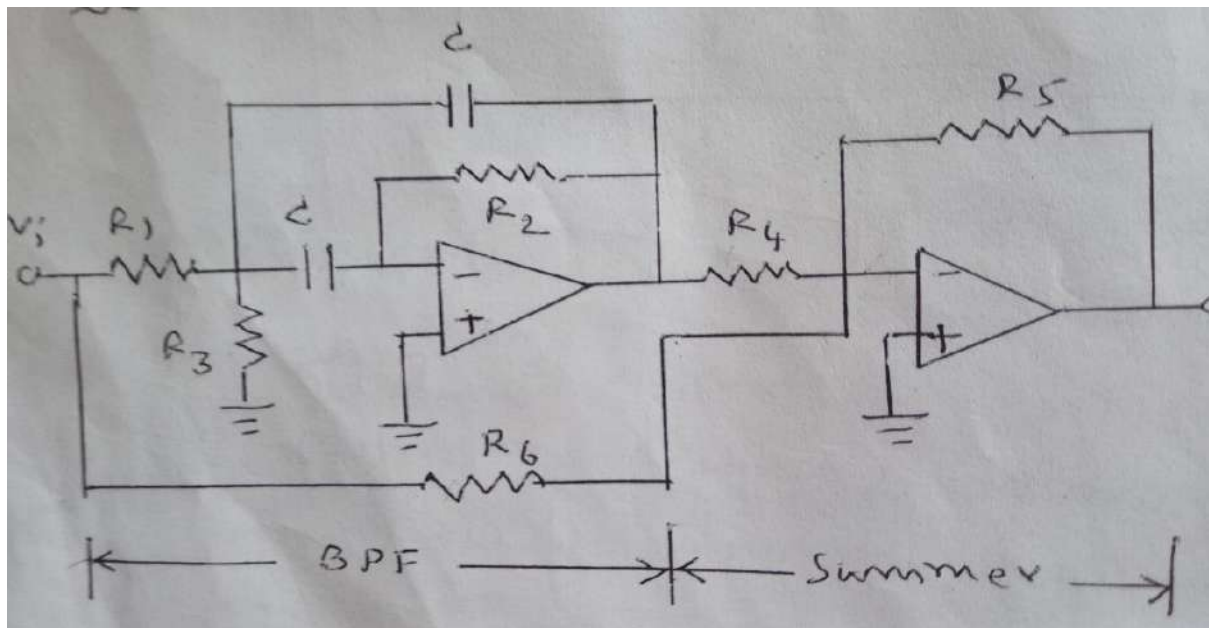


Fig. 10 (a)

Second way of realizing a second order notch filter (Twin-T filter):

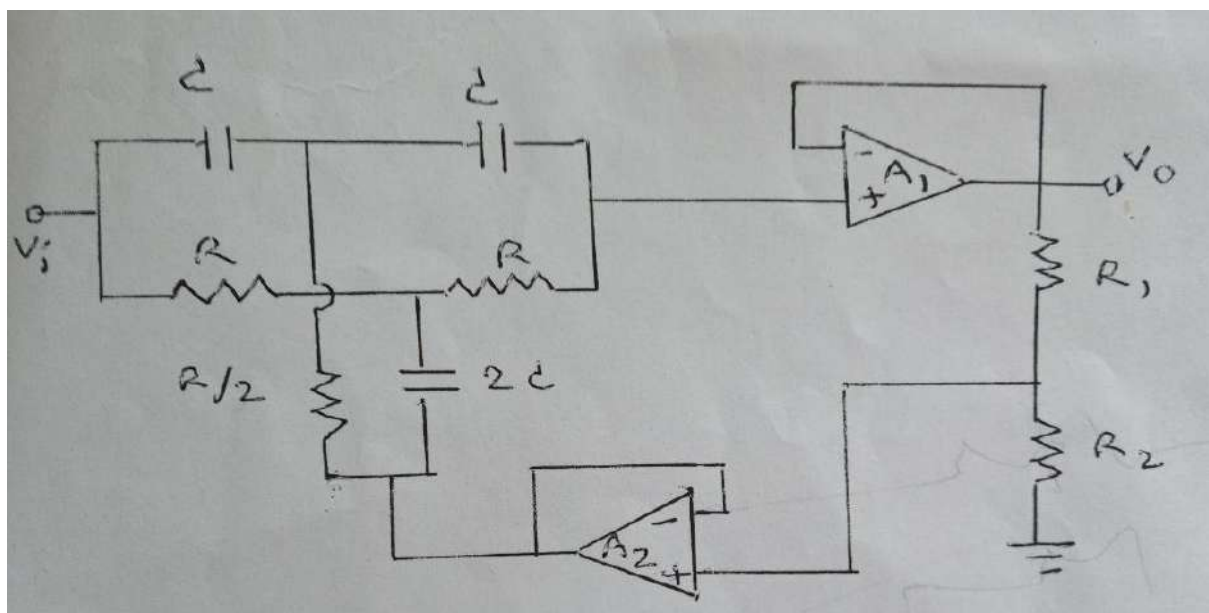


Fig. 10 (b) Twin-T notch filter

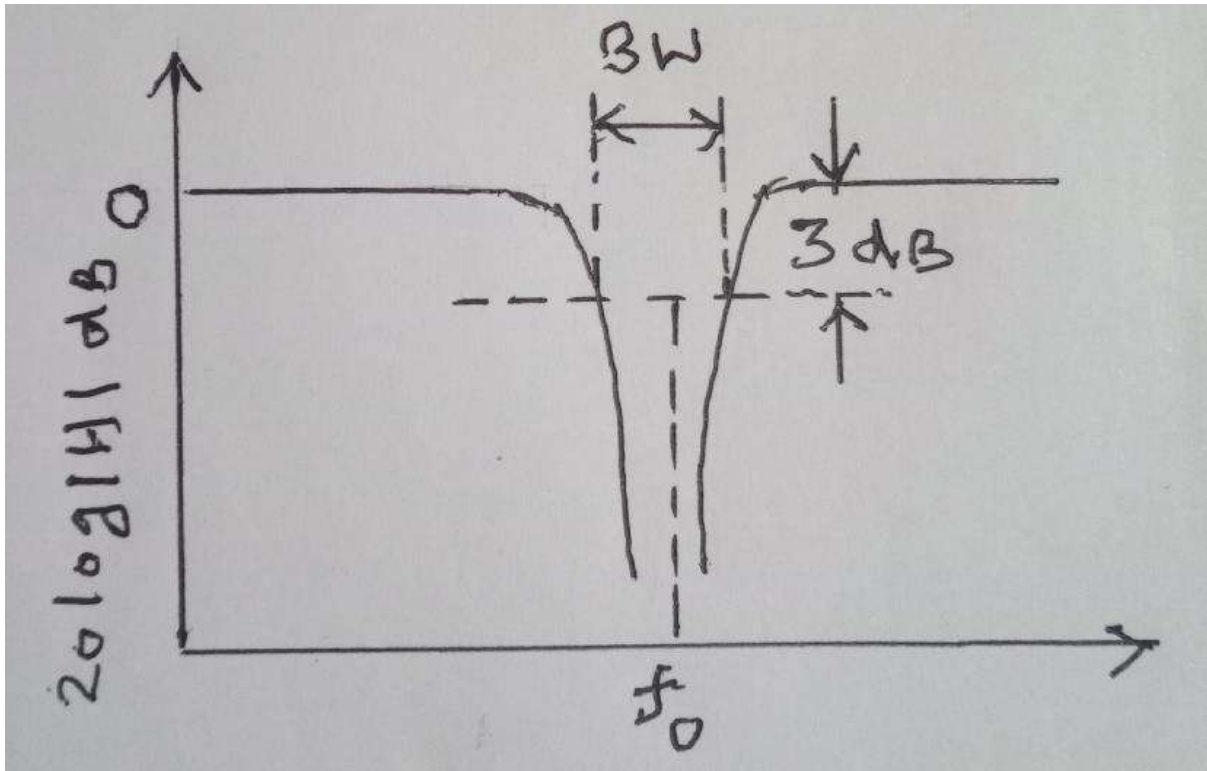


Fig. 10 (c) Frequency response of notch filter

Fig. 10 (b) shows a Twin-T notch filter.

If f_l = Lower cutoff frequency

f_h = Higher cutoff frequency

f_o = Center frequency

Q = Quality Factor

From the analysis of the circuit, we can show that

$$f_o = \frac{1}{2 \pi RC}$$

$$\text{Bandwidth} = BW = f_h - f_l = 4 f_o (1 - K)$$

$$Q = \frac{f_o}{BW} = \frac{1}{4-K}$$

As K approaches unity, Q factor becomes very large and bandwidth approaches 0. Mismatches between resistors and capacitors also limit the value of Q and bandwidth.

R_1 and R_2 are used to adjust gain of the filter.

Fig. 10 (c) shows the frequency response of notch filter.

Problem 5: Design a 50 Hz active notch filter.

Solution:

Consider the Twin-T filter in Fig. 10 (b)

$$\text{Given that } f_o = \frac{1}{2\pi RC} = 50 \text{ Hz}$$

$$\text{Let } C = 0.1 \mu\text{F} = 0.1 \times 10^{-6} \text{ F}$$

$$\begin{aligned} \text{Then } R &= \frac{1}{2\pi f_o C} \\ &= \frac{1}{2\pi \times 50 \times 0.1 \times 10^{-6}} = 31.8 \text{ K}\Omega \end{aligned}$$

For $R/2$, we can use two $31.8 \text{ K}\Omega$ in parallel.

For $2C$, we can use two capacitors in parallel.

ALL PASS FILTERS (APFs)

All pass filters (APFs) allow all frequency components of input signal without any attenuation. Their main advantage is they provide desired phase shift at any frequency. Thus, APFs are used in phase correction in analog systems (e.g.: Analog telephone systems).

APFs are also called delay equalizers or phase correctors.

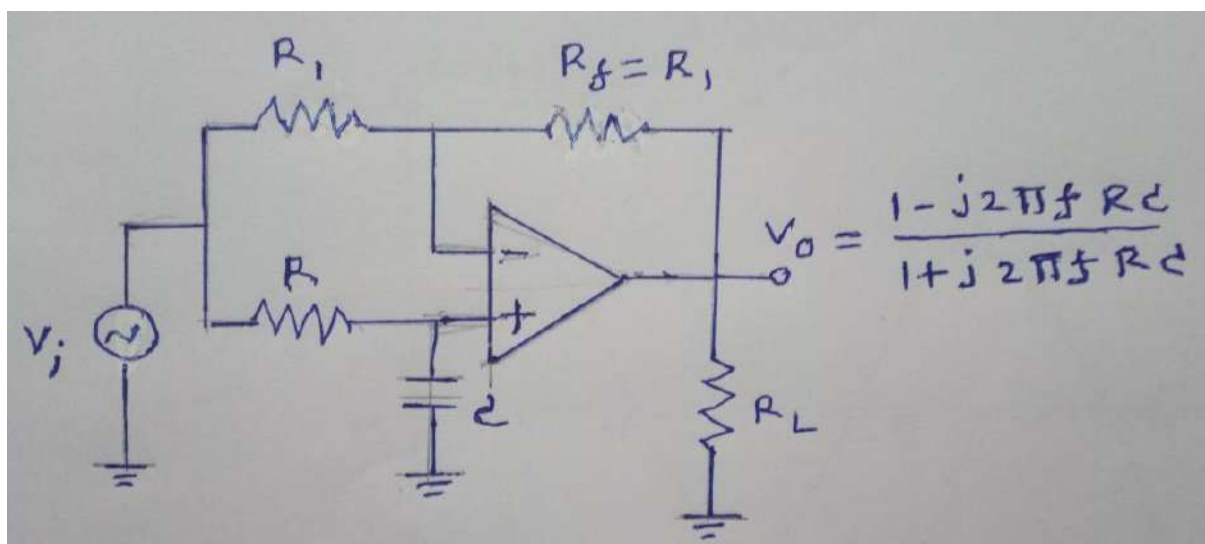


Fig. 11 (a) All Pass Filter

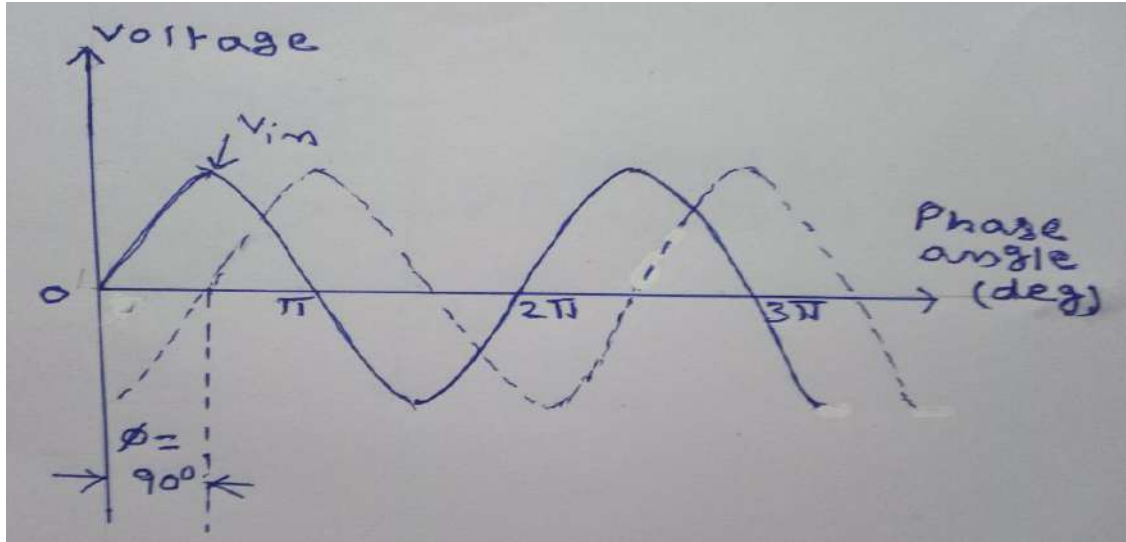


Fig. 11 (b) Waveforms of All Pass Filter

Fig. 11 (a) shows an All Pass Filter where v_i is input voltage and v_o is output voltage and $R_f = R_1$. Fig. 11 (b) shows waveforms for All Pass Filter.

Let the voltage at node 'a' is v_a .

By using super position theorem, we can write

$$v_o = -\frac{R_f}{R_1} \cdot v_i + \left(1 + \frac{R_f}{R_1}\right)v_a$$

Since $R_f = R_1$, above equation becomes

$$v_o = -v_i + 2v_a \quad \dots (1)$$

$$\text{But } v_a = v_i \cdot \frac{\frac{1}{sC}}{R + \frac{1}{sC}} = v_i \cdot \frac{1}{1 + sRC} \quad \dots (2)$$

Eqs. (1) and (2) $\Rightarrow$

$$\begin{aligned} v_o &= -v_i + 2v_i \cdot \frac{1}{1 + sRC} \\ &= v_i \left(-1 + \frac{2}{1 + sRC} \right) \\ &= v_i \frac{(-1 - sRC + 2)}{1 + sRC} \\ &= v_i \frac{1 - sRC}{1 + sRC} \\ &= v_i \frac{1 - j\omega RC}{1 + j\omega RC} \end{aligned}$$

$$\text{i.e., } \frac{v_o}{v_i} = \frac{1 - j\omega RC}{1 + j\omega RC}$$

$$= \frac{1-j2\pi fRC}{1+j2\pi fRC}$$

∴ Magnitude of $\frac{v_o}{v_i}$ is given by

$$\left| \frac{v_o}{v_i} \right| = \frac{\sqrt{1+(2\pi fRC)^2}}{\sqrt{1+(2\pi fRC)^2}} = 1$$

i.e., $|v_o| = |v_i|$ for all frequencies.

The phase shift Φ between v_o and v_i is given by

$$\begin{aligned}\Phi &= -\tan^{-1}(2\pi fRC) - \tan^{-1}(2\pi fRC) \\ &= -2\tan^{-1}(2\pi fRC)\end{aligned}$$

Thus, the phase shift can be varied with frequency for a given R and C.

We can obtain phase shift from 0 to 180° as we change the frequency from 0 to ∞ .

As phase shift here is negative, the output v_o lags input v_i .

The phase shift can be made positive by interchanging R and C in Fig. 11 (a)

555 TIMER (Introduction)

- A 555 timer is a monolithic IC that can produce accurate and highly stable time delays or oscillations.
- It operates with supply range of + 5 V and produces a delay ranging from 'µsecs' to hours.
- It is compatible with TTL and CMOS logic circuits.
- It is available as an 8-pin metal can, an 8-pin mini-DIP or 14-pin DIP.

Applications of 555 timer:

1. Monostable multivibrator
2. Astable multivibrator
3. Waveform (Pulse, ramp and square waves) generator
4. Burglar and toxic alarms
5. Voltage regulators
6. Traffic control
7. Digital logic probes
8. Temperature measurement and control
9. Infrared transmitters.

PIN Diagram of 555 timer:

Fig. 1 (a) represents the pin diagram of a 555 timer.

Here R and C are external resistor and capacitor. Let us assume that the width of trigger pulse is very small.

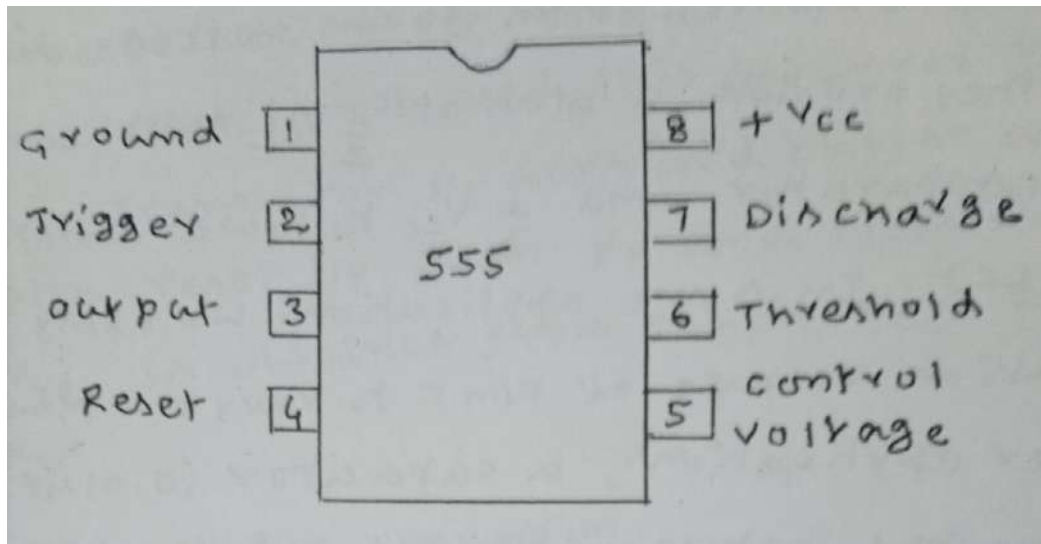


Fig. 1 (a): Pin diagram of 555 Timer

Functional diagram of a 555 timer:

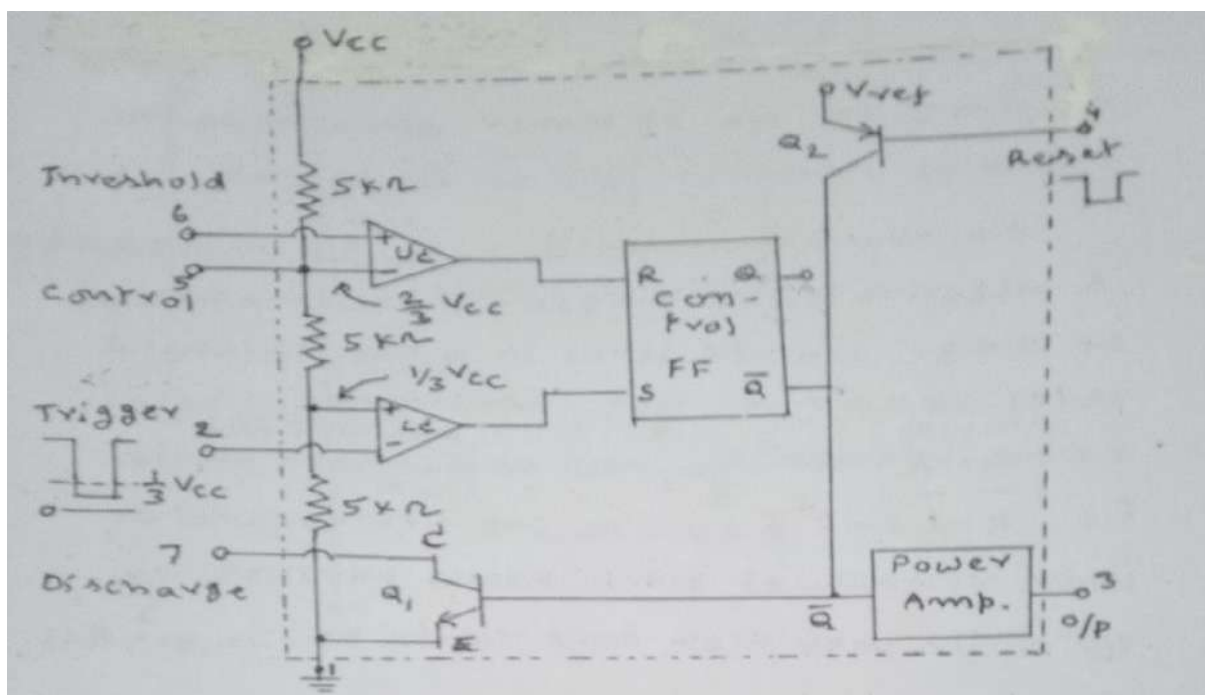


Fig. 1 (b): Functional diagram

Fig. 1 (b) shows its functional diagram. Three $5\text{ K}\Omega$ resistors form voltage divider. They provide a bias of $\frac{2}{3} V_{CC}$ to the **upper comparator (UC)** and $\frac{1}{3} V_{CC}$ to the **lower comparator (LC)**. In some applications, we apply modulation voltage at pin 5 to vary the time. In other applications, a capacitor ($0.01\mu\text{F}$) is connected between pin 5 and ground to by-pass noise or ripple from the supply. Q and Q' are outputs of control Flip-Flop(FF). Outputs of **UC** and **LC** are R and S inputs of FF respectively. **Power amplifier** is basically an inverter. Its output at pin 3 is output of timer. Since Q' is the input of inverter, output at pin 3 is Q.

In standby mode, $Q=0$, $Q' = 1$. So, o/p at pin 3 = $Q = 0$. A negative going triggering pulse is applied at pin 2. Its dc level is $>$ the threshold level of **LC** (i.e., $\frac{1}{3} V_{CC}$). When trigger pulse passes through $\frac{V_{CC}}{3}$, output of **LC** goes high and sets the **FF**. i.e., $Q = 1$ and $Q' = 0$. During + ve excursion, when voltage at pin 6 passes through $\frac{2}{3} V_{CC}$, o/p of **UC** goes high and resets the **FF**. i.e., $Q = 0$ and $Q' = 1$.

Reset input at pin 4 is used to reset the FF, irrespective of o/p of **LC**. This input is $< 0.4\text{ V}$. When the reset input is not used, it is connected to V_{CC} .

Transistor Q_2 acts as a buffer and isolates reset i/p from FF and transistor Q_1 . V_{ref} is applied from supply V_{CC} . It drives Q_2 .

MONOSTABLE OPERATION USING 555 TIMER

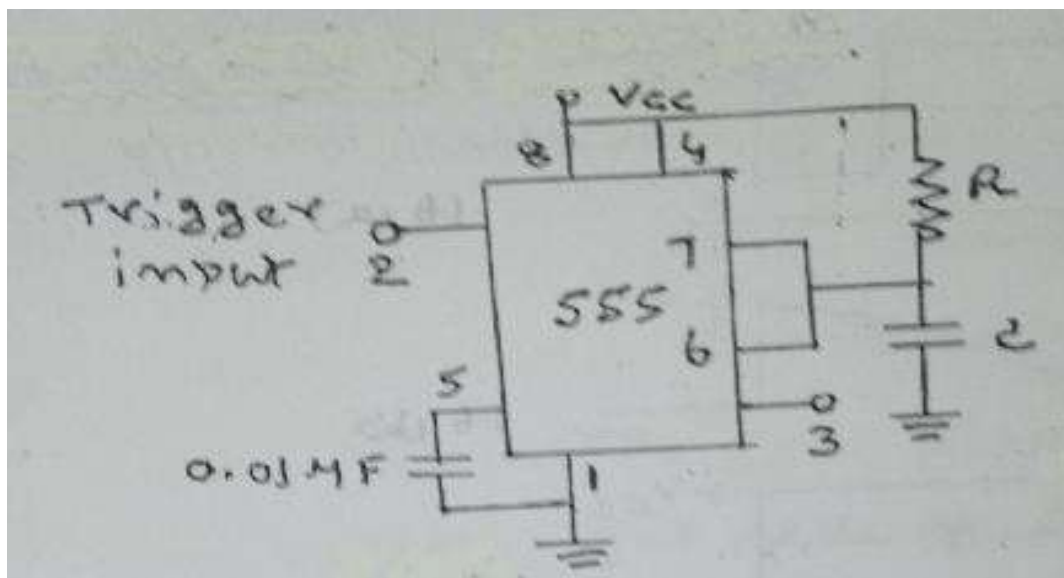


Fig. 2 (a):Pin Connections for Monostable multivibrator

[illegible]

Trigger $\frac{1}{3}V_{CC}$

Additional pulse has no effect on output

Fig. (a)

Capacitor voltage $\frac{2}{3}V_{CC}$

Fig. (b)

output $+V_{CC}$ T

Fig. (c)

Fig. 3: Waveforms of Monostable multivibrator

In standby mode, FF is reset. i.e., $Q = 0$ and $Q' = 1$. Here Q' is the input to transistor Q_1 . Since $Q' = 1$, Q_1 is ON (i.e., $V_{CE} = 0$). So, capacitor is shorted to ground. Output at pin 3 = $Q = 0$.

Fig. 3(a) shows the triggering pulse.

As trigger pulse passes through $\frac{V_{CC}}{3}$, FF is set. i.e., $Q = 1$ and $Q' = 0$.

Since $Q' = 0$, Q_1 is OFF. So, capacitor is not short circuited (i.e., capacitor is unclamped). Output at pin 3 = $Q = 1$.

The timing cycle begins now.

Now C charges exponentially through R towards V_{CC} , with a time constant RC as shown in Fig. 3 (b).

After a time T (say), capacitor voltage v_c is just $>\frac{2}{3} V_{CC}$. So, UC resets the FF. i.e., $Q = 0$ and $Q' = 1$.

Since $Q' = 0$, Q_1 is ON. Then C discharges rapidly to ground potential.

The o/p returns to standby state or ground potential as shown in Fig.3 (c)

If a second trigger pulse is given as shown in the right side of fig. 3(a), before T, it has no effect on the operation of the circuit.

Derivation for Output Pulse Width 'T':

We know that capacitor charge equation is given by

$$v_c(t) = v_f + (v_i - v_f)e^{-t/RC} \dots (1)$$

where v_i = Initial voltage = 0

v_f = Final (target) voltage = V_{CC}

∴ Eq. (1) becomes

$$\begin{aligned} v_c(t) &= V_{CC} + (0 - V_{CC}) e^{-t/RC} \\ &= V_{CC} (1 - e^{-t/RC}) \dots (2) \end{aligned}$$

At $t = T$, $v_c(t) = \frac{2}{3} V_{CC}$

∴ Eq. (2) becomes

$$\frac{2}{3} V_{CC} = V_{CC} (1 - e^{-T/RC})$$

$$\text{i.e., } e^{-T/RC} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$\text{or } e^{T/RC} = \ln(3)$$

$$\text{i.e., } T = RC \ln(3)$$

$$\text{i.e., } T = 1.1 RC \text{ seconds}$$

Applications of Monostable Multivibrator:

1. Frequency Divider
2. Pulse Stretcher
3. Pulse Width Modulation (PWM)
4. Linear Ramp Generator

Problem 1: Design a monostable multivibrator using 555 Timer, shown in Fig. 2 (b) with a pulse width of 100 m Sec.

Solution:

$$\text{Given } T = 1.1 RC = 100 \times 10^{-3} \text{ Sec}$$

$$\text{Choose } R = 100 \text{ K}\Omega = 10^5 \Omega$$

$$\text{Then } 100 \times 10^{-3} = 1.1 \times 10^5 \times C$$

$$\therefore C = \frac{100 \times 10^{-3}}{1.1 \times 10^5} = 0.909 \mu\text{F} = 1 \mu\text{F}$$

ASTABLE OPERATION USING 555 TIMER

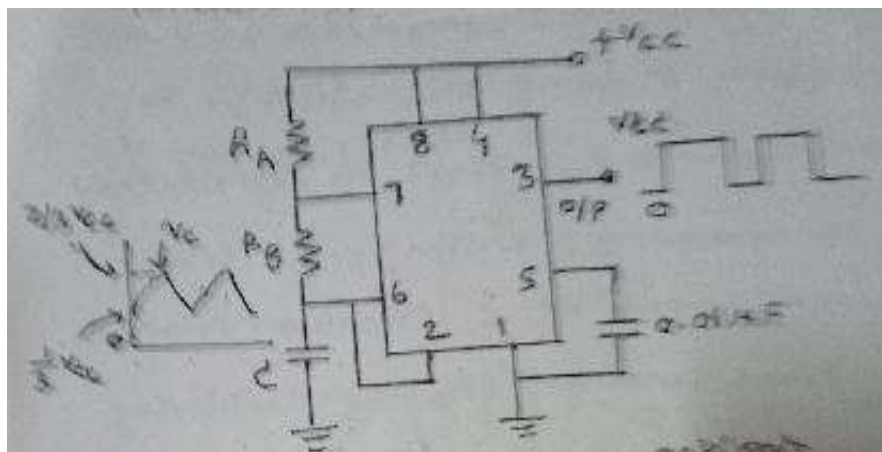


Fig. 4 (a): Pin Connections for Astable operation

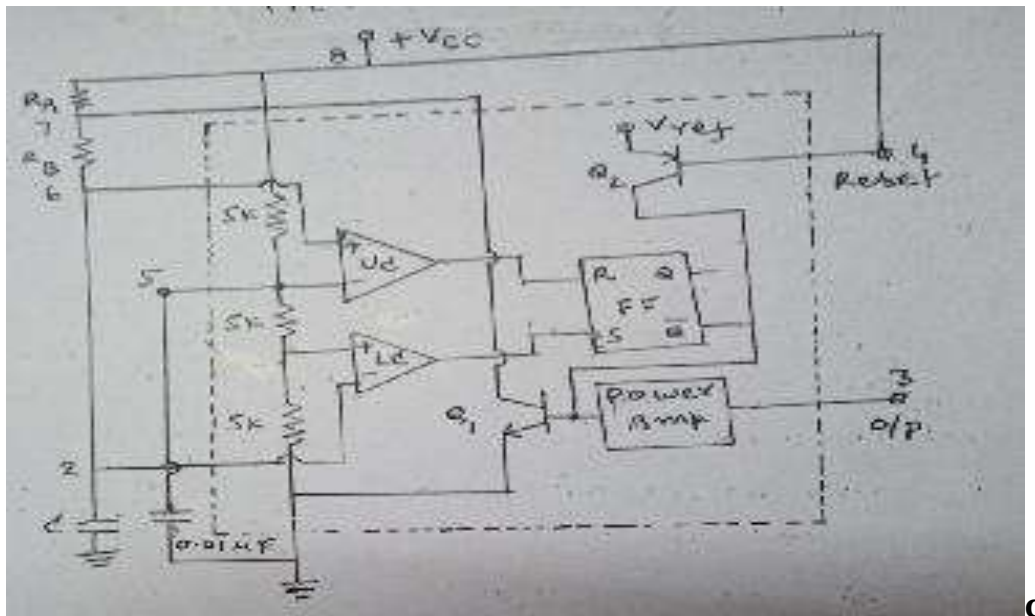


Fig. 4 (b): Functional Diagram for Astable Operation

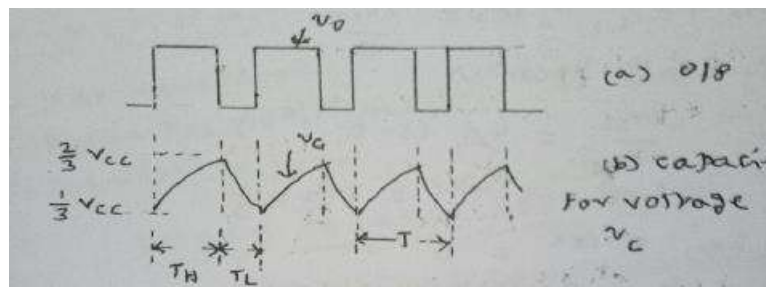


Fig. 5 (a) and (b): Waveforms of Astable Multivibrator

Fig. 4 (a) represents the pin connection diagram for 555 timer in astable mode. R_A and R_B are external resistors and C is external capacitor. Fig. 4 (b) shows the functional diagram. Compared to monostable operation, timing resistor R is split into two sections R_A and R_B . Pin 7 (collector of Q_1) is connected to the junction of A and B . When V_{CC} is connected, external capacitor C charges towards V_{CC} through R_A and R_B , with a time constant of $(R_A + R_B)C$. During this time output at pin 3 = High (i.e., $Q = 1$ and $Q' = 0$). Since $Q' = 0$, C is unclamped.

When v_c is just $> \frac{2}{3} V_{CC}$, Upper comparator (UC) resets FF. i.e., $Q = 0$ and $Q' = 1$. So Q_1 is **ON** ($V_{CE} = 0$) and C discharges through R_B with a time constant $R_B C$. For better operation R_A and R_B are taken large to limit current.

During discharging, when v_c is just $< \frac{V_{CC}}{3}$, lower comparator (LC) sets the FF. i.e., $Q = 1$ and $Q' = 0$. So Q_1 is OFF ($V_{CE} = V_{CC}$) and C is unclamped. Thus, C is charged and discharged periodically between $\frac{2V_{CC}}{3}$ and $\frac{V_{CC}}{3}$ respectively.

Fig. 5 (a) and Fig. 5 (b) shows the waveforms of output and voltage v_c across capacitor respectively.

Derivation for Time Period 'T' of Output:

We know that capacitor charge equation is given by

$$v_c(t) = v_f + (v_i - v_f)e^{-t/RC} \dots (1)$$

where v_i = Initial voltage

v_f = Final (target) voltage

Let t_H = Time taken for C to charge from $\frac{V_{CC}}{3}$ to $\frac{2V_{CC}}{3} = t_1 - t_2$

Where t_1 = Time taken to charge from 0 to $\frac{2V_{CC}}{3}$

and t_2 = Time taken to charge from 0 to $\frac{V_{CC}}{3}$

Let t_L = Time taken for C to discharge from $\frac{2V_{CC}}{3}$ to $\frac{V_{CC}}{3}$

For t_1 , $v_i = 0$ and $v_f = V_{CC}$.

∴ Eq. (1) becomes

$$\begin{aligned} v_c(t) &= V_{CC} + (0 - V_{CC})e^{-t/RC} \\ &= V_{CC}(1 - e^{-t/RC}) \dots (2) \end{aligned}$$

At $t = t_1$, $v_c(t) = \frac{2}{3}V_{CC}$

∴ Eq. (2) becomes

$$\frac{2}{3}V_{CC} = V_{CC}(1 - e^{-t_1/RC})$$

$$\text{i.e., } e^{-t_1/RC} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$\text{or } e^{t_1/RC} = \ln(3)$$

$$\text{i.e., } t_1 = RC \ln(3)$$

$$\text{i.e., } t_1 = 1.1 RC$$

For t_2 , $v_i = 0$ and $v_f = V_{CC}$.

$\therefore$ Eq. (1) becomes

$$\begin{aligned} v_c(t) &= V_{CC} + (0 - V_{CC}) e^{-t/RC} \\ &= V_{CC} (1 - e^{-t/RC}) \dots\dots (3) \end{aligned}$$

$$\text{At } t = t_2, v_c(t) = \frac{V_{CC}}{3}$$

$\therefore$ Eq. (3) becomes

$$V_{CC}/3 = V_{CC} (1 - e^{-t_2/RC})$$

$$\text{i.e., } e^{-t_2/RC} = 1 - \frac{1}{3} = \frac{2}{3}$$

$$\text{i.e., } e^{t_2/RC} = \frac{3}{2}$$

Taking logarithms on both sides, we get

$$\text{i.e., } t_2 = RC \ln\left(\frac{3}{2}\right)$$

$$\text{i.e., } t_2 = 0.405 RC$$

$$\therefore t_H = t_1 - t_2 = 1.1 RC - 0.405 RC$$

$$= 0.69 RC \text{ (where } R = R_A + R_B)$$

$$\text{Thus } t_H = \mathbf{0.69 (R_A + R_B)} \dots\dots (4)$$

For t_L , $v_i = \frac{2V_{CC}}{3}$, $v_f = 0$

$\therefore$ Eq. (1) becomes

$$\begin{aligned} v_c(t) &= 0 + \left(\frac{2V_{CC}}{3} - 0\right) e^{-t/RC} \\ &= \frac{2V_{CC}}{3} e^{-t/RC} \dots\dots (5) \end{aligned}$$

$$\text{At } t = t_L, v_c(t) = \frac{V_{CC}}{3}$$

$\therefore$ Eq. (5) becomes

$$V_{CC}/3 = (2 V_{CC}/3) e^{-t_L/RC}$$

$$\text{i.e., } e^{-t_L/RC} = \frac{1}{2}$$

$$\text{i.e., } e^{t_L/RC} = 2$$

Taking logarithms on both sides, we get

$$t_L / RC = \ln (2)$$

$$\text{i.e., } t_L = RC \ln (2) = 0.69 RC$$

Here $R = R_B$

$$\therefore t_L = 0.69 R_B C \dots (6)$$

$$\therefore T = t_H + t_L$$

$$\text{i.e., } T = 0.69 (R_A + 2R_B) C \{\text{from eqs. (4) and (6)}\}$$

$$\text{Frequency} = \frac{1}{T} = \frac{1}{0.69 (R_A + 2R_B) C} = \frac{1.45}{(R_A + 2R_B) C}$$

$$\% \text{ Duty cycle} = \frac{t_L}{t_L + t_H} \times 100\%$$

$$= \frac{0.69 R_B C}{0.69 (R_A + 2R_B) C}$$

$$= \frac{R_B}{(R_A + 2R_B)} \times 100\%$$

Problem 2: For the astable multivibrator in Fig. 4 (b), $R_A = 6.8 \text{ K}\Omega$, $R_B = 3.3 \text{ K}\Omega$ and $C = 0.1 \text{ }\mu\text{F}$. Calculate t_{HIGH} , t_{LOW} , free running frequency and duty cycle.

Solution:

$$t_{\text{HIGH}} = 0.69 (R_A + 2 R_B)$$

$$= 0.69 (6.8 \times 10^3 + 2 \times 3.3 \times 10^3) \times 0.1 \times 10^{-6}$$

$$= 0.7 \text{ mSec}$$

$$t_{\text{LOW}} = t_L = 0.69 R_B C$$

$$= 0.69 \times 3.3 \times 10^3 \times 0.1 \times 10^{-6}$$

$$= 0.23 \text{ mSec}$$

$$f = \frac{1.45}{(R_A + 2 R_B) C} = \frac{1.45}{(6.8 \times 10^3 + 2 \times 3.3 \times 10^3) \times 0.1 \times 10^{-6}}$$

$$= 1.07 \text{ KHz}$$

$$\text{Duty cycle} = \frac{R_B}{(R_A + 2R_B)}$$

$$= \frac{3 \times 10^3}{6.8 \times 10^3 + 2 \times 3.3 \times 10^3} = 0.25$$

$$\% \text{ Duty cycle} = 25\%$$

Applications of Astable Multivibrator:

1. FSK Generator
2. Pulse Position Modulator (PPM)
3. Schmitt Trigger

555 timer as Schmitt Trigger:

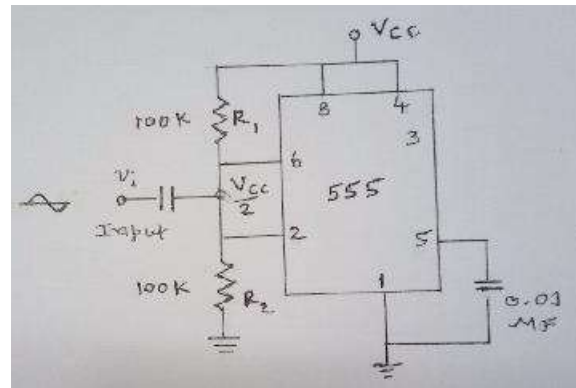


Fig. 6: 555 timer in Schmitt trigger operation

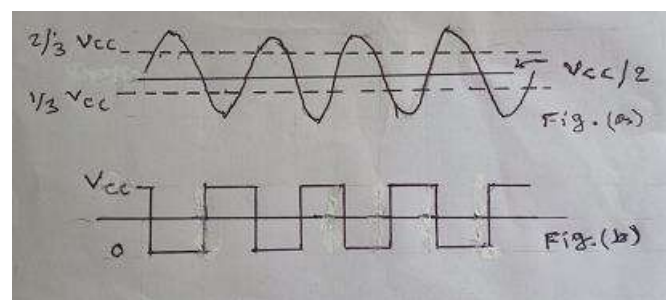


Fig. 7: Input and Output Waveforms

Fig. 6 shows the pin connections of 555 timer used as a Schmitt trigger. Here the two comparators are tied together and externally biased at $V_{CC}/2$ through R_1 and R_2 as shown. We know that Upper comparator trips at $\frac{2V_{CC}}{3}$ and lower comparator trips at $\frac{V_{CC}}{3}$. The bias provided by R_1 and R_2 is centered between these two limits. Now a sine wave is applied. If its amplitude exceeds $(\frac{2V_{CC}}{3} - \frac{V_{CC}}{3})$ reference levels, the internal FF sets and resets alternately and provides a square wave as shown in Fig. 7(a) and Fig. 7 (b) show the i/p signal. Here frequency of square wave is same as that of input signal.

PHASE LOCKED LOOPS (PLLs)

Phase Locked Loop (PLL) is an important block of linear systems. PLLs were first used in 1930s in communication applications. Previously, they were costly because they were realized in discrete form. Now PLLs are available as inexpensive ICs.

Principle of Operation of PLL:

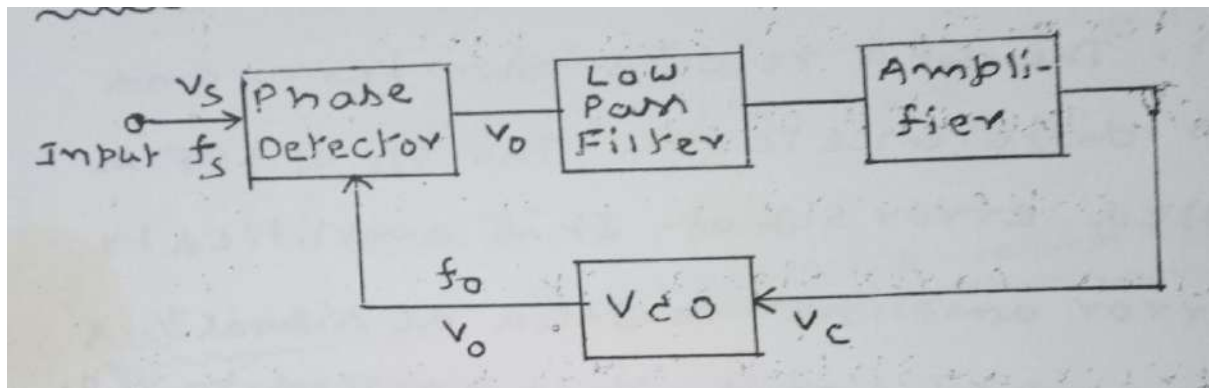


Fig. 8: Block diagram of PLL

Fig. 8 represents the block diagram of a PLL. It consists of a phase detector, Low Pass Filter (LPF), an amplifier and a Voltage Controlled Oscillator (VCO).

Let v_s = Input voltage
 f_s = Input frequency
 v_o = Output voltage
 f_o = Output frequency

Before i/p signal is applied, PLL is said to be in **free-running mode**. When i/p signal v_s of frequency f_s is applied to PLL, the phase detector (or mixer) compares the phase and frequency of v_s to that of the output v_o of VCO. If the 2 signals differ in frequency or phase angle, it generates an error voltage v_c .

The phase detector is basically a multiplier circuit. Its o/p mainly consists of sumterm ($f_s + f_o$) and difference term ($f_s - f_o$). The LPF rejects sum term and allow difference term. The o/p of LPF is called **error signal**. It is amplified by the error amplifier to get a dc signal ' v_c ' called **control signal**. This v_c is applied to VCO. It shifts the VCO frequency in a direction to reduce the difference between f_s and f_o . Once this action starts, PLL is said to be in **capture state**. The VCO frequency f_o continues to change until it equals the i/p frequency f_s . Then PLL is said to be in **locking state**. When locking occurs, the loop tracks any change in f_s .

Now the phase difference between i/p and o/p signals generates a corrective voltage v_c to shift the VCO frequency from f_o to f_s .

Important definitions related to PLL:

1. Lock-in range: It is the range of frequencies over which the PLL can maintain lock with the incoming signals.

2. Capture range: It is the range of frequencies over which the PLL can acquire lock with the i/p signals.

3. Pull-in time: It is the total time taken by PLL to establish lock.

More details (Short notes) on lock-in range and capture range:

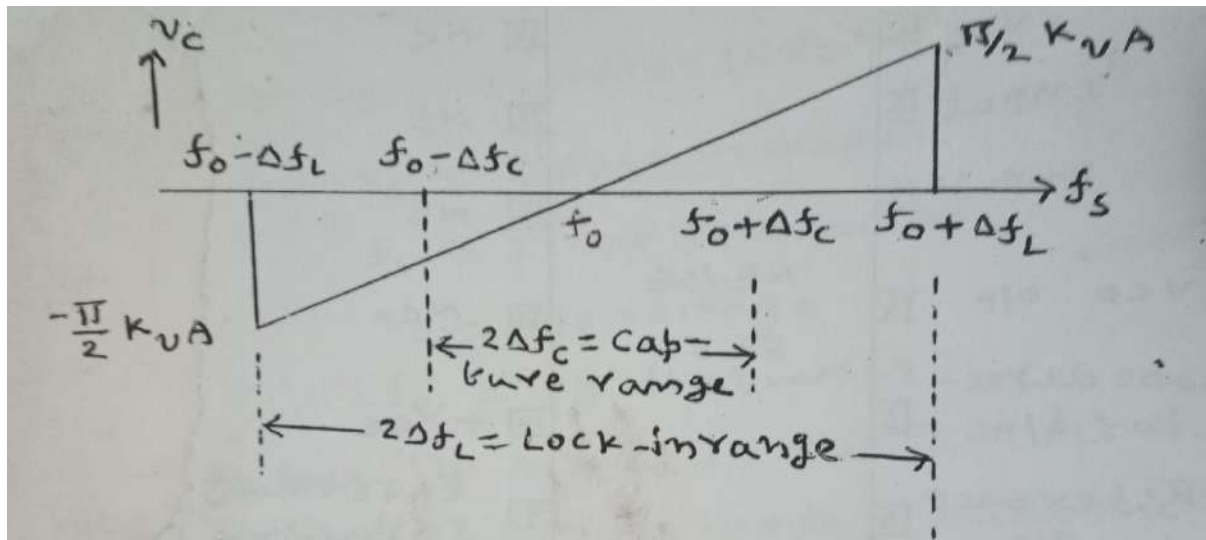


Fig. 9: Lock-in range and capture range of PLL

Let us consider a monolithic IC with analog phase detector.

Its **lock-in range** is given by

$$2 \Delta f_L = k_v k_\phi A \pi$$

Where k_v = Voltage to frequency transfer coefficient of PLL (**Hz/Volt**)

k_ϕ = Phase angle to voltage transfer coefficient of PLL (**Volt/Radian**)

and A = Voltage gain of amplifier

Its **capture range** is given by

$$2 \Delta f_C = 2 \sqrt{f_1 \cdot \Delta f_L}$$

Where $f_1 = \frac{1}{2\pi RC}$ = 3 dB frequency of LPF

$2 \Delta f_L$ = Total lock-in range

Fig. 9 shows the lock-in range $2 \Delta f_L$ and capture range $2 \Delta f_C$. Both ranges are expressed in % age of f_0 . Both ranges are symmetrically located w.r.t. VCO frequency f_0 . **Lock-in range is always > capture range.**

We need large capture range. But large capture range will make the PLL more susceptible to noise.

COMPONENTS OF PLL

- **Phase Detector (Phase comparator, or Mixer or multiplier circuit)**
- **Low Pass Filter**
- **Amplifier**
- **Voltage Controlled Oscillator**

Phase Detector:

Phase detector compares the phase and frequency of incoming signal v_s to that of output v_o of VCO. Its o/p mainly consists of sum term $(f_s + f_o)$ and difference term $(f_s - f_o)$. Output of phase detector is fed to the LPF.

There are 2 types of phase detectors: analog and digital. A balanced modulator is used as analog phase detector. An XOR gate serves as a digital phase detector.

Most of the monolithic PLL ICs use analog phase detectors. For discrete PLLs, digital phase detectors are preferred because of their simplicity.

Low Pass Filter:

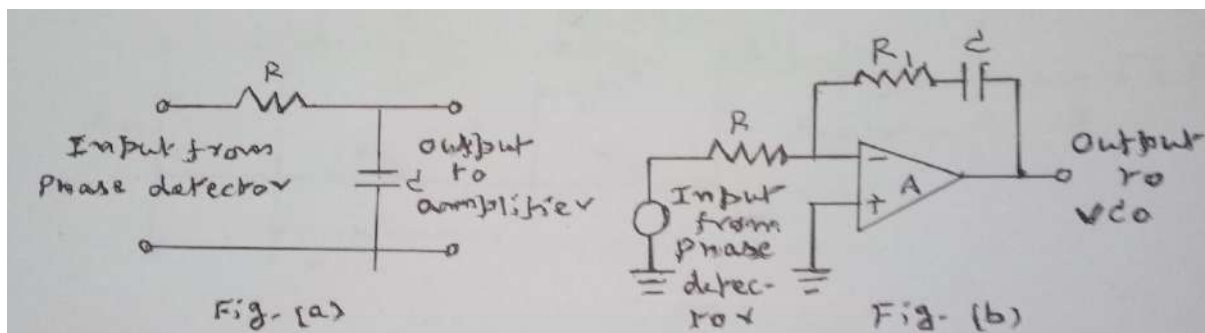


Fig.10: Low Pass Filter of PLL

Low pass filter removes the high frequency components and noise. It also controls the dynamic characteristics of the PLL such as lock-in and capture ranges, bandwidth and transient response.

If filter bandwidth is reduced, the response time increases. But it also reduces the capture range.

This produces a high noise immunity and locking stability.

Amplifier:

It is used to amplify the error signal, i.e., o/p of LPF.

Voltage Controlled Oscillator:

Initially when no input signal is given to PLL, it runs with a free running frequency f_o . When input is given, PLL action starts. Then v_c is the o/p of amplifier. It is a dc control voltage.

This v_c is applied to VCO. It shifts the VCO frequency in a direction to reduce the difference between f_s and f_o . Once this action starts, PLL is said to be in capture state. The VCO frequency f_o continues to change until it equals the i/p frequency f_s . Then PLL is said to be in locking state. When locking occurs, the loop tracks any change in f_s .

Now the phase difference between i/p and o/p signals generates a corrective voltage v_c to shift the VCO frequency from f_o to f_s .

MONOLITHIC PLL IC (NE/SE 565)

IC PLL 565 is available as a 14-pin DIP package and as a 10-pin metal can package.

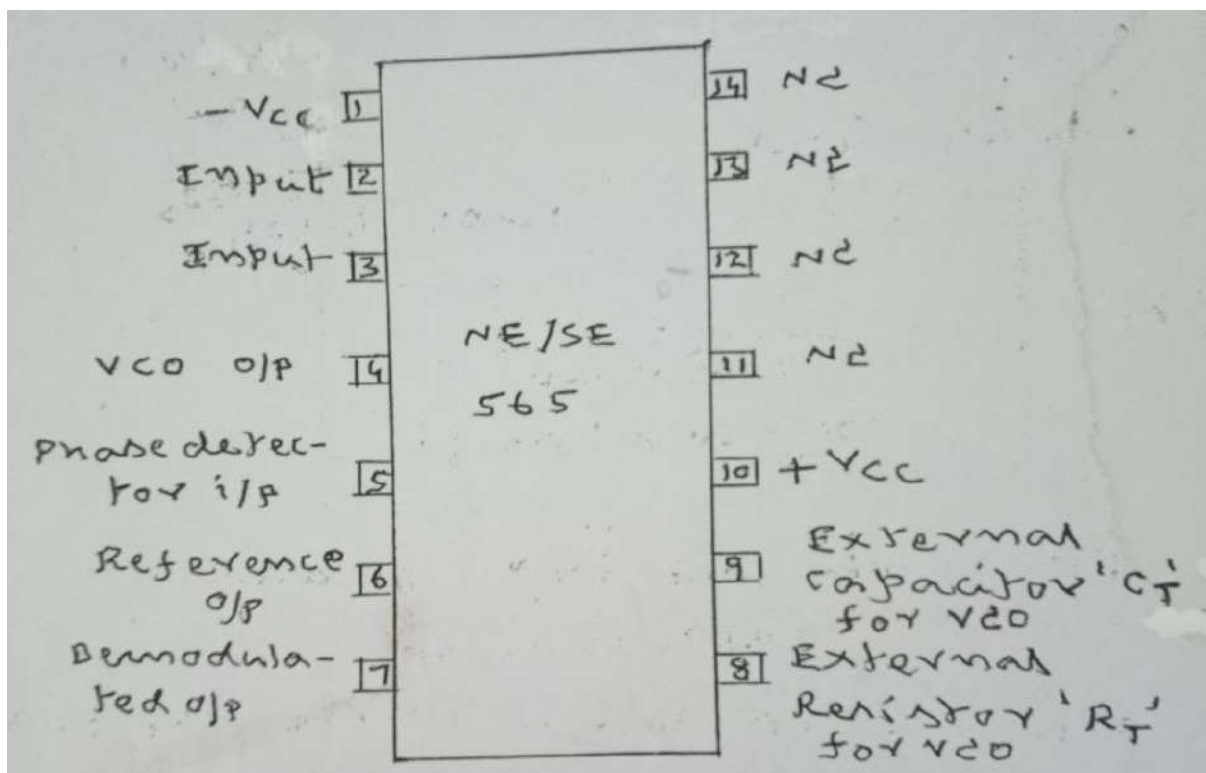


Fig. 11(a): Pin diagram of 565

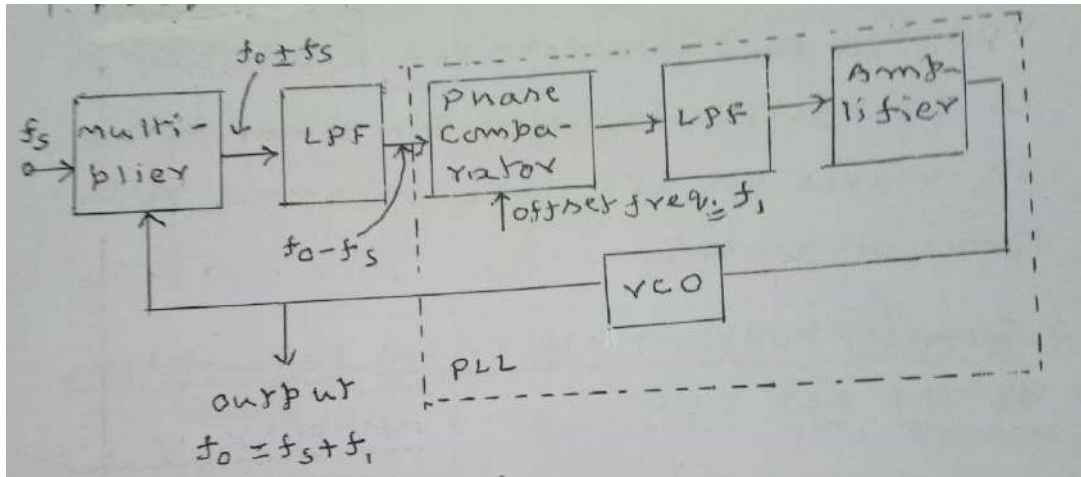


Fig. 12: Frequency translation using PLL

Here, a mixer (or multiplier) and an LPF are externally connected to PLL as shown in Fig. 12. Let f_s be the signal to be shifted in frequency (by an amount f_1). Let f_0 is the o/p of VCO. Then f_s and f_0 are the two inputs to the mixer (multiplier). Output of mixer contain $f_0 \pm f_s$.

$f_0 + f_s$ is rejected by LPF. So, LPF o/p contains $f_0 - f_s$.

This $f_0 - f_s$ is given as 1st input to phase comparator. Offset (or translation) frequency f_1 is given as 2nd i/p to comparator. When PLL is in locked state,

$$f_0 - f_s = f_1$$

i.e.,

$$f_0 = f_s + f_1$$

Thus, f_s is translated by an amount f_1 .

2. Frequency Multiplication and Division:

(a) Frequency Multiplication by N:

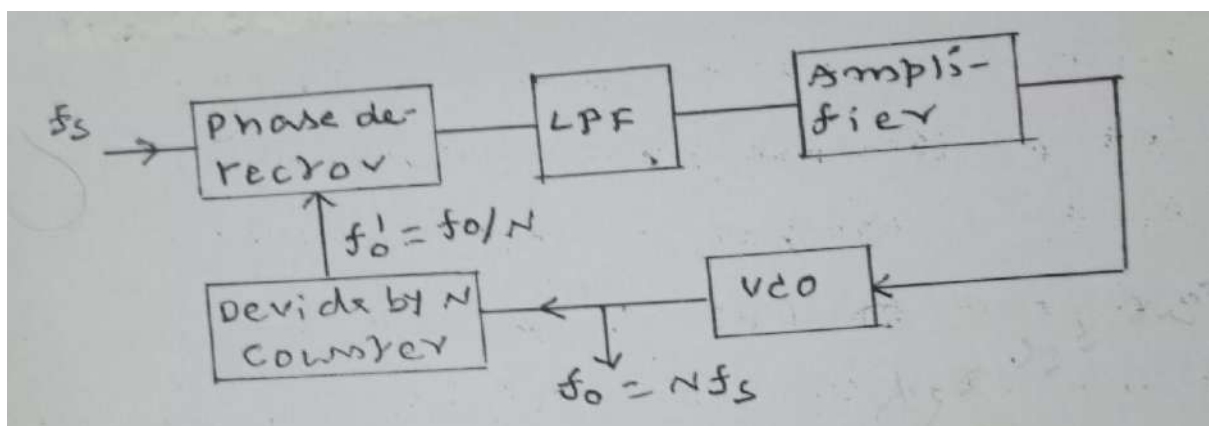


Fig. 13: Frequency Multiplier

Fig. 13 shows the block diagram of a frequency multiplier. Here a $\div N$ network (counter) is inserted between VCO and phase comparator. Let f_o' be the output. At locking,

$$f_s = f_o' = f_o/N$$

i.e., $f_o = N f_s$

Thus, the circuit acts as a frequency multiplier.

(b) Frequency Division by M:

Here $\div N$ network is not needed. If VCO is rich in harmonics, division is performed by locking M^{th} harmonic of VCO output to the input signal.

3. AM Detector:

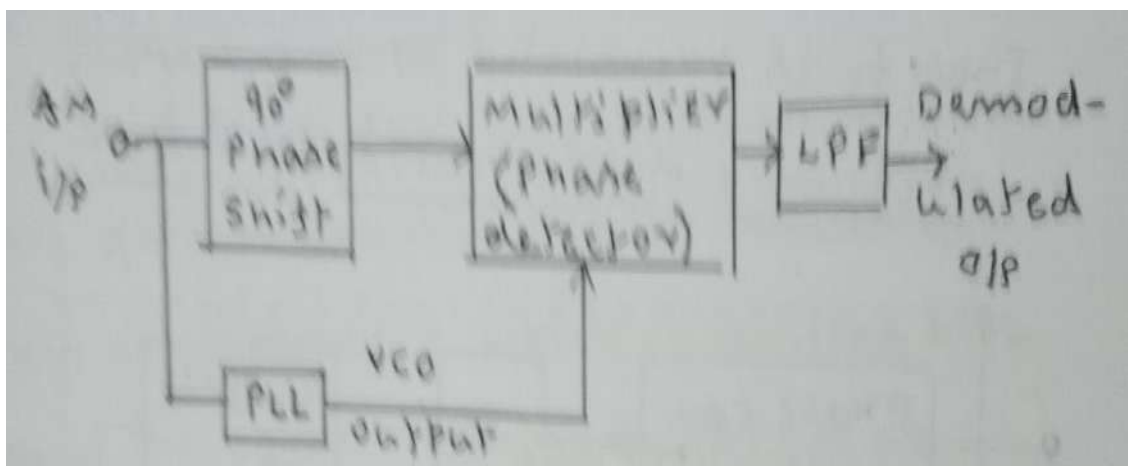


Fig. 14: AM Detector using PLL

Fig. 14 shows the block diagram of AM detector using PLL. Here PLL is locked to the carrier frequency of AM i/p. VCO o/p has same frequency of carrier. But it is 90° out of phase with AM signal. So, AM signal is shifted in phase by 90° before applying to multiplier. Thus, both inputs to multiplier are same in phase. Multiplier o/p consists of sum and difference terms. LPF allows only difference term. Output of LPF is demodulated o/p. This circuit has high selectivity and noise immunity.

4. FM demodulator:

Here PLL is locked to FM signal. VCO tracks the instantaneous frequency of the i/p signal. Output of LPF is demodulated o/p. It controls the VCO and maintains lock with the i/p signal.

5. FSK Demodulator:

In digital data communication, binary data is transmitted by means of a carrier frequency which is shifted between two pre-set values. This type of transmission is called Frequency Shift Keying (FSK). The binary data can be retrieved using an FSK demodulator using PLL.

Problem 3: Determine the dc control voltage v_c at lock, if the signal frequency $f_s = 10$ KHz, VCO free-running frequency is 10.66 KHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/Volt.

Solution:

We know that

$$f_s = f_0 + k_v v_c$$

$$\text{i.e., } v_c = \frac{f_s - f_0}{k_v}$$

$$\text{Given } f_s = 10 \text{ KHz} = 10000 \text{ Hz}$$

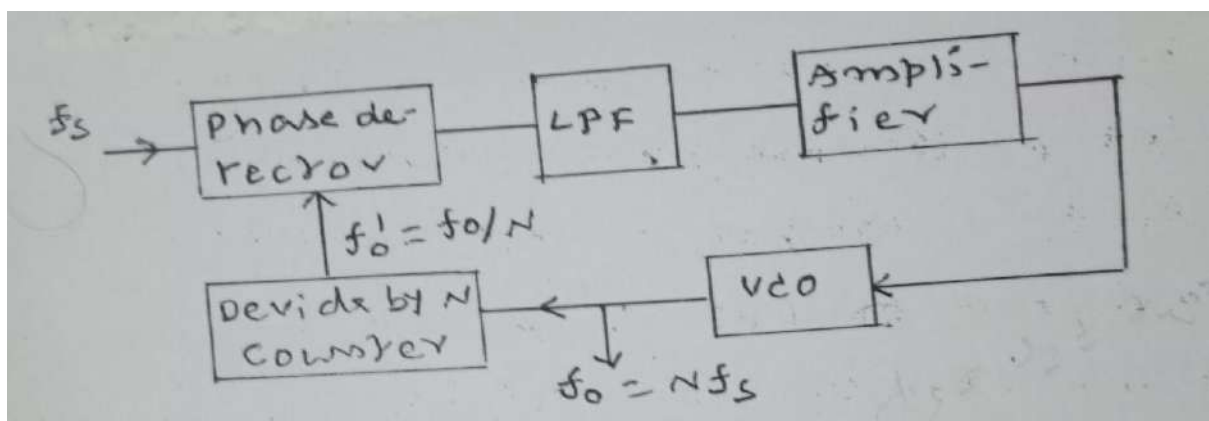
$$f_0 = 10.66 \text{ KHz} = 10660 \text{ Hz}$$

$$\text{And } k_v = 6600 \text{ Hz/Volt}$$

$$\therefore \text{DC control voltage } v_c = \frac{10000 - 10660}{6600} = -0.1 \text{ V}$$

Problem 4: For PLL, Determine the dc control voltage v_c at lock, if the signal frequency $f_s = 100$ KHz, VCO free running frequency is 5 MHz and the voltage to frequency transfer coefficient of VCO is 2 MHz/Volt and $N = 100$ in the frequency multiplier circuit given below. What is the dc voltage at lock?

Solution:



Given

$$f_s = 100 \text{ KHz}$$

$$f_0 = 5000 \text{ KHz}$$

$$N = 100$$

$$\therefore f_o = \frac{5000 \text{ KHz}}{N} = \frac{5000 \text{ KHz}}{100} = 50 \text{ Hz}$$

$$f_s = f_o' + k_v v_c$$

$$\begin{aligned} \text{i.e., } v_c &= \frac{f_s - f_o'}{k_v} \\ &= \frac{(100 - 50) \times 10^3}{2 \times 10^6} = 25 \text{ mV} \end{aligned}$$

Problem 5: A PLL has a free running frequency of 500 KHz and bandwidth of low pass filter (LPF) is 10 KHz. Will the loop acquire lock for an input signal of 600 KHz? Justify your answer. Assume that phase detector produces an o/p of 50 mV dc.

Solution:

O/p of phase detector contains sum term $f_s + f_o$ and difference term $f_s - f_o$

Given $f_s = 600 \text{ KHz}$ and $f_o = 500 \text{ KHz}$

$$f_s + f_o = 600 \text{ KHz} + 500 \text{ KHz} = 1100 \text{ KHz}$$

$$f_s - f_o = 600 \text{ KHz} - 500 \text{ KHz} = 100 \text{ KHz.}$$

Hence both sum and difference terms are outside the pass band.

So, loop will not acquire lock, irrespective of v_c value given.

QUESTION BANK ON UNIT-3

Main Questions

1. What are different types of Electrical filters? Define and describe the frequency response of each type.
2. Describe a first order LPF/HPF and derive the necessary expression for its transfer function. Also derive an expression for the magnitude of the Transfer Function in dB.
3. (a) What is a band pass filter? Derive an expression for the transfer function of a wide band pass filter.
(b) Problem on BPF.

4. What is an all pass filter (APF)? With the help of a diagram derive the necessary expressions for the magnitude of its o/p and phase angle between i/p and o/p. What is the main application of APF?
5. With the help of pin connection diagram and functional diagram explain the operation of a 555 timer in monostable mode. Derive an expression for its output pulse width.
5. With the help of pin connection diagram and functional diagram explain the operation of a 555 timer in astable mode. Derive an expression for its time period/frequency and duty cycle.
6. With the help of a block diagram, explain the principle of operation of PLL.
7. Describe 565 VCO used in PLL using Pin diagram and functional diagram.
8. Explain a monolithic IC (566 IC PLL)
9. Describe a second order LPF/HPF and derive the necessary expression for its transfer function. Also derive an expression for the magnitude of the Transfer Function in dB.

2 Marks Questions

1. Distinguish between analog active and passive filters.
2. What are the advantages of analog active filters over analog passive filters?
3. Draw the circuit of a first order wide BPF.
4. Draw the circuit of a wide BRF.
5. Draw the circuit of a notch filter.
6. What is an APF and what is its main application?
7. Draw the Circuit of a first order LPF.
8. Draw the Circuit of a first order HPF.
9. Draw the Circuit of a second order LPF.
10. Draw the Circuit of a second order HPF.
11. List the applications of a 555 timer in various areas.
12. Draw the block diagram of a PLL used for frequency translation.
13. Draw the block diagram of a PLL used for frequency multiplier.
14. What is the role of a phased detector in PLL?
15. What is the role of an LPF in PLL?

16. Define the terms lock-in range, capture range and pull-in time.
17. List the applications of a 555-timer used in monostable mode.
18. List the applications of a 555-timer used in astable mode.
19. What is the role of reset input in 555 timer?
20. What is the role of Pin 5 in a 555 timer?

UNIT-4

VOLTAGE REGULATORS AND CONVERTERS

Syllabus Contents:

Voltage Regulator: Introduction, Series OP–Amp regulator

, IC Voltage Regulators, IC 723 general purpose regulators, Switching regulators.

D to A and A to D Converters: Introduction, Basic DAC Techniques– Weighted resistor DAC, R–2R Ladder DAC, Inverted R–2R Ladder DAC, A to D Converters, Parallel comparator DAC, Counter type ADC, Successive approximation ADC, Dual slope ADC, DAC and ADC specifications.

D TO A & A TO D CONVERTERS

Some electronic systems operate on only digital signals. If analog signals are available, we need to convert them to digital form. This can be done by a circuit called Analog to Digital ('A to D' or A/D) converter or ADC.

Similarly, some electronic systems operate with only analog signals. If digital signals are available, we need to convert them to analog form. This can be done by a circuit called Digital to Analog ('D to A' or D/A) converter or DAC.

DIGITAL TO ANALOG CONVERTERS (DACs)

A DAC is a circuit which converts digital signals into analog form.

Basic DAC Technique:

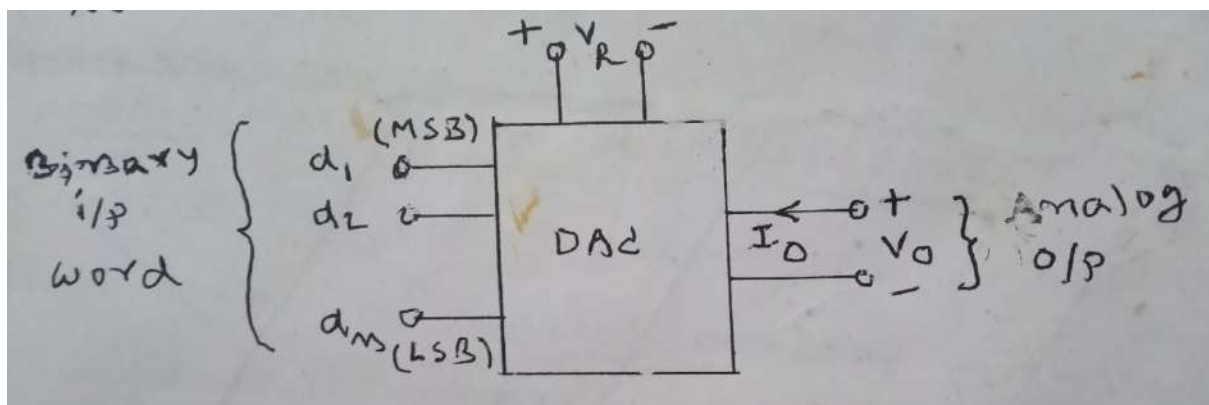


Fig. 1: Schematic diagram of a DAC

Fig. 1 shows the schematic diagram of an n-bit DAC. Its i/p is an n-bit binary word. It is combined with a reference voltage V_R to produce an analog o/p signal. It may be voltage or current. If o/p is voltage, it is given by

$$v_o = K V_{FS} (d_1 2^{-1} + 2^{-2} + \dots \dots \dots d_n 2^{-n})$$

Where

v_o = o/p voltage

V_{FS} = Full scale o/p voltage

K = Scaling factor (usually $K = 1$)

$d_1 d_2 \dots d_n$ = n-bit binary fractional word with decimal point at the left.

d_1 = MSB with a weight of $\frac{V_{FS}}{2}$

d_n = LSB with a weight of $\frac{V_{FS}}{2^n}$

Types of DACs:

1. Binary weighted resistor type DAC
2. r- ladder type DAC
3. Inverted R-2R ladder type DAC

1. BINARY WEIGHTED RESISTOR TYPE DAC

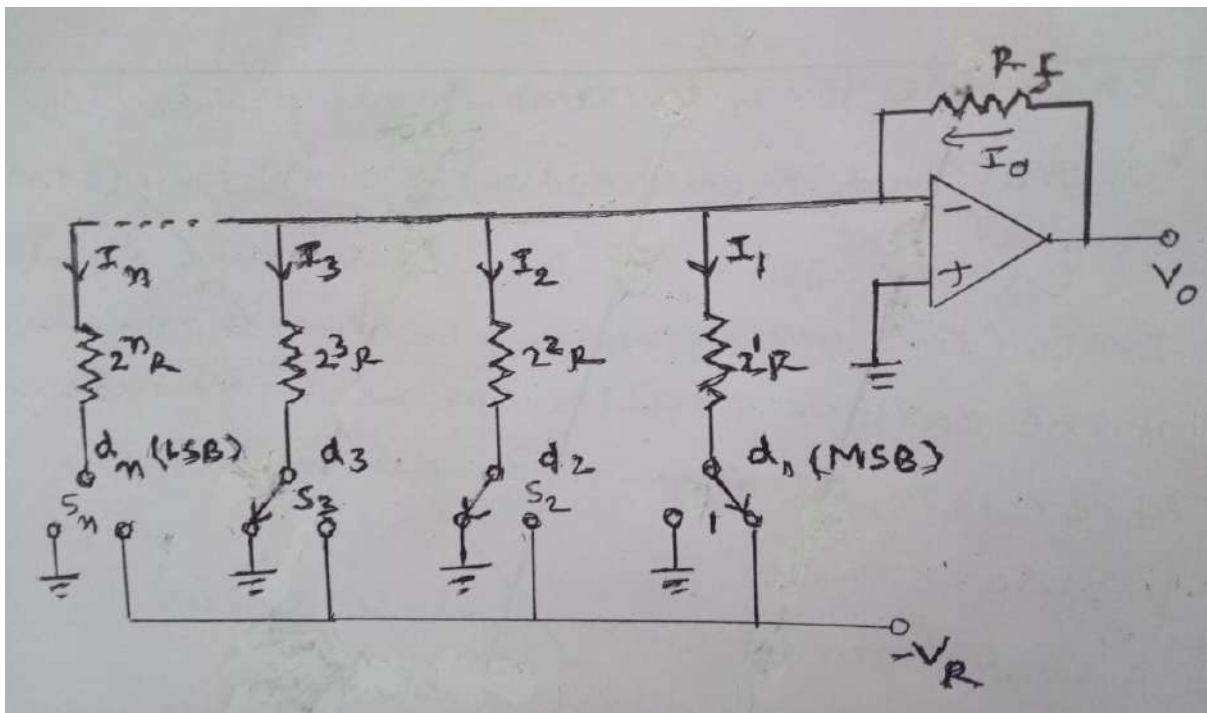


Fig. 2 (a): Binary weighted resistor type DAC

Fig. 2 (a) shows a binary weighted resistor type DAC. Here opamp is in inverting mode. We can also use non-inverting mode.

Opamp is a summing amplifier. It acts as a current-to-voltage converter.

$S_1, S_2, \dots, S_n$ are MOSFET switches used as Single pole double throw (SPDT) switches.

Upper end of any switch is connected to – ve terminal of opamp. Lower end of any switch S_i ($i = 1, 2, \dots, n$) has two positions. In left position, S_i is grounded. In right position, it connects a resistor $2^i R$ to reference voltage $-V_R$. Polarity of V_R may be + ve or – ve. Here V_R is taken – ve.

From Fig. 2 (a), we write

$$\begin{aligned}
 I_0 &= I_1 + I_2 + \dots + I_n \\
 &= \frac{V_R}{2^1 R} d_1 + \frac{V_R}{2^2 R} d_2 + \dots + \frac{V_R}{2^n R} d_n \\
 &= \frac{V_R}{R} \{d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}\} \\
 \therefore v_o &= I_0 R_f = V_R \frac{R_f}{R} \{d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}\} \dots (1)
 \end{aligned}$$

But general equation of a DAC is

$$v_o = K V_{FS} (d_1 2^{-1} + 2^{-2} + \dots + d_n 2^{-n}) \dots (2)$$

Comparing eqs. (1) and (2). We get

$$R_f = R \quad K = 1 \quad \text{and} \quad V_{FS} = V_R$$

Accuracy and stability of this DAC depends on the accuracy and temperature tracking of resistors.

Fig. 2 (b) show the transfer characteristics of a 3-bit weighted resistor DAC. It is a staircase waveform. The inclined dashed line passes through averages of o/p value in each step.

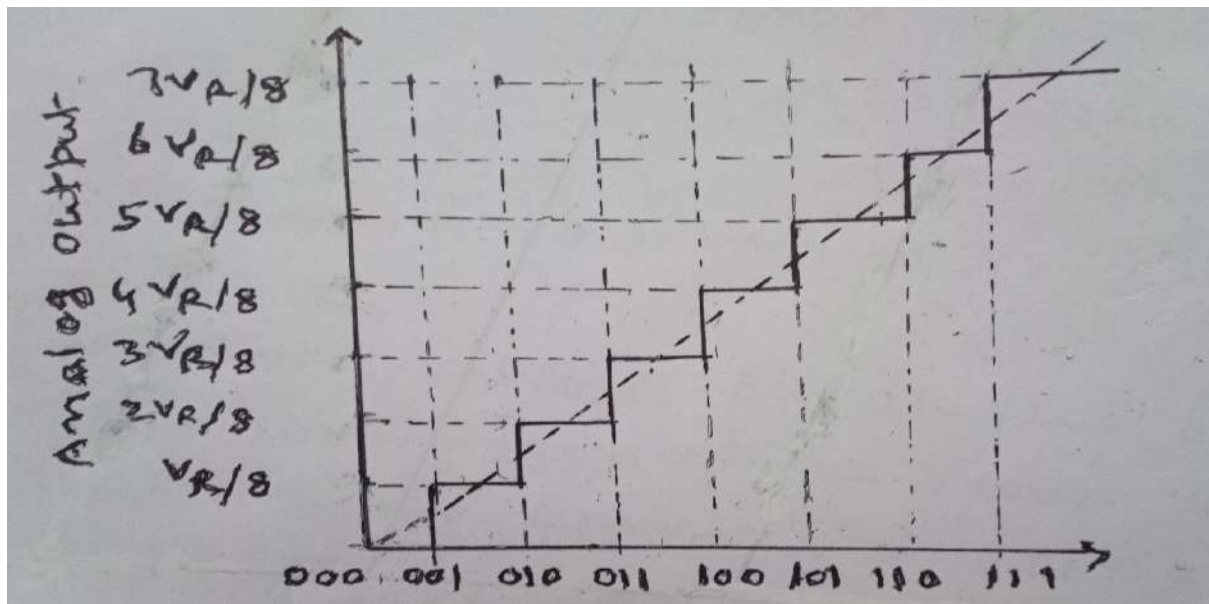


Fig. 2 (b) Waveform for binary weighted DAC

Problem with this DAC:

It needs wide range of resistor values. We use large number of bits to increase the resolution. This increases the range of resistor values.

Example:

If smallest resistor is $2.5\text{ K}\Omega$, largest one is $5.2\text{ M}\Omega$. Such large resistance cannot be fabricated in IC form. Also, voltage drop across it affects the accuracy.

If smallest resistor is $< 2.5\text{ K}\Omega$, it causes loading effect.

So, this type of DAC is very difficult to fabricate in IC form.

2. R-2R LADDER TYPE DAC

Wide range of resistors are required in binary weighted resistor DAC. This problem can be avoided by using R-2R ladder DAC, where only two resistor values are required.

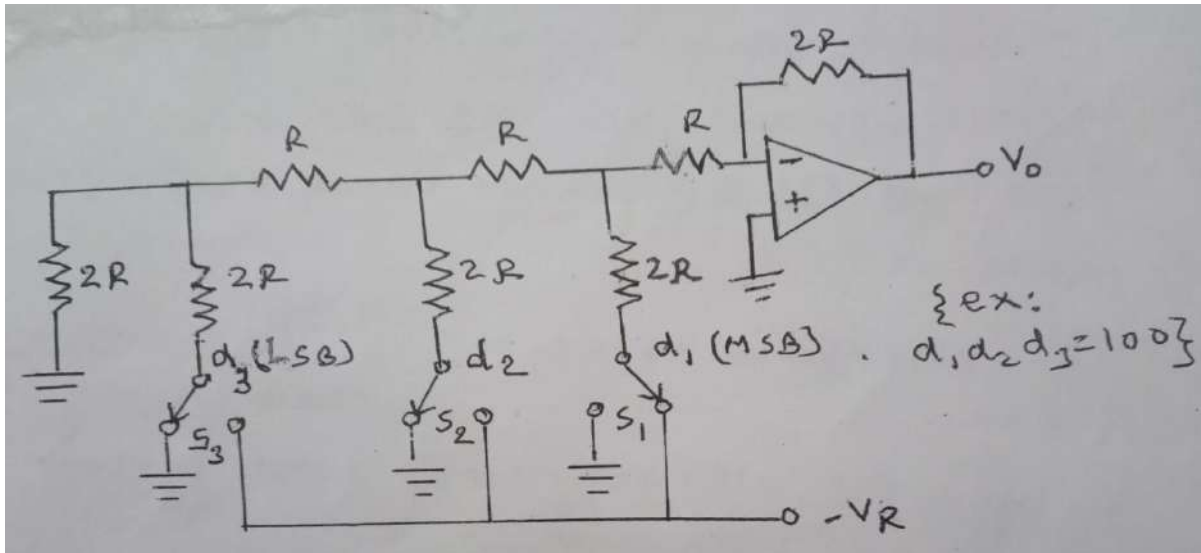


Fig. 3 (a): R-2R ladder type DAC

Fig. 3 (a) shows a 3-bit R-2R ladder DAC. Its binary input word is $d_1 d_2 d_3$, where d_1 = and d_3 = LSB. S_1 , S_2 and S_3 are 3 MOSFET switches used as Single pole double throw (SPDT) switches.

Upper end of each switch is connected to – ve terminal of opamp. Lower end of any switch S_i ($i = 1, 2, 3$) has two positions. In left position, S_i is grounded. In right position, it connects a resistor $2R$ to reference voltage $-V_R$. Polarity of V_R may be + ve or – ve. Here V_R is taken – ve.

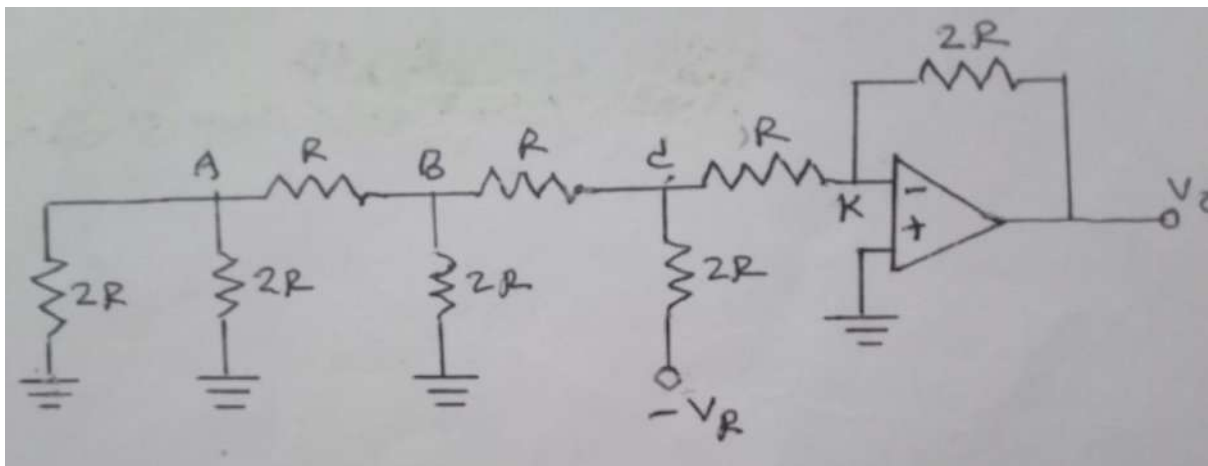


Fig. 3 (b)

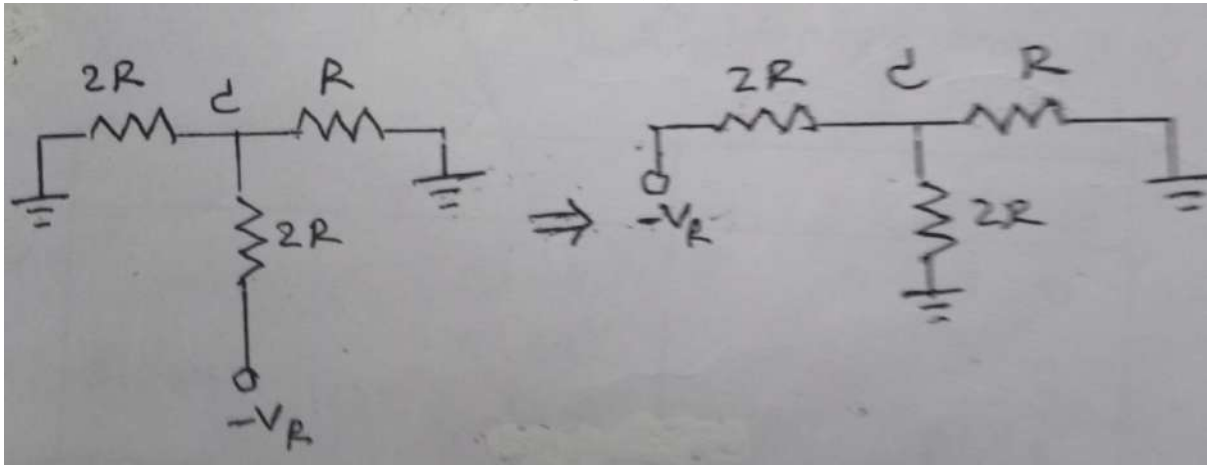


Fig. 3 (c)

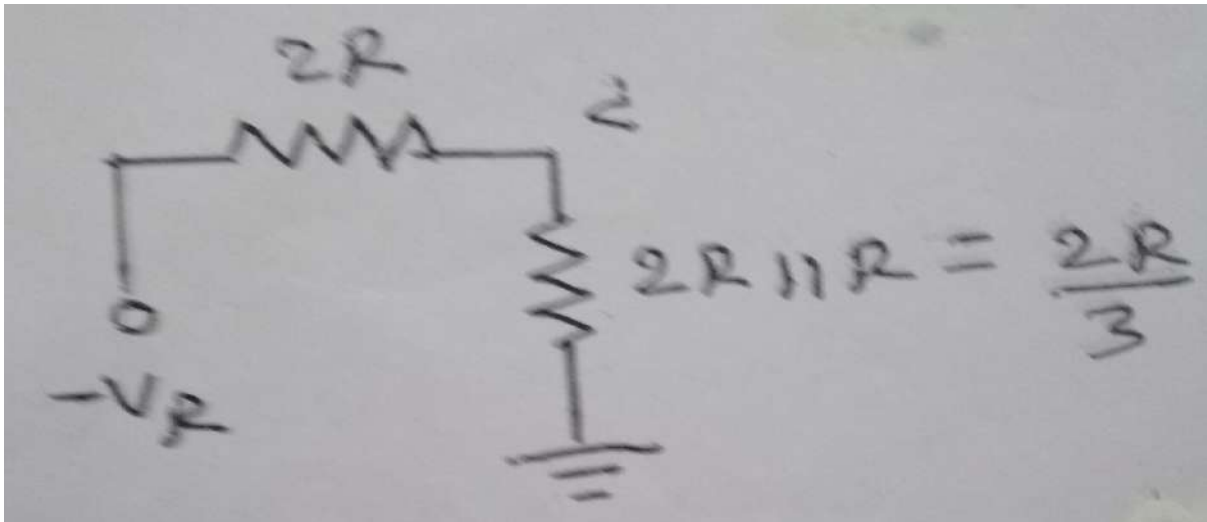


Fig. 3 (d)

Fig. 3 (b) shows equivalent circuit for Fig. 3 (a), where $d_1 d_2 d_3 = 100$.

Using network analysis, Fig. 3 (b) reduces to Fig. 3 (c) and then Fig. 3 (d).

$$\text{Voltage at node C} = -V_R \cdot \frac{\frac{2R}{3}}{2R + \frac{2R}{3}} = -V_R \cdot \frac{2R}{8R} = -\frac{V_R}{4}$$

Then Fig. 3 (e) represents the final circuit.

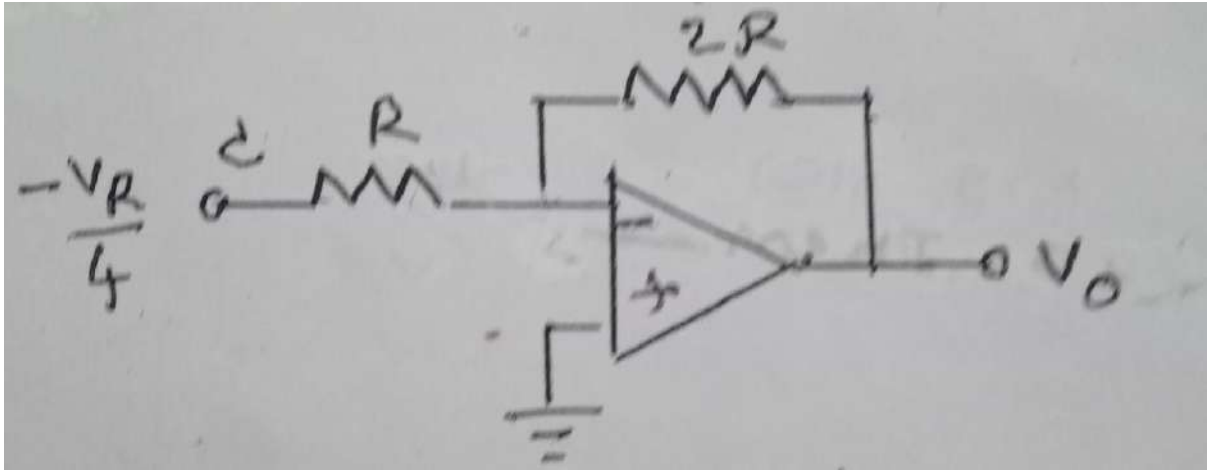


Fig. 3 (e) Final equivalent circuit

From Fig. 3 (e), we get

$$v_o = -\frac{V_R}{4} \left(\frac{-2R}{R} \right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

Similarly, we can find v_o for any value of $d_1 d_2 d_3$.

3. INVERTED R-2R LADDER TYPE DAC

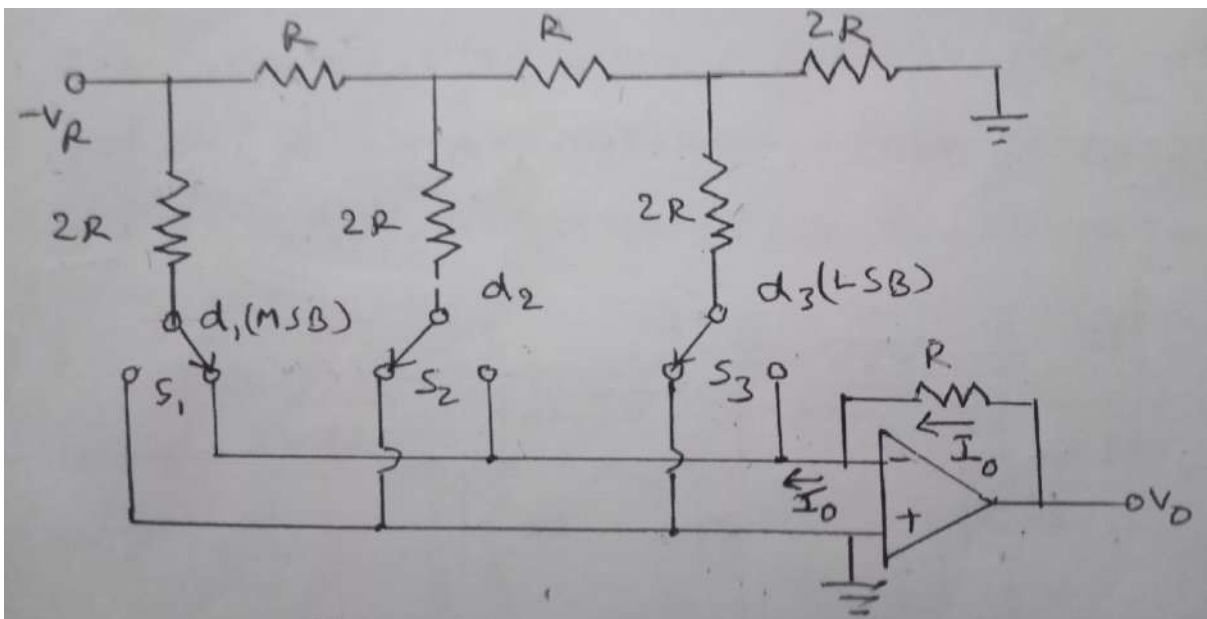


Fig. 4 (a): 3-bit Inverted ladder DAC

Fig. 4 (a) shows a 3-bit Inverted ladder DAC. Compared to ladder DAC, positions of MSB and LSB are interchanged.

S_1 , S_2 and S_3 are 3 MOSFET switches of SPDT type. In left position, S_i is grounded. In right position, any switch is connected to the – ve terminal of an

ideal opamp, which acts as a virtual ground. Since both terminals of any switch are at ground potential, current flowing in any resistor branch is constant and independent of switch position (i.e., input binary word).

Important property of this circuit is that current divides equally at each node. It is because equivalent resistance to the left of any node or right of any node is $2R$.

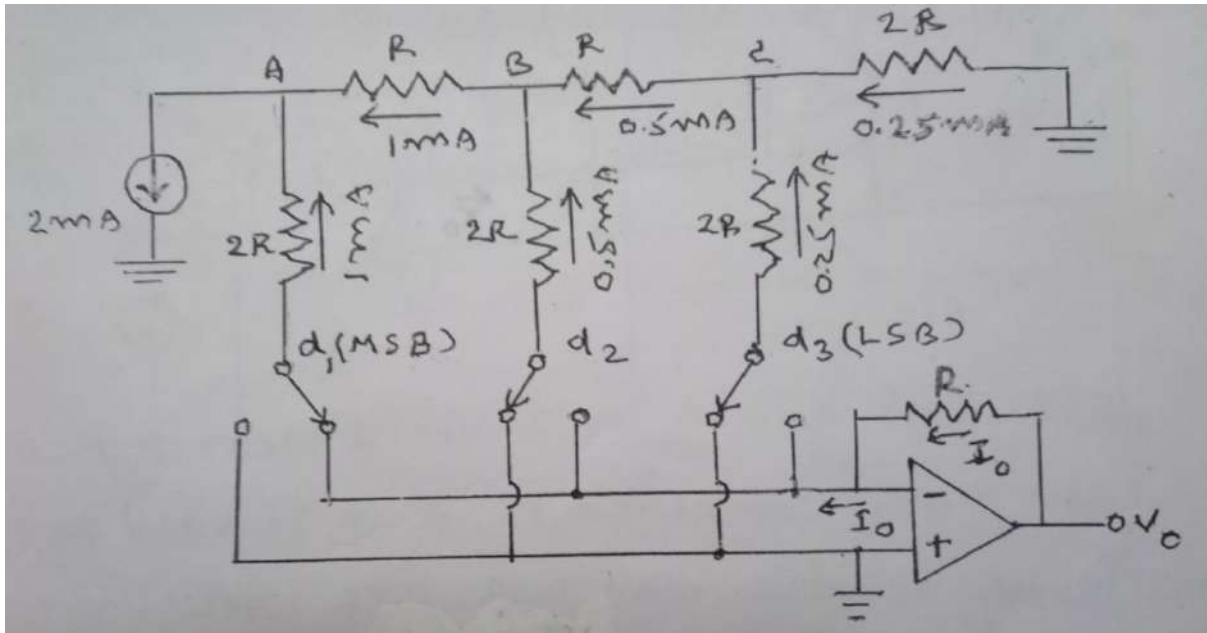


Fig. 4 (b) Illustrative example with 2 mA current

Fig. 4 (b) illustrates the division of a 2 mA current at each node. For example, current divides equally as 1 mA to the left and right of node A.

Current remains constant in any resistive branch. So, nodal voltages remain constant at $\frac{V_R}{2^0}$, $\frac{V_R}{2^1}$ and $\frac{V_R}{2^2}$. But current I_0 in feedback resistor depends on input binary word.

The circuit works on the principle of summing currents and operates in current mode.

Problem 4.1: The basic step of an 8-bit DAC is 10.2 mV. If 00000000 represents 0 Volts, what is the o/p produced if the i/p is 10010111?

Solution:

The o/p produced for input 10010111

$$= 10.2 \text{ mV} (1 \times 2^7 + 0 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$$

$$= 10.2 \text{ mV} \times 151 = 1.54 \text{ V}$$

Problem 4.2: Calculate the values of LSB, MSB and full-scale output for an 8-bit DAC for 0 to 10 V range.

Solution:

$$\text{LSB} = \frac{V_{FS}}{2^n} \text{ and } \text{MSB} = \frac{V_{FS}}{2}$$

Given that $V_{FS} = 10 \text{ V}$ and $n = 8$

$$\therefore \text{LSB} = \frac{10 \text{ V}}{256} = .039 \text{ V} = 39 \text{ mV}$$

$$\text{MSB} = \frac{10 \text{ V}}{2} = 5 \text{ V}$$

$$\begin{aligned} \text{Full scale o/p} &= V_{FS} - 1 \text{ LSB} \\ &= 10 \text{ V} - 0.039 \text{ V} \\ &= 9.961 \text{ V} \end{aligned}$$

Problem 4.3: What o/p voltage would be produced by a 4-bit DAC whose o/p range is 0 to 10 V, for a digital input 0110?

Solution:

$$\text{Output voltage} = V_{FS} (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4})$$

Given that $V_{FS} = 10 \text{ V}$ and $d_1 d_2 d_3 d_4 = 0110$

$$\begin{aligned} \therefore \text{Output voltage} &= 10 \text{ V} (0 \times \frac{1}{2} + 1 \times \frac{1}{4} + 1 \times \frac{1}{8} + 0 \times \frac{1}{16}) \\ &= \frac{30}{8} \text{ V} = 3.75 \text{ V} \end{aligned}$$

ANALOG TO DIGITAL CONVERTERS (DACs)

An ADC is a circuit which converts analog signals into digital form.

Basic ADC Technique:

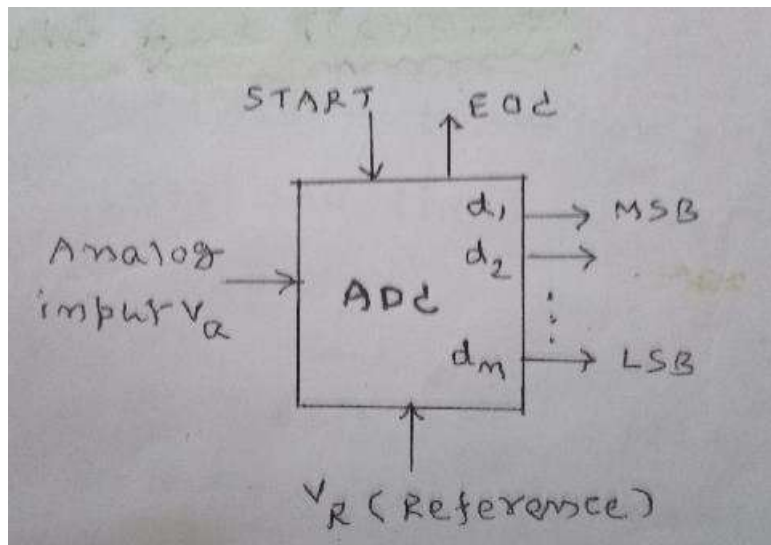


Fig. 5: Schematic diagram of an n-bit ADC

Fig. 5 shows the schematic diagram of an n-bit ADC. V_a is its analog input voltage. Its digital o/p is $d_1 d_2 \dots d_n$, where $d_1 = \text{MSB}$ and $d_n = \text{LSB}$.

Functional value of **output** = $D = d_1 2^{-1} + 2^{-2} + \dots + d_n 2^{-n}$

ADC has 2 additional control lines START and EOC. START input indicates beginning of conversion, EOC (End of conversion) output indicates end of data conversion.

Applications of ADCs:

- (i) Microprocessor interfacing
- (ii) To directly drive LCD and LED displays
- (iii) Digital voltmeters

Classification of ADCs:

ADCs are mainly classified as Direct type ADCs and Integrating type ADCs.

Direct type ADCs compare a given analog signal with internally generated equivalent signal.

Direct type ADCs:

1. Flash type ADC
2. Counter type ADC
3. Servo tracking ADC
4. Successive approximation type ADC

Integrating type ADCs (Indirect type ADCs) perform conversion in an indirect manner. They first convert the analog signal to a linear function of time (or frequency) and then to a digital code

Integrating type ADCS:

1. Single slope ADC
2. Dual slope ADC

Direct Type ADCs:

1. FLASH TYPE ADC (PARALLEL COMPARATOR TYPE ADC)

It is the simplest, **fastest** and costly ADC.

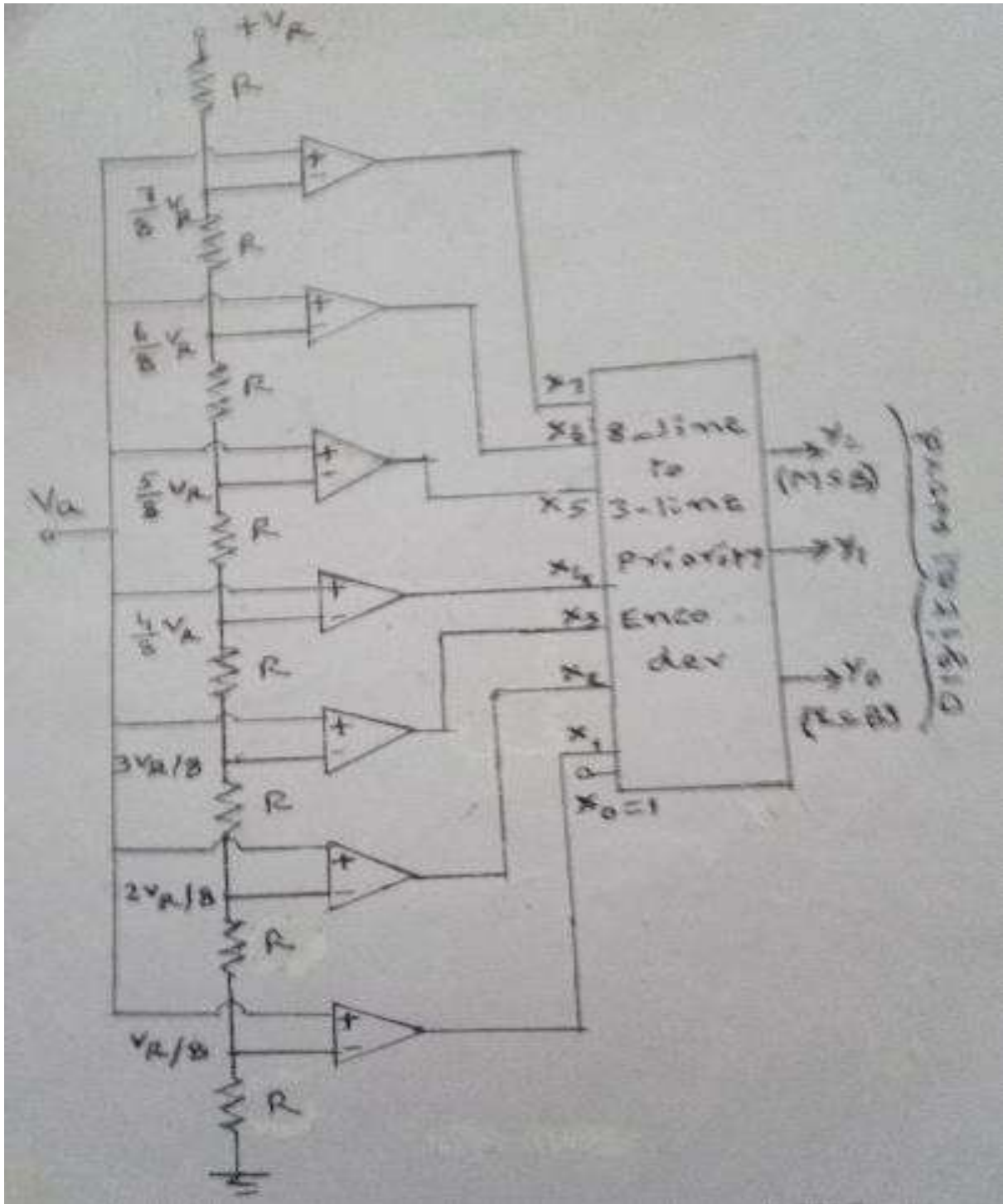


Fig. 6 (a): 3-bit flash ADC

Fig. 6 (a) shows the circuit of a 3-bit flash ADC. It consists of a voltage divider, 7 comparators and an 8-line to 3-line priority encoder. Analog voltage V_a is applied to the +ve terminal of opamp comparators, $X_1, X_2, \dots, X_7$ are the outputs of the comparators as shown. $X_0, X_1, \dots, X_7$ are the inputs to priority encoder, where $X_0 = 1$. $Y_2 Y_1 Y_0$ is the binary output word where $Y_2 = \text{MSB}$ and $Y_0 = \text{LSB}$.

8 resistors form a voltage divider between reference voltage V_R and ground. Let v_d be the input, fed to $-$ ve terminal of opamps, where v_d changes from $\frac{V_R}{8}$ to $\frac{7V_R}{8}$ as shown.

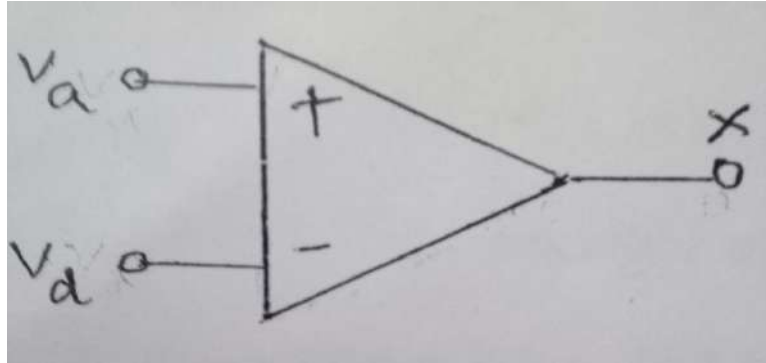


Fig. 6 (b) Comparator

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

Fig. 6 (c) Comparator truth table

Input voltage v_a	X7	X6	X5	X4	X3	X2	X1	X0	Y2	Y1	Y0
0 to $\frac{5V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to $\frac{8V_R}{8}$	1	1	1	1	1	1	1	1	1	1	1

Fig. 6 (d) Truth table for flash ADC

Fig. 6 (b) shows any comparator circuit. Fig. 6 (c) shows truth table of comparator. Fig. 6 (d) shows the truth table for the flash ADC. The circuit compares v_a with each nodal voltage.

Here conversion takes place in parallel (simultaneously) rather than sequentially. Conversion time is limited by speed of comparators and speed of priority encoder.

Drawback of the flash ADC:

An n -bit flash ADC requires $2^n - 1$ comparators where n is the number of bits in binary o/p word. i.e., number of comparators approximately doubles for each added bit. Also, the larger the value of n , the more complex is the priority encoder.

SUCCESSIVE APPROXIMATION TYPE ADC

It uses successive approximation technique and converts analog voltage to digital form.

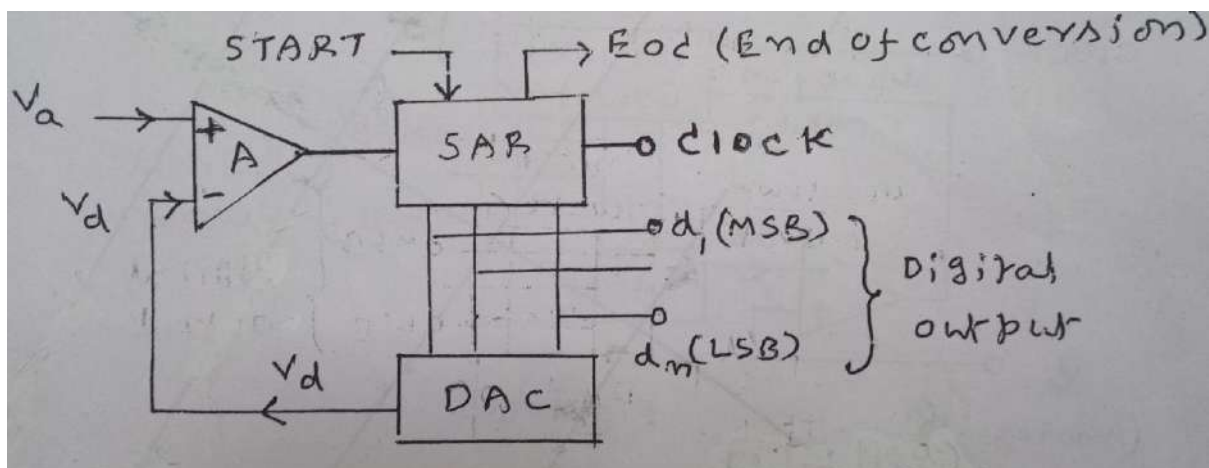


Fig. 7 (a)

Fig. 7 (a) shows the block diagram of an 8-bit successive approximation ADC. SAR stands for successive approximation register. Opamp 'A' is used as a comparator. V_a is the analog voltage to be converted to digital form. V_d is the analog o/p voltage of DAC. Output of SAR is a digital word $d_1 d_2 \dots d_n$, where $d_1 = \text{MSB}$ and $d_8 = \text{LSB}$.

This 8-bit ADC requires 8 clock pulses for conversion process. An extra (9th) pulse is used to load the output register and reinitialize the circuit.

SAR finds required value of each bit in digital o/p by trial and error.

When SAR receives START command, it sets MSB to '1' and other bits to zero. So, trial word is 10000000.

Comparator compares v_a and v_d .

If $v_d < v_a$, trial word is < correct word. Then MSB is left at 1 and next (2^{nd}) MSB is set to 1.

If $v_d > v_a$, trial word is > correct word. Then MSB is set to 0 and next (2^{nd}) MSB is set to 1.

The procedure is repeated for all bits (from MSB to LSB). Whenever $v_d > v_a$, the comparator changes its state.

For simplicity's sake, let us consider a 4-bit ADC as an example.

Then, Fig. 7 (b) indicates the conversion sequence for a typical analog input.

Correct digital word	v_d	Comparator output
1 1 0 1 ↑ MSB ↑ 2 nd MSB ↑ LSB	1 0 0 0	1
	1 1 0 0	1
	1 1 1 0	0
	1 1 0 1	1
	1 1 0 1	—

Fig. 7 (b): Conversion sequence

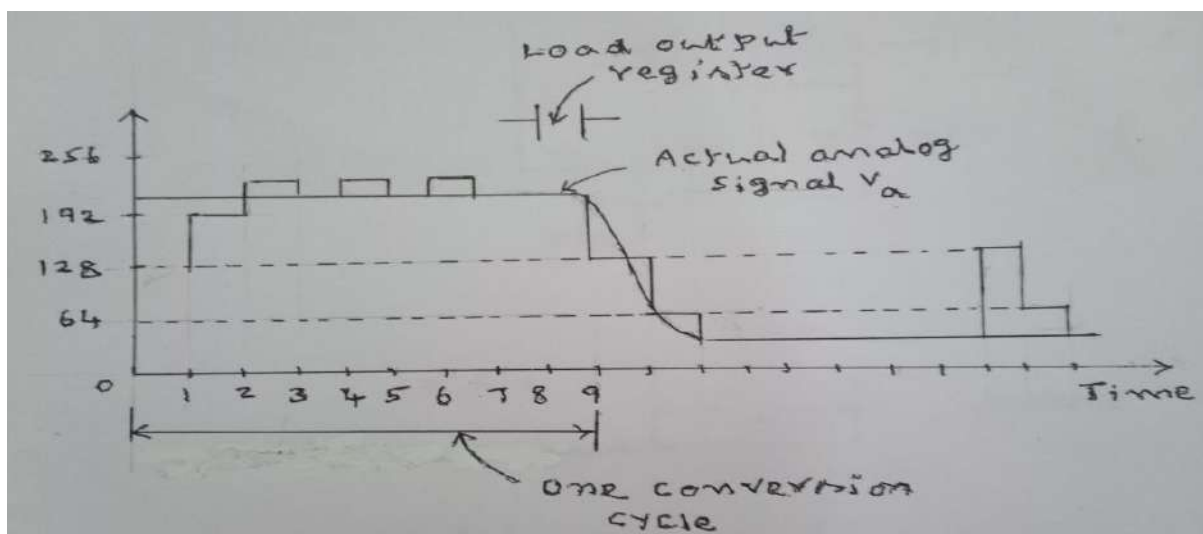


Fig. 7 (c): DAC output waveform

Fig. 7 (c) shows DAC o/p voltage waveform. Here the o/p voltage becomes successively closer to the actual analog i/p voltage.

DUAL SLOPE ADC (DUAL RAMP ADC)

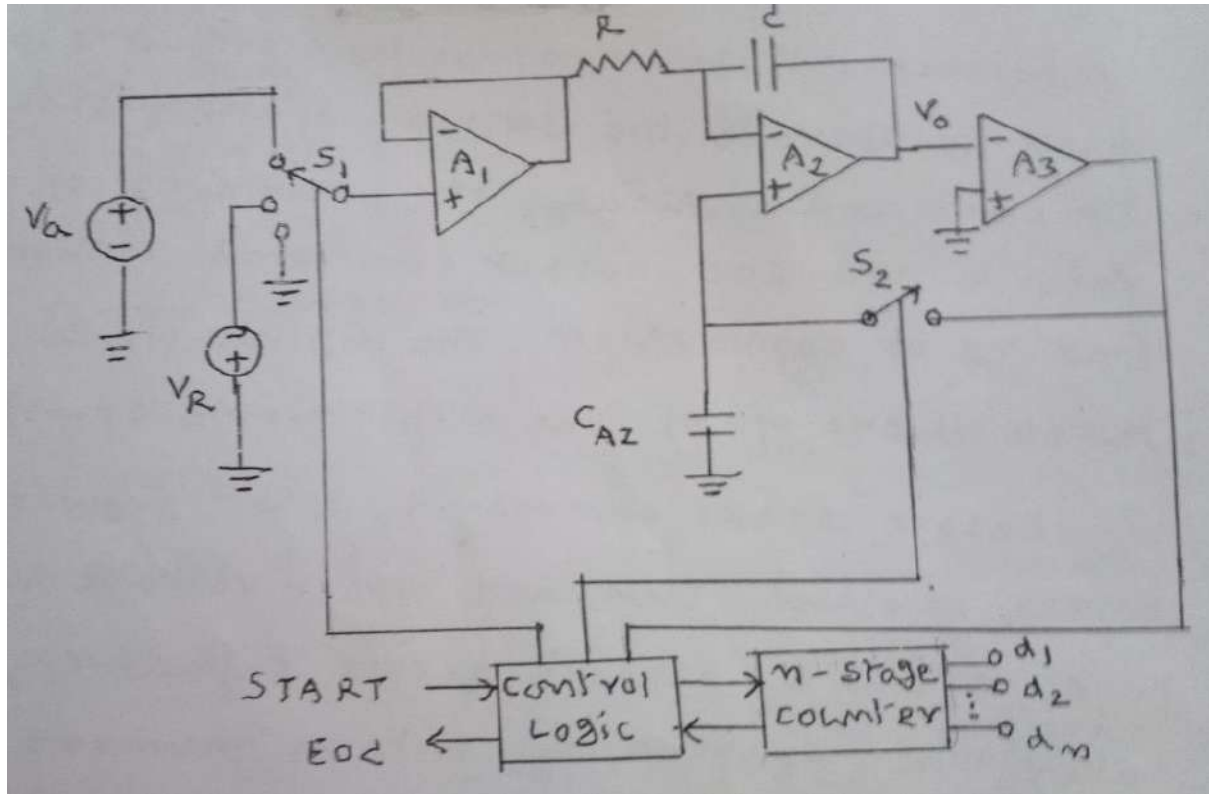
**Fig. 8 (a): Functional diagram of dual slope ADC.**

Fig. 8 (a) shows functional diagram of dual slope ADC. Opamps A_1 , A_2 and A_3 act as buffer, integrator and comparator respectively. V_a is analog i/p voltage. – V_R is an internal reference voltage. Control logic circuitry is used to operate the switches S_1 and S_2 . START input command indicates the beginning of conversion and EOC output command indicates the ending of conversion. The digital o/p is taken at the o/p of the n-bit ripple counter.

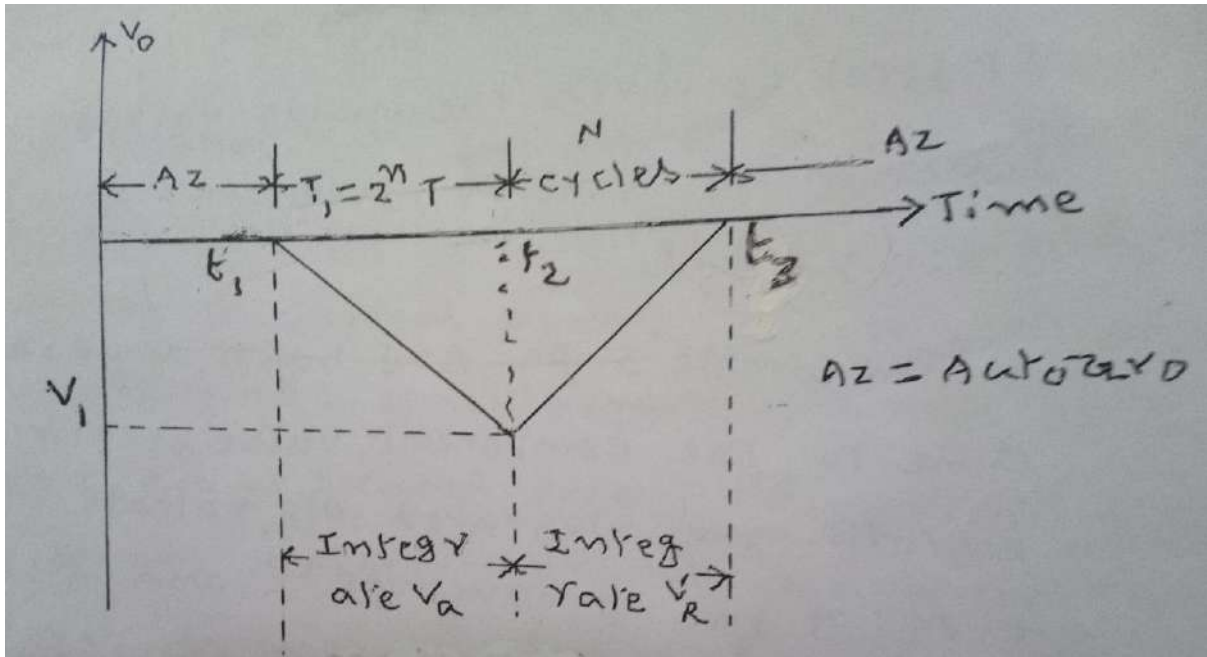


Fig. 8 (b) Output waveform for dual slope ADC

Fig. 8 (b) shows the o/p waveform for dual slope ADC. Before start command, S_1 is grounded and S_2 is closed. Then any offset voltage due to A_1 , A_2 and A_3 appears across capacitor C_{AZ} (AZ means auto zero). Later, when S_2 opens, C_{AZ} acts as memory and holds i/p offset compensating voltage.

Let START command is given at $t = t_1$. Then control logic opens S_2 and connects S_1 to v_a . It also enables counter start from zero count. The counter resets after 2^n clock pulses, say at $t = t_2$. Let T be the clock period. Then time of integration T_1 for v_a is given by

$T_1 = t_2 - t_1 = 2^n T$ where n is the number of bits of ripple counter.

During T_1 , output of integrator v_o is – ve going ramp voltage.

After T_1 control logic connects S_1 to $-V_R$. Now $-V_R$ is integrated and v_o is a + ve going ramp voltage. When v_o becomes zero at $t = t_3$ (say after N clock pulses), control logic issues EOC command.

Derivation:

$$T_1 = t_2 - t_1 = 2^n T \quad \dots (1)$$

$$t_3 - t_2 = NT \quad \dots (2)$$

For an integrator

$$v_o = - \frac{1}{RC} \int v_i dt \quad \dots (3)$$

At $t = t_2$, $v_o = V_1$ (as shown in figure)

Here $v_i = v_a$

∴ Eq. (3) becomes

$$\begin{aligned} V_1 &= -\frac{1}{RC} \int_{t_1}^{t_2} v_a dt = -\frac{v_a}{RC} (t_2 - t_1) \\ &= -\frac{v_a}{RC} 2^n T \quad \{\text{From eq. (1)}\} \\ &\dots\dots (4) \end{aligned}$$

V_1 is given in terms of V_R as

$$\begin{aligned} V_1 &= -\frac{1}{RC} \int_{t_3}^{t_2} -V_R dt = \frac{V_R}{RC} (t_2 - t_3) \\ &= \frac{V_R}{RC} (-NT) \quad \{\text{using Eq. (2)}\} \\ &= -\frac{V_R NT}{RC} \dots\dots (5) \end{aligned}$$

Eqs. (4) and (5) $\Rightarrow$

$$-\frac{v_a}{RC} 2^n T = -\frac{V_R}{RC} NT$$

$$\text{i.e.,} \quad v_a = V_R \left(\frac{N}{2^n} \right)$$

Since V_R and n are constant, v_a is directly proportional to N and is independent of R , C and T .

Advantages of dual slope ADC:

- (i) It is available in monolithic form, which is compatible with microprocessors and LED displays.
- (ii) It provides excellent noise rejection.
- (iii) Suitable for accurate measurement of slowly varying signals (e.g.: outputs of thermocouples and weighing scales)
- (iv) Used in many instrumentation and control systems.

Disadvantage:

It has long conversion time (around 20 mSec). i.e., it is slow.

Problem 4.4: A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum i/p voltage is + 10 V. The maximum integrator o/p voltage should be – 8 V, when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 μ F. Find the value of resistor R . Refer to Fig. 8 (a).

Solution:

$$\text{Clock period} = \frac{1}{4 \text{ MHz}} = \frac{1}{4 \times 10^6} \text{ Hz}$$

$$t_2 - t_1 = 2^n T = \frac{2^{16}}{4 \times 10^6} = 16.38 \text{ mS}$$

$$\text{Output of integrator } v_o = - \frac{v_a}{RC} (t_2 - t_1)$$

$$\text{Given } v_o = -8 \text{ V, } v_a = 10 \text{ V and } C = 0.1 \times 10^{-6}$$

$$\begin{aligned} \therefore R &= \frac{-1}{v_o C} v_a (t_2 - t_1) \\ &= \frac{-1}{-8 \times 0.1 \times 10^{-6}} \times 10 \times 16.38 \times 10^{-3} \\ &= 205 \Omega \end{aligned}$$

Problem 4.5: If analog voltage in the problem 4.4 is 4.129 V, find the equivalent digital number.

Solution:

$$v_a = V_R \left(\frac{N}{2^n} \right)$$

$$\begin{aligned} \therefore N &= \frac{v_a}{v_R} 2^n \\ &= \left(\frac{4.129 \text{ V}}{8 \text{ V}} \right) 2^{16} \\ &= 33825 \end{aligned}$$

Above decimal value is equivalent to the binary value 1000010000100001

DAC/ADC SPECIFICATIONS**1. Resolution:**

It is the smallest change in DAC output, when its i/p is changed. It is given as

$$\text{Resolution} = \frac{V_{FS}}{2^N - 1} \text{ volts (= 1 LSB increment)}$$

Where V_{FS} = Full scale o/p voltage

and n = number of bits

Resolution of ADC is defined as the smallest change in analog input for one-bit change at the o/p.

Example: For an 8-bit DAC with $V_{FS} = 10 \text{ V}$,

$$\text{Resolution} = \frac{10}{2^8 - 1} = 0.3922$$

$$\% \text{ Resolution} = \text{Resolution} \times 100\% = 39.22\%$$

2. Linearity:

It tells how close is the actual o/p of a DAC to its ideal o/p. It is expressed as a fraction of LSB or % age of V_{FS} . It is determined by the fitted line passing through measured outputs.

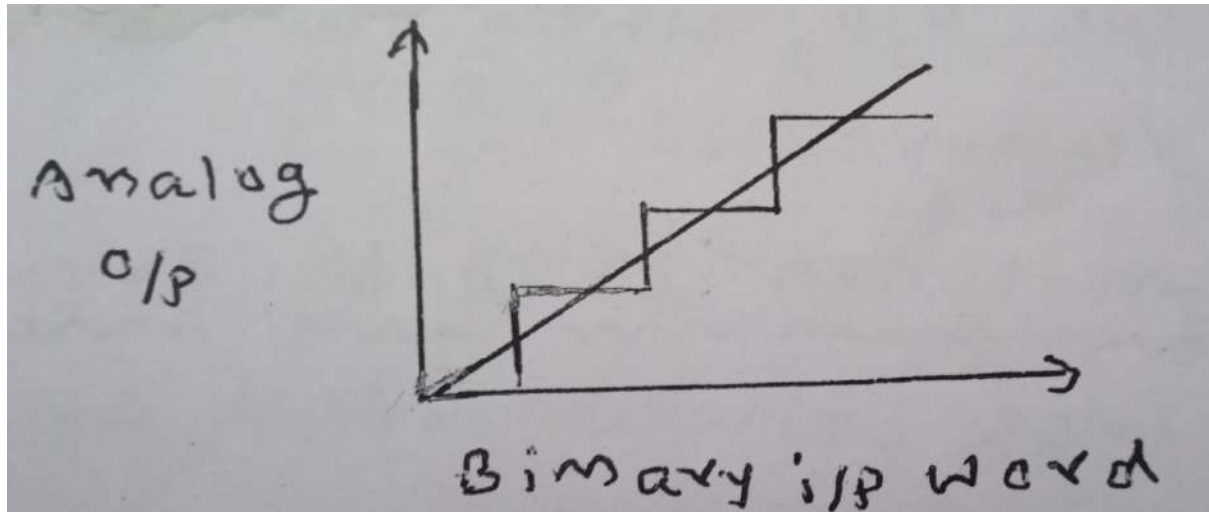


Fig. 9: Linearity

If the staircase o/p waveform is symmetrical w.r.t. the line as shown in Fig. 9, DAC is said to be linear. Otherwise, DAC is said to have linearity error.

3. Offset and Gain Errors:

Offset error is the o/p of DAC for a digital code, for which the o/p should be zero. Gain error is the difference in slope between the gain of ideal DAC and actual gain. They are indicated in Fig. 10 and Fig. 11 respectively.

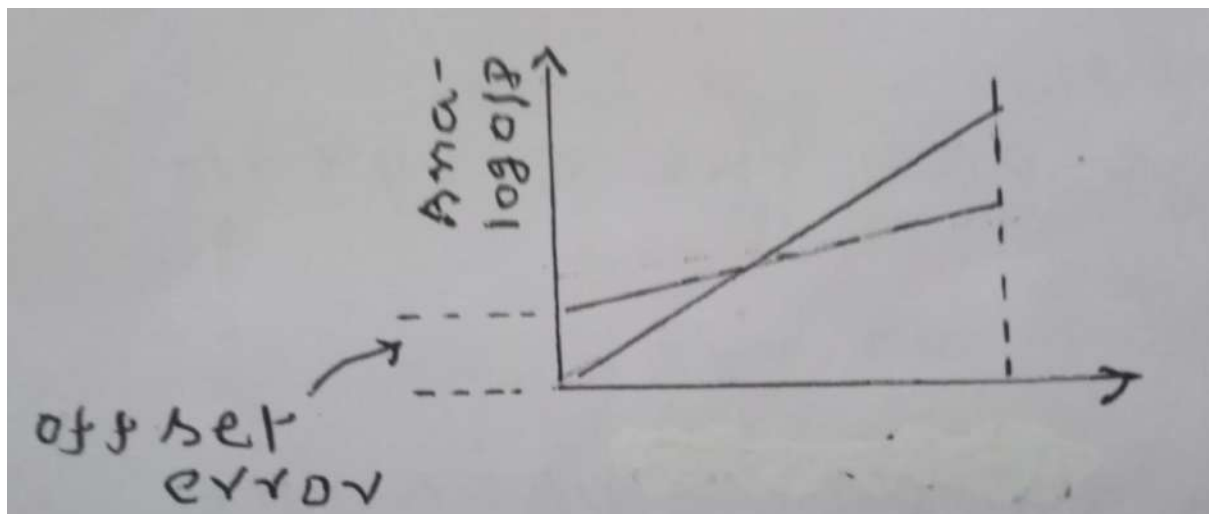
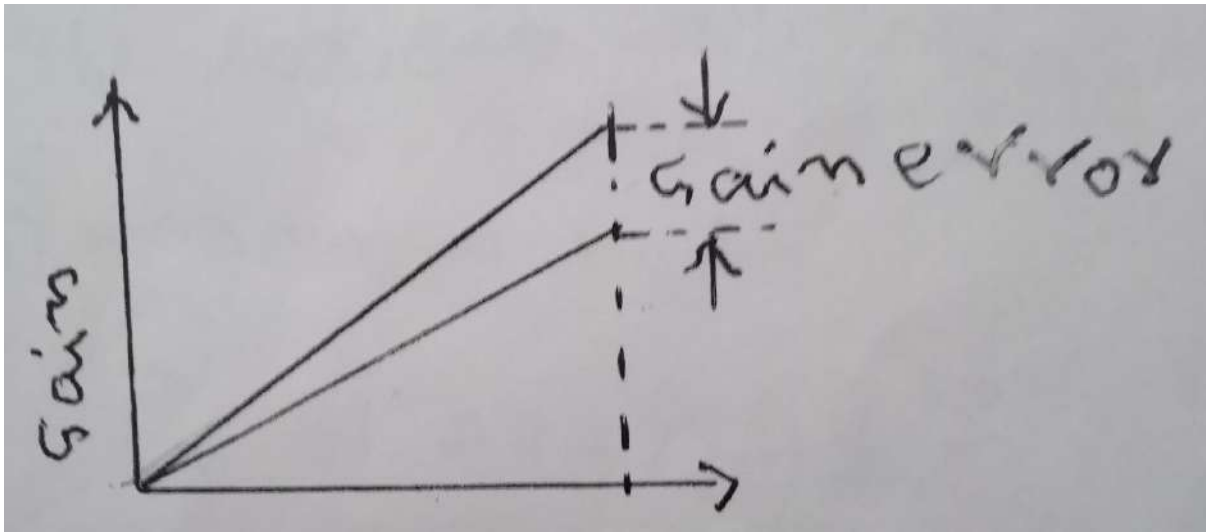


Fig. 10: Offset error**Fig. 11: Gain error****4. Settling Time:**

It is the time taken by the DAC output to settle within a range of $\pm \left(\frac{1}{2}\right)$ LSB of its final value. It ranges from 100 nS to 10 μ S.

5. Accuracy:

(i) Absolute Accuracy:

It is the maximum deviation between actual o/p and ideal o/p of a DAC.

(ii) Relative accuracy:

It is the maximum deviation between actual o/p and ideal o/p, when gain and offset errors are removed.

(iii) It is the difference between the ideal and measured o/p for successive binary i/p codes.

6. Monotonicity:

A monotonic DAC is a DAC whose analog o/p increases for increase in its digital i/p. For a monotonic DAC, the error is $< \pm \left(\frac{1}{2}\right)$ LSB.

All commercially available DACs are monotonic.

7. Stability:

The performance of a DAC changes with temperature, age and power supply variations. So, all its parameters must be specified over full temperature range.

VOLTAGE REGULATORS

A Voltage Regulator is a circuit that provides a constant voltage which is independent of variations in line voltage, load current and temperature.

SERIES OP-AMP REGULATOR

Classification of Voltage regulators:

Voltage regulators can be mainly classified as series (linear) and switching regulators.

In series regulator, a power transistor is connected between unregulated i/p and load. The transistor operates in active (linear region). So, it is also called linear regulator. Voltage drops across it is used to maintain constant voltage.

In switching regulator, a power transistor is used as a high frequency switch. i.e., power transistor operates in cutoff or saturation region. It doesn't conduct current continuously. This gives more efficiency than series regulators.

Comparison between series and switching regulators:

Series voltage regulators	Switching regulators
Few external parts required	More external parts
Simple design	Complicated design
Less noise	More noise
Less efficient	More efficient
More heat generation	Less heat generation
Only step-down operation is possible.	Step-up, step-down and – ve volt operations are possible

First 3 points are advantages and remaining are disadvantages.

SERIES OP-AMP REGULATOR:

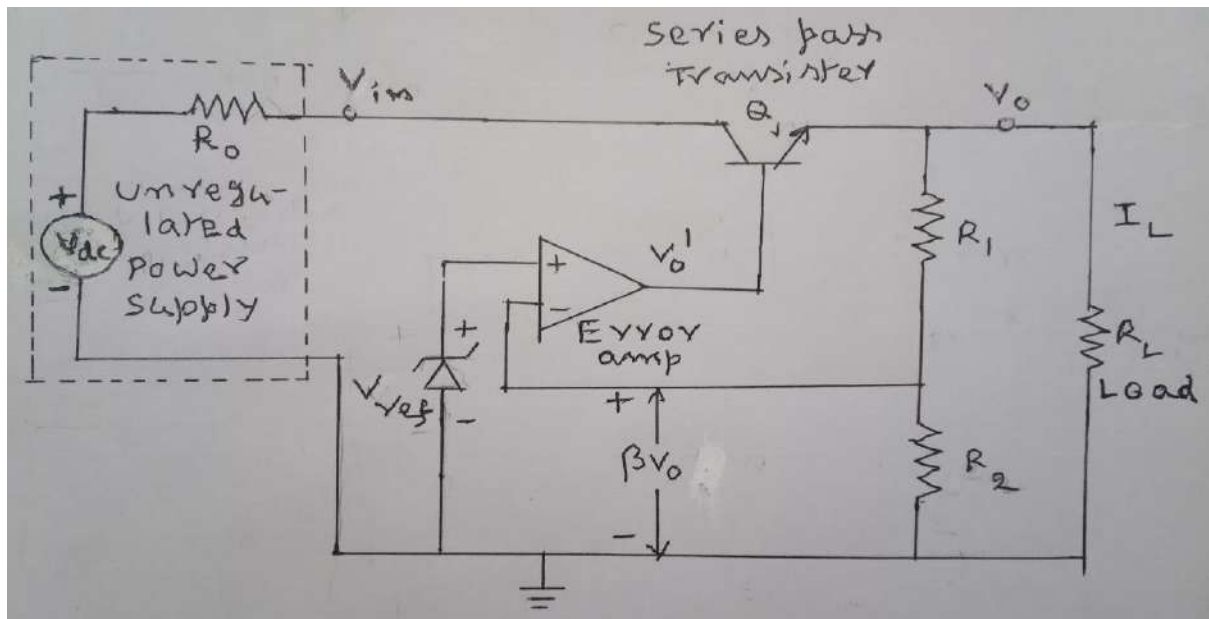


Fig. 1: Series OP-AMP regulator

A Voltage Regulator is a circuit that provides a constant voltage which is independent of variations in line voltage, load current and temperature.

Fig. 1 shows a regulated power supply using opamp. The circuit has 4 parts.

1. Reference Voltage Circuit (A Zener diode circuit)
2. Error Amplifier (An opamp)
3. Series Pass Transistor (A power transistor)
4. Feedback network (A voltage divider)

Let V_{in} = Unregulated input voltage

V_o = Regulated o/p voltage

Q_1 = power transistor acting as a series pass transistor

V_{ref} = Reference voltage

V_o' = Output of error amplifier (opamp)

$R_1 - R_2$ = Voltage divider

Operation:

Q_1 is connected in series between V_{in} and V_o . Q_1 acts as an emitter follower. Thus, it provides sufficient current to drive the load. $R_1 - R_2$ samples V_o . The sampled voltage is compared with V_{ref} obtained by Zener diode.

$(V_{ref} - \beta V_o)$ is the input of error amplifier

v_o' is the o/p of error amplifier.

v_o' is used to drive Q_1 .

If V_o increases, βV_o also increases, where $\beta = \frac{R_2}{R_1 + R_2}$. So, $(V_{ref} - \beta V_o)$ reduces.

Hence o/p of error amp also reduces. As a result, V_o reduces (Here $V_o = V_o'$ for emitter follower). Thus, the increase in v_o is nullified. Similarly, any decrease in V_o is also compensated.

IC VOLTAGE REGULATORS

Voltage regulators are available as monolithic ICs. They are mainly of 2 types: 3 terminal ICs and 723 General purpose IC

IC Voltage regulators can be available as:

(A) Three Terminal Fixed Voltage Regulators

1. Positive Voltage regulators (e.g.: 78XX series)
2. Negative Voltage regulators (e.g.: 79XX series)

(B) 723 General purpose Voltage Regulators

78XX (+ ve Voltage regulators):

They are fixed positive voltage regulators. XX is output voltage of the regulator. (XX = 5, 6, 8, 12, 15, 18 and 24 V). For example, 7808 has an o/p voltage of + 8 volts.

79XX (– ve Voltage regulators):

They are fixed negative voltage regulators. with output voltage options – 5 V, – 6 V, – 8 V, – 12 V, – 15 V, – 18 V, – 24 V. For example, 7908 has an o/p voltage of – 8 volts.

Output options – 2 V and – 5.2 V are also available with 79XX series.

IC Voltage regulators are available in TO-3 (metal package) and TO-220 (Plastic package).

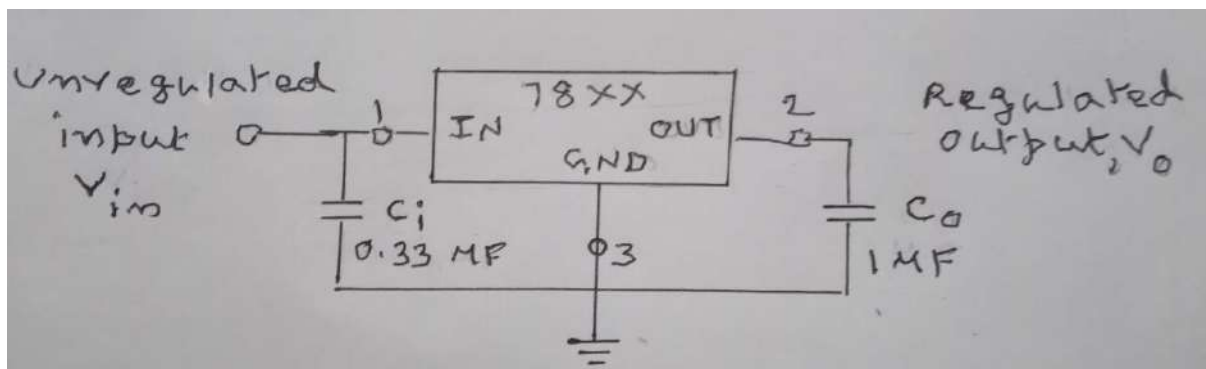


Fig. 2: A three terminal Voltage regulator

Fig. 2 shows a 3 terminal + ve IC Voltage regulator. Capacitor C_i is connected between input terminal and ground. Capacitor C_o is connected between output terminal and ground.

C_i is used to reduce the inductive effects due to long leads used. C_o is used improve transient response.

Important characteristics of 3 terminal IC regulators:

- (i) They are available as 78XX series and 79XX series.
- (ii) $V_{in} \geq (V_o + 2)$ Volts (e.g.: If $V_o = 5$ V, then $V_{in} \geq 5+2$ (i.e., 7 V), where V_{in} = Unregulated input voltage input voltage and V_o = Regulated o/p voltage
- (iii) Output current of voltage regulator can be varied from 0 up to its rated value $I_{o(max)}$. When it is $I_{o(max)}$, more heat is dissipated. So, heat sinks are provided to handle it.
- (iv) IC has built in temperature sensor. It turns off IC when IC becomes too hot (when temperature $> 125^\circ\text{C}$). O/p current drops and remains there until IC is cooled sufficiently.

Performance parameters of Voltage regulators:

1. Line regulation (or Input regulation)
2. Load Regulation
3. Ripple Rejection

1. Line regulation (or Input regulation):

It is the % change in V_o for a change in the i/p voltage V_{in} . It is expressed in mV or as % of V_o . Its typical value for 7805 is 3 mV.

2. Load Regulation:

It is the change in V_o for a change in load current. It is expressed in mV or as a % of V_o . Its typical value for 7805 is 15 mV, for $5\text{ mA} < I_o < 1.5\text{ A}$.

3. Ripple Rejection:

The voltage regulator can also reduce the amplitude of the ripple voltage. It is expressed in dB. Its typical value for 7805 is 78 dB.

723 GENERAL PURPOSE REGULATOR

Limitations of 3 terminal regulators:

1. No short circuit protection
2. Output (+ ve or – ve) voltage is fixed

723 general purpose regulator can overcome the above limitations. It can be adjusted over a wide range of + ve or – ve regulated voltage. Boosting of current is also possible by connecting external components.

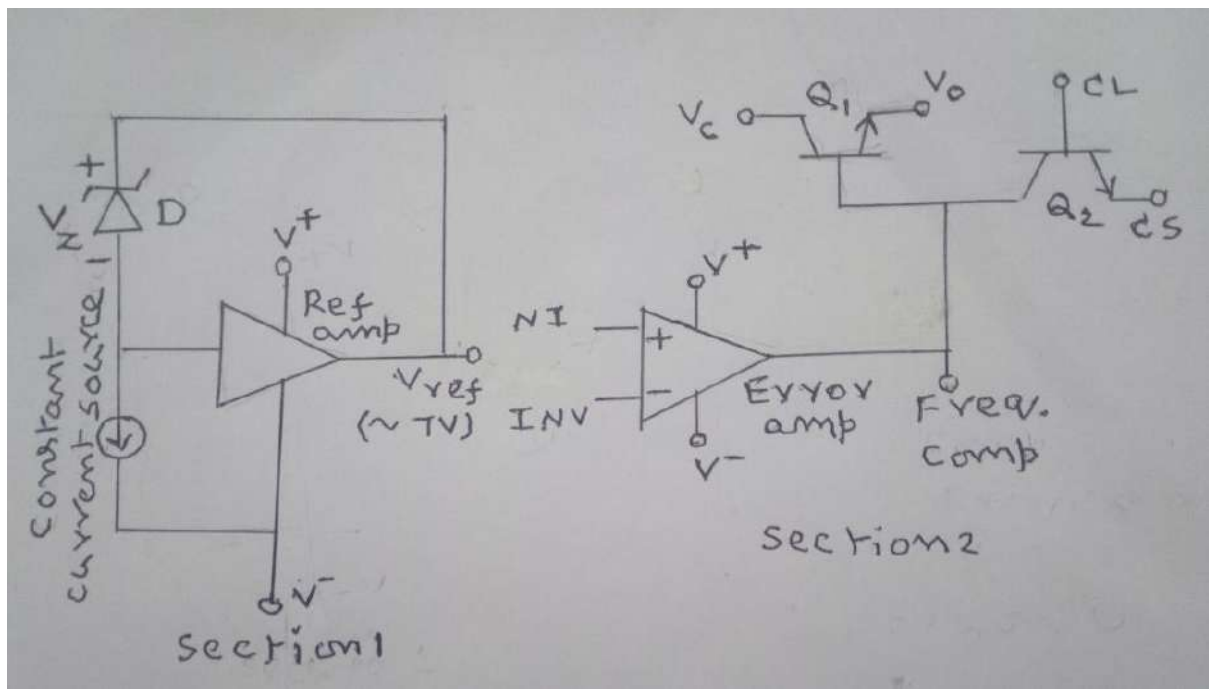


Fig. 3 (a): Functional Block Diagram of 723 regulator

Fig. 3 (a) shows the functional diagram of 723 regulator IC. It is available as 14-pin DIP package and 10-pin metal can package. It has 2 separate sections.

Section1: It contains Zener diode, constant current source and reference amplifier. It produces a fixed voltage of 7 V at the terminal V_{ref} . Because of constant current source, Zener diode outputs a fixed voltage.

Section2: It contains an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2 . The error amplifier compares a sample of o/p voltage applied at the INV input terminal with a reference voltage V_{ref} applied at the NI input terminal. The error (difference) signal controls the conduction of Q_1 .

These two sections are not connected internally. But IC provides the facility to connect.

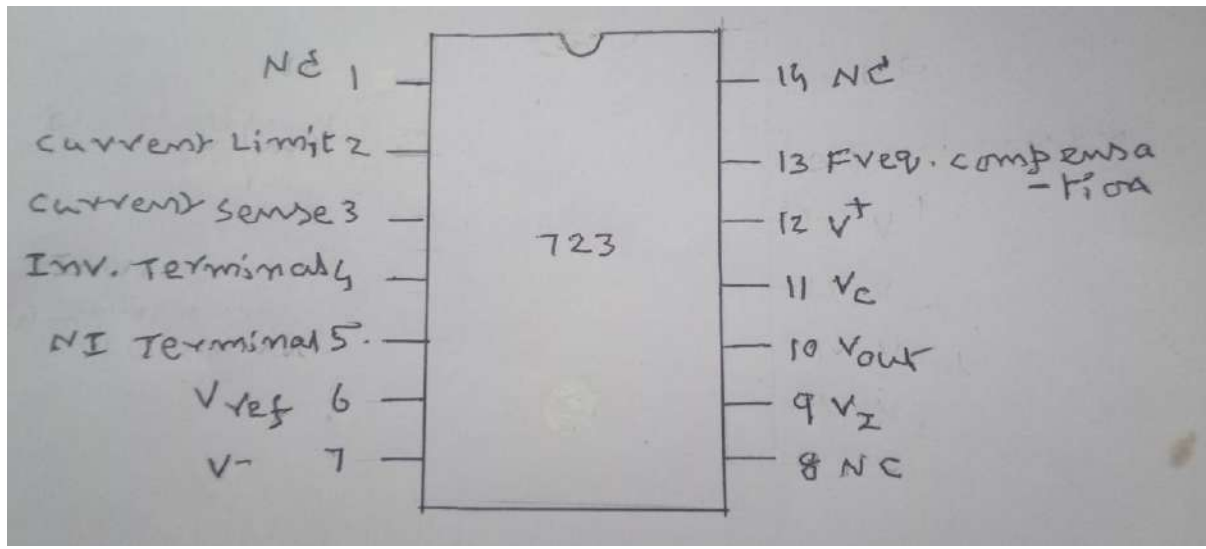


Fig. 3 (b): Pin Diagram of 14-pin DIP of 723

Fig. 3 (b) shows the pin diagram of 723 for a 14-pin DIP.

723 AS A LOW-VOLTAGE REGULATOR

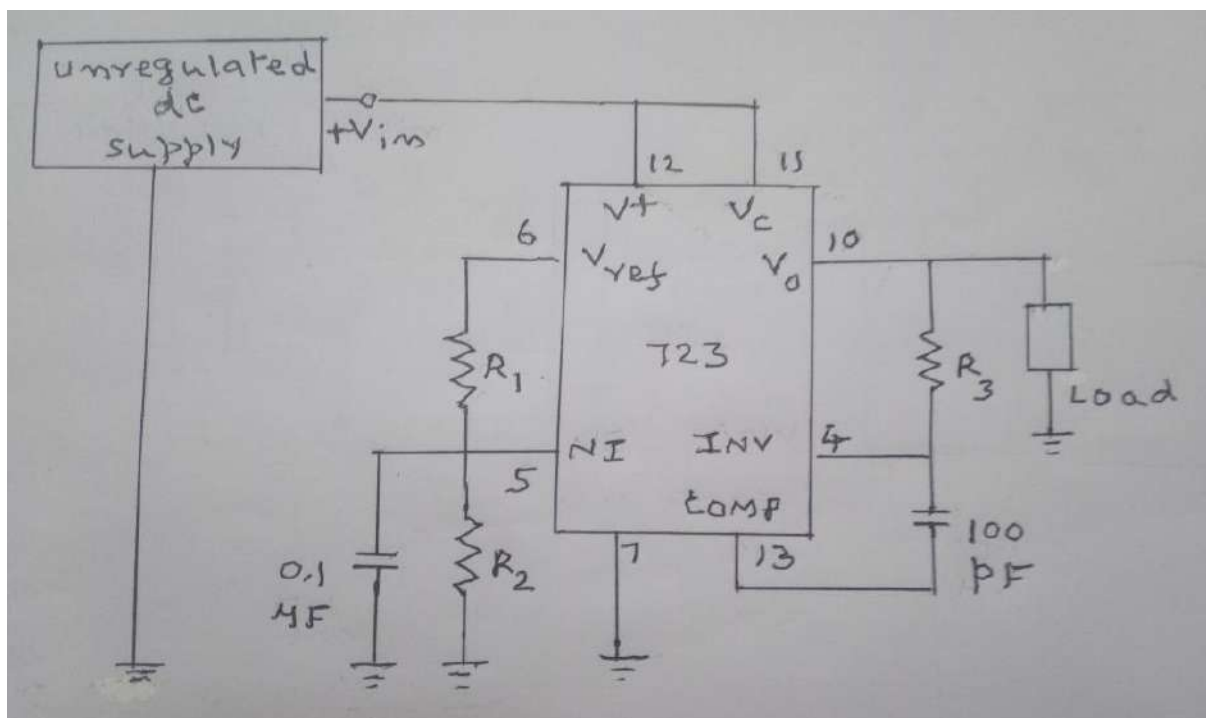


Fig. 4 (a): Pin Connections for a Low Voltage 723 Regulator

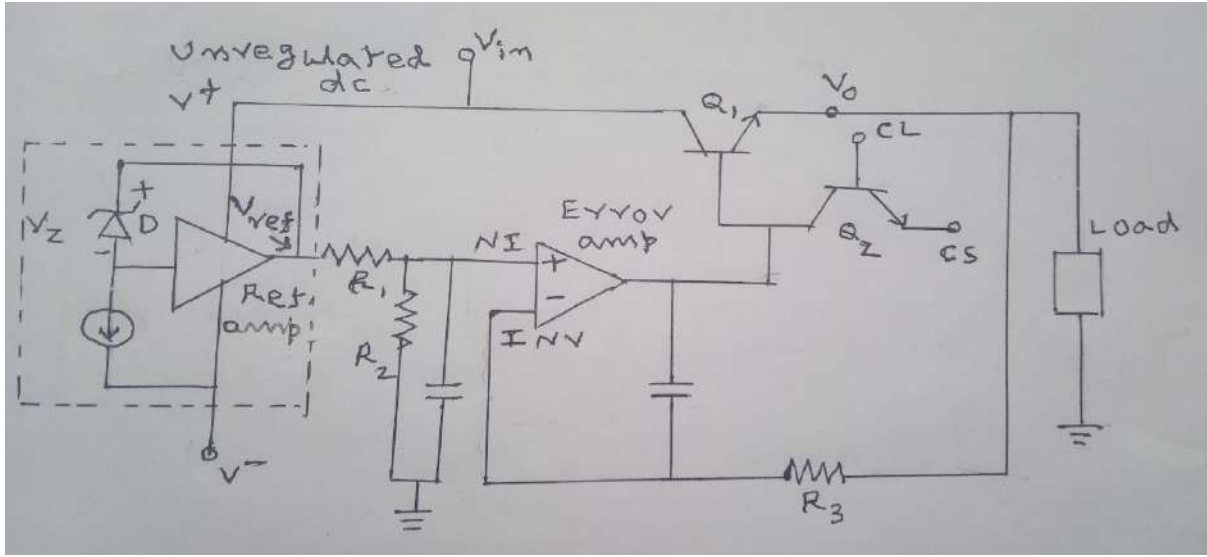


Fig. 4 (b): Functional Diagram for a Low Voltage Regulator

Fig. 4 (a) shows the schematic of 723 used as a low-voltage (2 to 7 V) regulator. V_{in} is the unregulated i/p and V_o is the regulated o/p. V_o is feedback to the INV terminal through R_3 . V_{NI} is the voltage at the non-inverting terminal NI.

$$V_{NI} = V_{ref} \frac{R_2}{R_1 + R_2} \text{ (Here } R_1\text{-}R_2 \text{ is acting as a voltage divider)}$$

If V_o becomes low, voltage at INV also becomes low. So, input of error amplifier becomes high and so its o/p also becomes high. This output drives Q_1 . So, voltage across load increases. Thus, initial drop in the load voltage is compensated. Similarly, any increase in the load voltage or changes in the input voltage are regulated.

Reference voltage is typically 7.15 V.

$$\therefore V_o = 7.15 * \frac{R_2}{R_1 + R_2} < 7.15 \text{ V}$$

Thus, the circuit acts as a low-voltage regulator (< 7 V)

The role of CL (Current limiting) and CS (Current sensing) terminals in Fig. 4 (b) is described below.

Current Limit Protection (Role of CL and CS)

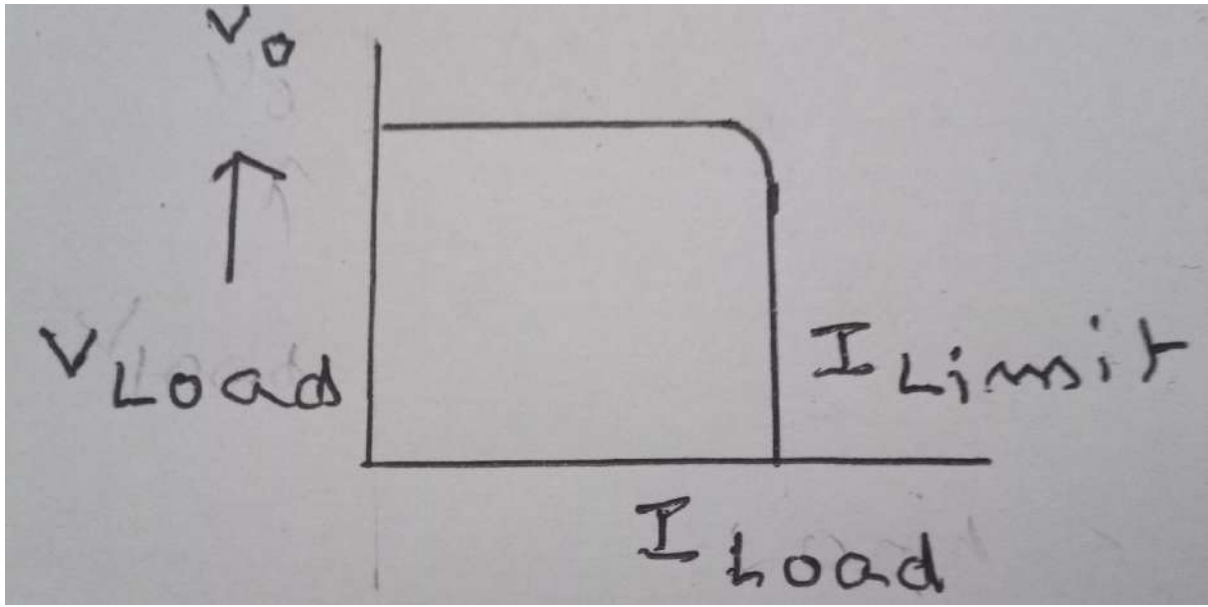


Fig. 5 (a) Characteristic Curve for Current Limiting

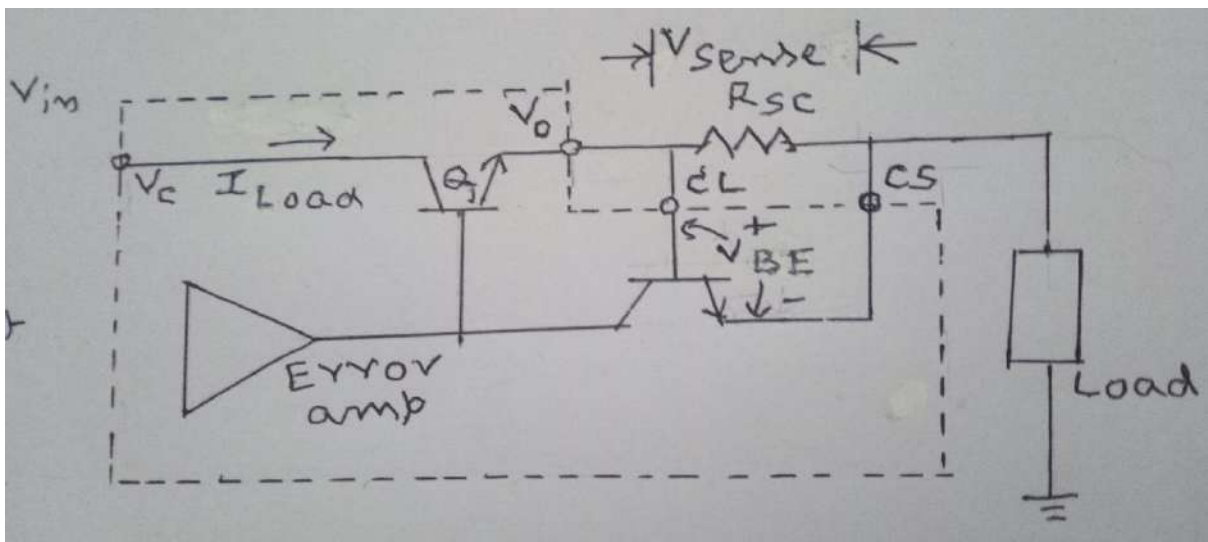


Fig. 5 (b) Current Limit Protection Circuit

The circuit in Fig. 4 (b) does not provide protection when current is large or under short circuit conditions. Circuit shown in Fig. 6 (b) provides such protection.

Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.

Fig. 5 (a) shows the characteristic curve of a current limited power supply. Here Output voltage remains constant up to I_{limit} . Beyond this point o/p voltage drops. The value of I_{limit} is set by connecting an external resistor R_{sc} between terminals CL and CS.

The CL terminal is also connected to output terminal V_o . CS terminal is connected to the load. It is not shown in Fig. 5 (b).

The load current produces a small voltage drop V_{sense} drop across R_{sc} . This voltage is applied to base emitter junction of Q_2

When this voltage is nearly 0.6 V, transistor Q_2 turns on

Now a part of the current from error amplifier goes to the collector of Q_2 . Thus, base current of Q_1 decreases. Hence emitter current of Q_1 reduces. Thus, any increase in load current will be nullified. Similarly, any decrease in load current is also compensated.

$$\text{Here, } I_{\text{limit}} = \frac{V_{\text{sense}}}{R_{sc}} = \frac{0.5 \text{ V}}{R_{sc}}$$

This method of current limiting is also called current sensing technique.

723 AS A HIGH-VOLTAGE REGULATOR

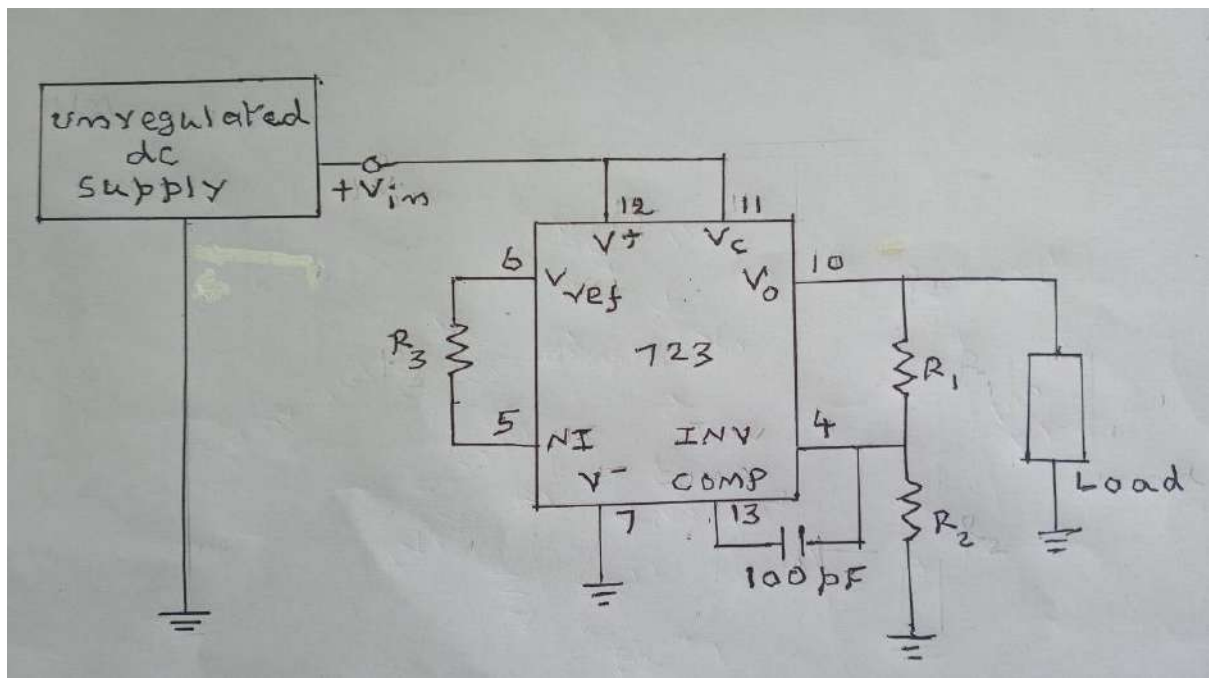


Fig. 6: High Voltage 723 Regulator

723 can also be used as a high voltage regulator to produce $> 7 \text{ V}$.

Fig. 6 shows the circuit of 723 used as high-voltage regular. Here the NI terminal is directly connected to V_{ref} through R_3 . So, voltage at the NI terminal is V_{ref} .

The error amplifier operates in non-inverting mode. Its gain is given by

$$A_v = 1 + \frac{R_1}{R_2}$$

$$\therefore V_o = 7.15 \left(1 + \frac{R_1}{R_2} \right)$$

SWITCHING REGULATORS (OR SWITCHED MODE REGULATORS)

In series regulator, a power transistor is connected between unregulated i/p and load. The transistor operates in active (linear region). So, it is also called linear regulator. Voltage drops across it is used to maintain constant voltage.

In switching regulator, a power transistor is used as a high frequency switch. i.e., power transistor operates in cutoff or saturation region. It doesn't conduct current continuously. Hence, the power transmitted across the pass transistor is in discrete pulses rather than as a steady current flow. When the device is cutoff, there is no current and so no power dissipation. In saturation region, there is power dissipation, but it is less. This gives more efficiency than series regulators.

Switched voltage regulators rely on pulse width modulation (PWM) to control the average value of o/p voltage. The average value of a repetitive waveform depends on the area under the waveform. If the duty cycle is varied as shown in Fig. 7, the average value also changes correspondingly.

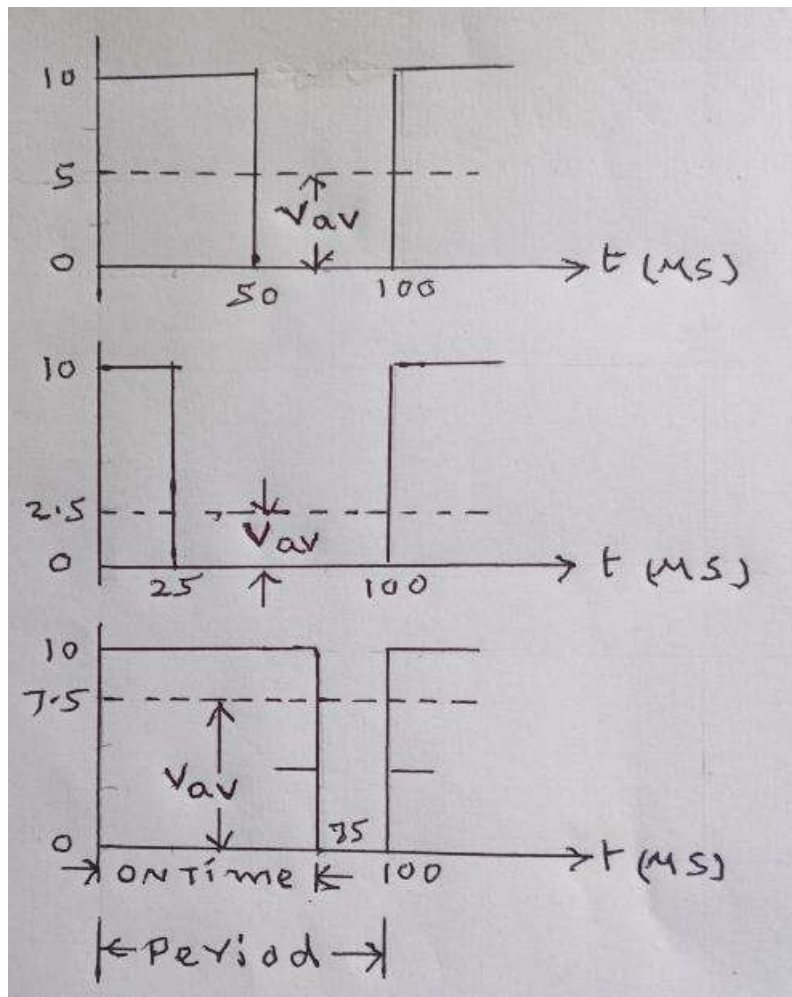


Fig. 7: PWM and Average Value

Advantages of Switching regulators over Series regulators:

1. More efficient
2. Less heat generation
3. Step-up, step-down and – ve volt operations are possible

Disadvantages of Switching regulators:

1. They need more external parts
2. Design is complex
3. More noisy

QUESTION BANK

Main Questions

1. Describe a binary weighted resistor type ADC. What are the drawbacks of it?
2. Describe a R–2R ladder type ADC. What are its drawbacks?

3. Describe a binary weighted resistor type ADC.
4. With the help of diagrams and truth tables, explain the operation of a flash type ADC.
5. With the help of necessary diagrams, explain the operation of a Successive approximation type ADC.
6. With the help of necessary diagrams, explain the operation of a Dual slope ADC. Mention its advantages and drawbacks.
7. Compare various DACs. Describe the specifications of DACs/ADCs.
8. Distinguish between series and switching regulators. Describe the functioning of series opamp regulator.
9. What is the need of 723 regulator? Describe the pin diagram and functional diagrams of the same.
10. Describe how IC 723 is used as low-voltage regulator.
11. Describe how IC 723 is used as high-voltage regulator.
12. Describe a switching regulator and pulse width modulation used by it.

2 Marks Questions

1. Describe the basic DAC/ADC technique.
2. What is the problem with binary weighted resistor type ADC?
3. What is the drawback of R–2R ladder ADC?
4. What are the advantages and disadvantages of a dual slope ADC?
5. Describe any two specifications of DACs/ADCs.
6. Mention the advantages of switching regulator. over series voltage regulators.
7. Mention the disadvantages of switching regulator. over series voltage regulators.
8. Define line regulation and load regulation.
9. What are the output voltage options available for 78XX/79XX?
10. What are the disadvantages of three terminal IC regulators?
11. Draw the pin diagram of 723.
12. Draw the pin diagram of a 78XX voltage regulator.

Topic from UNIT-2

SINUSOIDAL OSCILLATORS

Oscillator:

Oscillator is a circuit that produces an ac voltage or current waveform. The waveform may be sinusoidal or non-sinusoidal. In later case, it is normally called a waveform generator.

An oscillator doesn't need any input. It takes the energy from dc supply and converts it to ac signal. A sinusoidal oscillator can be realized by placing a

frequency-selective network in the feedback path of an amplifier. The active device used in amplifier may be a transistor or opamp. Feedback is + ve feedback.

Types of Oscillators:

1. RC Phase Shift Oscillator
2. Wien Bridge Oscillator
3. Colpitt's Oscillator
4. Hartley Oscillator
5. Clap Oscillator
6. Crystal Oscillator

Principle of Oscillations (Barkhausen criterion):

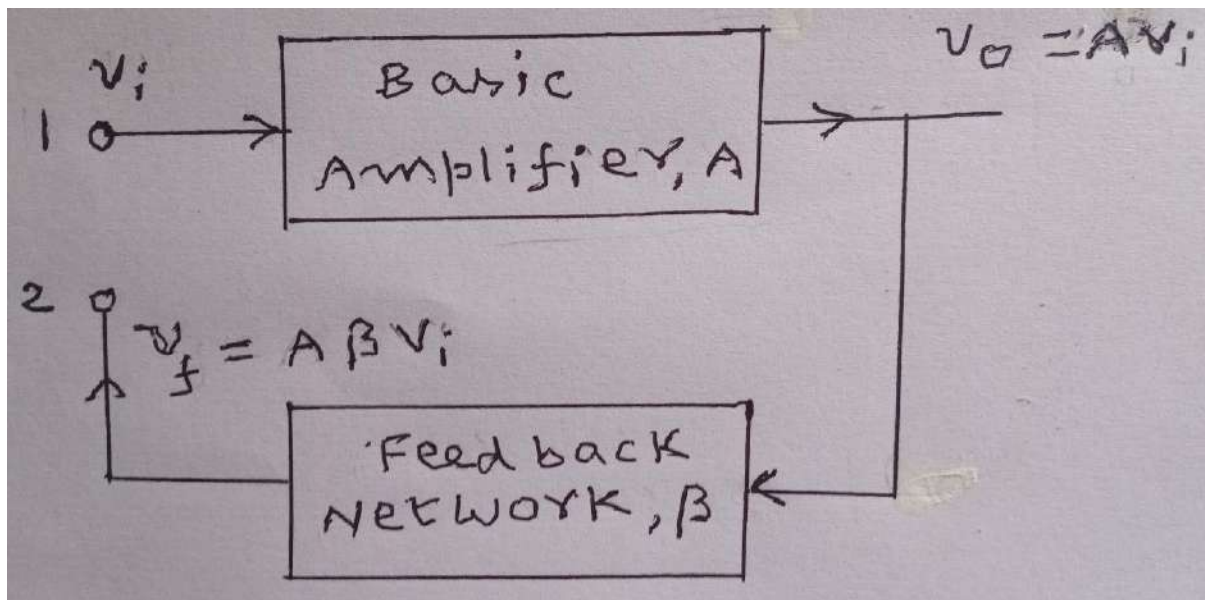


Fig. 1

Fig. 1 represents the basic schematic of an oscillator. Here

v_i = Input voltage

v_o = Output voltage

v_f = Feedback signal

A = Gain of basic amplifier

β = Gain of frequency selective network = feedback factor

Let the points 1 and 2 are not connected. Then let us apply the input signal v_i .

From Fig. 1, We get $v_f = A \beta v_i$

If the values of A and β are adjusted such that $A \beta = 1$,

Then $v_f = v_i$

Now let us connect points '1' and '2' and remove external signal v_i , the circuit will continue to provide same output, without external input.

Barkhausen Criteria:

There are two conditions to get oscillations. They are

$$|A\beta| = 1$$

$$\angle A\beta = 0^\circ \text{ or multiple of } 360^\circ$$

Above two conditions are called Barkhausen criteria.

First condition says that magnitude of loop gain $A\beta$ is 1.

Second condition says that total phase shift of the circuit is 0° or multiple of 360° .

Practical considerations:

Suppose $A\beta$ is exactly 1. Then due to ageing, replacement of transistors, temperature, changes in circuit parameters $A\beta$ may become < 1 . Then gain (or o/p) of the circuit goes on decreasing. So, oscillations will die out. (1 to 5 %) So, $A\beta$ is taken slightly more than unity. Then o/p will go on increasing. But it is limited by the non-linearity of active device. Thus o/p becomes constant when the active device enters saturation.

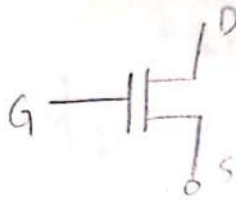
There is no ac input to an oscillator. It uses noise signal like switching transient as the initial input.

Unit - V

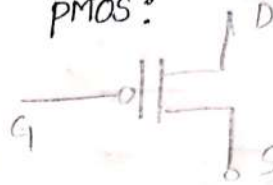
Digital IC's

CMOS logic levels : (Complementary Metal oxide Semi Conductor)

NMOS:



PMOS :



If Gate voltage $G=0$ CMOS will be off, drain to source act as Open Circuit

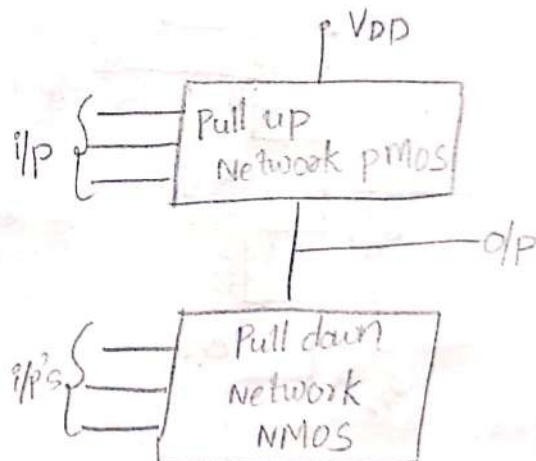
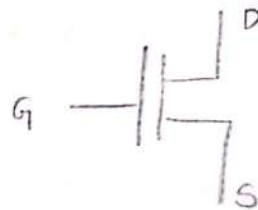
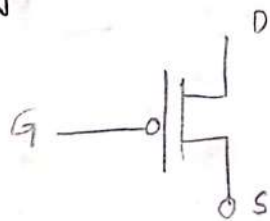
Open Circuit
If Gate Voltage $G=1$ CMOS will be ON, drain to source act as Short Circuit

PMOS:

PMOS.
If Gate Voltage $G=0$ CMOS will be ON, drain to Source act as Short Circuit

as Short circuit
If Gate voltage $G=1$ CMOS will be OFF, Source to drain as open circuit

CMOS Logic Circuit:

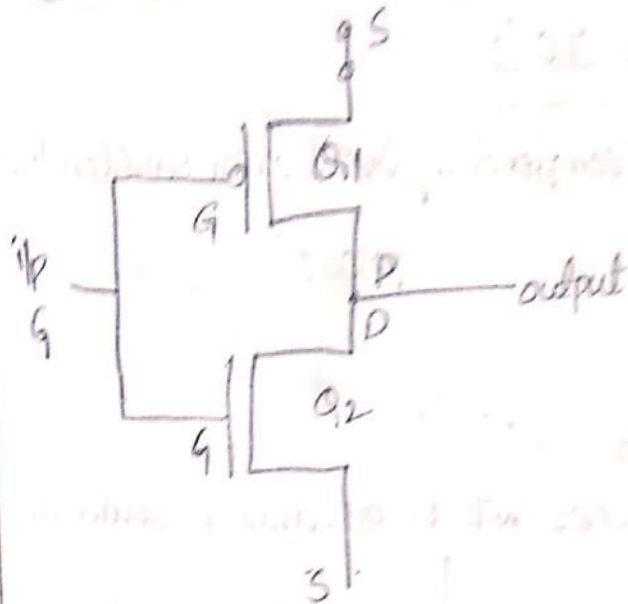


AND $\rightarrow$ PMOS-parallel
NMOS $\rightarrow$ series

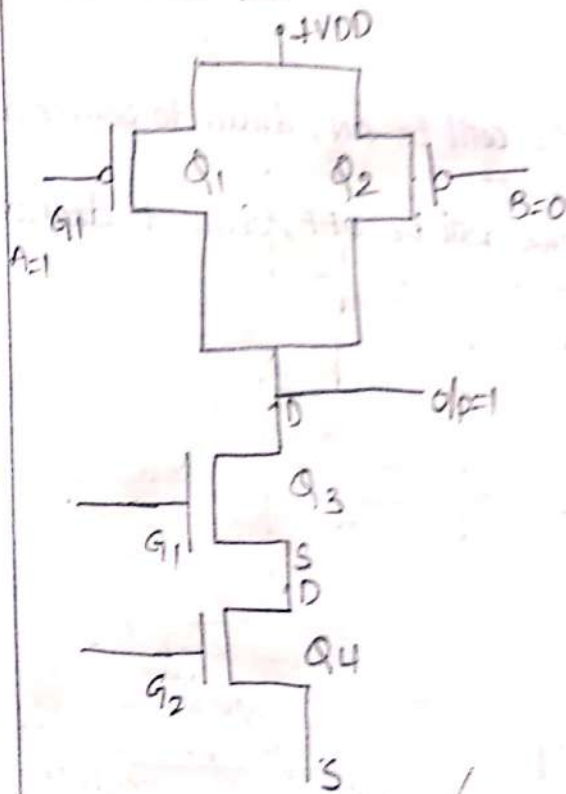
OR $\rightarrow$ PMOS $\rightarrow$ series
NMOS $\rightarrow$ parallel

$$\begin{array}{r} 250 \\ 125 \\ \hline 125 \\ 65 \\ \hline 40 \end{array}$$

CMOS Inverter:

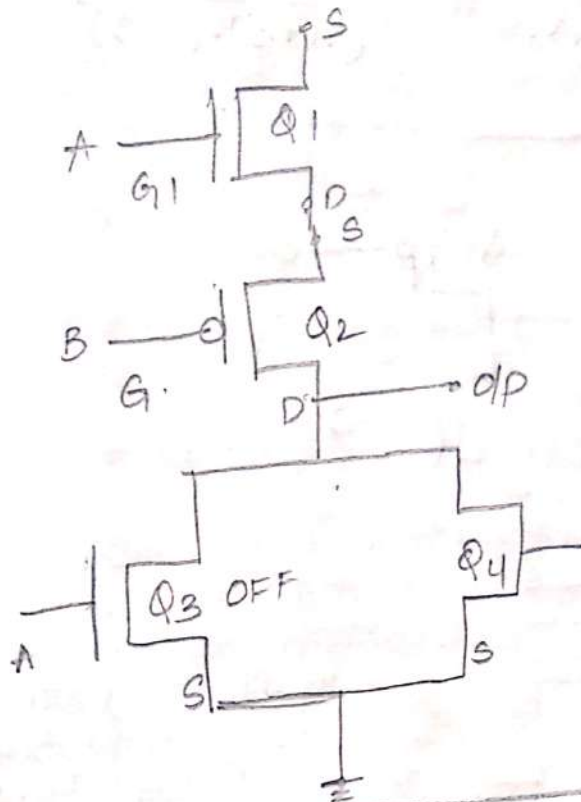


CMOS NAND Gate:



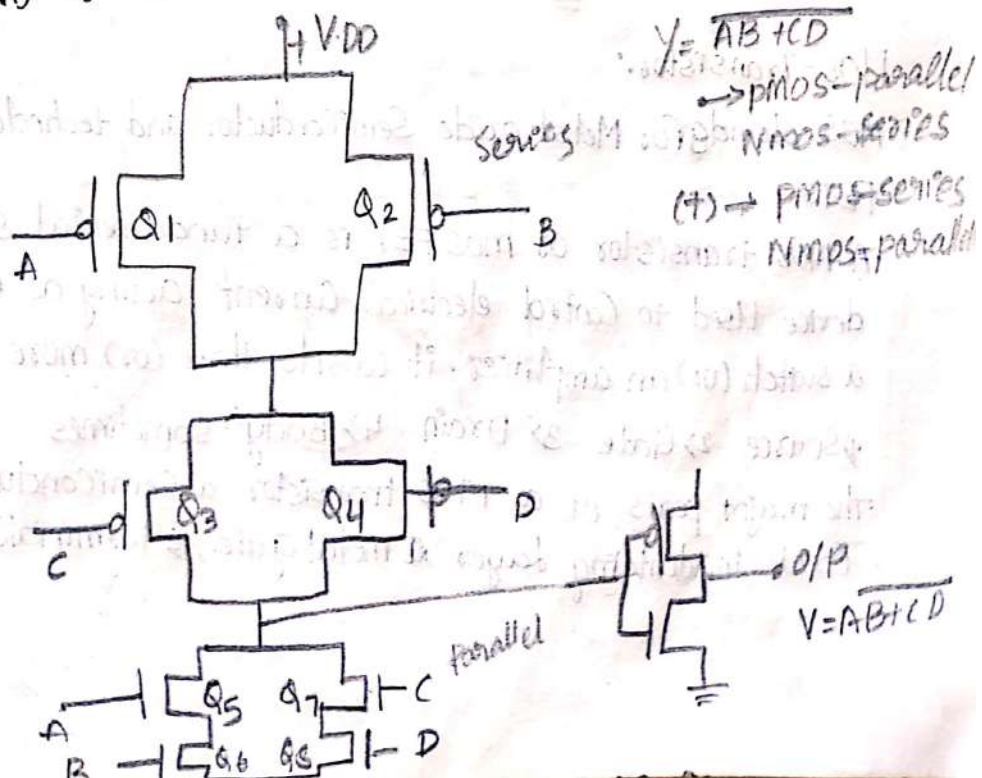
ip		PMOS		NMOS		Q1
A	B	Q1	Q2	Q3	Q4	y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

CMOS NOR gate



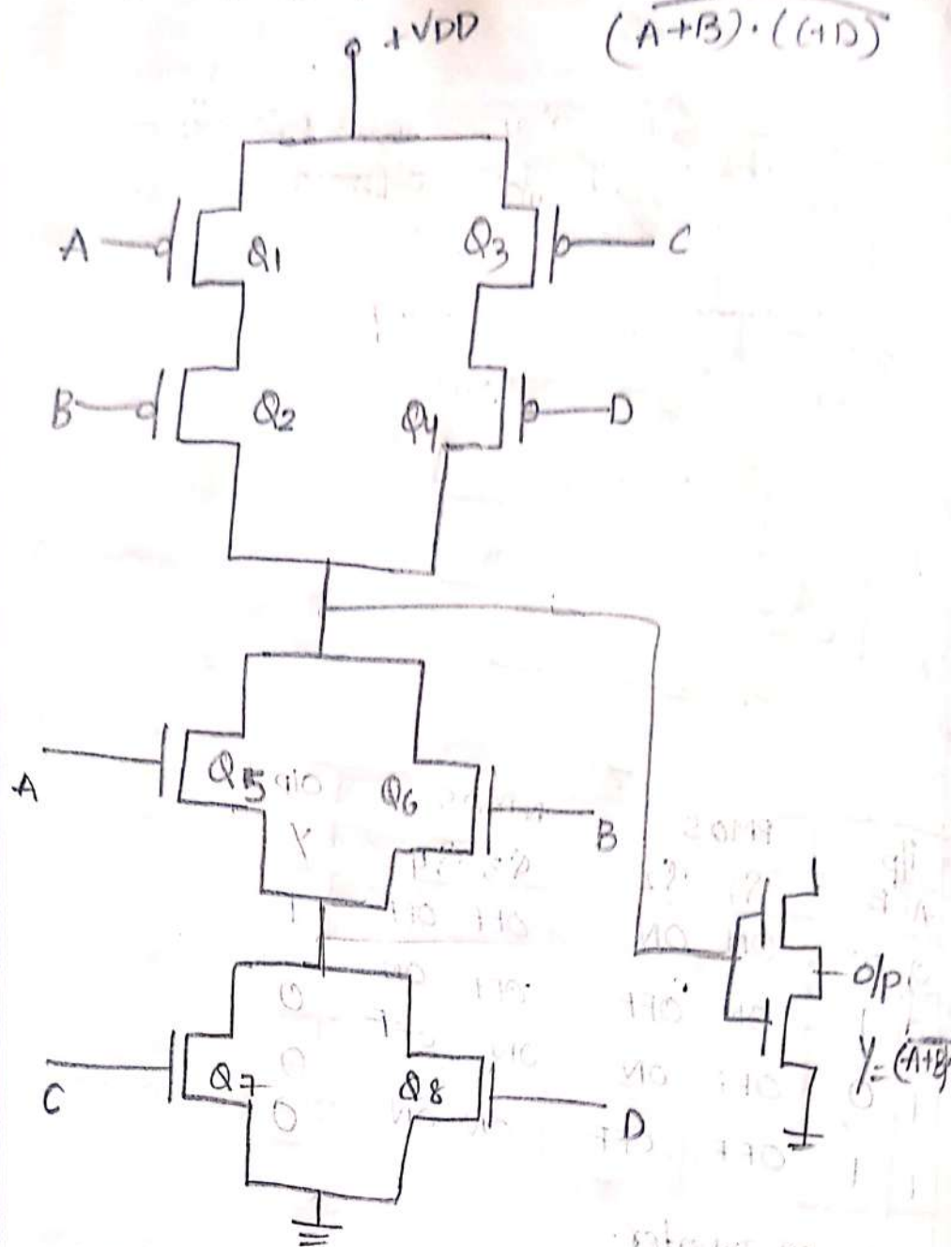
i/p		PMOS		NMOS		O/p
A	B	Q1	Q2	Q3	Q4	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

AND-OR-Inverter.



OR-AND-Invert (OAI)

$$(A+B) \cdot (\neg D)$$



MOS-Transistor:

MOS stands for Metal oxide Semiconductor and technology used FETS

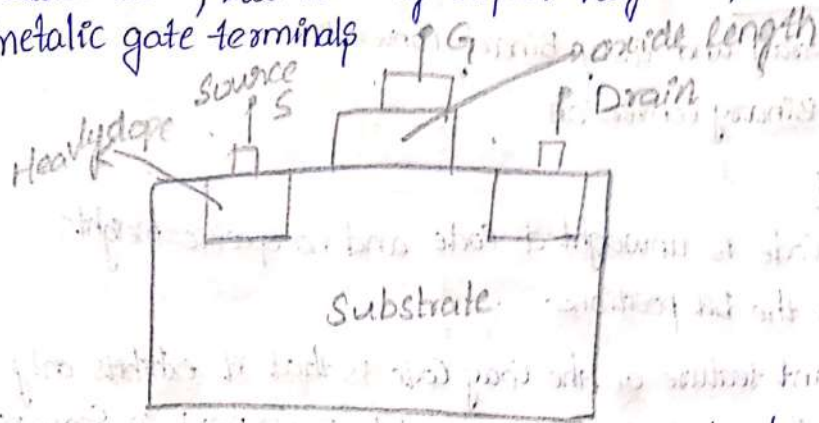
A MOS transistor or MOS FET is a fundamental Semiconductor device used to control electrical current acting as either a switch (or) an amplifier. It consists of three (or) more terminals.

1) Source 2) Gate 3) Drain 4) Body. Sometimes

The major parts of a MOS transistor are a Semiconductor, Oxide insulating layer, a metal gate, & terminals.

Construction of MOS Transistor:

- A MOS Transistor Consists of a lightly doped Semiconductor Substrate, two heavily doped Regions, oxide layer and metallic gate terminals.



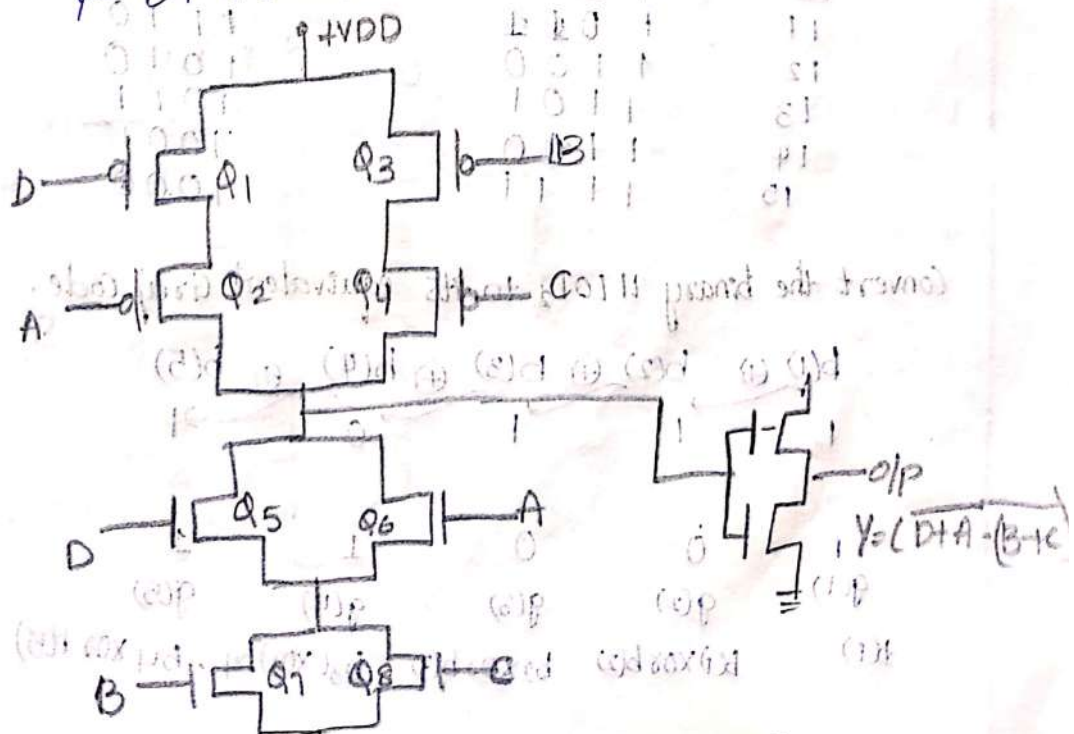
- To Construct a mos Transistor two lightly doped Semiconductor Substrate is taken into which two heavily Semiconductor Regions are refused, which acts as Source and drain of the MOS-Transistor. an oxide layer made up of SiO_2 Silicon dioxide deposited at on the lightly doped Semiconductor substrate to which metallic gate terminals is attached.
- These oxide layer acts as an insulating layer b/w the metallic gate terminals and the lightly doped Semiconductor Substrate.

1. N-MOS (N-channel MOS)
2. P-MOS (P-channel MOS)

Implementation of any function using CMOS logic:

Ex: Boolean Expression using CMOS logic.

$$Y = \overline{D + A \cdot (B + C)}$$



Combinational Logic IC's

Code Converters:

- Binary Gray and Gray-Binary Conversion
- BCD to Binary Conversion

Gray Code:

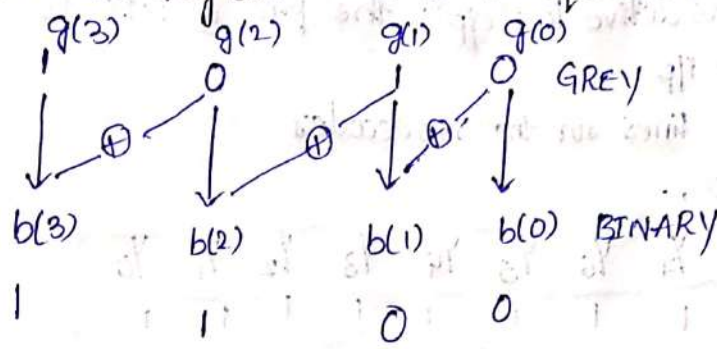
- The gray code is unweighted code and no specific weights assigned to the bit positions.
- The important feature of the Gray code is that it exhibits only a single bit change from one code word to the next in sequence.
- This property is an important one in many applications, such as shaft position encoders: where error susceptibility increases with the number of bit changes b/w adjacent numbers in a sequence.

Decimal Number	4 bit Binary number A B C D	4 bit Gray Code G ₁ G ₂ G ₃ G ₄
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 1 1 0
4	0 1 0 0	0 1 1 1
5	0 1 0 1	0 1 0 1
6	0 1 1 0	0 1 0 0
7	0 1 1 1	1 1 0 0
8	1 0 0 0	1 1 0 1
9	1 0 0 1	1 1 1 1
10	1 0 1 0	1 1 1 0
11	1 0 1 1	1 0 1 0
12	1 1 0 0	1 0 1 1
13	1 1 0 1	1 0 0 1
14	1 1 1 0	1 0 0 0
15	1 1 1 1	

Convert the binary 11101_2 to its equivalent Gray code.

$$\begin{array}{ccccccccc} b(1) & \oplus & b(2) & \oplus & b(3) & \oplus & b(4) & \oplus & b(5) \\ 1 & & 1 & & 1 & & 0 & & 1 \\ \hline g(1) & & 0 & & 0 & & 1 & & 1 \\ b(1) & & g(2) & & g(3) & & g(4) & & g(5) \\ b(1) & & b(1) \oplus b(2) & & b(2) \oplus b(3) & & b(3) \oplus b(4) & & b(4) \oplus b(5) \end{array}$$

Convert the Grey Code 1010 to its equivalent Binary:



$$b(3) = g(3)$$

$$b(2) = b(3) \oplus g(2)$$

$$b(1) = b(2) \oplus g(1)$$

$$b(0) = b(1) \oplus g(0)$$

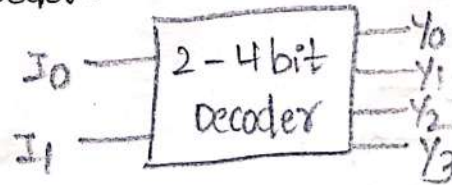
BCD to Binary Conversion:

weight : 80 40 20 10 8 4 2 1

Bit designation : $B_3 B_2 B_1 B_0$ $A_3 A_2 A_1 A_0$

Example: Convert the BCD number

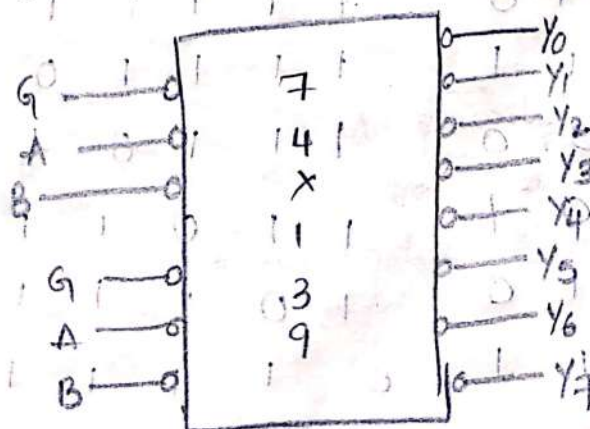
Decoder:-



Truth table

Enable	I_0	I_1	Y_0	Y_1	Y_2	Y_3
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	0	1	0	0

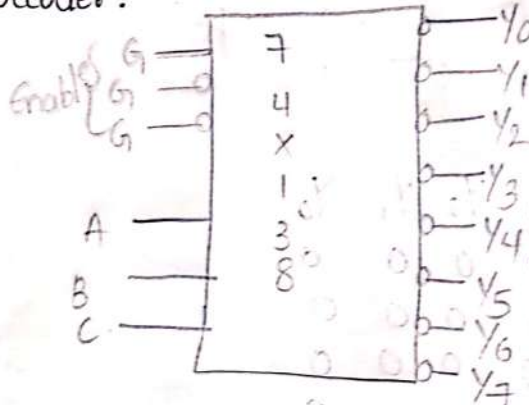
74x139 Decoder:-



- IC 74x139 has active low o/p's the active low enable i/p
- A & B are the i/p lines for the 3x8 decoder
- When enable $G=0$,

Enable	B	A	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
X	0	0	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	0	1	1
0	1	0	1	1	1	1	0	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

3x8 Decoder:

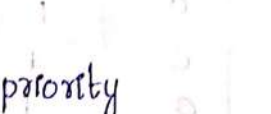


Enable	i/p			o/p								
G ₁	G ₂		C	B	A	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁
x	x	x	x	x	x	x	x	x	x	x	x	x
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	1	1	1	0	1
1	0	0	0	1	1	1	1	1	1	0	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1
1	0	0	1	1	0	1	1	0	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1





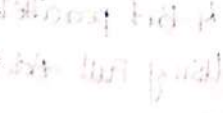
2^n : n -encoder
 n : 2^n -decoder



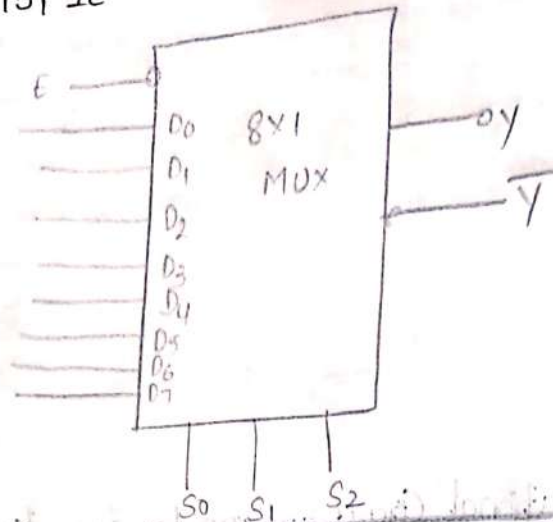
0
1 1

in below fig.

May 18 1914



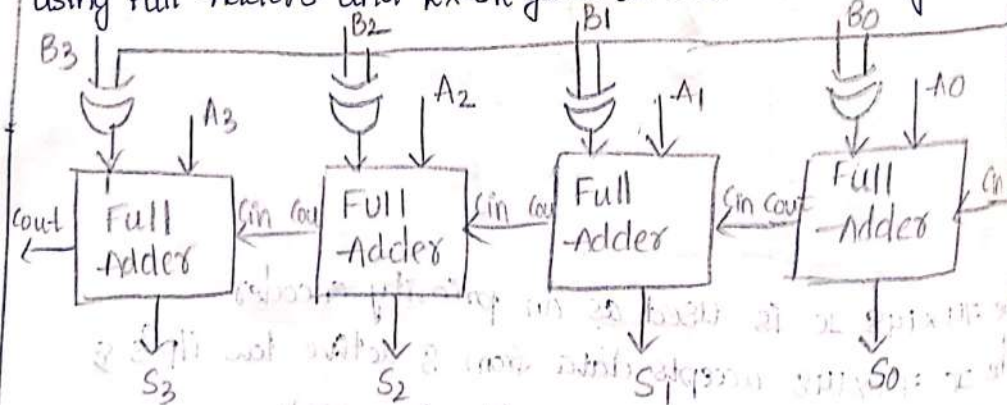
Multiplexer :-
74x151 IC



Enable	S ₀	S ₁	S ₂	Y	$\overline{Y}$
1	X	X	X	X	X
0	0	0	0	D ₀	$\overline{D_0}$
0	0	0	1	D ₁	$\overline{D_1}$
0	0	1	0	D ₂	$\overline{D_2}$
0	0	1	1	D ₃	$\overline{D_3}$
0	1	0	0	D ₄	$\overline{D_4}$
0	1	0	1	D ₅	$\overline{D_5}$
0	1	1	0	D ₆	$\overline{D_6}$
0	1	1	1	D ₇	$\overline{D_7}$

4-Bit parallel Adder/Subtractor:

4-Bit parallel Adder/Subtractor Circuit can be Constructed by using Full Adders and EX-OR gates as shown in the figure.



- The logic Circuit has an additional input called the Carry input M, which determines the addition or Subtraction.
- When M=1, the Circuit is a Subtractor and when M=0, the Circuit becomes Adder.

The EX-OR gate Consists of two inputs to which one is Connected to the B and other to input M.

When $M=0$, B EX-OR of 0 produce B. then full adders add the B with A with Carry input zero and hence an addition operation is performed.

When $M=1$, B EX-OR of 0 produce B Complement and also Carry input is 1. Hence the Complemented B inputs are added to A and 1 is added through the input Carry, nothing but a 2's Complement operation. the Subtraction operation is performed.

Magnitude Comparator:

Magnitude Comparator is a Combinational Circuit that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number.

The Comparison of two numbers is an operation that determines if one number is greater than, less than, or equal to the other number.

The Outcome of the Comparison is Specified by three binary variables that indicate whether $A > B$, $A = B$, or $A < B$.

Truth Table for a Comparator:

A	B	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

CMOS 40xx Series

Specifications:

- power Consumption
- Operating Voltage. - 3V to 15V or more.
- Input Impedance.
- Noise Immunity
- Static Sensitivity

Applications:

- Portable electronics due to low power Consumption.
- Implementing Combinational and Sequential Circuits, such as Counters and Shift Register.
- Applications requiring a Single power Supply.

TTL 74 Series:

Specifications:

- power Consumption
- speed
- Output Drive.
- Logic levels
- Noise Immunity

Applications:

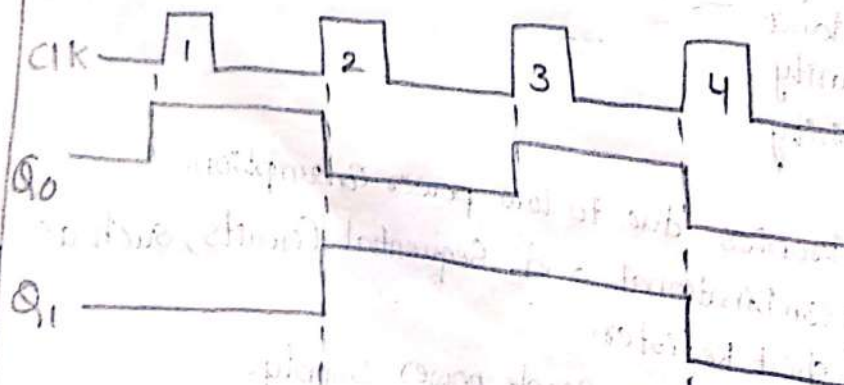
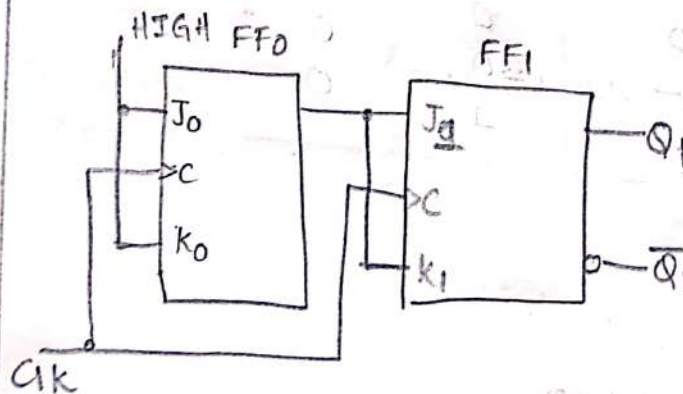
- General-purpose digital logic implementation, including counters, and buffers
- Applications where speed is a primary concern, such as in digital designs.

Sequential Logic IC's:

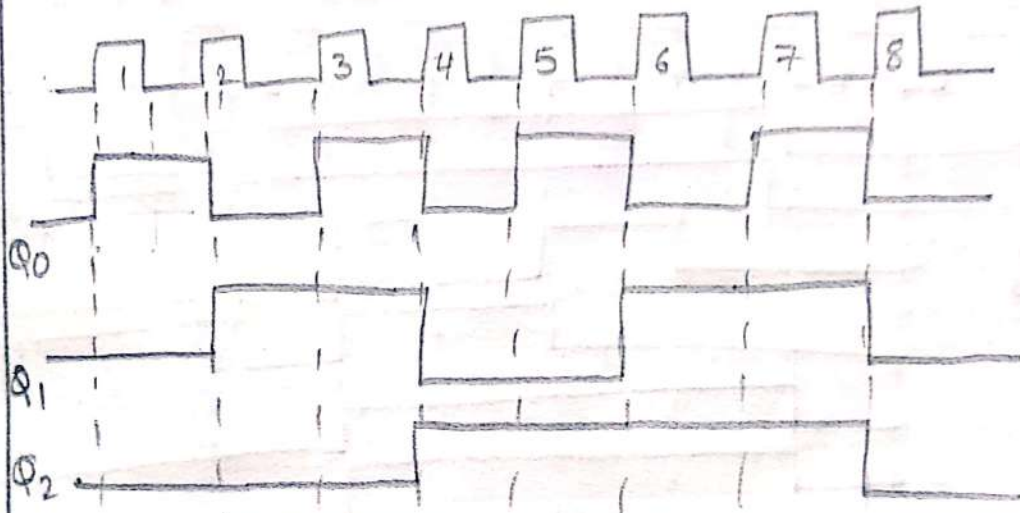
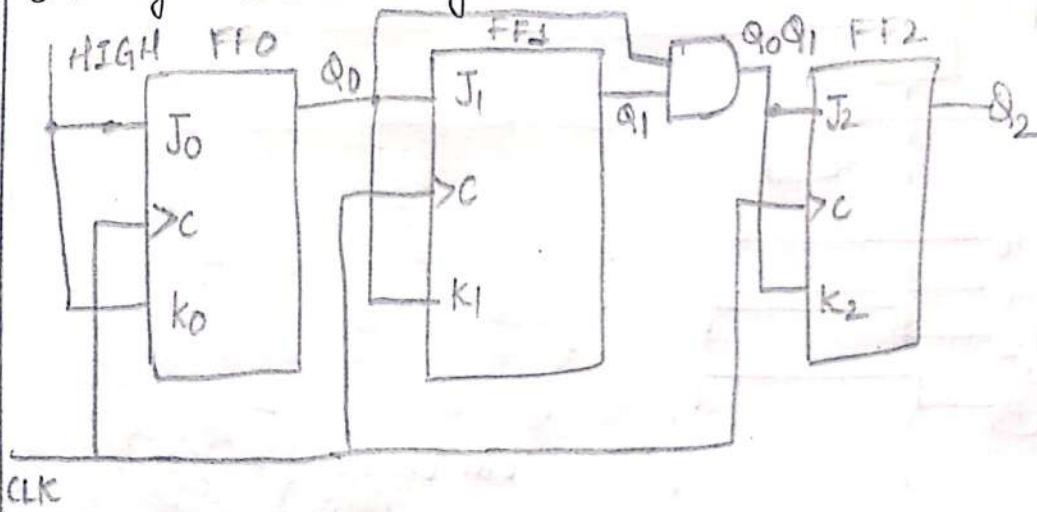
Synchronous Counters:

In a Synchronous Counter all flip-flops are clocked together with a common clock pulse, Synchronous Counters overcome the disadvantage of accumulated propagation delays, but generally they require more circuitry to control state changes.

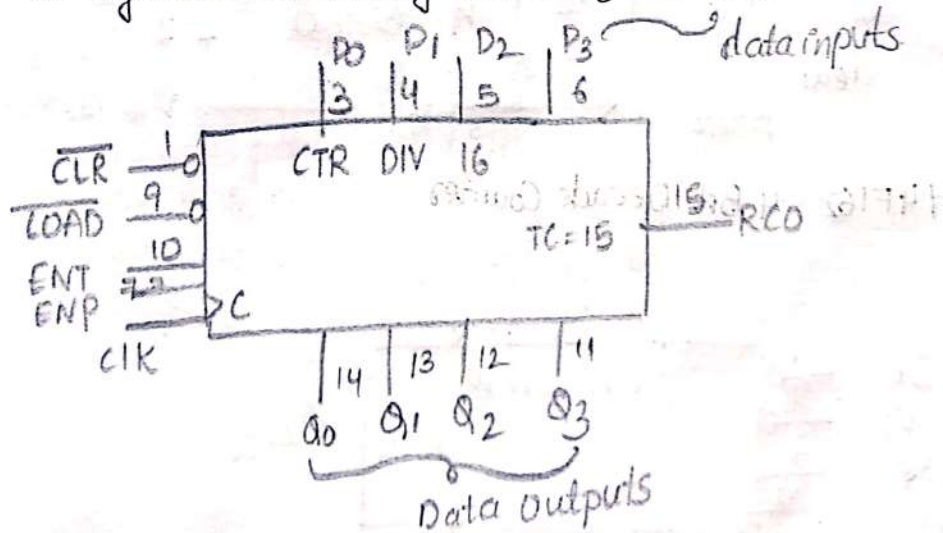
2-Bit Synchronous Counters:

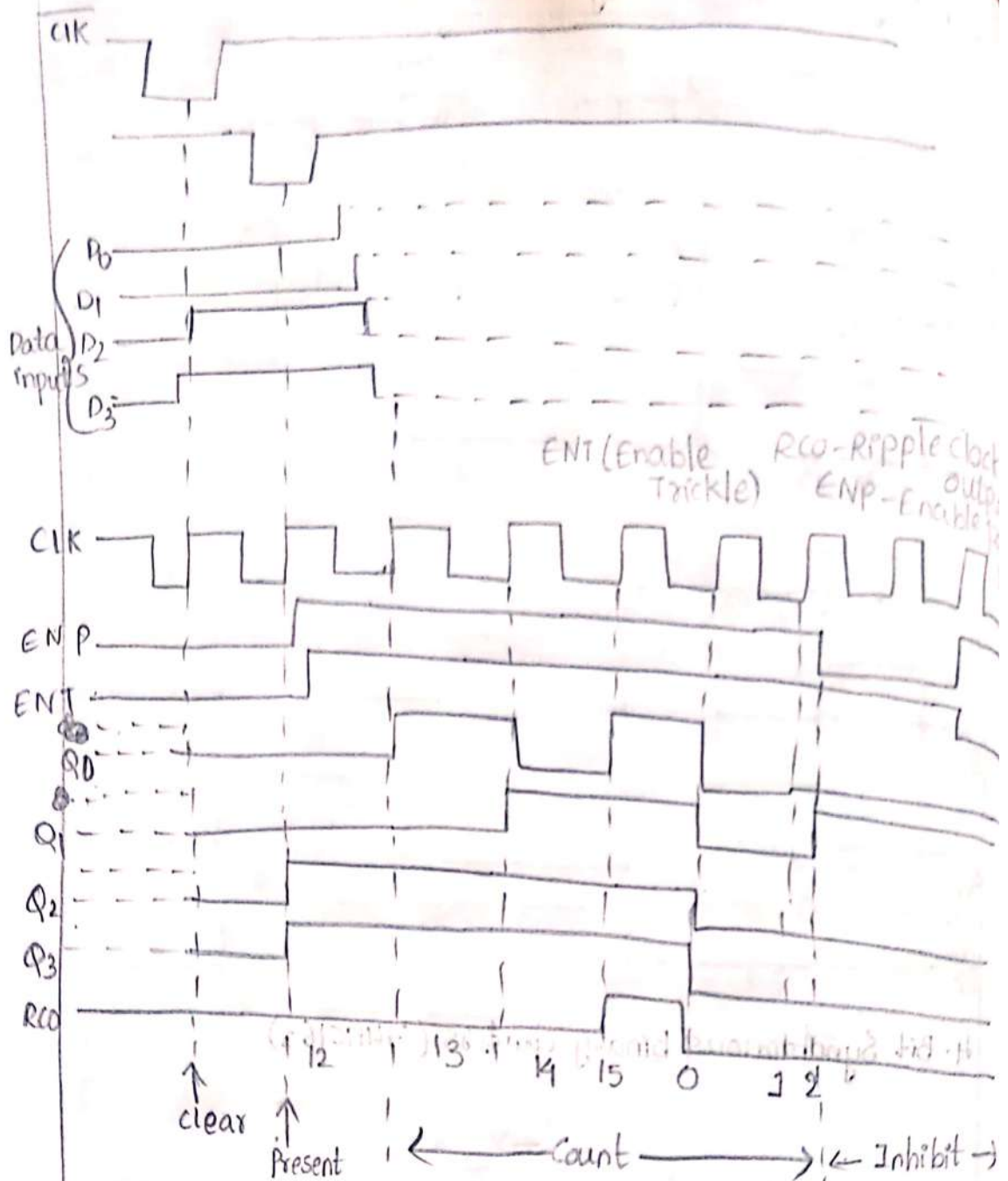


3-Bit Synchronous Binary Counters:

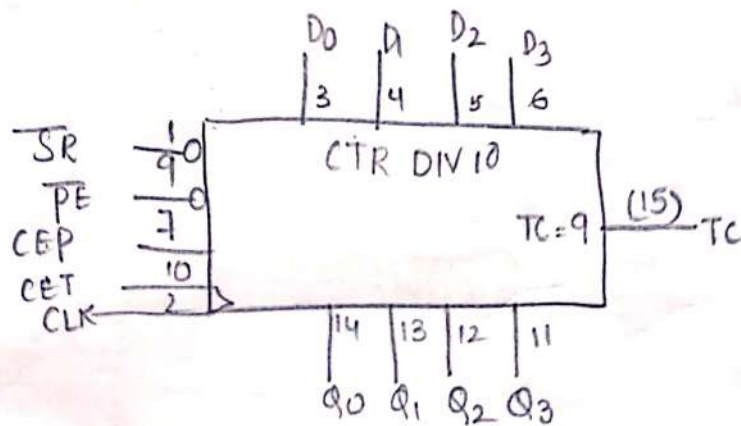


4-Bit Synchronous Binary Counters (74HC163)

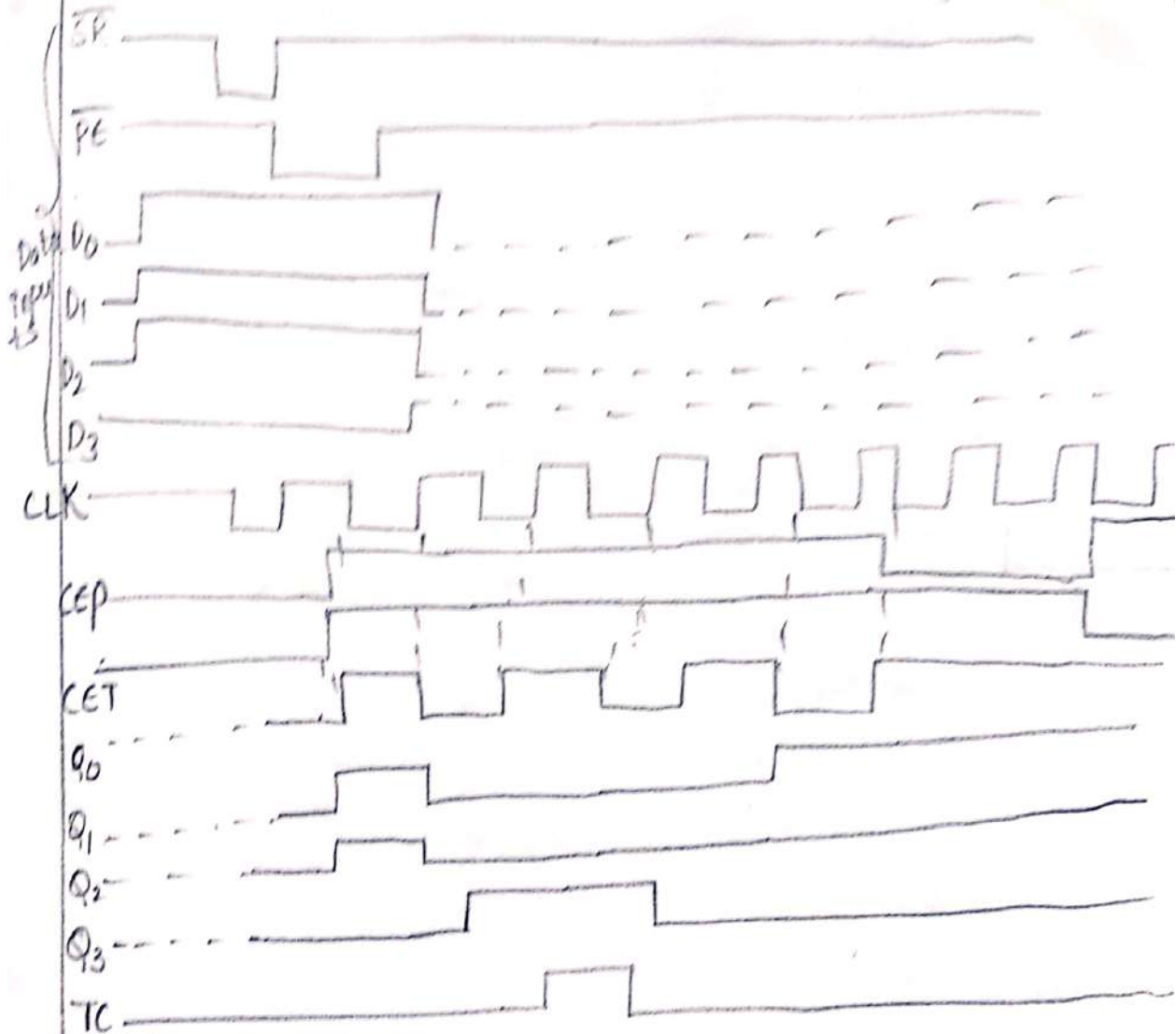




74F162 - 4 Bit Decade Counter



SR reset counter CEP (count enable parallel) and CET (count enable trickle) is high



Shift Registers:

Types of Shift Registers:

1. Serial-in to Serial-out (SISO)
2. Serial-in to parallel-out (SIPO)
3. parallel-in to Serial-out (PISO)
4. parallel-in to parallel-out (PIPO)

MOS Field Effect Transistor (MOSFET)

Introduction:-

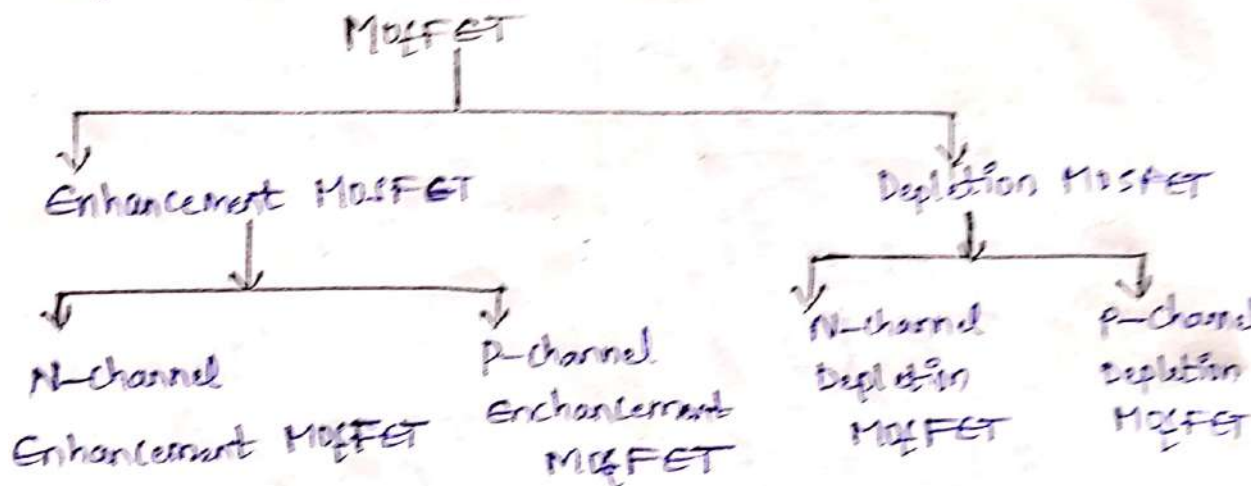
→ A MOSFET can also be called as Insulated gate field effect transistor [IG-FET] or Metal oxide silicon transistor [MOST].

→ There are two basic forms of MOSFET:

(i) Enhancement MOSFET

(ii) Depletion MOSFET

→ The each classification is classified into two types i.e., N-channel & P-channel.



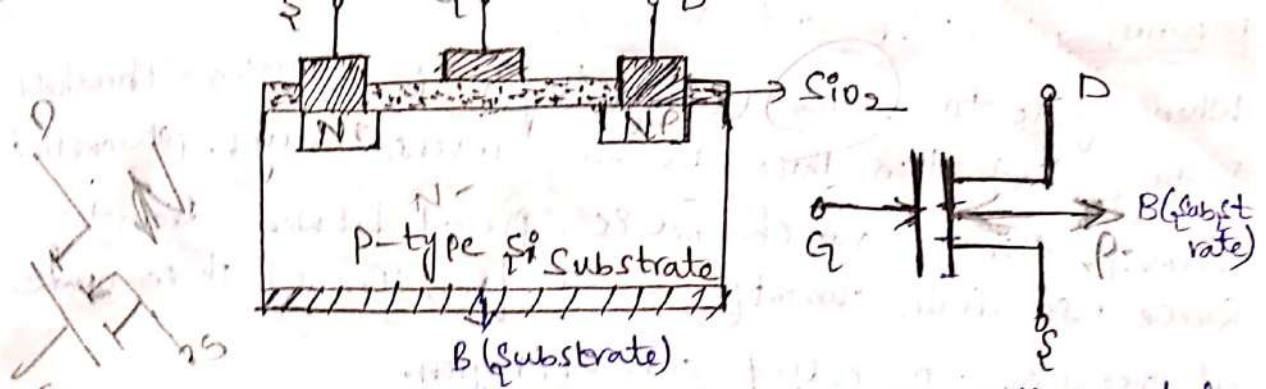
N-channel Enhancement MOSFET:-

Construction of N-channel Enhancement MOSFET:-

→ Two heavily doped n-regions are diffused in a lightly doped p-type silicon substrate. One of these regions is called as source (S) and another one is called as drain (D). They are separated by 10^{-3} inches.

→ A thin layer of SiO_2 is grown over the surface of the p-substrate, i.e., on the surface of the p-substrate between two n-regions.

→ A thin layer of aluminum is formed over the layer of SiO_2 that forms the gate terminal (G). as shown in below figure.



In enhancement MOSFET the channel is not diffused but it is induced when positive gate voltage is applied.

[For N-channel enhancement MOSFET]

Operation of N-channel enhancement MOSFET:-

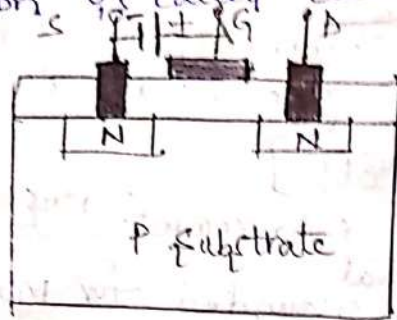
- Generally the substrate is grounded for MOSFET
- When the gate is applied with positive voltage (V_{GS}) then the negative charge carriers within the p-substrate [minority charge carriers] (electrons) attract to the positive gate and accumulate between the source and drain regions.
- These negative charge carriers which are minority carriers in p-type substrate form an inversion layer.
- These induced a channel between the source and drain regions.
- As the positive voltage on gate increases the induced negative charge increases. Hence the conductivity increases and current flows from drain to source through induced channel. Hence the drain current is enhanced by positive gate voltage.

(2.1) The minimum gate voltage V_{GS} that is required to form the channel is known as threshold voltage (V_T).

→ The operation of enhancement MOSFET is better understood from the following conditions.

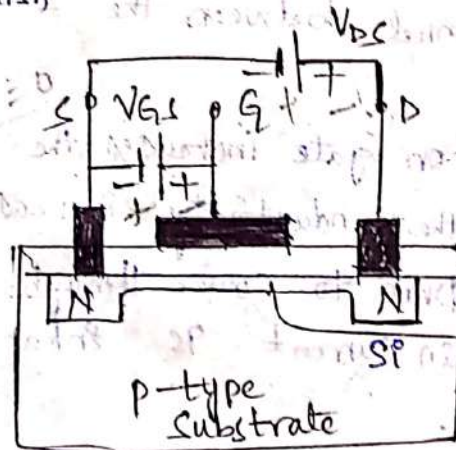
① When $V_{GS} < V_t$ and $V_{DS} = 0$:

When gate to source voltage (V_{GS}) is less than threshold voltage (V_t) then there is no inversion layer (channel) is formed. Hence no channel is present between drain to source. so drain current (I_D) is 0. [i.e., $I_D = 0$] This mode of operation is called cut-off region.



② When $V_{GS} > V_t$ and $V_{DS} \leq V_{GS} - V_t$

When gate to source voltage is greater than threshold voltage hence a channel is gets induced between drain to source. During these if V_{DS} is such that $V_{DS} < V_{GS} - V_t$. The charge carriers from source region move towards the drain region through the channel and establish drain current I_D that flows from drain to source.



The mode of operation is known as ohmic region or active region.

③ When $V_{GS} > V_t$ and $V_{DS} \geq V_{GS} - V_t$

When $V_{GS} > V_t$ and channel is established between drain and source now if V_{DS} such that $V_{DS} \geq V_{GS} - V_t$ the channel gets depleted.

The channel is pinched off at a particular point $V_{DS} = V_{GS} - V_t$ the channel becomes pinched off due to which the current becomes saturated i.e., I_D becomes constant. This mode of operation is known as saturation region.

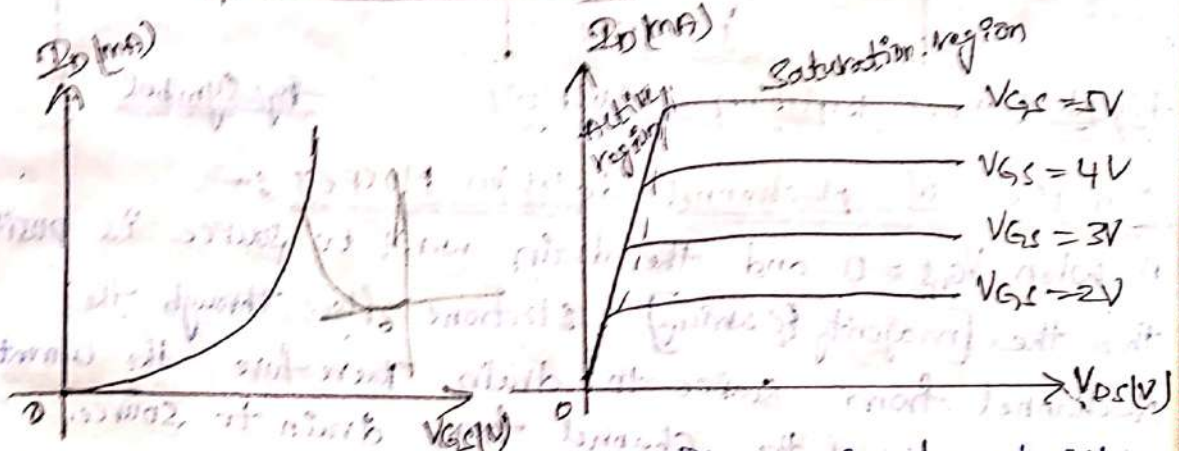
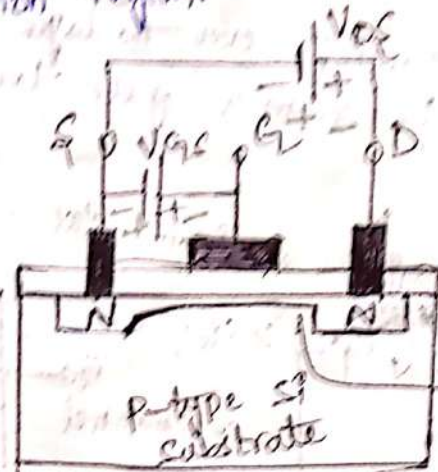


Fig:- Transfer characteristics of N-channel enhancement MOSFET

Fig:- Drain characteristics of N-channel enhancement MOSFET

The above figure shows the drain and transfer characteristics of N-channel enhancement MOSFET. In these case the relationship b/w I_D and V_{GS}

$$I_D = K [V_{GS} - V_t]^2$$

Depletion MOSFET:-

N-channel Depletion MOSFET:-

Construction:-

Two heavily doped n-regions are diffused into a lightly doped p-type silicon substrate. one of these regions called as source and another one is called as drain.

A channel is deposited close to the source and drain. A thin layer of SiO_2 is deposited over the surface of the p-substrate and holes are cut into this layer allowing contact with source and drain using aluminium metal contact.

→ A thin metal layer is deposited over the layer of SiO_2 between the two N-regions to form a gate terminal.

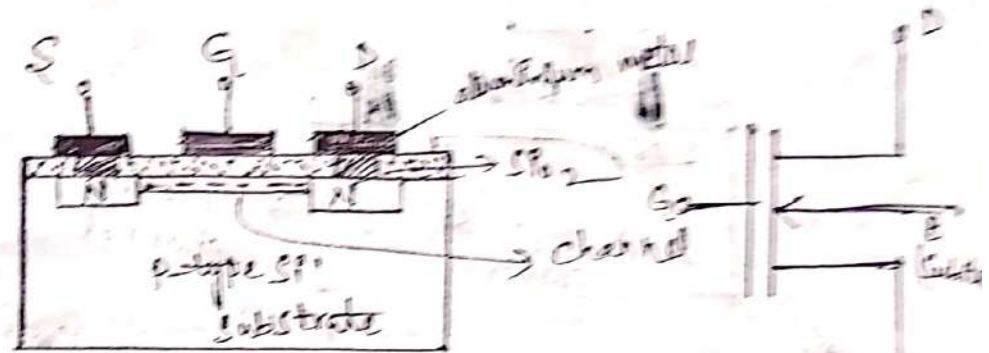


Fig. 1 N-channel depletion MOSFET

Fig. 1 N-channel MOSFET

Operation of N-channel depletion MOSFET:-

1) When $V_{GS} = 0$ and the drain w.r.t to source is positive then the [majority (carriers)] electrons flow through the N-channel from source to drain. Therefore the current I_D flow through the channel from drain to source.

2) Now if V_{GS} is increased ($V_{GS} > 0$) the channel width is increased due to which the drain current (I_D) increases.

3) If V_{GS} is decreased from i.e., $V_{GS} < 0$ the depleted channel between drain and source will get depleted as the majority charge carriers of p-substrate are attracted towards the negative gate terminal. Since $V_{GS} < 0$.

4) Hence in the N-channel depletion mode MOSFET the channel is enhanced when $V_{GS} > 0$ and is depleted when $V_{GS} < 0$. Hence it is also called as dual-mode MOSFET.

For more information about MOSFETs, visit the following link: <https://www.youtube.com/watch?v=...>

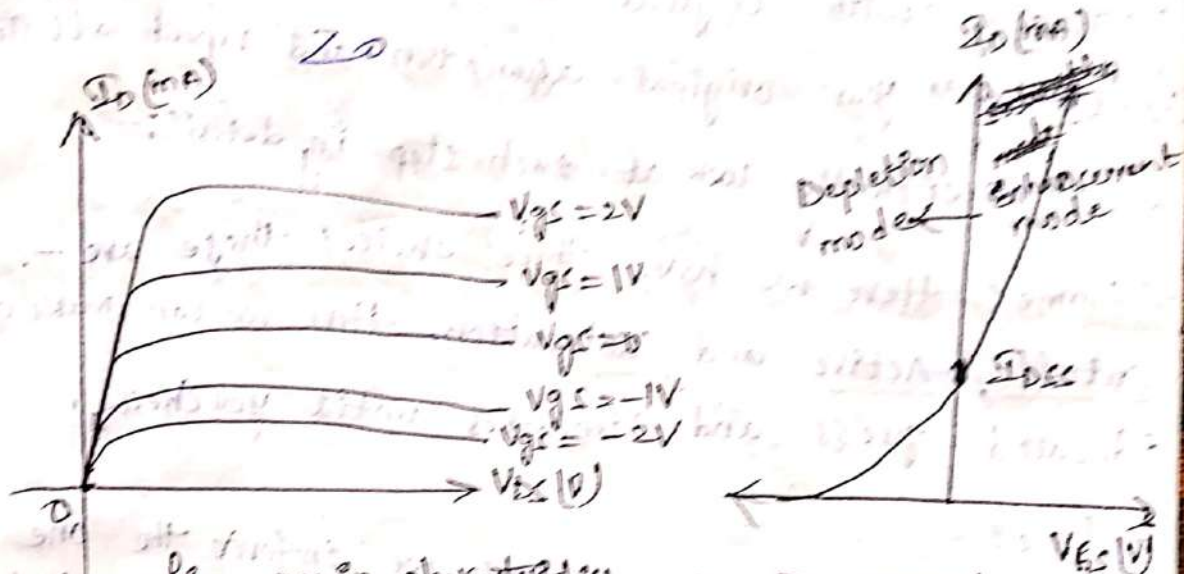
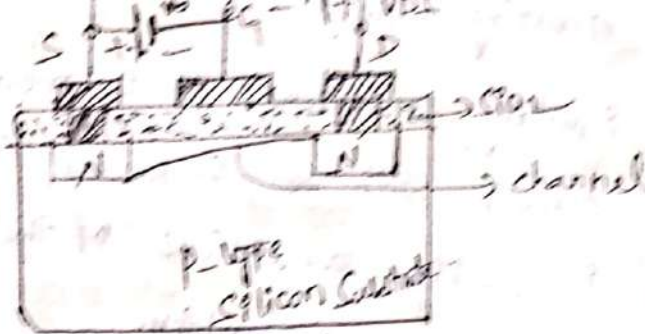


Fig. - Drain characteristics

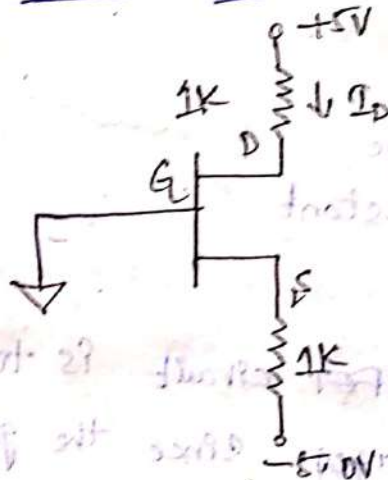
Fig. - Transfer characteristics

→ The above figures are the drain & transfer characteristics of n-channel depletion MOSFET.

→ The relationship b/w I_D and V_{GS} is

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

* MOSFET circuit at D.C.:-



here constant $K = 0.4 \text{ mA/V}^2$
 $V_T = 2V$

Steps for D.C. analysis of MOSFET circuit:-

To analyse MOSFET ckt with DC source, we must follow the these five steps:-